Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	FR81S
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, CSIO, EBI/EMI, I²C, LINbus, SPI, UART/USART
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	111
Program Memory Size	576KB (576K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 40x8/10b; D/A 2x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f575bhspmc-gsk5e1

1. Product Lineup

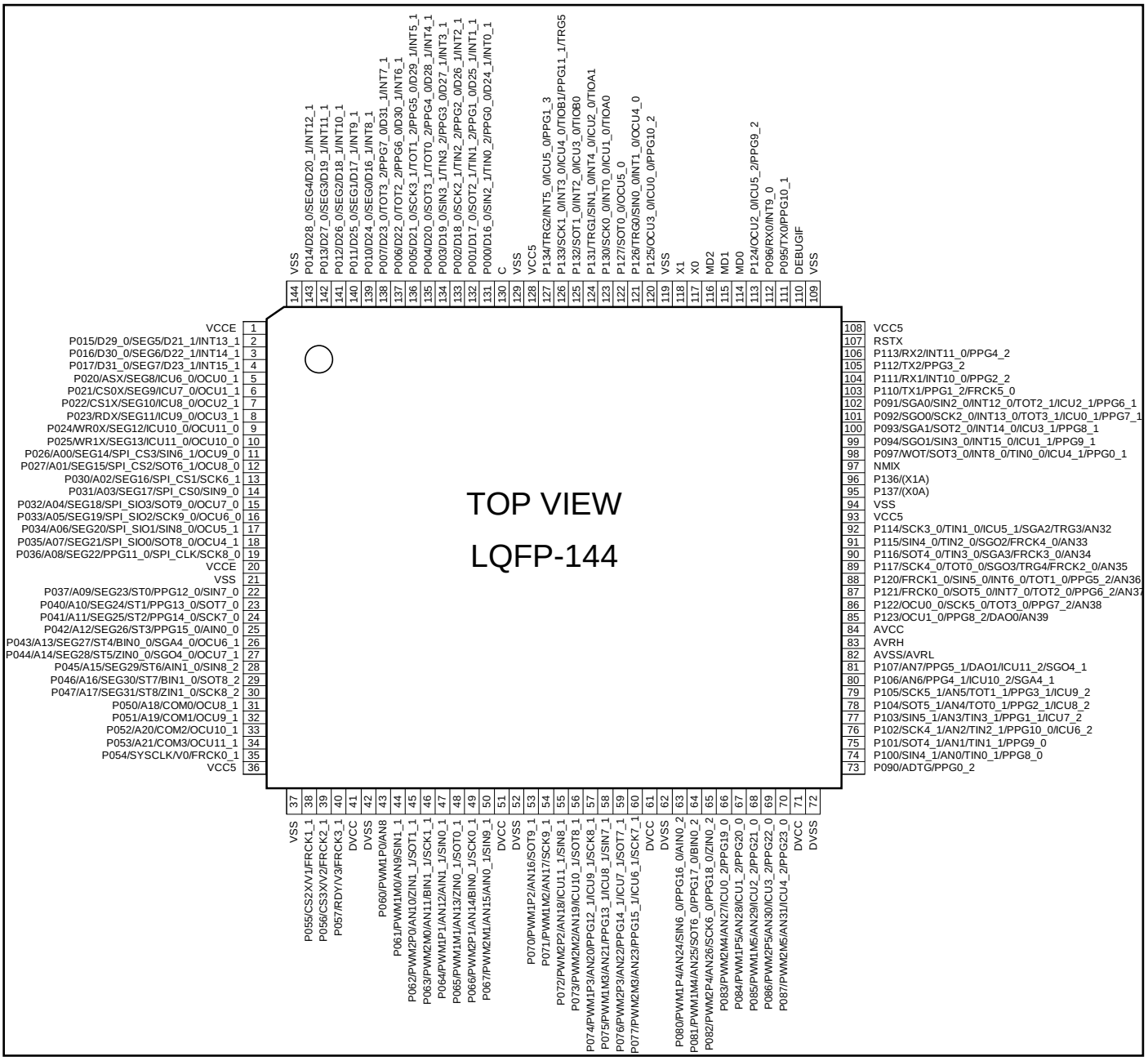
Item \ Product	MB91F575B(S)/C(S)	MB91F575BH(S)/CH(S)
System Clock	On chip PLL Clock multiple method	
Minimum instruction execution time	Around 12.5ns (80MHz)	
Sub clock	Yes(Non-S series) No(S series)	
FLASH Capacity (Program)	512 + 64KB	
FLASH Capacity (Work)	64KB	
RAM	40KB + 8KB	
BI-ROM	4KB	
GDC	None	
External BUS I/F	Address : 22-bit Data :16-bit (Part of the External BUS I/F pins can select the power supply 5V or 3.3V)	
DMA Controller	16 channels	
Base Timer(16bit)	2 channels	
Free-run Timer(32bit)	6 channels	
Input capture(32bit)	12 channels	
Output Compare(32bit)	12 channels	
Reload Timer(16bit)	7 channels	
PPG timer(16bit)	24 channels	
Up/down Counter	2 channels	
Clock Supervisor	Yes	
D/A converter	2 channels	
External Interrupt	16 channels	
A/D converter (8bit/10bit)	40 channels	
LIN-UART	6 channels	
Multi-Function serial communication	4 channels[*1]	
HS-SPI	Yes Up to 16MHz Note: In this series, the HS-SPI function is prohibited.	
LCD Controller	32seg × 4com(Static drive 8seg × 1com)	
CAN	64msg × 1 channel / 32msg × 2 channels	
Stepping Motor Controller	6 channels	

Item \ Product	MB91F577B(S)/C(S)	MB91F577BH(S)/CH(S)
System Clock	On chip PLL Clock multiple method	
Minimum instruction execution time	Around 12.5ns (80MHz)	
Sub clock	Yes(Non-S series) No(S series)	
FLASH Capacity (Program)	1024 + 64KB	
FLASH Capacity (Work)	64KB	
RAM	64KB + 8KB	
BI-ROM	4KB	
GDC	None	
External BUS I/F	Address : 22-bit Data :16-bit (Part of the External BUS I/F pins can select the power supply 5V or 3.3V)	
DMA Controller	16 channels	
Base Timer(16bit)	2 channels	
Free-run Timer(32bit)	6 channels	
Input capture(32bit)	12 channels	
Output Compare(32bit)	12 channels	
Reload Timer(16bit)	7 channels	
PPG timer(16bit)	24 channels	
Up/down Counter	2 channels	
Clock Supervisor	Yes	
D/A converter	2 channels	
External Interrupt	16 channels	
A/D converter (8bit/10bit)	40 channels	
LIN-UART	6 channels	
Multi-Function serial communication	4 channels[*1]	
HS-SPI	Yes Up to 16MHz Note: In this series, the HS-SPI function is prohibited.	
LCD Controller	32seg × 4com(Static drive 8seg × 1com)	
CAN	64msg × 1 channel / 32msg × 2 channels	
Stepping Motor Controller	6 channels	
Sound Generator	5 channels	

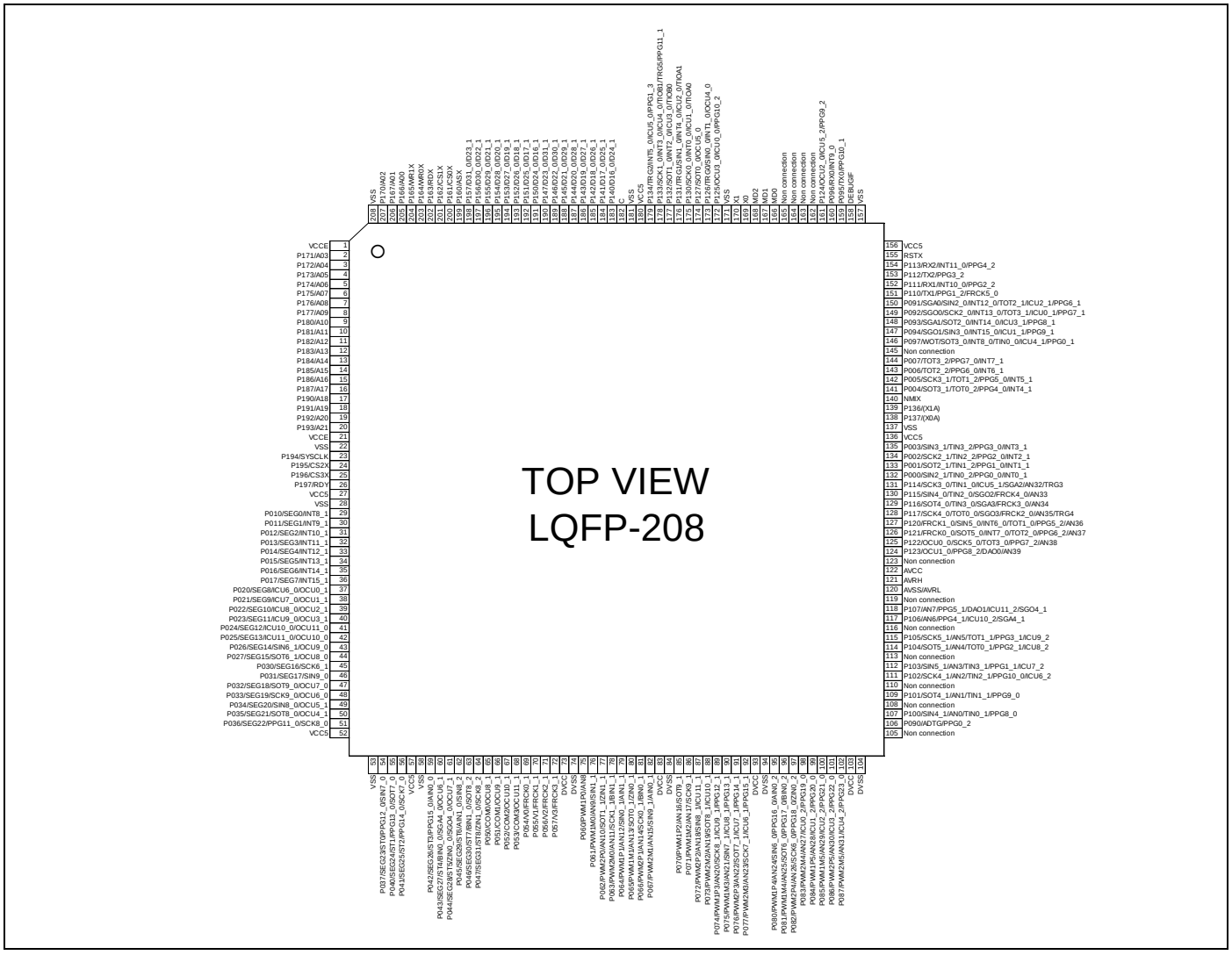
Item \ Product	MB91F 578C(S)(M)	MB91F 578CH(S)(M)	MB91F 579C(S)(M)	MB91F 579CH(S)(M)
Hardware Watchdog	Yes			
Clock supervisor	Initial value "ON"	Initial value "OFF"	Initial value "ON"	Initial value "OFF"
CRC generation	Yes			
Low-voltage detection reset (External low-voltage detection)	Yes			
Low-voltage detection reset (Internal low-voltage detection)	Yes			
Package	LQFP-144 LQFP-208 (with suffix "M")			
Others	Flash Products			
On Chip Debug	Yes			

*1: I^2C only supported by ch.0 and ch.1.

2. Pin Assignment (LQFP-144)



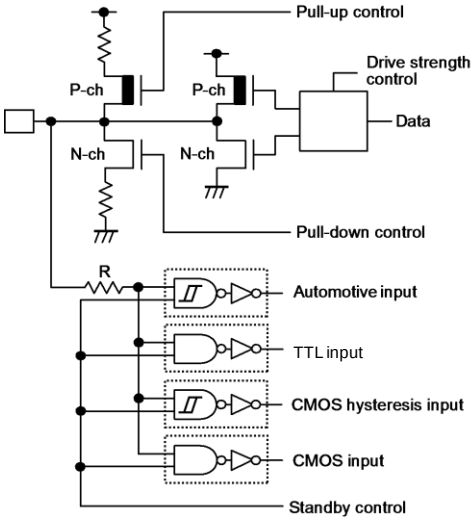
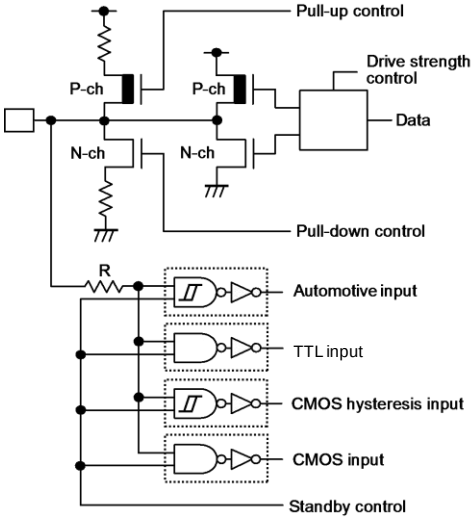
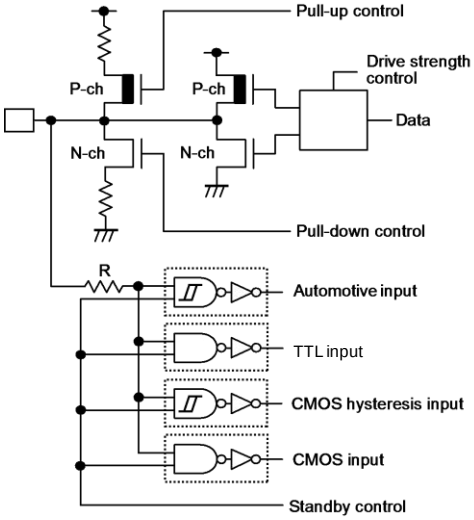
3. Pin Assignment (LQFP-208)

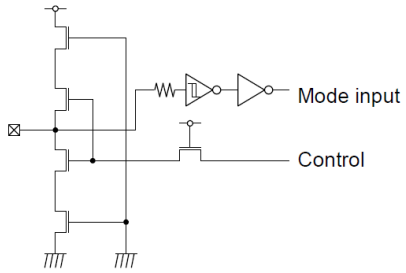
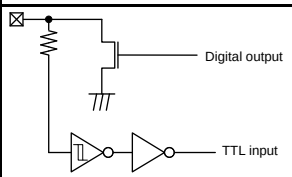
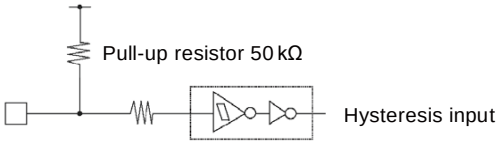
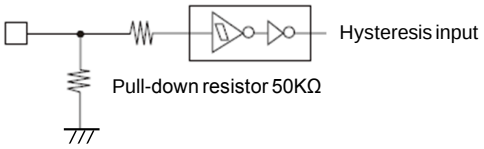
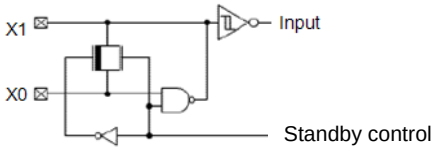
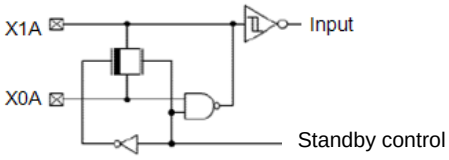


Pin Number	Pin Name	I/O Circuit Type	Function Description
26	P043	I	General-Purpose I/O Port
	A13		External Bus Address Output pin
	SEG27		LCDC Segment(Duty)Output pin
	ST4		LCDC Segment(Static)Output pin
	BIN0_0		Up/down Counter BIN Input pin ch.0 relocation 0
	SGA4_0		Sound Generator SGA Output pin ch.4 relocation 0
	OCU6_1		Output Compare Output pin ch.6 relocation 1
27	P044	I	General-Purpose I/O Port
	A14		External Bus Address Output pin
	SEG28		LCDC Segment(Duty)Output pin
	ST5		LCDC Segment(Static)Output pin
	ZIN0_0		Up/down Counter ZIN Input pin ch.0 relocation 0
	SGO4_0		Sound Generator SGO Output pin ch.4 relocation 0
	OCU7_1		Output Compare Output pin ch.7 relocation 1
28	P045	I	General-Purpose I/O Port
	A15		External Bus Address Output pin
	SEG29		LCDC Segment(Duty)Output pin
	ST6		LCDC Segment(Static)Output pin
	AIN1_0		Up/down Counter AIN Input pin ch.1 relocation 0
	SIN8_2		Multi-function Serial Input pin ch.8 relocation 2
29	P046	I	General-Purpose I/O Port
	A16		External Bus Address Output pin
	SEG30		LCDC Segment(Duty)Output pin
	ST7		LCDC Segment(Static)Output pin
	BIN1_0		Up/down Counter BIN Input pin ch.1 relocation 0
	SOT8_2		Multi-function Serial Output pin ch.8 relocation 2
30	P047	I	General-Purpose I/O Port
	A17		External Bus Address Output pin
	SEG31		LCDC Segment(Duty)Output pin
	ST8		LCDC Segment(Static)Output pin
	ZIN1_0		Up/down Counter ZIN Input pin ch.1 relocation 0
	SCK8_2		Multi-function Serial Clock I/O pin ch.8 relocation 2
31	P050	I	General-Purpose I/O Port
	A18		External Bus Address Output pin
	COM0		LCDC Segment(Duty)Common Output pin
	OCU8_1		Output Compare Output pin ch.8 relocation 1
32	P051	I	General-Purpose I/O Port
	A19		External Bus Address Output pin
	COM1		LCDC Segment(Duty)Common Output pin
	OCU9_1		Output Compare Output pin ch.9 relocation 1

Pin Number	Pin Name	I/O Circuit Type	Function Description
82	P067	K	General-Purpose I/O Port
	PWM2M1		SMC Output pin ch.1
	AN15		ADC Analog Input pin ch.15
	SIN9_1		Multi-function Serial Input pin ch.9 relocation 1
	AIN0_1		Up/down Counter AIN Input pin ch.0 relocation 1
83	DVCC	-	Power Supply pin for SMC high current
84	DVSS	-	GND pin for SMC high current
85	P070	K	General-Purpose I/O Port
	PWM1P2		SMC Output pin ch.2
	AN16		ADC Analog Input pin ch.16
	SOT9_1		Multi-function Serial Output pin ch.9 relocation 1
86	P071	K	General-Purpose I/O Port
	PWM1M2		SMC Output pin ch.2
	AN17		ADC Analog Input pin ch.17
	SCK9_1		Multi-function Serial Clock I/O pin ch.9 relocation 1
87	P072	K	General-Purpose I/O Port
	PWM2P2		SMC Output pin ch.2
	AN18		ADC Analog Input pin ch.18
	SIN8_1		Multi-function Serial Input pin ch.8 relocation 1
	ICU11_1		Input Capture Input pin ch.11 relocation 1
88	P073	K	General-Purpose I/O Port
	PWM2M2		SMC Output pin ch.2
	AN19		ADC Analog Input pin ch.19
	SOT8_1		Multi-function Serial Output pin ch.8 relocation 1
	ICU10_1		Input Capture Input pin ch.10 relocation 1
89	P074	K	General-Purpose I/O Port
	PWM1P3		SMC Output pin ch.3
	AN20		ADC Analog Input pin ch.20
	SCK8_1		Multi-function Serial Clock I/O pin ch.8 relocation 1
	ICU9_1		Input Capture Input pin ch.9 relocation 1
	PPG12_1		PPG Output pin ch.12 relocation 1
90	P075	K	General-Purpose I/O Port
	PWM1M3		SMC Output pin ch.3
	AN21		ADC Analog Input pin ch.21
	SIN7_1		LIN_UART Serial Input pin ch.7 relocation 1
	ICU8_1		Input Capture Input pin ch.8 relocation 1
	PPG13_1		PPG Output pin ch.13 relocation 1
91	P076	K	General-Purpose I/O Port
	PWM2P3		SMC Output pin ch.3
	AN22		ADC Analog Input pin ch.22
	SOT7_1		LIN_UART Serial Output pin ch.7 relocation 1
	ICU7_1		Input Capture Input pin ch.7 relocation 1
	PPG14_1		PPG Output pin ch.14 relocation 1
92	P077	K	General-Purpose I/O Port
	PWM2M3		SMC Output pin ch.3
	AN23		ADC Analog Input pin ch.23
	SCK7_1		LIN_UART Serial Clock I/O pin ch.7 relocation 1
	ICU6_1		Input Capture Input pin ch.6 relocation 1
	PPG15_1		PPG Output pin ch.15 relocation 1

Pin Number	Pin Name	I/O Circuit Type	Function Description
106	P090	M	General-Purpose I/O Port
	ADTG		ADC External Trigger Input pin
	PPG0_2		PPG Output pin ch.0 relocation 2
107	P100	J	General-Purpose I/O Port
	SIN4_1		LIN_UART Serial Input pin ch.4 relocation 1
	AN0		ADC Analog Input pin ch.0
	TIN0_1		Reload Timer Event Input pin ch.0 relocation 1
	PPG8_0		PPG Output pin ch.8 relocation 0
108	Non connection	-	Non connection
109	P101	J	General-Purpose I/O Port
	SOT4_1		LIN_UART Serial Output pin ch.4 relocation 1
	AN1		ADC Analog Input pin ch.1
	TIN1_1		Reload Timer Event Input pin ch.1 relocation 1
	PPG9_0		PPG Output pin ch.9 relocation 0
110	Non connection	-	Non connection
111	P102	J	General-Purpose I/O Port
	SCK4_1		LIN_UART Serial Clock I/O pin ch.4 relocation 1
	AN2		ADC Analog Input pin ch.2
	TIN2_1		Reload Timer Event Input pin ch.2 relocation 1
	PPG10_0		PPG Output pin ch.10 relocation 0
	ICU6_2		Input Capture Input pin ch.6 relocation 2
112	P103	J	General-Purpose I/O Port
	SIN5_1		LIN_UART Serial Input pin ch.5 relocation 1
	AN3		ADC Analog Input pin ch.3
	TIN3_1		Reload Timer Event Input pin ch.3 relocation 1
	PPG1_1		PPG Output pin ch.1 relocation 1
	ICU7_2		Input Capture Input pin ch.7 relocation 2
113	Non connection	-	Non connection
114	P104	J	General-Purpose I/O Port
	SOT5_1		LIN_UART Serial Output pin ch.5 relocation 1
	AN4		ADC Analog Input pin ch.4
	TOT0_1		Reload Timer Output pin ch.0 relocation 0
	PPG2_1		PPG Output pin ch.2 relocation 1
	ICU8_2		Input Capture Input pin ch.8 relocation 2
115	P105	J	General-Purpose I/O Port
	SCK5_1		LIN_UART Serial Clock I/O pin ch.5 relocation 1
	AN5		ADC Analog Input pin ch.5
	TOT1_1		Reload Timer Output pin ch.1 relocation 1
	PPG3_1		PPG Output pin ch.3 relocation 1
	ICU9_2		Input Capture Input pin ch.9 relocation 2
116	Non connection	-	Non connection
117	P106	J	General-Purpose I/O Port
	AN6		ADC Analog Input pin ch.6
	PPG4_1		PPG Output pin ch.4 relocation 1
117	ICU10_2	J	Input Capture Input pin ch.10 relocation 2
	SGA4_1		Sound Generator SGA Output pin ch.4 relocation 1

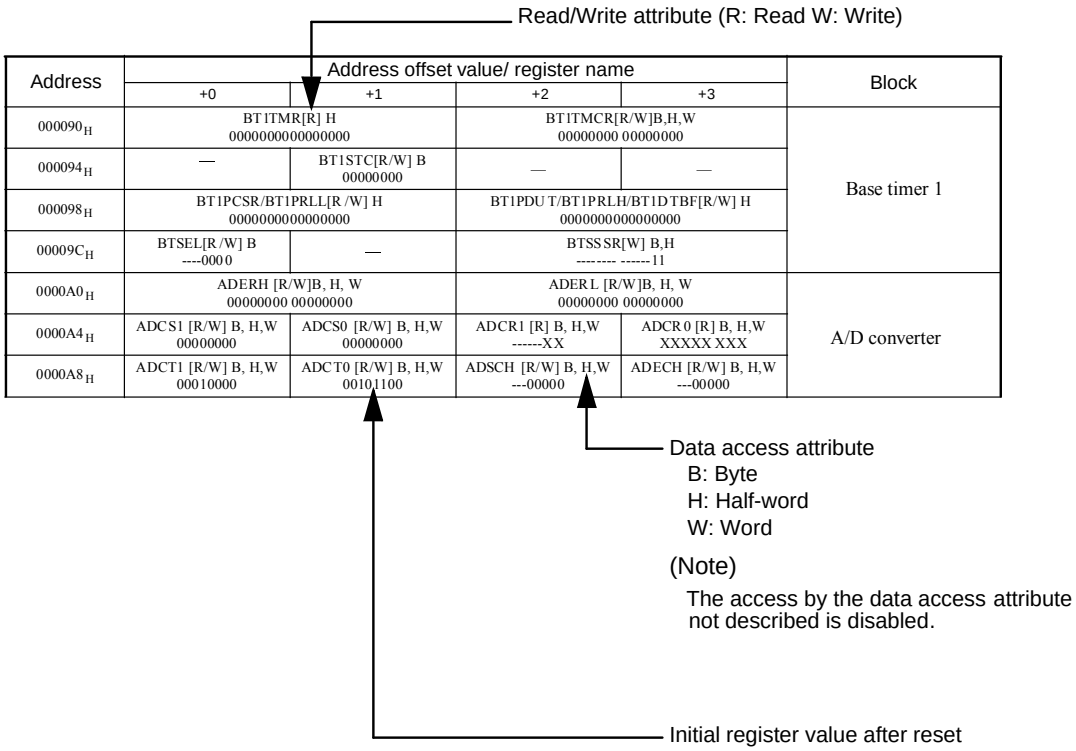
Type	Circuit	Remarks
M		General-purpose I/O port. IOH = -1/-2mA, IOL = 1/2mA Pull-up resistor control Pull-down resistor control Automotive level input TTL level input CMOS level hysteresis input CMOS level input
M2		General-purpose I/O port. IOH = -1/-2mA(@VCCE = 5V), IOH = -0.5/-1mA(@VCCE = 3.3V), IOL = 1/2mA(@VCCE = 5V), IOL = 0.5/1mA(@VCCE = 3.3V) Pull-up resistor control Pull-down resistor control Automotive level input TTL level input CMOS level hysteresis input CMOS level input
N		General-purpose I/O port with I^2C output IOH = -1/-2/-3mA, IOL = 1/2/3mA Pull-up resistor control Pull-down resistor control Automotive level input TTL level input CMOS level hysteresis input CMOS level input

Type	Circuit	Remarks
A		Mode pin
B		DEBUG I/F pin
R		CMOS level hysteresis input
R2		CMOS level hysteresis input
X		Main oscillation I/O
Y		Sub oscillation I/O

11. I/O Map

The following I/O map shows the relationship between memory space and registers for peripheral resources.

Legend of I/O Map



Address	Address offset value/ register name				Block
	+0	+1	+2	+3	
000090_H	BT1TMR[R] H 0000000000000000		BT1TMCR[R/W]B,H,W 00000000 00000000		Base timer 1
000094_H	—	BT1STC[R/W] B 00000000	—	—	
000098_H	BT1PCSR/BT1PRLL[R /W] H 0000000000000000		BT1PDU T/BT1PRLH/BT1D TBF[R/W] H 0000000000000000		
$00009C_H$	BTSEL[R /W] B ----0000	—	BTSS SR[W] B,H -------- ------11		
$0000A0_H$	ADERH [R/W]B, H, W 00000000 00000000		ADER L [R/W]B, H, W 00000000 00000000		A/D converter
$0000A4_H$	ADCS1 [R/W] B, H,W 00000000	ADCS0 [R/W] B, H,W 00000000	ADCR1 [R] B, H,W ------XX	ADCR 0 [R] B, H,W XXXXX XXX	
$0000A8_H$	ADCT1 [R/W] B, H,W 00010000	ADCT0 [R/W] B, H,W 00101100	ADSCH [R/W] B, H,W ---00000	ADECH [R/W] B, H,W ---00000	

The initial register value after reset indicates as follows:

"1": Initial value "1"

"0": Initial value "0"

"X": Initial value undefined

"-": Reserved bit/Undefined bit

"*": Initial value "0" or "1" according to the setting

Note:

It is prohibited to access addresses not described here.

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000530_H	CCRTSELR [R/W] B,H,W 0------0	—	CCPMUCR0 [R/W] B,H,W 0-----00	CCPMUCR1 [R/W] B,H,W 0--00000	Clock control 2
000534_H	—	—	—	—	
000538_H	—	—	—	—	
$00053C_H$	—	—	—	—	
000540_H to $00054C_H$	—	—	—	—	Reserved
000550_H	EIRR0[R/W] B,H,W XXXXXXXX	ENIR0[R/W] B,H,W 00000000	ELVR0[R/W] B,H,W 00000000 00000000		External interrupt (INT0 to INT7)
000554_H	EIRR1[R/W] B,H,W XXXXXXXX	ENIR1[R/W] B,H,W 00000000	ELVR1[R/W] B,H,W 00000000 00000000		External interrupt (INT8 to INT15)
000558_H	—	—	—	—	Reserved
$00055C_H$	—	—	WTDR[R/W] H 00000000 00000000		Real-time clock
000560_H	—	WTCRH [R/W] B ------00	WTCRM [R/W] B,H 00000000	WTCRL [R/W] B,H ----00-0	
000564_H	—	WTBRH [R/W] B --XXXXXX	WTBRM [R/W] B XXXXXXXX	WTBRL [R/W] B XXXXXXXX	
000568_H	WTHR [R/W] B,H ---00000	WTMR [R/W] B,H --000000	WTSR [R/W] B --000000	—	
$00056C_H$	—	CSVCR[R/W]B -001110- -001010-*[3]	—	—	Clock supervisor
000570_H to $00057C_H$	—	—	—	—	Reserved
000580_H	REGSEL [R/W] B,H,W 0110011-	—	—	—	Regulator control
000584_H	LVD5R [R/W] B,H,W -------1	LVD5F [R/W] B,H,W 0-100--1	LVD [R/W] B,H,W 01000--0	—	Low-voltage detection
000588_H to $00058C_H$	—	—	—	—	Reserved

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000590_H	PMUSTR [R/W] B,H,W 0-----1X	PMUCTLR [R/W] B,H,W 0-00----	PWRTMCTL [R/W] B,H,W -----011	—	PMU
000594_H	PMUINTF0 [R/W] B,H,W 00000000	PMUINTF1 [R/W] B,H,W 00000000	PMUINTF2 [R/W] B,H,W 0000----	—	
000598_H	—	—	—	—	
$00059C_H$ to $0005A4_H$	—	—	—	—	Reserved
$0005A8_H$	LCDCMR [R/W] B,H,W 0-------	LCRS [R/W] B,H,W 00000000	LCR0 [R/W] B,H,W 00010000	LCR1 [R/W] B,H,W --------	LCD controller
$0005AC_H$	VRAM0[R/W] B,H,W 00000000	VRAM1[R/W] B,H,W 00000000	VRAM2[R/W] B,H,W 00000000	VRAM3[R/W] B,H,W 00000000	
$0005B0_H$	VRAM4[R/W] B,H,W 00000000	VRAM5[R/W] B,H,W 00000000	VRAM6[R/W] B,H,W 00000000	VRAM7[R/W] B,H,W 00000000	
$0005B4_H$	VRAM8[R/W] B,H,W 00000000	VRAM9[R/W] B,H,W 00000000	VRAM10[R/W] B,H,W 00000000	VRAM11[R/W] B,H,W 00000000	
$0005B8_H$	VRAM12[R/W] B,H,W 00000000	VRAM13[R/W] B,H,W 00000000	VRAM14[R/W] B,H,W 00000000	VRAM15[R/W] B,H,W 00000000	
$0005BC_H$	LDR0[R/W] B,H,W -------0	LDR1[R/W] B,H,W 00000000	—	—	
$0005C0_H$ to $0005FC_H$	—	—	—	—	Reserved
000600_H	ASR0 [R/W] W 00000000 00000000 -------- 1111-001				External bus Interface [S]
000604_H	ASR1 [R/W] W XXXXXXXX XXXXXXXX -------- XXXX-XX0				
000608_H	ASR2 [R/W] W XXXXXXXX XXXXXXXX -------- XXXX-XX0				
$00060C_H$	ASR3 [R/W] W XXXXXXXX XXXXXXXX -------- XXXX-XX0				
000610_H to $00063C_H$	—	—	—	—	Reserved [S]

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$000F00_H$	EPILR00[R/W] B,H,W 00000000	EPILR01[R/W] B,H,W 00000000	EPILR02[R/W] B,H,W 00000000	EPILR03[R/W] B,H,W 00000000	Extended Port input level selection register *4:MB91F578/9 only
$000F04_H$	EPILR04[R/W] B,H,W 00000000	EPILR05[R/W] B,H,W 00000000	EPILR06[R/W] B,H,W 00000000	EPILR07[R/W] B,H,W 00000000	
$000F08_H$	EPILR08[R/W] B,H,W 00000000	EPILR09[R/W] B,H,W 00000000	EPILR10[R/W] B,H,W 00000000	EPILR11[R/W] B,H,W 00000000	
$000F0C_H$	EPILR12[R/W] B,H,W 00000000	EPILR13[R/W] B,H,W 00-00000	EPILR14[R/W] B,H,W 00000000*4	EPILR15[R/W] B,H,W 00000000*4	
$000F10_H$	EPILR16[R/W] B,H,W 00000000*4	EPILR17[R/W] B,H,W 00000000*4	EPILR18[R/W] B,H,W 00000000*4	EPILR19[R/W] B,H,W 00000000*4	
$000F1C_H$	—	—	—	—	Reserved
$000F20_H$	PODR00[R/W] B,H,W 00000000	PODR01[R/W] B,H,W 00000000	PODR02[R/W] B,H,W 00000000	PODR03[R/W] B,H,W 00000000	Port output drive register *4:MB91F578/9 only
$000F24_H$	PODR04[R/W] B,H,W 00000000	PODR05[R/W] B,H,W 00000000	PODR06[R/W] B,H,W 00000000	PODR07[R/W] B,H,W 00000000	
$000F28_H$	PODR08[R/W] B,H,W 00000000	PODR09[R/W] B,H,W 00000000	PODR10[R/W] B,H,W 00000000	PODR11[R/W] B,H,W 00000000	
$000F2C_H$	PODR12[R/W] B,H,W 00000000	PODR13[R/W] B,H,W 00-00000	PODR14[R/W] B,H,W 00000000*4	PODR15[R/W] B,H,W 00000000*4	
$000F30_H$	PODR16[R/W] B,H,W 00000000*4	PODR17[R/W] B,H,W 00000000*4	PODR18[R/W] B,H,W 00000000*4	PODR19[R/W] B,H,W 00000000*4	
$000F34_H$	—	EPODR01 [R/W] B,H,W 00000000	EPODR02 [R/W] B,H,W 00000000	EPODR03 [R/W] B,H,W -0000000	Extended Port output drive register
$000F38_H$	EPODR06 [R/W] B,H,W 00000000	EPODR07 [R/W] B,H,W 00000000	EPODR08 [R/W] B,H,W 00000000	—	
$000F3C_H$	—	—	—	—	Reserved
$000F40_H$	PORTEN [R/W] B,H,W -------0	—	—	—	Port input enable register
$000F44_H$ to $000F6C_H$	—	—	—	—	Reserved
$000F70_H$	RCRH0[W] H,W XXXXXXXX	RCRL0[W] B,H,W XXXXXXXX	UDCRH0[R] H,W 00000000	UDCRL0[R] B,H,W 00000000	Up/down counter 0
$000F74_H$	CCR0[R/W] B,H 00000000 -0001000		—	CSR0[R/W] B 00000000	
$000F78_H$ to $000F7C_H$	—	—	—	—	Reserved

12. Interrupt Vector Table

This list shows the assignments of interrupt factors and interrupt vectors/interrupt control registers.

Interrupt Vector

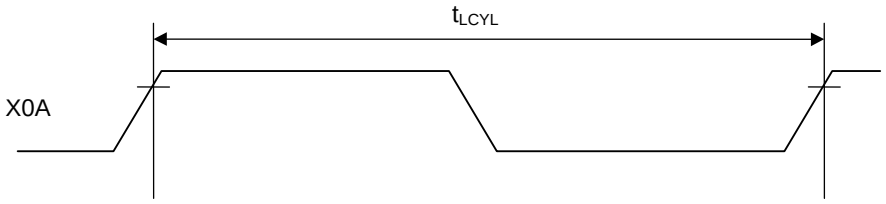
Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN *1
	Decimal	Hexa-decimal				
Reset	0	00	-	$3FC_H$	$000FFFFC_H$	-
System reserved	1	01	-	$3F8_H$	$000FFFF8_H$	-
System reserved	2	02	-	$3F4_H$	$000FFFF4_H$	-
System reserved	3	03	-	$3F0_H$	$000FFFF0_H$	-
System reserved	4	04	-	$3EC_H$	$000FFFEC_H$	-
FPU exception	5	05	-	$3E8_H$	$000FFFE8_H$	-
Exception of instruction access protection violation	6	06	-	$3E4_H$	$000FFFE4_H$	-
Exception of data access protection violation	7	07	-	$3E0_H$	$000FFFE0_H$	-
Data access error interrupt	8	08	-	$3DC_H$	$000FFFDC_H$	-
INTE instruction	9	09	-	$3D8_H$	$000FFFD8_H$	-
Instruction break	10	0A	-	$3D4_H$	$000FFFD4_H$	-
System Reserved	11	0B	-	$3D0_H$	$000FFFD0_H$	-
System Reserved	12	0C	-	$3CC_H$	$000FFFCC_H$	-
System Reserved	13	0D	-	$3C8_H$	$000FFFC8_H$	-
Exception of illegal instruction	14	0E	-	$3C4_H$	$000FFFC4_H$	-
NMI request/ XBS RAM double-bit error detection/ Backup RAM double-bit error detection	15	0F	15 (F_H) Fixed	$3C0_H$	$000FFFC0_H$	-
External interrupt 0-7	16	10	ICR00	$3BC_H$	$000FFFBC_H$	0
External interrupt 8-15	17	11	ICR01	$3B8_H$	$000FFFB8_H$	1
Reload timer 0/1/4/5	18	12	ICR02	$3B4_H$	$000FFFB4_H$	2(*2)
Reload timer 2/3/6	19	13	ICR03	$3B0_H$	$000FFFB0_H$	3(*2)
Multi-function serial interface ch.0 (reception completed)/ Multi-function serial interface ch.0 (status)	20	14	ICR04	$3AC_H$	$000FFFAC_H$	4 (*3)
Multi-function serial interface ch.0 (transmission completed)	21	15	ICR05	$3A8_H$	$000FFFA8_H$	5
Multi-function serial interface ch.1 (reception completed)/ Multi-function serial interface ch.1 (status)	22	16	ICR06	$3A4_H$	$000FFFA4_H$	6 (*3)
Multi-function serial interface ch.1 (transmission completed)	23	17	ICR07	$3A0_H$	$000FFFA0_H$	7
LIN-UART2 (reception completed)	24	18	ICR08	$39C_H$	$000FFF9C_H$	8
LIN-UART2 (transmission completed)	25	19	ICR09	398_H	$000FFF98_H$	9
LIN-UART3 (reception completed)	26	1A	ICR10	394_H	$000FFF94_H$	10

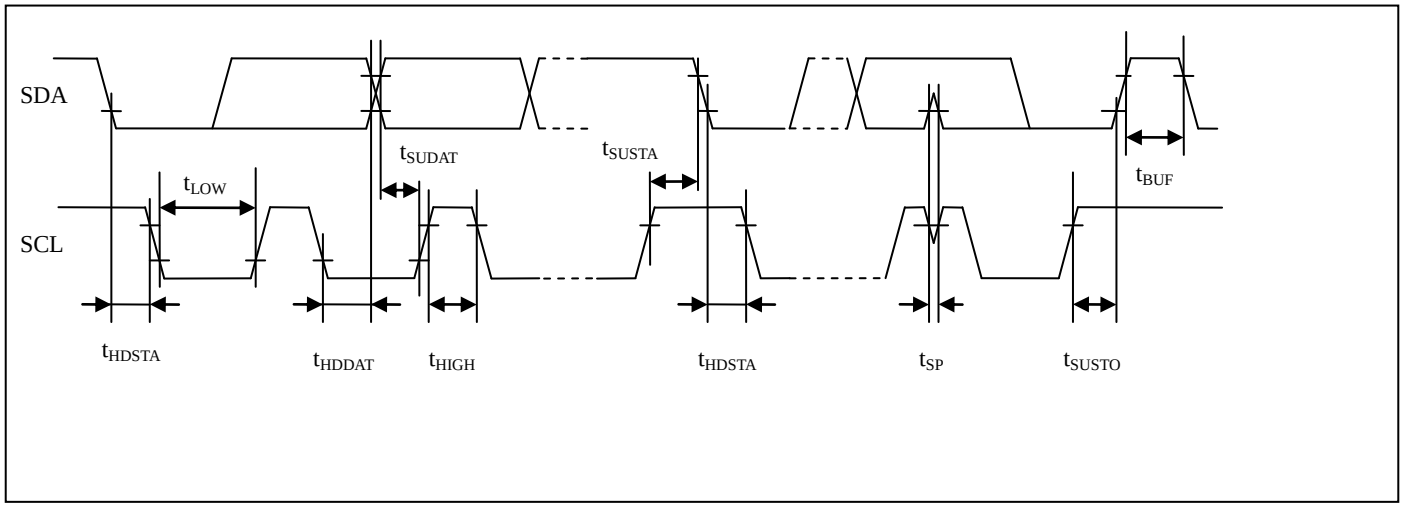
13.4.2 Sub clock timing (products without s-suffix)

(T_A: Recommended operating conditions, V_{CC} = 5.0V±10%, V_{SS} = DV_{SS} = AV_{SS} = 0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Source oscillation clock frequency	F_{CL}	X0A,X1A	–	–	32.768	–	kHz	
Source oscillation clock cycle time	t_{LCYL}	X0A,X1A		–	30.52	–	µs	

X0A,X1A clock timing




SDA
SCL
tLOW
tSUDAT
tSUSTA
tBUF
tHDSTA
tHDDAT
tHIGH
tHDSTA
tSP
tSUSTO

Bit setting: ESCR: SCES = 1, ECCR: SCDE = 1

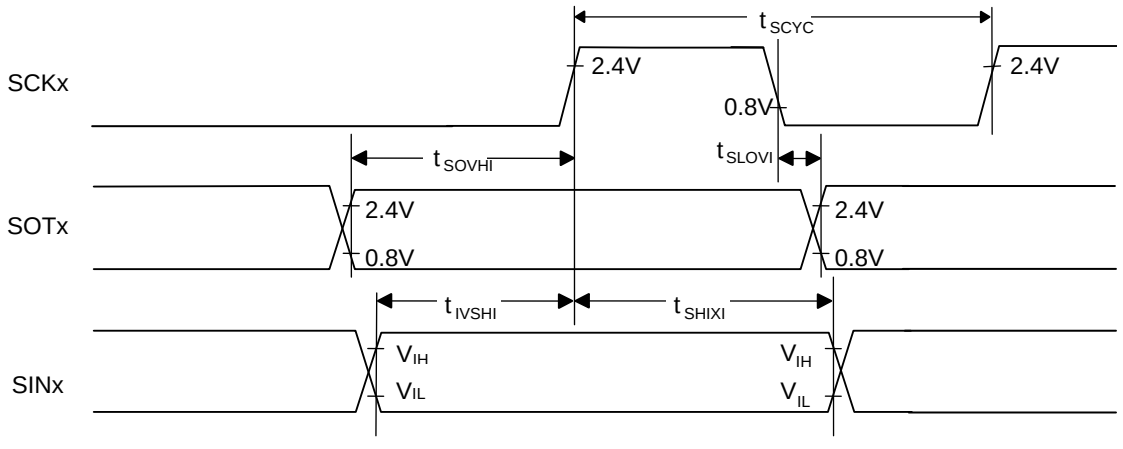
(T_A: Recommended operating conditions, $V_{CC}5$ = 5.0V±10%, $V_{CC}E$ = 5.0V±10%, V_{SS} = AV_{SS} = 0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7	–	$5t_{CPP}$	–	ns	Internal shift clock Mode: C_L=80pF+1 • TTL
SCK ↓→ SOT delay time	t_{SLOVI}	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7, SOT2,SOT3, SOT4,SOT5, SOT6,SOT7		-50	+50	ns	
Valid SIN→ SCK ↑ setup time	t_{IVSHI}	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7, SIN2,SIN3, SIN4,SIN5, SIN6,SIN7		t_{CPP}+80	–	ns	
SCK ↑→ Valid SIN hold time	t_{SHIXI}			0	–	ns	
SOT → SCK ↑ delay time	t_{SOVHI}	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7, SOT2,SOT3, SOT4,SOT5, SOT6,SOT7		$3t_{CPP}$-70	–	ns	

Notes:

- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operation clock used and other parameters. Refer to Hardware Manual for details.

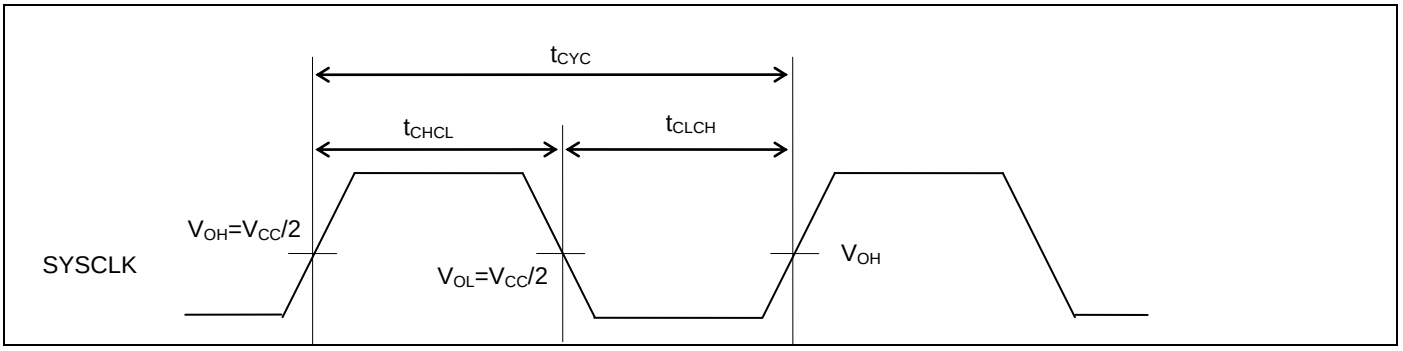
Internal shift clock mode



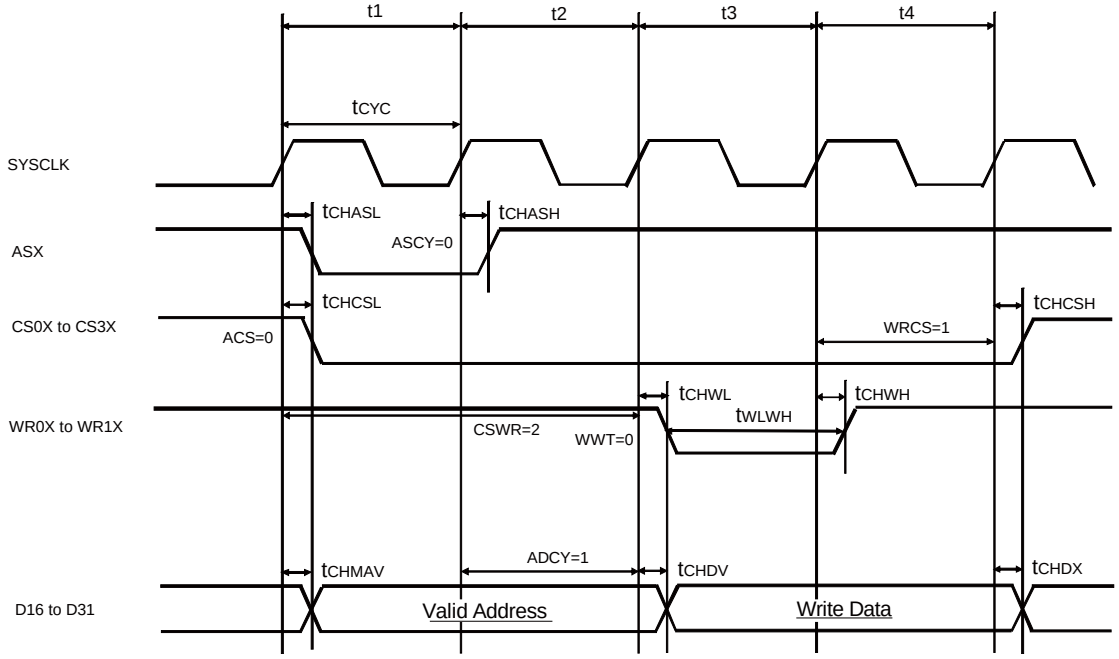
13.4.13 Clock output timing

(T_A: Recommended operating conditions, $V_{CC}5 = V_{CC}E = AV_{CC} = 5.0V \pm 10\%$, $V_{SS} = AV_{SS} = 0.0V$)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Cycle time	t_{CYC}	SYSCLK	—	t_{CPT}	—	ns	
SYSCLK ↑→ SYSCLK ↓	t_{CHCL}	SYSCLK		(1/2 t_{CYC}) - 7	(1/2 t_{CYC}) + 7	ns	
SYSCLK ↓→ SYSCLK ↑	t_{CLCH}	SYSCLK		(1/2 t_{CYC}) - 7	(1/2 t_{CYC}) + 7	ns	



External bus I/F (synchronous mode, write operation, and multiplex mode) timing



External bus I/F (synchronous mode, write operation, and split mode) timing