Infineon Technologies - MB91F577BHPMC-GSK5E1 Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	FR81S
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, CSIO, EBI/EMI, I²C, LINbus, SPI, UART/USART
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	111
Program Memory Size	1.0625MB (1.0625M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	72K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 40x8/10b; D/A 2x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f577bhpmc-gsk5e1

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1. Product Lineup

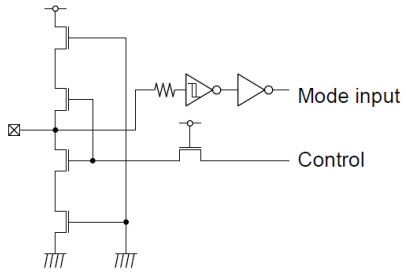
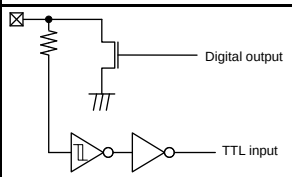
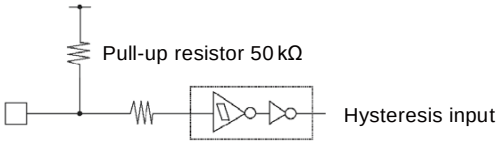
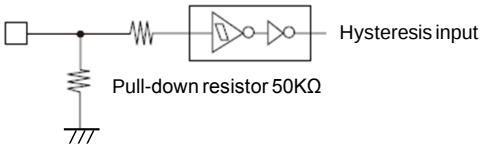
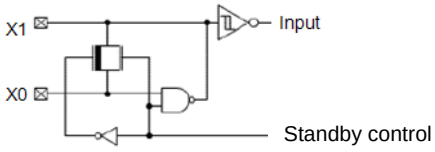
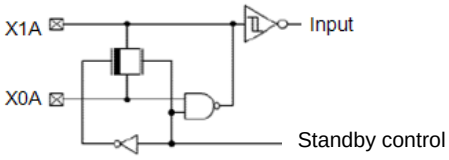
Item \ Product	MB91F575B(S)/C(S)	MB91F575BH(S)/CH(S)
System Clock	On chip PLL Clock multiple method	
Minimum instruction execution time	Around 12.5ns (80MHz)	
Sub clock	Yes(Non-S series) No(S series)	
FLASH Capacity (Program)	512 + 64KB	
FLASH Capacity (Work)	64KB	
RAM	40KB + 8KB	
BI-ROM	4KB	
GDC	None	
External BUS I/F	Address : 22-bit Data :16-bit (Part of the External BUS I/F pins can select the power supply 5V or 3.3V)	
DMA Controller	16 channels	
Base Timer(16bit)	2 channels	
Free-run Timer(32bit)	6 channels	
Input capture(32bit)	12 channels	
Output Compare(32bit)	12 channels	
Reload Timer(16bit)	7 channels	
PPG timer(16bit)	24 channels	
Up/down Counter	2 channels	
Clock Supervisor	Yes	
D/A converter	2 channels	
External Interrupt	16 channels	
A/D converter (8bit/10bit)	40 channels	
LIN-UART	6 channels	
Multi-Function serial communication	4 channels[*1]	
HS-SPI	Yes Up to 16MHz Note: In this series, the HS-SPI function is prohibited.	
LCD Controller	32seg × 4com(Static drive 8seg × 1com)	
CAN	64msg × 1 channel / 32msg × 2 channels	
Stepping Motor Controller	6 channels	

Item \ Product	MB91F577B(S)/C(S)	MB91F577BH(S)/CH(S)
System Clock	On chip PLL Clock multiple method	
Minimum instruction execution time	Around 12.5ns (80MHz)	
Sub clock	Yes(Non-S series) No(S series)	
FLASH Capacity (Program)	1024 + 64KB	
FLASH Capacity (Work)	64KB	
RAM	64KB + 8KB	
BI-ROM	4KB	
GDC	None	
External BUS I/F	Address : 22-bit Data :16-bit (Part of the External BUS I/F pins can select the power supply 5V or 3.3V)	
DMA Controller	16 channels	
Base Timer(16bit)	2 channels	
Free-run Timer(32bit)	6 channels	
Input capture(32bit)	12 channels	
Output Compare(32bit)	12 channels	
Reload Timer(16bit)	7 channels	
PPG timer(16bit)	24 channels	
Up/down Counter	2 channels	
Clock Supervisor	Yes	
D/A converter	2 channels	
External Interrupt	16 channels	
A/D converter (8bit/10bit)	40 channels	
LIN-UART	6 channels	
Multi-Function serial communication	4 channels[*1]	
HS-SPI	Yes Up to 16MHz Note: In this series, the HS-SPI function is prohibited.	
LCD Controller	32seg × 4com(Static drive 8seg × 1com)	
CAN	64msg × 1 channel / 32msg × 2 channels	
Stepping Motor Controller	6 channels	
Sound Generator	5 channels	

Item \ Product	MB91F 578C(S)(M)	MB91F 578CH(S)(M)	MB91F 579C(S)(M)	MB91F 579CH(S)(M)
System Clock	On chip PLL Clock multiple method			
Minimum instruction execution time	Around 12.5ns (80MHz)			
Sub clock	Yes(Non-S series) No(S series)			
FLASH Capacity (Program)	1536 + 64KB		2048 + 64KB	
FLASH Capacity (Work)	64KB			
RAM	96KB + 16KB		128KB + 16KB	
BI-ROM	4KB			
GDC	None			
External BUS I/F	Address : 22-bit Data :16-bit (Part of the External BUS I/F pins can select the power supply 5V or 3.3V)			
DMA Controller	16 channels			
Base Timer(16bit)	2 channels			
Free-run Timer(32bit)	6 channels			
Input capture(32bit)	12 channels			
Output Compare(32bit)	12 channels			
Reload Timer(16bit)	7 channels			
PPG timer(16bit)	24 channels			
Up/down Counter	2 channels			
Clock Supervisor	Yes			
D/A converter	2 channels			
External Interrupt	16 channels			
A/D converter (8bit/10bit)	40 channels			
LIN-UART	6 channels			
Multi-Function serial communication	4 channels[*1]			
HS-SPI	No			
LCD Controller	32seg × 4com(Static drive 8seg × 1com)			
CAN	64msg × 1 channel / 32msg × 2 channels			
Stepping Motor Controller	6 channels			
Sound Generator	5 channels			
Software Watchdog	Yes			

Pin Number	Pin Name	I/O Circuit Type	Function Description
17	P034	H/I4[*1]	General-Purpose I/O Port
	A06		External Bus Address Output pin
	SEG20		LCDC Segment(Duty)Output pin
	SPI_SIO1		HS_SPI SDATA1 I/O pin (Not supported)
	SIN8_0		Multi-function Serial Input pin ch.8 relocation 0
	OCU5_1		Output Compare Output pin ch.5 relocation 1
18	P035	H/I4[*1]	General-Purpose I/O Port
	A07		External Bus Address Output pin
	SEG21		LCDC Segment(Duty)Output pin
	SPI_SIO0		HS_SPI SDATA0 I/O pin (Not supported)
	SOT8_0		Multi-function Serial Output pin ch.8 relocation 0
	OCU4_1		Output Compare Output pin ch.4 relocation 1
19	P036	H/I4[*1]	General-Purpose I/O Port
	A08		External Bus Address Output pin
	SEG22		LCDC Segment(Duty)Output pin
	PPG11_0		PPG Output pin ch.11 relocation 0
	SPI_CLK		HS_SPI SCLK I/O pin (Not supported)
	SCK8_0		Multi-function Serial Clock I/O pin ch.8 relocation 0
22	P037	I	General-Purpose I/O Port
	A09		External Bus Address Output pin
	SEG23		LCDC Segment(Duty)Output pin
	ST0		LCDC Segment(Static)Output pin
	PPG12_0		PPG Output pin ch.12 relocation 0
	SIN7_0		LIN_UART Serial Input pin ch.7 relocation 0
23	P040	I	General-Purpose I/O Port
	A10		External Bus Address Output pin
	SEG24		LCDC Segment(Duty)Output pin
	ST1		LCDC Segment(Static)Output pin
	PPG13_0		PPG Output pin ch.13 relocation 0
	SOT7_0		LIN_UART Serial Output pin ch.7 relocation 0
24	P041	I	General-Purpose I/O Port
	A11		External Bus Address Output pin
	SEG25		LCDC Segment(Duty)Output pin
	ST2		LCDC Segment(Static)Output pin
	PPG14_0		PPG Output pin ch.14 relocation 0
	SCK7_0		LIN_UART Serial Clock I/O pin ch.7 relocation 0
25	P042	I	General-Purpose I/O Port
	A12		External Bus Address Output pin
	SEG26		LCDC Segment(Duty)Output pin
	ST3		LCDC Segment(Static)Output pin
	PPG15_0		PPG Output pin ch.15 relocation 0
	AIN0_0		Up/down Counter AIN Input pin ch.0 relocation 0

Pin Number	Pin Name	I/O Circuit Type	Function Description
27	VCC5	-	+5.0v Power Supply pin
28	VSS	-	GND pin
29	P010	H	General-Purpose I/O Port
	SEG0		LCDC Segment(Duty)Output pin
29	INT8_1	H	External Interrupt Request Input pin ch.8 relocation 1
30	P011	I	General-Purpose I/O Port
	SEG1		LCDC Segment(Duty)Output pin
	INT9_1		External Interrupt Request Input pin ch.9 relocation 1
31	P012	I	General-Purpose I/O Port
	SEG2		LCDC Segment(Duty)Output pin
	INT10_1		External Interrupt Request Input pin ch.10 relocation 1
32	P013	I	General-Purpose I/O Port
	SEG3		LCDC Segment(Duty)Output pin
	INT11_1		External Interrupt Request Input pin ch.11 relocation 1
33	P014	I	General-Purpose I/O Port
	SEG4		LCDC Segment(Duty)Output pin
	INT12_1		External Interrupt Request Input pin ch.12 relocation 1
34	P015	I	General-Purpose I/O Port
	SEG5		LCDC Segment(Duty)Output pin
	INT13_1		External Interrupt Request Input pin ch.13 relocation 1
35	P016	I	General-Purpose I/O Port
	SEG6		LCDC Segment(Duty)Output pin
	INT14_1		External Interrupt Request Input pin ch.14 relocation 1
36	P017	I	General-Purpose I/O Port
	SEG7		LCDC Segment(Duty)Output pin
	INT15_1		External Interrupt Request Input pin ch.15 relocation 1
37	P020	I	General-Purpose I/O Port
	SEG8		LCDC Segment(Duty)Output pin
	ICU6_0		Input Capture Input pin ch.6 relocation 0
	OCU0_1		Output Compare Output pin ch.0 relocation 1
38	P021	I	General-Purpose I/O Port
	SEG9		LCDC Segment(Duty)Output pin
	ICU7_0		Input Capture Input pin ch.7 relocation 0
	OCU1_1		Output Compare Output pin ch.1 relocation 1
39	P022	I	General-Purpose I/O Port
	SEG10		LCDC Segment(Duty)Output pin
	ICU8_0		Input Capture Input pin ch.8 relocation 0
	OCU2_1		Output Compare Output pin ch.2 relocation 1
40	P023	I	General-Purpose I/O Port
	SEG11		LCDC Segment(Duty)Output pin
	ICU9_0		Input Capture Input pin ch.9 relocation 0
	OCU3_1		Output Compare Output pin ch.3 relocation 1
41	P024	I	General-Purpose I/O Port
	SEG12		LCDC Segment(Duty)Output pin
	ICU10_0		Input Capture Input pin ch.10 relocation 0
	OCU11_0		Output Compare Output pin ch.11 relocation 0
42	P025	I	General-Purpose I/O Port
	SEG13		LCDC Segment(Duty)Output pin
	ICU11_0		Input Capture Input pin ch.11 relocation 0
	OCU10_0		Output Compare Output pin ch.10 relocation 0

Type	Circuit	Remarks
A		Mode pin
B		DEBUG I/F pin
R		CMOS level hysteresis input
R2		CMOS level hysteresis input
X		Main oscillation I/O
Y		Sub oscillation I/O

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000440_H	ICR00 [R/W] B, H, W ---11111	ICR01 [R/W] B, H, W ---11111	ICR02 [R/W] B, H, W ---11111	ICR03 [R/W] B, H, W ---11111	Interrupt controller [S]
000444_H	ICR04 [R/W] B, H, W ---11111	ICR05 [R/W] B, H, W ---11111	ICR06 [R/W] B, H, W ---11111	ICR07 [R/W] B, H, W ---11111	
000448_H	ICR08 [R/W] B, H, W ---11111	ICR09 [R/W] B, H, W ---11111	ICR10 [R/W] B, H, W ---11111	ICR11 [R/W] B, H, W ---11111	
$00044C_H$	ICR12 [R/W] B, H, W ---11111	ICR13 [R/W] B, H, W ---11111	ICR14 [R/W] B, H, W ---11111	ICR15 [R/W] B, H, W ---11111	
000450_H	ICR16 [R/W] B, H, W ---11111	ICR17 [R/W] B, H, W ---11111	ICR18 [R/W] B, H, W ---11111	ICR19 [R/W] B, H, W ---11111	
000454_H	ICR20 [R/W] B, H, W ---11111	ICR21 [R/W] B, H, W ---11111	ICR22 [R/W] B, H, W ---11111	ICR23 [R/W] B, H, W ---11111	
000458_H	ICR24 [R/W] B, H, W ---11111	ICR25 [R/W] B, H, W ---11111	ICR26 [R/W] B, H, W ---11111	ICR27 [R/W] B, H, W ---11111	
$00045C_H$	ICR28 [R/W] B, H, W ---11111	ICR29 [R/W] B, H, W ---11111	ICR30 [R/W] B, H, W ---11111	ICR31 [R/W] B, H, W ---11111	
000460_H	ICR32 [R/W] B, H, W ---11111	ICR33 [R/W] B, H, W ---11111	ICR34 [R/W] B, H, W ---11111	ICR35 [R/W] B, H, W ---11111	
000464_H	ICR36 [R/W] B, H, W ---11111	ICR37 [R/W] B, H, W ---11111	ICR38 [R/W] B, H, W ---11111	ICR39 [R/W] B, H, W ---11111	
000468_H	ICR40 [R/W] B, H, W ---11111	ICR41 [R/W] B, H, W ---11111	ICR42 [R/W] B, H, W ---11111	ICR43 [R/W] B, H, W ---11111	
$00046C_H$	ICR44 [R/W] B, H, W ---11111	ICR45 [R/W] B, H, W ---11111	ICR46 [R/W] B, H, W ---11111	ICR47 [R/W] B, H, W ---11111	
000470_H to $00047C_H$	—	—	—	—	Reserved [S]
000480_H	RSTRR [R] B,H,W XXXX--XX	RSTCR [R/W] B,H,W 111----0	STBCR [R/W] B,H,W * 000---11	—	Reset control [S] Power consumption control [S] *: Writing to STBCR by DMA is not permitted
000484_H	—	—	—	—	Reserved [S]

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$0004E0_H$	SCR8/(IBCR8) [R/W] B,H,W 0--00000	SMR8 [R/W] B,H,W 000-0000	SSR8 [R/W] B,H,W 0-000011	ESCR8/(IBSR8) [R/W] B,H,W -0000000	Multi-UART8 *1: Byte access is permitted only for access to lower 8 bits
$0004E4_H$	RDR8/(TDR8)[R/W] B,H,W *1 -------0 00000000		BGR8 [R/W] H,W 00000000 00000000		
$0004E8_H$	—	—	—	—	
$0004EC_H$	FCR18 [R/W] B,H,W ---00100	FCR08 [R/W] B,H,W -0000000	FBYTE28 [R/W] B,H,W 00000000	FBYTE18 [R/W] B,H,W 00000000	
$0004F0_H$	SCR9/(IBCR9) [R/W] B,H,W 0--00000	SMR9 [R/W] B,H,W 000-0000	SSR9 [R/W] B,H,W 0-000011	ESCR9/(IBSR9) [R/W] B,H,W -0000000	Multi-UART9 *1: Byte access is permitted only for access to lower 8 bits
$0004F4_H$	RDR9/(TDR9)[R/W] B,H,W *1 -------0 00000000		BGR9 [R/W] H,W 00000000 00000000		
$0004F8_H$	—	—	—	—	
$0004FC_H$	FCR19 [R/W] B,H,W ---00100	FCR09 [R/W] B,H,W -0000000	FBYTE29 [R/W] B,H,W 00000000	FBYTE19 [R/W] B,H,W 00000000	
000500_H to $00050C_H$	—	—	—	—	Reserved
000510_H	CSELR [R/W] B,H,W 001---00	CMONR [R] B,H,W 001---00	MTMCR [R/W] B,H,W 00001111	STMCR [R/W] B,H,W 0000-111	Clock control [S]
000514_H	PLLCR [R/W] B,H,W -------- 11110000		CSTBR [R/W] B,H,W -0000000	PTMCR [R/W] B,H,W 00------	
000518_H	—	—	CPUAR [R/W] B,H,W 0----XXX	—	Reset [S]
$00051C_H$	—	—	—	—	Reserved [S]
000520_H	CCPSSELR [R/W] B,H,W -------0	—	—	CCPSDIVR [R/W] B,H,W -000-000	Clock control 2
000524_H	—	CCPLLFBR [R/W] B,H,W -0000000	CCSSFBR0 [R/W] B,H,W --000000	CCSSFBR1 [R/W] B,H,W ---00000	
000528_H	—	CCSSCCR0 [R/W] B,H,W ----0000	CCSSCCR1[R/W]H,W 000----- --------		
$00052C_H$	—	CCCGRCR0 [R/W] B,H,W 00----00	CCCGRCR1 [R/W] B,H,W 00000000	CCCGRCR2 [R/W] B,H,W 00000000	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$000E00_H$	DDR00[R/W] B,H,W 00000000	DDR01[R/W] B,H,W 00000000	DDR02[R/W] B,H,W 00000000	DDR03[R/W] B,H,W 00000000	Data direction Register *4:MB91F578/9 only
$000E04_H$	DDR04[R/W] B,H,W 00000000	DDR05[R/W] B,H,W -0000000	DDR06[R/W] B,H,W 00000000	DDR07[R/W] B,H,W 00000000	
$000E08_H$	DDR08[R/W] B,H,W 00000000	DDR09[R/W] B,H,W 00000000	DDR10[R/W] B,H,W 00000000	DDR11[R/W] B,H,W 00000000	
$000E0C_H$	DDR12[R/W] B,H,W 00000000	DDR13[R/W] B,H,W 00-00000	DDR14[R/W] B,H,W 00000000*4	DDR15[R/W] B,H,W 00000000*4	
$000E10_H$	DDR16[R/W] B,H,W 00000000*4	DDR17[R/W] B,H,W 00000000*4	DDR18[R/W] B,H,W 00000000*4	DDR19[R/W] B,H,W 00000000*4	
$000E14_H$ to $000E1C_H$	—	—	—	—	Reserved
$000E20_H$	PFR00[R/W] B,H,W 00000000	PFR01[R/W] B,H,W 00000000	PFR02[R/W] B,H,W 00000000	PFR03[R/W] B,H,W 10000000	Port function register *4:MB91F578/9 only
$000E24_H$	PFR04[R/W] B,H,W 11111111	PFR05[R/W] B,H,W 11111111	PFR06[R/W] B,H,W 00000000	PFR07[R/W] B,H,W 00000000	
$000E28_H$	PFR08[R/W] B,H,W 00000000	PFR09[R/W] B,H,W 0-000000	PFR10[R/W] B,H,W 00000000	PFR11[R/W] B,H,W 00000000	
$000E2C_H$	PFR12[R/W] B,H,W 00000000	PFR13[R/W] B,H,W 00-00000	PFR14[R/W] B,H,W 00000000*4	PFR15[R/W] B,H,W 00000000*4	
$000E30_H$	PFR16[R/W] B,H,W 00000000*4	PFR17[R/W] B,H,W 00000000*4	PFR18[R/W] B,H,W 00000000*4	PFR19[R/W] B,H,W 00000000*4	
$000E34_H$ to $000E3C_H$	—	—	—	—	Reserved
$000E40_H$	PDDR00[R] B,H,W XXXXXXXX	PDDR01[R] B,H,W XXXXXXXX	PDDR02[R] B,H,W XXXXXXXX	PDDR03[R] B,H,W XXXXXXXX	Input data direct read register *4:MB91F578/9 only
$000E44_H$	PDDR04[R] B,H,W XXXXXXXX	PDDR05[R] B,H,W XXXXXXXX	PDDR06[R] B,H,W XXXXXXXX	PDDR07[R] B,H,W XXXXXXXX	
$000E48_H$	PDDR08[R] B,H,W XXXXXXXX	PDDR09[R] B,H,W XXXXXXXX	PDDR10[R] B,H,W XXXXXXXX	PDDR11[R] B,H,W XXXXXXXX	
$000E4C_H$	PDDR12[R] B,H,W XXXXXXXX	PDDR13[R] B,H,W XX-XXXXX	PDDR14[R] B,H,W XXXXXXXX*4	PDDR15[R] B,H,W XXXXXXXX*4	
$000E50_H$	PDDR16[R] B,H,W XXXXXXXX*4	PDDR17[R] B,H,W XXXXXXXX*4	PDDR18[R] B,H,W XXXXXXXX*4	PDDR19[R] B,H,W XXXXXXXX*4	
$000E54_H$ to $000E5C_H$	—	—	—	—	Reserved

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$000EA0_H$	PPCR00[R/W] B,H,W 11111111	PPCR01[R/W] B,H,W 11111111	PPCR02[R/W] B,H,W 11111111	PPCR03[R/W] B,H,W 11111111	Port pull-up/down control register *4:MB91F578/9 only
$000EA4_H$	PPCR04[R/W] B,H,W 11111111	PPCR05[R/W] B,H,W 11111111	PPCR06[R/W] B,H,W 11111111	PPCR07[R/W] B,H,W 11111111	
$000EA8_H$	PPCR08[R/W] B,H,W 11111111	PPCR09[R/W] B,H,W 11111111	PPCR10[R/W] B,H,W 11111111	PPCR11[R/W] B,H,W 11111111	
$000EAC_H$	PPCR12[R/W] B,H,W 11111111	PPCR13[R/W] B,H,W 11-11111	PPCR14[R/W] B,H,W 11111111*4	PPCR15[R/W] B,H,W 11-11111*4	
$000EB0_H$	PPCR16[R/W] B,H,W 11111111*4	PPCR17[R/W] B,H,W 11111111*4	PPCR18[R/W] B,H,W 11111111*4	PPCR19[R/W] B,H,W 11-11111*4	
$000EBC_H$	—	—	—	—	Reserved
$000EC0_H$	PPER00[R/W] B,H,W 00000000	PPER01[R/W] B,H,W 00000000	PPER02[R/W] B,H,W 00000000	PPER03[R/W] B,H,W 00000000	Port pull-up/down enable register *4:MB91F578/9 only
$000EC4_H$	PPER04[R/W] B,H,W 00000000	PPER05[R/W] B,H,W 00000000	PPER06[R/W] B,H,W 00000000	PPER07[R/W] B,H,W 00000000	
$000EC8_H$	PPER08[R/W] B,H,W 00000000	PPER09[R/W] B,H,W 00000000	PPER10[R/W] B,H,W 00000000	PPER11[R/W] B,H,W 00000000	
$000ECC_H$	PPER12[R/W] B,H,W 00000000	PPER13[R/W] B,H,W 00-00000	PPER14[R/W] B,H,W 00000000*4	PPER15[R/W] B,H,W 00000000*4	
$000ED0_H$	PPER16[R/W] B,H,W 00000000*4	PPER17[R/W] B,H,W 00000000*4	PPER18[R/W] B,H,W 00000000*4	PPER19[R/W] B,H,W 00000000*4	
$000EDC_H$	—	—	—	—	Reserved
$000EE0_H$	PILR00[R/W] B,H,W 11111111	PILR01[R/W] B,H,W 11111111	PILR02[R/W] B,H,W 11111111	PILR03[R/W] B,H,W 11111111	Port input level selection register *4:MB91F578/9 only
$000EE4_H$	PILR04[R/W] B,H,W 11111111	PILR05[R/W] B,H,W 11111111	PILR06[R/W] B,H,W 11111111	PILR07[R/W] B,H,W 11111111	
$000EE8_H$	PILR08[R/W] B,H,W 11111111	PILR09[R/W] B,H,W 11111111	PILR10[R/W] B,H,W 11111111	PILR11[R/W] B,H,W 11111111	
$000EEC_H$	PILR12[R/W] B,H,W 11111111	PILR13[R/W] B,H,W 11-11111	PILR14[R/W] B,H,W 11111111*4	PILR15[R/W] B,H,W 11111111*4	
$000EF0_H$	PILR16[R/W] B,H,W 11111111*4	PILR17[R/W] B,H,W 11111111*4	PILR18[R/W] B,H,W 11111111*4	PILR19[R/W] B,H,W 11111111*4	
$000EFC_H$	—	—	—	—	Reserved

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$000FD0_H$	IPCP6 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input capture 6,7
$000FD4_H$	IPCP7 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000FD8_H$	ICFS67 [R/W] B, H, W ------00	—	LSYNS1 [R/W] B,H,W ----0000	ICS67 [R/W] B, H, W 00000000	
$000FDC_H$	IPCP8 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input capture 8,9
$000FE0_H$	IPCP9 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000FE4_H$	ICFS89 [R/W] B, H, W ------00	—	—	ICS89 [R/W] B, H, W 00000000	
$000FE8_H$	IPCP10 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input capture 10,11
$000FEC_H$	IPCP11 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000FF0_H$	ICFS1011 [R/W] B, H, W ------00	—	—	ICS1011 [R/W] B, H, W 00000000	
$000FF4_H$ to $000FFC_H$	—	—	—	—	Reserved
001000_H	SACR [R/W] B,H,W -------0	PICD [R/W] B,H,W ----0011	—	—	Clock control
001004_H to $00103C_H$	—	—	—	—	Reserved
001040_H	—	SGDER0 [R/W] B,H,W 00000000	SGCR0[R/W] B,H,W -0000-0- 000--000		Sound generator 0
001044_H	SGAR0[R/W] B,H,W 00000000 00000000		SGFR0[R/W] B,H,W 00000000	SGNR0[R/W] B,H,W 00000000	
001048_H	SGTCR0[R/W] B,H,W 00000000	SGIDR0[R/W] B,H,W 00000000	SGPCR0[R/W] B,H,W 00000000 11111111		
$00104C_H$	SGDMAR0[W] B,H,W 00000000 00000000 00000000 00000000				
001050_H to $00105C_H$	—	—	—	—	Reserved
001060_H	—	SGDER1[R/W] B,H,W 00000000	SGCR1[R/W] B,H,W -0000-0- 000--000		Sound generator 1
001064_H	SGAR1[R/W] B,H,W 00000000 00000000		SGFR1[R/W] B,H,W 00000000	SGNR1[R/W] B,H,W 00000000	
001068_H	SGTCR1[R/W] B,H,W 00000000	SGIDR1[R/W] B,H,W 00000000	SGPCR1[R/W] B,H,W 00000000 11111111		
$00106C_H$	SGDMAR1[W] B,H,W 00000000 00000000 00000000 00000000				

(T_A: Recommended operating conditions, $V_{CC}5$ = 5.0V±10%, $V_{CC}E$ = 5.0V±10%, V_{SS} = DV_{SS} = AV_{SS} = 0.0V)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	$I_{CC}5$	$V_{CC}5$	At normal operation Operating frequency F_{CP} = 80MHz, Fcpp = 40MHz	—	60	100	mA	*4
						125		*5
			FLASH write Operating frequency F_{CP} = 80MHz, Fcpp = 40MHz	—	75	115	mA	*3, *4
						140		*3, *5
			At FLASH erase Operating frequency F_{CP} = 80MHz, Fcpp = 40MHz	—	75	115	mA	*3, *4
						140		*3, *5
	$I_{CCS}5$		At sleep mode Operating frequency F_{CP} = 80MHz, Fcpp = 40MHz	—	20	60	mA	*4
						75		*5
	$I_{CCBS}5$		At bus sleep mode Operating frequency F_{CP} = 80MHz, Fcpp = 40MHz	—	15	55	mA	*4
						70		*5
	$I_{CCT}5$		At RTC mode 4MHz source oscillation	—	750	1400	µA	When using external clock*1, T_A = 25˚C
				—	900	1550	µA	When using crystal, T_A = 25˚C
	$I_{CCTS}5$		At RTC mode shutdown 4MHz source oscillation	—	170	330	µA	When using external clock*1, T_A = 25˚C
				—	320	480	µA	When using crystal, T_A = 25˚C
	$I_{CCH}5$		At stop mode	—	400	1200	µA	T_A = 25˚C
	$I_{CCHS}5$		At stop mode shutdown	—	120	240	µA	T_A = 25˚C

13.4.4 Power-on Conditions

(T_A: Recommended operating conditions, V_{SS} = 0.0V)

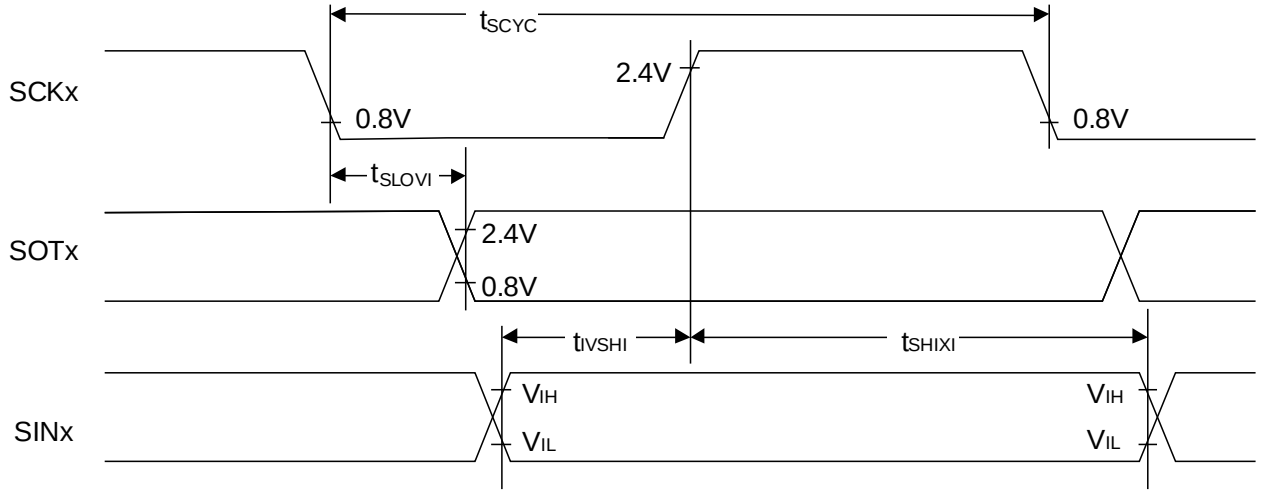
Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Level detection voltage	–	$V_{CC}5$	–	2.1	2.3	2.5	V	When turning on power for microcontroller
Level detection hysteresis width	–	$V_{CC}5$	–	–	–	125	mV	During voltage drop
Level detection time	–	–	–	–	–	30	us	*1
Slope detection undetected standard	–	$V_{CC}5$	$V_{CC}5$ = at level detection release level time	–	–	4	mV/µs	*2
Power off time	t_{OFF}	$V_{CC}5$	–	50	–	–	ms	*3

*1: If the fluctuation of the power supply is faster than the low voltage detection time, there is the possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

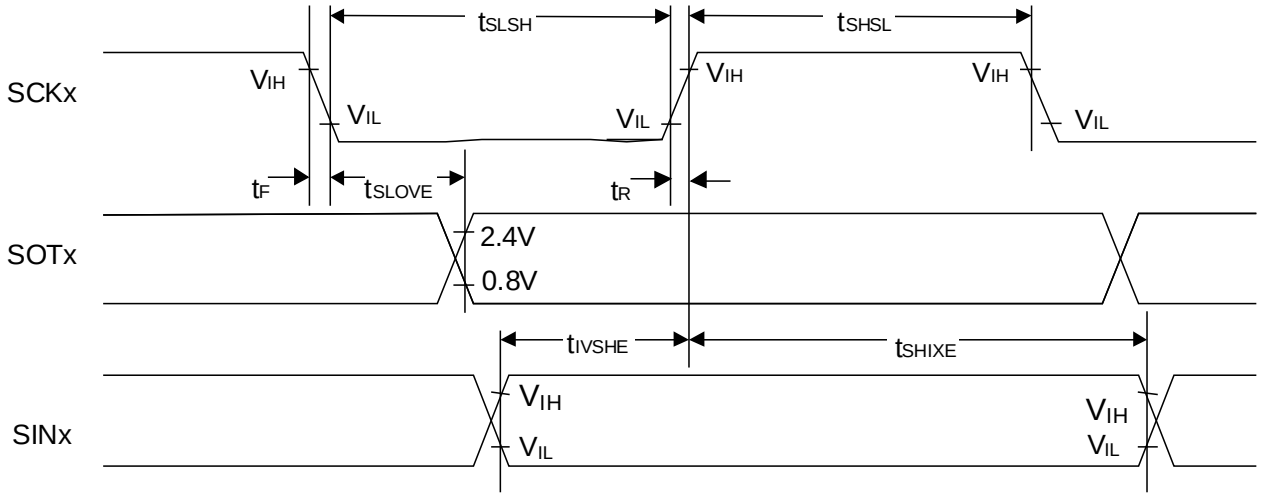
*2: When setting the power supply fluctuation to this standard or less, it is possible to suppress the slope detection. This is the standard when the power supply fluctuation is stable.

*3: This time is to start the slope detection at next power on after power down and internal charge loss

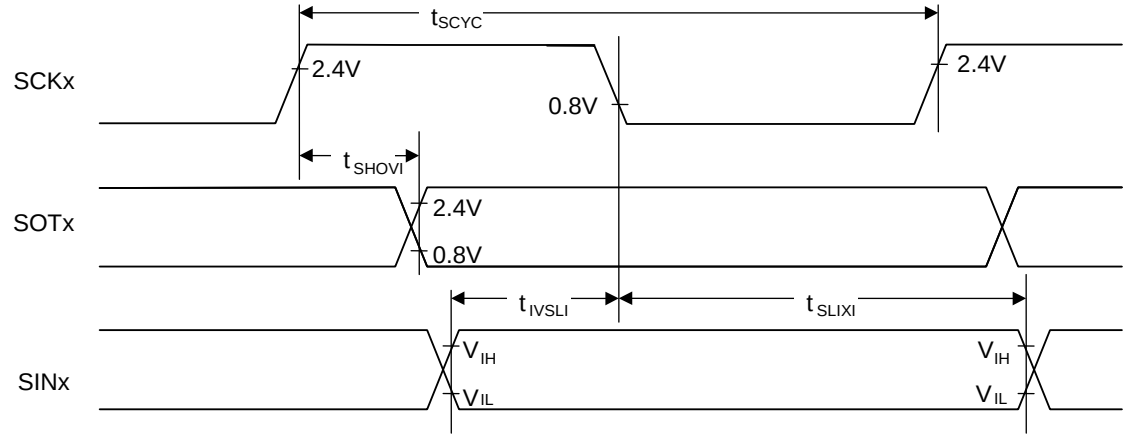
• Internal shift clock mode



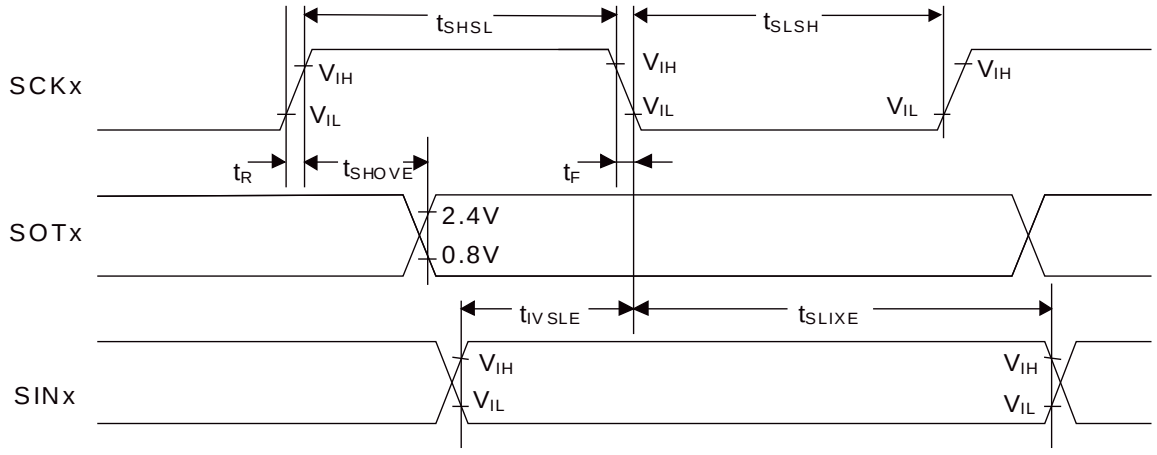
• External shift clock mode



Internal shift clock mode



External shift clock mode



Bit setting: ESCR: SCES = 0, ECCR: SCDE = 1

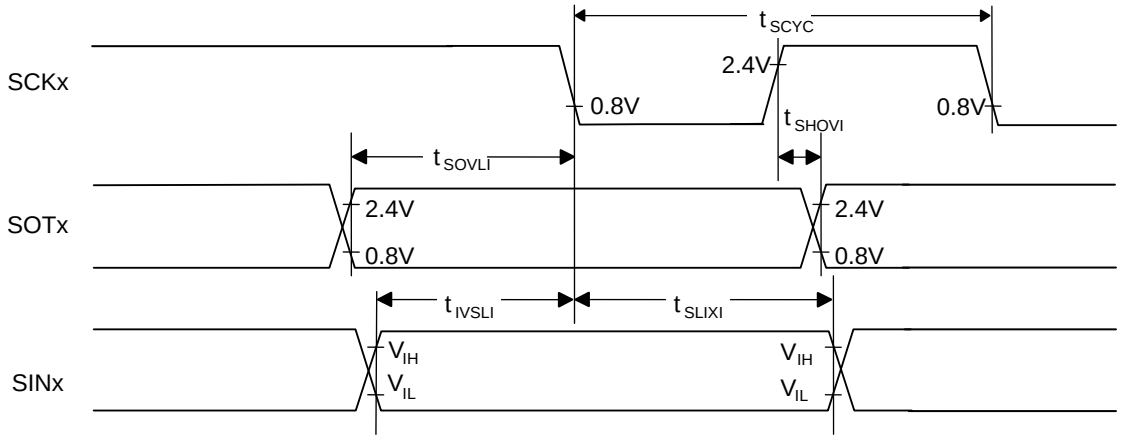
(T_A: Recommended operating conditions, $V_{CC}5$ = 5.0V±10%, $V_{CC}E$ = 5.0V±10%, V_{SS} = AV_{SS} = 0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7	–	$5t_{CPP}$	–	ns	Internal shift clock mode: C_L=80pF+1 • TTL
SCK ↑→ SOT delay time	t_{SHOVI}	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7, SOT2,SOT3, SOT4,SOT5, SOT6,SOT7		-50	+50	ns	
Valid SIN → SCK ↓setup time	t_{IVSLI}	SCK2,SCK3,SCK4, SCK5,SCK6,SCK7, SIN2,SIN3, SIN4,SIN5, SIN6,SIN7		t_{CPP}+80	–	ns	
SCK ↓→ Valid SIN hold time	t_{SLIXI}			0	–	ns	
SOT → SCK ↓ delay time	t_{SOVLI}	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7, SOT2,SOT3, SOT4,SOT5, SOT6,SOT7		$3t_{CPP}$-70	–	ns	

Notes:

- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operation clock used and other parameters. Refer to Hardware Manual for details.

Internal shift clock mode



13.4.14 External bus I/F (synchronous mode) timing

(T_A: Recommended operating conditions, $V_{CC}5 = V_{CC}E = AV_{CC} = 5.0V \pm 10\%$, $V_{SS} = AV_{SS} = 0.0V$)
(External load capacitance 50pF)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Cycle time	t_{CYC}	SYSCLK	25	–	ns	
ASX delay time	t_{CHASL}, t_{CHASH}	SYSCLK, ASX	0.5	18	ns	
CS0X to CS3X delay time	t_{CHCSL}, t_{CHCSH}	SYSCLK, CS0X to CS3X	0.5	18	ns	
A00 to A21 delay time	t_{CHAV}, t_{CHAX}	SYSCLK, A00 to A21	0.5	18	ns	
RDX delay time	t_{CHRL}, t_{CHRH}	SYSCLK, RDX	0.5	18	ns	
RDX minimum pulse	t_{RLRH}	RDX	t_{CYC}× 2 - 20	–	ns	RWT=1, set RWT to 1 or more. *
Data setup → RDX ↑ time	t_{DSRH}	RDX, D16 to D31	18 + t_{CYC}	–	ns	RWT=1, set RWT to 1 or more. *
RDX ↑→ data hold	t_{RHDH}		0	–	ns	
WRnX delay time	t_{CHWL}, t_{CHWH}	SYSCLK, WR0X, WR1X	0.5	18	ns	
WRnX minimum pulse width	t_{WLWH}	WR0X, WR1X	t_{CYC} - 10	–	ns	WWT=0 *
SYSCLK ↑→ data output time	t_{CHDV}	SYSCLK, D16 to D31	0.5	18	ns	
SYSCLK ↑→ data hold time	t_{CHDX}		–	18	ns	Set WRCS to 1 or more.
SYSCLK ↑→ address output time	t_{CHMAV}	SYSCLK, D16 to D31	0.5	18	ns	
SYSCLK ↑→ address hold time	t_{CHMAX}		–	18	ns	In multiplex mode, set as follows: Set CSWR and CSRD to 2 or more. ASCY must satisfy the following conditions because of setting ADCY>ASCY and protocol violation prevention. ADCY + 1 ≤ ACS + CSRD ADCY + 1 ≤ ACS + CSWR ASCY + 1 ≤ ACS + CSRD ASCY + 1 ≤ ACS + CSWR Refer to Hardware Manual for details.

*: If the bus is expanded by automatic wait insertion or RDY input, add time (t_{CYC} × the number of expanded cycles) to the rated value.

13.4.17 HS-SPI timing

(T_A: Recommended operating conditions, $V_{CC}5 = V_{CC}E = AV_{CC} = 5.0V \pm 10\%$, $V_{SS} = AV_{SS} = 0.0V$)
(External load capacitance 20pF)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYCM}	SPI_CLK	Master	62.5	—	ns	*1 *2
			Slave	100	—	ns	
Valid CS → CLK start time (mode0/mode2)	$t_{OSLSK02}$	SPI_CLK, SPI_CS0, SPI_CS1, SPI_CS2, SPI_CS3	—	$1.5 \times t_{SCYCM} - 15$	—	ns	
Valid CS → CLK start time (mode1/mode3)	$t_{OSLSK13}$			$t_{SCYCM} - 15$	—	ns	
CLK end → Invalid CS time (mode0/mode2)	$t_{OSKSL02}$			t_{SCYCM} -10	—	ns	
CLK end → Invalid CS time (mode1/mode3)	$t_{OSKSL13}$			$1.5 \times t_{SCYCM}$ -10	—	ns	
SIO data output time	t_{OSDAT}	SPI_CLK, SPI_SIO0, SPI_SIO1, SPI_SIO2, SPI_SIO3	Master	-10	15	ns	
			Slave	—	28	ns	
SIO setup	t_{DSSET}	SPI_CLK, SPI_SIO0, SPI_SIO1, SPI_SIO2, SPI_SIO3	—	22	—	ns	
SIO hold	t_{SDHOLD}			$0.5 \times t_{SCYCM}$	—	ns	

*1: $V_{CC}E = 5.0V \pm 10\%$, or $V_{CC}E = 3.0$ to $3.6V$

*2: In the voltage range shown in *1, this parameter is defined when IOH is -2mA and IOL is 2mA.

13.7 Flash memory

13.7.1 Electrical characteristics

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	–	200	800	ms	8 Kbyte sector*1, excluding internal preprogramming time
	–	300	1100	ms	8 Kbyte sector*1, including internal preprogramming time
	–	400	2000	ms	64 Kbyte sector*1, excluding internal preprogramming time
	–	700	3700	ms	64 Kbyte sector*1, including internal preprogramming time
8-bit writing time	–	9	288	µs	Exclusive of overhead time at system level*1
16-bit writing time	–	12	384	µs	Exclusive of overhead time at system level*1
ECC writing time	–	9	288	µs	Exclusive of overhead time at system level*1
Erase cycle*2/ Data retain time	1,000 cycles/ 20 years, 10,000 cycles/ 10 years, 100,000 cycles/ 5 years	–	–	–	Average T_A = +85°C*3

*1: The guaranteed value for erasure up to 100,000 cycles.

*2: Number of erase cycles for each sector.

*3: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85°C).

13.7.2 Notes

While the Flash memory is written or erased, shutdown of the external power ($V_{CC}5$) is prohibited.

In the application system where $V_{CC}5$ might be shut down while writing or erased, be sure to turn the power off by using an external low-voltage detection function.

To put it concretely, after the external power supply voltage falls below the detection voltage (V_{DL}*1), hold $V_{CC}5$ at 2.7V or more within the duration calculated by the following expression:

$$Td^{*1}[\mu s] + (\text{period of PCLK } [\mu s] \times 257) + 50\ [\mu s]$$

*1: See “13.4. AC characteristics, 13.4.10. Low voltage detection (External low-voltage detection)”.