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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	16MHz
Connectivity	I²C
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	5
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	D/A 1x7b, 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.154", 3.90mm Width)
Supplier Device Package	8-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4013sxi-410t

More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article KBA86521, How to Design with PSoC 3, PSoC 4, and PSoC 5LP. Following is an abbreviated list for PSoC 4:

- Overview: PSoC Portfolio, PSoC Roadmap
- Product Selectors: PSoC 1, PSoC 3, PSoC 4, PSoC 5LP
  In addition, PSoC Creator includes a device selection tool.
- Application notes: Cypress offers a large number of PSoC application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with PSoC 4 are:
  - AN79953: Getting Started With PSoC 4
  - AN88619: PSoC 4 Hardware Design Considerations
  - AN86439: Using PSoC 4 GPIO Pins
  - AN57821: Mixed Signal Circuit Board Layout
  - AN81623: Digital Design Best Practices
  - AN73854: Introduction To Bootloaders
  - AN89610: ARM Cortex Code Optimization
- Technical Reference Manual (TRM) is in two documents:
  - Architecture TRM details each PSoC 4 functional block.
  - Registers TRM describes each of the PSoC 4 registers.
- Development Kits:
  - CY8CKIT-040, PSoC 4000 Pioneer Kit, is an easy-to-use and inexpensive development platform with debugging capability. This kit includes connectors for Arduino™ compatible shields and Digilent® Pmod™ daughter cards.
  - The MiniProg3 device provides an interface for flash programming and debug.

PSoC Creator

PSoC Creator is a free Windows-based Integrated Design Environment (IDE). It enables concurrent hardware and firmware design of PSoC 3, PSoC 4, and PSoC 5LP based systems. Create designs using classic, familiar schematic capture supported by over 100 pre-verified, production-ready PSoC Components; see the list of component datasheets. With PSoC Creator, you can:

1. Drag and drop component icons to build your hardware system design in the main design workspace
2. Codesign your application firmware with the PSoC hardware, using the PSoC Creator IDE C compiler
3. Configure components using the configuration tools
4. Explore the library of 100+ components
5. Review component datasheets

Figure 1. CapSense Example Project in PSoC Creator

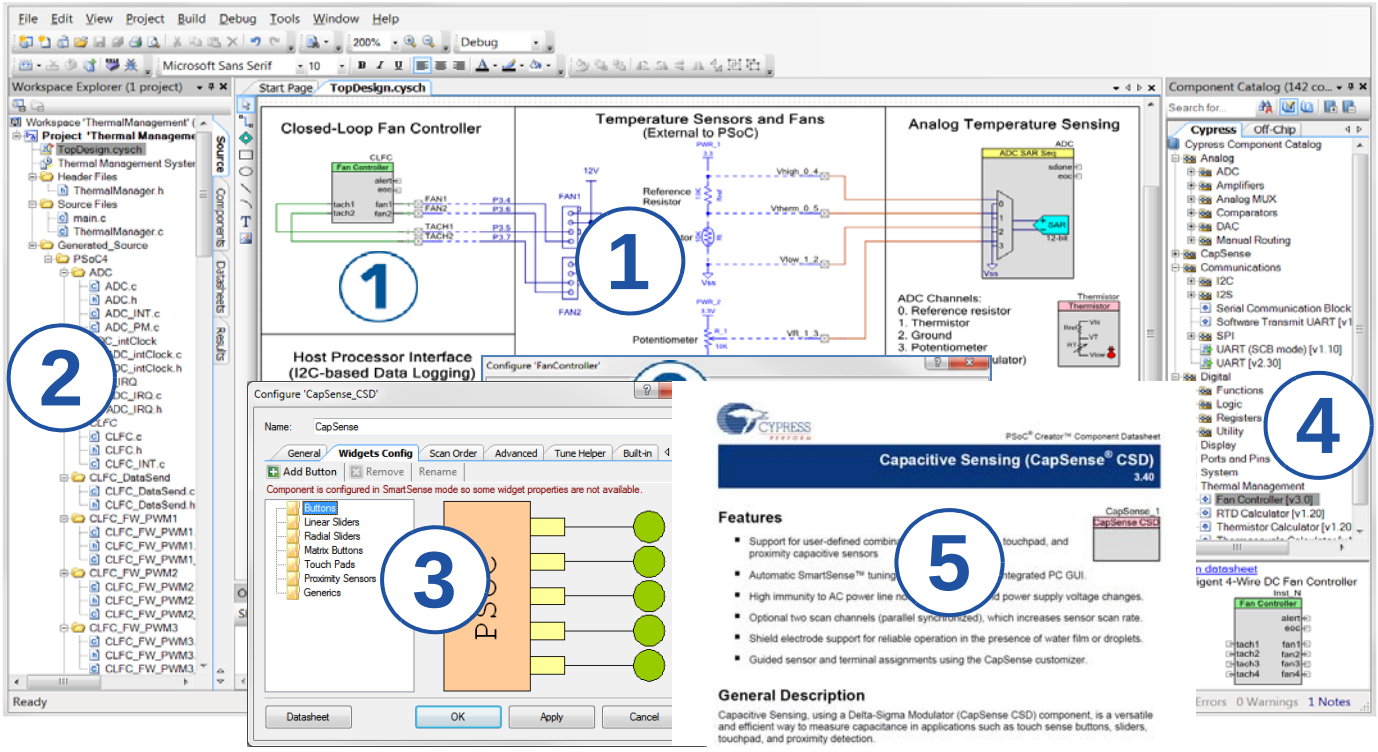
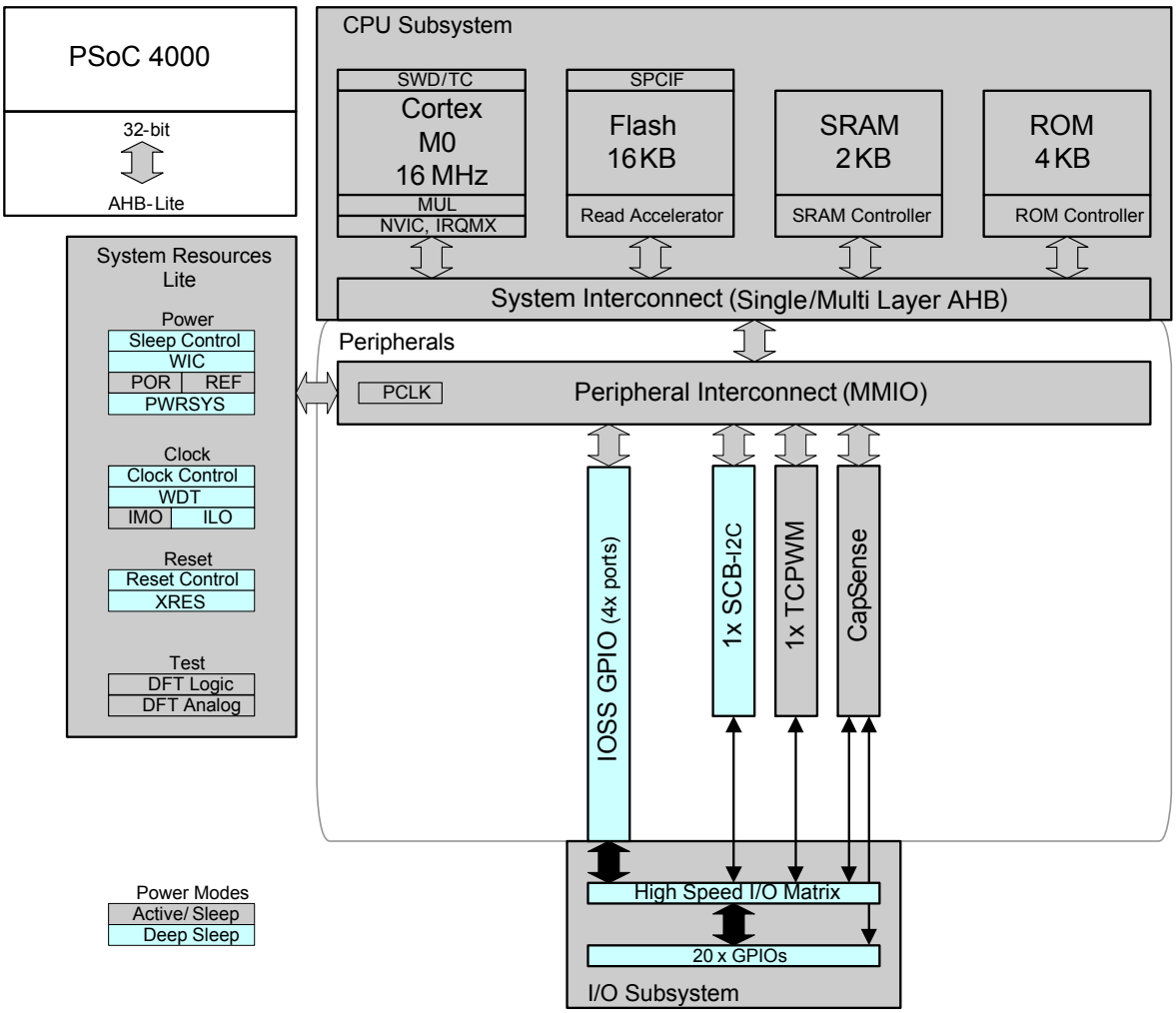


Figure 2. Block Diagram



PSoC 4000 devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware.

The ARM Serial-Wire Debug (SWD) interface supports all programming and debug features of the device.

Complete debug-on-chip functionality enables full-device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC Creator IDE provides fully integrated programming and debug support for the PSoC 4000 devices. The SWD interface is fully compatible with industry-standard third-party tools. The PSoC 4000 family provides a level of security not possible with multi-chip application solutions or with microcontrollers. It has the following advantages:

- Allows disabling of debug features
- Robust flash protection
- Allows customer-proprietary functionality to be implemented in on-chip programmable blocks

The debug circuits are enabled by default and can only be disabled in firmware. If they are not enabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables debugging.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. All programming, debug, and test interfaces are disabled when maximum device security is enabled. Therefore, PSoC 4000, with device security enabled, may not be returned for failure analysis. This is a trade-off the PSoC 4000 allows the customer to make.

Pinouts

All port pins support GPIO. Ports 0, 1, and 2 support CSD CapSense and analog multiplexed bus connections. TCPWM functions and Alternate Functions are multiplexed with port pins as follows for the five PSoC 4000 packages.

Table 1. Pin Descriptions

28-Pin SSOP		24-Pin QFN		16-Pin QFN		16-Pin SOIC		8-Pin SOIC			
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	TCPWM Signals	Alternate Functions
20	VSS										
21	P0.0/TRIN0	1	P0.0/TRIN0							TRIN0: Trigger Input 0	
22	P0.1/TRIN1/CMPO_0	2	P0.1/TRIN1/CMPO_0	1	P0.1/TRIN1/CMPO_0	3	P0.1/TRIN1/CMPO_0			TRIN1: Trigger Input 1	CMPO_0: Sense Comp Out
23	P0.2/TRIN2	3	P0.2/TRIN2	2	P0.2/TRIN2	4	P0.2/TRIN2			TRIN2: Trigger Input 2	
24	P0.3/TRIN3	4	P0.3/TRIN3							TRIN3: Trigger Input 3	
25	P0.4/TRIN4/CMPO_0/EXT_CLK	5	P0.4/TRIN4/CMPO_0/EXT_CLK	3	P0.4/TRIN4/CMPO_0/EXT_CLK	5	P0.4/TRIN4/CMPO_0/EXT_CLK	2	P0.4/TRIN4/CMPO_0/EXT_CLK	TRIN4: Trigger Input 4	CMPO_0: Sense Comp Out, External Clock, CMOD Cap
26	VCC	6	VCC	4	VCC	6	VCC	3	VCC		
27	VDD	7	VDD	6	VDD	7	VDD	4	VDD		
28	VSS	8	VSS	7	VSS	8	VSS	5	VSS		
1	P0.5	9	P0.5	5	VDDIO	9	P0.5				
2	P0.6	10	P0.6	8	P0.6	10	P0.6				
3	P0.7	11	P0.7								
4	P1.0	12	P1.0								
5	P1.1/OUT0	13	P1.1/OUT0	9	P1.1/OUT0	11	P1.1/OUT0	6	P1.1/OUT0	OUT0: PWM OUT 0	
6	P1.2/SCL	14	P1.2/SCL	10	P1.2/SCL	12	P1.2/SCL				I2C Clock
7	P1.3/SDA	15	P1.3/SDA	11	P1.3/SDA	13	P1.3/SDA				I2C Data
8	P1.4/UND0	16	P1.4/UND0							UND0: Underflow Out	
9	P1.5/OVF0	17	P1.5/OVF0							OVF0: Overflow Out	
10	P1.6/OVF0/UND0/nOUT0 /CMPO_0	18	P1.6/OVF0/UND0/nOUT0 /CMPO_0	12	P1.6/OVF0/UND0/nOUT0/CMPO_0	14	P1.6/OVF0/UND0/nOUT0/CMPO_0	7	P1.6/OVF0/UND0/nOUT0/CMPO_0	nOUT0: Complement of OUT0, UND0, OVF0 as above	CMPO_0: Sense Comp Out, Internal Reset function[1]

Note
1. Must not have load to ground during POR (should be an output).

Table 1. Pin Descriptions *(continued)*

28-Pin SSOP		24-Pin QFN		16-Pin QFN		16-Pin SOIC		8-Pin SOIC			
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	TCPWM Signals	Alternate Functions
11	VSS										
12	No Connect (NC)[2]										
13	P1.7/MATCH/EXT_CLK	19	P1.7/MATCH/EXT_CLK	13	P1.7/MATCH/EXT_CLK	15	P1.7/MATCH/EXT_CLK			MATCH: Match Out	External Clock
14	P2.0	20	P2.0			16	P2.0				
15	VSS										
16	P3.0/SDA/SWD_IO	21	P3.0/SDA/SWD_IO	14	P3.0/SDA/SWD_IO	1	P3.0/SDA/SWD_IO	8	P3.0/SDA/SWD_IO		I2C Data, SWD I/O
17	P3.1/SCL/SWD_CLK	22	P3.1/SCL/SWD_CLK	15	P3.1/SCL/SWD_CLK	2	P3.1/SCL/SWD_CLK	1	P3.1/SCL/SWD_CLK		I2C Clock, SWD Clock
18	P3.2	23	P3.2	16	P3.2					OUT0:PWM OUT 0	
19	XRES	24	XRES								XRES: External Reset

Descriptions of the Pin functions are as follows:

VDD: Power supply for both analog and digital sections.

VDDIO: Where available, this pin provides a separate voltage domain (see the Power section for details).

VSS: Ground pin.

VCCD: Regulated digital supply (1.8 V ±5%).

Pins belonging to Ports 0, 1, and 2 can all be used as CSD sense or shield pins connected to AMUXBUS A or B. They can also be used as GPIO pins that can be driven by the firmware, in addition to their alternate functions listed in the Table 1.

Pins on Port 3 can be used as GPIO, in addition to their alternate functions listed above.

The following packages are provided: 28-pin SSOP, 24-pin QFN, 16-pin QFN, 16-pin SOIC, and 8-pin SOIC.

Note
2. This pin is not to be used; it must be left floating.

Figure 4. 28-Pin SSOP Pinout

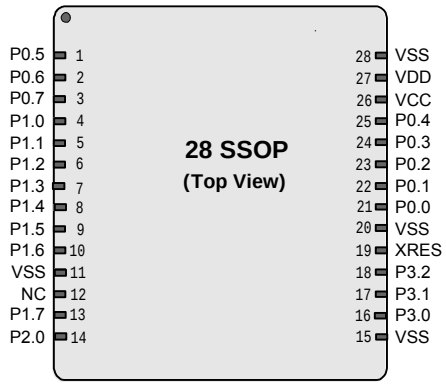


Figure 5. 24-pin QFN Pinout

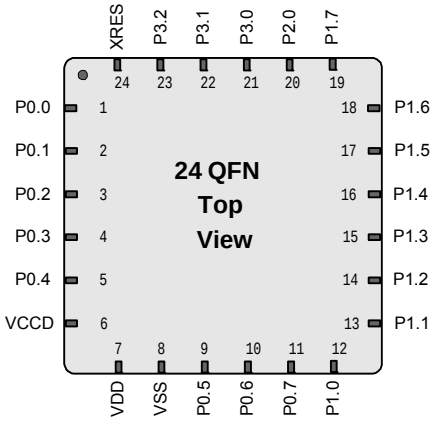


Figure 6. 16-Pin QFN Pinout

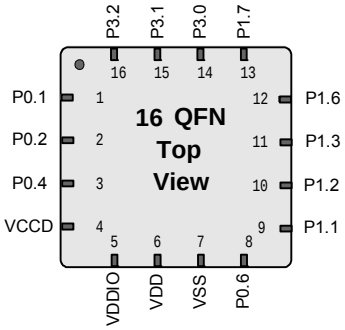
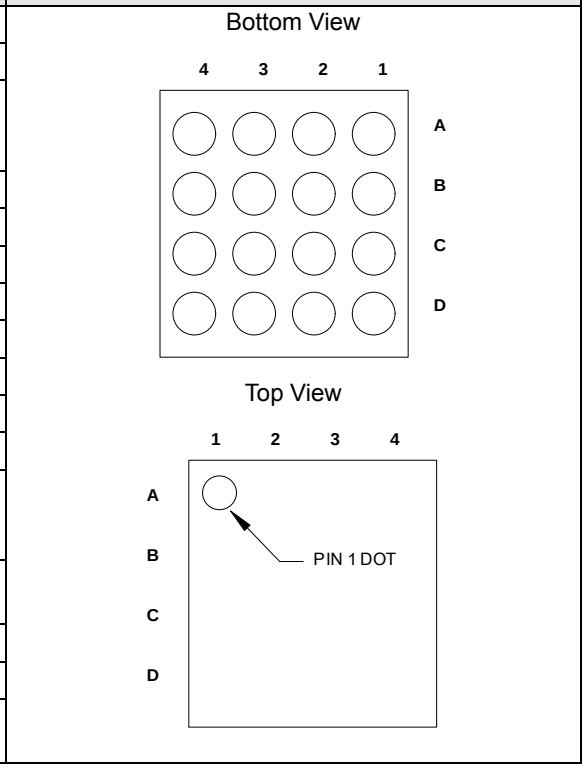


Table 2. 16-ball WLCSP Pin Descriptions and Diagram

Pin	Name	TCPWM Signal	Alternate Functions	Pin Diagram
B4	P3.2	OUT0:PWMOUT0	–	
C3	P0.2/TRIN2	TRIN2:Trigger Input 2	–	
C4	P0.4/TRIN4/CMPO_0/ EXT_CLK	TRIN4:Trigger Input 4	CMPO_0: Sense Comp Out, Ext. Clock, CMOD Cap	
D4	VCCD	–	–	
D3	VDD	–	–	
D2	VSS	–	–	
C2	VDDIO	–	–	
D1	P0.6	–	–	
C1	P1.1/OUT0	OUT0:PWMOUT0	–	
B1	P1.2/SCL	–	I^2C Clock	
A1	P1.3/SDA	–	I^2C Data	
A2	P1.6/OVF0/UND0/nOUT0/CMPO_0	nOUT0:Complement of OUT0, UND0, OVF0	CMPO_0: Sense Comp Out, Internal Reset function[3]	
B2	P1.7/MATCH/ EXT_CLK	MATCH: Match Out	External Clock	
A3	P2.0	–	–	
B3	P3.0/SDA/SWD_IO	–	I^2C Data, SWD I/O	
A4	P3.1/SCL/SWD_CLK	–	I^2C Clock, SWD Clock	

Note
3. Must not have load to ground during POR (should be an output).

Power

The following power system diagrams (Figure 9 and Figure 10) show the set of power supply pins as implemented for the PSoC 4000. The system has one regulator in Active mode for the digital circuitry. There is no analog regulator; the analog circuits run directly from the V_{DD} input. There is a separate regulator for the Deep Sleep mode. The supply voltage range is either 1.8 V ±5% (externally regulated) or 1.8 V to 5.5 V (unregulated externally; regulated internally) with all functions and circuits operating over that range.

The V_{DDIO} pin, available in the 16-pin QFN package, provides a separate voltage domain for the following pins: P3.0, P3.1, and P3.2. P3.0 and P3.1 can be I^2C pins and the chip can thus communicate with an I^2C system, running at a different voltage (where $V_{DDIO} \leq V_{DD}$). For example, V_{DD} can be 3.3 V and V_{DDIO} can be 1.8 V.

The PSoC 4000 family allows two distinct modes of power supply operation: Unregulated External Supply and Regulated External Supply.

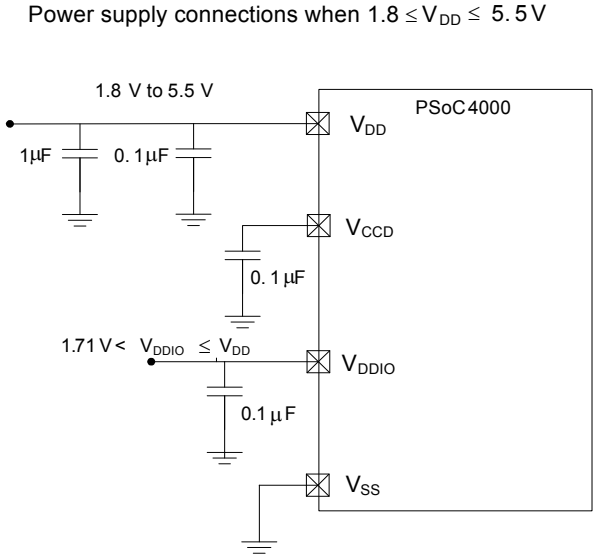
Unregulated External Supply

In this mode, the PSoC 4000 is powered by an external power supply that can be anywhere in the range of 1.8 to 5.5 V. This range is also designed for battery-powered operation. For example, the chip can be powered from a battery system that starts at 3.5 V and works down to 1.8 V. In this mode, the internal regulator of the PSoC 4000 supplies the internal logic and the V_{CCD} output of the PSoC 4000 must be bypassed to ground via an external capacitor (0.1 µF; X5R ceramic or better).

Bypass capacitors must be used from V_{DD} to ground. The typical practice for systems in this frequency range is to use a capacitor in the 1-µF range, in parallel with a smaller capacitor (0.1 µF, for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

An example of a bypass scheme follows (V_{DDIO} is available on the 16-QFN package).

Figure 9. 16-pin QFN Bypass Scheme Example - Unregulated External Supply



Regulated External Supply

In this mode, the PSoC 4000 is powered by an external power supply that must be within the range of 1.71 to 1.89 V; note that this range needs to include the power supply ripple too. In this mode, the V_{DD} and V_{CCD} pins are shorted together and bypassed. The internal regulator should be disabled in the firmware. Note that in this mode VDD (VCCD) should never exceed 1.89 in any condition, including flash programming.

An example of a bypass scheme follows (V_{DDIO} is available on the 16-QFN package).

Figure 10. 16-pin QFN Bypass Scheme Example - Regulated External Supply

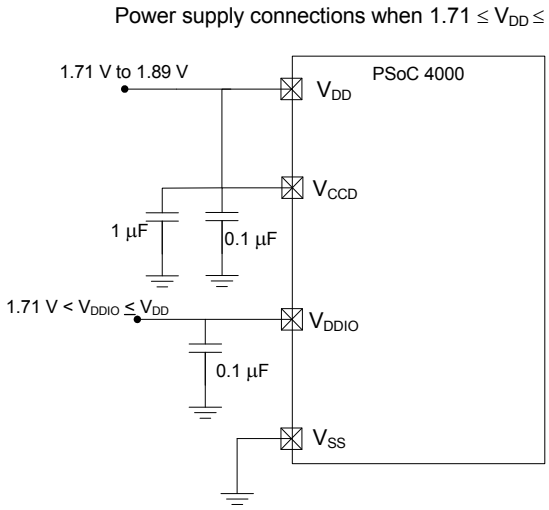


Table 4. DC Specifications *(continued)*

Typical values measured at V_{DD} = 3.3 V and 25 °C.

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
Deep Sleep Mode, V_{DD} = 3.6 to 5.5 V (Regulator on)							
SID34	I_{DD29}	I^2C wakeup and WDT on	–	2.5	12	µA	
Deep Sleep Mode, V_{DD} = V_{CCD} = 1.71 to 1.89 V (Regulator bypassed)							
SID37	I_{DD32}	I^2C wakeup and WDT on	–	2.5	9.2	µA	
XRES Current							
SID307	I_{DD_XR}	Supply current while XRES asserted	–	2	5	mA	

Table 5. AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID48	F_{CPU}	CPU frequency	DC	–	16	MHz	$1.71 \le V_{DD} \le 5.5$
SID49[5]	T_{SLEEP}	Wakeup from Sleep mode	–	0	–	µs	
SID50[5]	$T_{DEEPSLEEP}$	Wakeup from Deep Sleep mode	–	35	–	µs	

GPIO

Table 6. GPIO DC Specifications (referenced to V_{DDIO} for 16-Pin QFN V_{DDIO} pins)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID57	V_{IH}[6]	Input voltage high threshold	0.7 × V_{DD}	–	–	V	CMOS Input
SID58	V_{IL}	Input voltage low threshold	–	–	0.3 × V_{DD}	V	CMOS Input
SID241	V_{IH}[6]	LVTTL input, V_{DD} < 2.7 V	0.7× V_{DD}	–	–	V	
SID242	V_{IL}	LVTTL input, V_{DD} < 2.7 V	–	–	0.3 × V_{DD}	V	
SID243	V_{IH}[6]	LVTTL input, $V_{DD} \ge$ 2.7 V	2.0	–	–	V	
SID244	V_{IL}	LVTTL input, $V_{DD} \ge$ 2.7 V	–	–	0.8	V	
SID59	V_{OH}	Output voltage high level	V_{DD} –0.6	–	–	V	I_{OH} = 4 mA at 3 V V_{DD}
SID60	V_{OH}	Output voltage high level	V_{DD} –0.5	–	–	V	I_{OH} = 1 mA at 1.8 V V_{DD}
SID61	V_{OL}	Output voltage low level	–	–	0.6	V	I_{OL} = 4 mA at 1.8 V V_{DD}
SID62	V_{OL}	Output voltage low level	–	–	0.6	V	I_{OL} = 10 mA at 3 V V_{DD}
SID62A	V_{OL}	Output voltage low level	–	–	0.4	V	I_{OL} = 3 mA at 3 V V_{DD}
SID63	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	
SID64	$R_{PULLDOWN}$	Pull-down resistor	3.5	5.6	8.5	kΩ	
SID65	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	25 °C, V_{DD} = 3.0 V
SID66	C_{IN}	Input capacitance	–	3	7	pF	

Notes
5. Guaranteed by characterization.
6. V_{IH} must not exceed V_{DD} + 0.2 V.

Table 6. GPIO DC Specifications (referenced to V_{DDIO} for 16-Pin QFN V_{DDIO} pins) *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID67[7]	V_{HYSTTL}	Input hysteresis LVTTL	15	40	–	mV	$V_{DD} \geq 2.7$ V
SID68[7]	$V_{HYSCMOS}$	Input hysteresis CMOS	0.05 × V_{DD}	–	–	mV	$V_{DD} < 4.5$ V
SID68A[7]	$V_{HYSCMOS5V5}$	Input hysteresis CMOS	200	–	–	mV	$V_{DD} > 4.5$ V
SID69[7]	I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	–	–	100	µA	
SID69A[7]	I_{TOT_GPIO}	Maximum total source or sink chip current	–	–	85	mA	

Table 7. GPIO AC Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID70	T_{RISEF}	Rise time in fast strong mode	2	–	12	ns	3.3 V V_{DD}, Cload = 25 pF
SID71	T_{FALLF}	Fall time in fast strong mode	2	–	12	ns	3.3 V V_{DD}, Cload = 25 pF
SID72	T_{RISES}	Rise time in slow strong mode	10	–	60	–	3.3 V V_{DD}, Cload = 25 pF
SID73	T_{FALLS}	Fall time in slow strong mode	10	–	60	–	3.3 V V_{DD}, Cload = 25 pF
SID74	$F_{GPIOUT1}$	GPIO F_{OUT}; 3.3 V ≤ V_{DD} ≤ 5.5 V. Fast strong mode.	–	–	16	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID75	$F_{GPIOUT2}$	GPIO F_{OUT}; 1.71 V≤ V_{DD}≤ 3.3 V. Fast strong mode.	–	–	16	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID76	$F_{GPIOUT3}$	GPIO F_{OUT}; 3.3 V ≤ V_{DD} ≤ 5.5 V. Slow strong mode.	–	–	7	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID245	$F_{GPIOUT4}$	GPIO F_{OUT}; 1.71 V ≤ V_{DD} ≤ 3.3 V. Slow strong mode.	–	–	3.5	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID246	F_{GPIOIN}	GPIO input operating frequency; 1.71 V ≤ V_{DD} ≤ 5.5 V	–	–	16	MHz	90/10% V_{IO}

Note
7. Guaranteed by characterization.

XRES

Table 8. XRES DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID77	V_{IH}	Input voltage high threshold	0.7 × V_{DD}	–	–	V	CMOS Input
SID78	V_{IL}	Input voltage low threshold	–	–	0.3 × V_{DD}	V	CMOS Input
SID79	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	
SID80	C_{IN}	Input capacitance	–	3	7	pF	
SID81[8]	$V_{HYSXRES}$	Input voltage hysteresis	–	0.05* V_{DD}	–	mV	Typical hysteresis is 200 mV for V_{DD} > 4.5V

Table 9. XRES AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID83[8]	$T_{RESETWIDTH}$	Reset pulse width	5	–	–	µs	
BID#194[8]	$T_{RESETWAKE}$	Wake-up time from reset release	–	–	3	ms	

Analog Peripherals

Comparator

Table 10. Comparator DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID330[8]	I_{CMP1}	Block current, High Bandwidth mode	–	–	110	µA	
SID331[8]	I_{CMP2}	Block current, Low Power mode	–	–	85	µA	
SID332[8]	$V_{OFFSET1}$	Offset voltage, High Bandwidth mode	–	10	30	mV	
SID333[8]	$V_{OFFSET2}$	Offset voltage, Low Power mode	–	10	30	mV	
SID334[8]	Z_{CMP}	DC input impedance of comparator	35	–	–	MΩ	
SID338[8]	VINP_COMP	Comparator input range	0	–	3.6	V	Max input voltage is lower of 3.6 V or V_{DD}
SID339	VREF_COMP	Comparator internal voltage reference	1.188	1.2	1.212	V	

Note
8. Guaranteed by characterization.

Table 11. Comparator AC Specifications (Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID336[8]	T_{COMP1}	Response Time High Bandwidth mode, 50-mV overdrive	–	–	90	ns	
SID337[8]	T_{COMP2}	Response Time Low Power mode, 50-mV overdrive	–	–	110	ns	

CSD

Table 12. CSD and IDAC Block Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
CSD and IDAC Specifications							
SYS.PER#3	VDD_RIPPLE	Max allowed ripple on power supply, DC to 10 MHz	–	–	±50	mV	VDD > 2V (with ripple), 25 °C T_A, Sensitivity = 0.1 pF
SYS.PER#16	VDD_RIPPLE_1.8	Max allowed ripple on power supply, DC to 10 MHz	–	–	±25	mV	VDD > 1.75V (with ripple), 25 C T_A, Parasitic Capacitance (C_P) < 20 pF, Sensitivity ≥ 0.4 pF
SID.CSD#15	VREFHI	Reference Buffer Output	1.1	1.2	1.3	V	
SID.CSD#16	IDAC1IDD	IDAC1 (8-bits) block current	–	–	1125	µA	
SID.CSD#17	IDAC2IDD	IDAC2 (7-bits) block current	–	–	1125	µA	
SID308	V_{CSD}	Voltage range of operation	1.71	–	5.5	V	1.8 V ±5% or 1.8 V to 5.5 V
SID308A	VCOMPIDAC	Voltage compliance range of IDAC	0.8	–	V_{DD} –0.8	V	
SID309	$IDAC1_{DNL}$	DNL for 8-bit resolution	–1	–	1	LSB	
SID310	$IDAC1_{INL}$	INL for 8-bit resolution	–3	–	3	LSB	
SID311	$IDAC2_{DNL}$	DNL for 7-bit resolution	–1	–	1	LSB	
SID312	$IDAC2_{INL}$	INL for 7-bit resolution	–3	–	3	LSB	
SID313	SNR	Ratio of counts of finger to noise. Guaranteed by characterization	5	–	–	Ratio	Capacitance range of 9 to 35 pF, 0.1 pF sensitivity
SID314	$IDAC1_{CRT1}$	Output current of IDAC1 (8 bits) in high range	–	612	–	µA	
SID314A	$IDAC1_{CRT2}$	Output current of IDAC1(8 bits) in low range	–	306	–	µA	
SID315	$IDAC2_{CRT1}$	Output current of IDAC2 (7 bits) in high range	–	304.8	–	µA	
SID315A	$IDAC2_{CRT2}$	Output current of IDAC2 (7 bits) in low range	–	152.4	–	µA	
SID320	$IDAC_{OFFSET}$	All zeroes input	–	–	±1	LSB	
SID321	$IDAC_{GAIN}$	Full-scale error less offset	–	–	±10	%	
SID322	$IDAC_{MISMATCH}$	Mismatch between IDACs	–	–	7	LSB	
SID323	$IDAC_{SET8}$	Settling time to 0.5 LSB for 8-bit IDAC	–	–	10	µs	Full-scale transition. No external load.
SID324	$IDAC_{SET7}$	Settling time to 0.5 LSB for 7-bit IDAC	–	–	10	µs	Full-scale transition. No external load.
SID325	CMOD	External modulator capacitor.	–	2.2	–	nF	5-V rating, X7R or NP0 cap.

Table 25. External Clock Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID305[14]	ExtClkFreq	External clock input frequency	0	–	16	MHz	
SID306[14]	ExtClkDuty	Duty cycle; measured at $V_{DD/2}$	45	–	55	%	

Table 26. Block Specs

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID262[14]	$T_{CLKSWITCH}$	System clock source switching time	3	–	4	Periods	

Note
14. Guaranteed by characterization.

Ordering Information

The PSoC 4000 part numbers and features are listed in the following table. All package types are available in Tape and Reel.

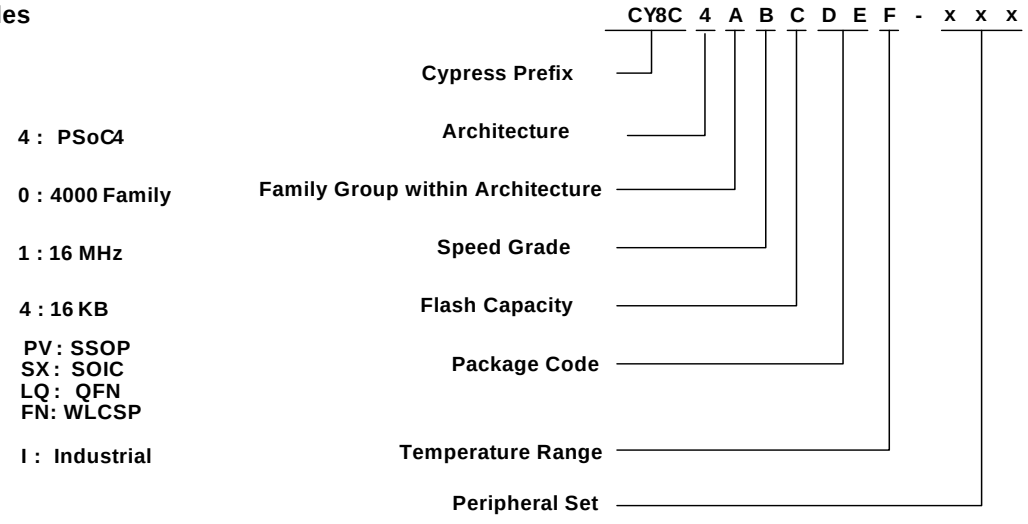
Category	MPN	Feature									Package					
		Max CPU Speed (MHz)	Flash (KB)	SRAM (KB)	CapSense	7-bit IDAC	8-bit IDAC	Comparators	TCPWM Blocks	I2C	16 -WLCSP	8-SOIC	16-SOIC	16-QFN	24-QFN	28-SSOP
CY8C4013	CY8C4013SXI-400	16	8	2	–	–	–	–	1	1	–	✔	–	–	–	–
	CY8C4013SXI-410	16	8	2	–	1	1	1	1	1	–	✔	–	–	–	–
	CY8C4013SXI-411	16	8	2	–	1	1	1	1	1	–	–	✔	–	–	–
	CY8C4013LQI-411	16	8	2	–	1	1	1	1	1	–	–	–	✔	–	–
CY8C4014	CY8C4014SXI-420	16	16	2	✔	1	1	1	1	1	–	✔	–	–	–	–
	CY8C4014SXI-411	16	16	2	–	1	1	1	1	1	–	–	✔	–	–	–
	CY8C4014SXI-421	16	16	2	✔	1	1	1	1	1	–	–	✔	–	–	–
	CY8C4014LQI-421	16	16	2	✔	1	1	1	1	1	–	–	–	✔	–	–
	CY8C4014LQI-412	16	16	2	–	1	1	1	1	1	–	–	–	–	✔	–
	CY8C4014LQI-422	16	16	2	✔	1	1	1	1	1	–	–	–	–	✔	–
	CY8C4014PVI-412	16	16	2	–	1	1	1	1	1	–	–	–	–	–	✔
	CY8C4014PVI-422	16	16	2	✔	1	1	1	1	1	–	–	–	–	–	✔
	CY8C4014FNI-421	16	16	2	✔	1	1	1	1	1	✔	–	–	–	–	–
Other	CY8C4014LQI-SLT1	16	16	2	✔	1	1	1	1	1	–	–	–	✔	–	–
	CY8C4014LQI-SLT2	16	16	2	✔	1	1	1	1	1	–	–	–	–	✔	–

Part Numbering Conventions

PSoC 4 devices follow the part numbering convention described in the following table. All fields are single-character alphanumeric (0, 1, 2, …, 9, A,B, …, Z) unless stated otherwise.

The part numbers are of the form CY8C4ABCDEF-XYZ where the fields are defined as follows.

Examples



The Field Values are listed in the following table:

Field	Description	Values	Meaning
CY8C	Cypress prefix		
4	Architecture	4	PSoC 4
A	Family	0	4000 Family
B	CPU speed	1	16 MHz
		4	48 MHz
C	Flash capacity	3	8 KB
		4	16 KB
		5	32 KB
		6	64 KB
		7	128 KB
DE	Package code	SX	SOIC
		LQ	QFN
		PV	SSOP
		FN	WLCSP
F	Temperature range	I	Industrial
XYZ	Attributes code	000-999	Code of feature set in specific family

Packaging

Table 27. Package List

Spec ID#	Package	Description
BID#47A	28-Pin SSOP	28-pin 5 × 10 × 1.65mm SSOP with 0.65-mm pitch
BID#26	24-Pin QFN	24-pin 4 × 4 × 0.6 mm QFN with 0.5-mm pitch
BID#33	16-Pin QFN	16-pin 3 × 3 × 0.6 mm QFN with 0.5-mm pitch
BID#40	16-Pin SOIC	16-pin (150 Mil) SOIC
BID#47	8-Pin SOIC	8-pin (150 Mil) SOIC
BID#147A	16-Ball WLCSP	16-Ball 1.47 × 1.58 × 0.4 mm

Table 28. Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
T_A	Operating ambient temperature		–40	25	85	°C
T_J	Operating junction temperature		–40	–	100	°C
T_{JA}	Package θ_{JA} (28-pin SSOP)		–	66.6	–	°C/Watt
T_{JC}	Package θ_{JC} (28-pin SSOP)		–	34	–	°C/Watt
T_{JA}	Package θ_{JA} (24-pin QFN)		–	38	–	°C/Watt
T_{JC}	Package θ_{JC} (24-pin QFN)		–	5.6	–	°C/Watt
T_{JA}	Package θ_{JA} (16-pin QFN)		–	49.6	–	°C/Watt
T_{JC}	Package θ_{JC} (16-pin QFN)		–	5.9	–	°C/Watt
T_{JA}	Package θ_{JA} (16-pin SOIC)		–	142	–	°C/Watt
T_{JC}	Package θ_{JC} (16-pin SOIC)		–	49.8	–	°C/Watt
T_{JA}	Package θ_{JA} (16-ball WLCSP)		–	90	–	°C/Watt
T_{JC}	Package θ_{JC} (16-ball WLCSP)		–	0.9	–	°C/Watt
T_{JA}	Package θ_{JA} (8-pin SOIC)		–	198	–	°C/Watt
T_{JC}	Package θ_{JC} (8-pin SOIC)		–	56.9	–	°C/Watt

Table 29. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
All	260 °C	30 seconds

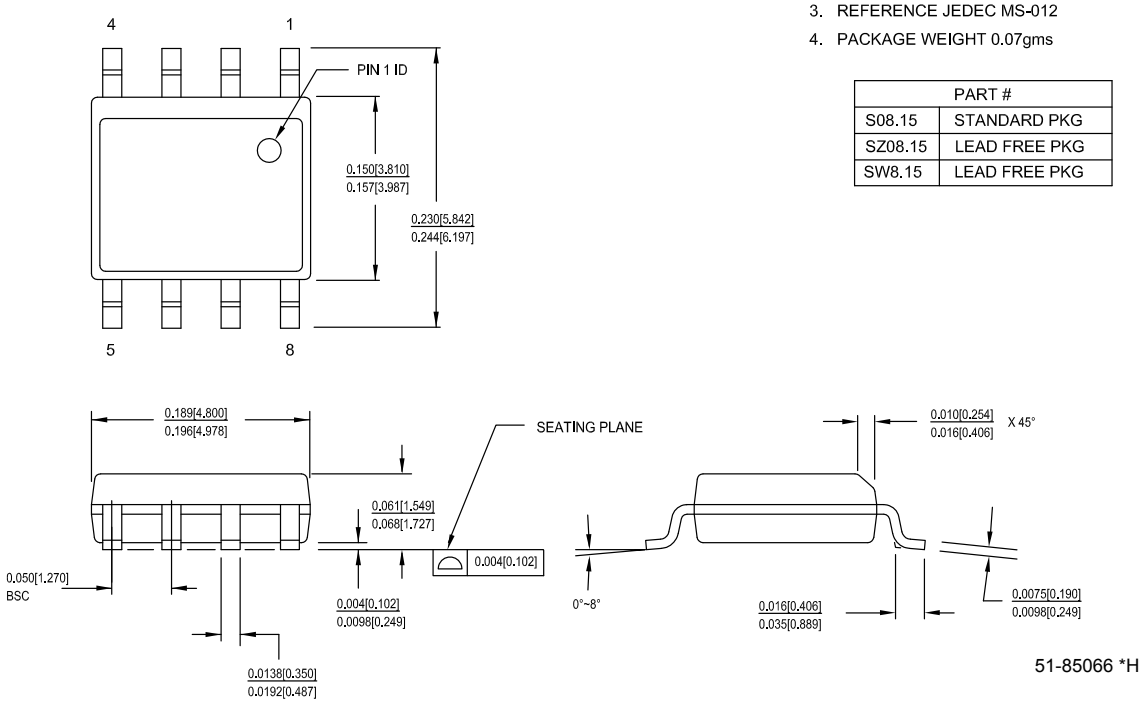
Table 30. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-020

Package	MSL
All except WLCSP	MSL 3
16-ball WLCSP	MSL1

Figure 15. 8-pin (150-mil) SOIC Package Outline

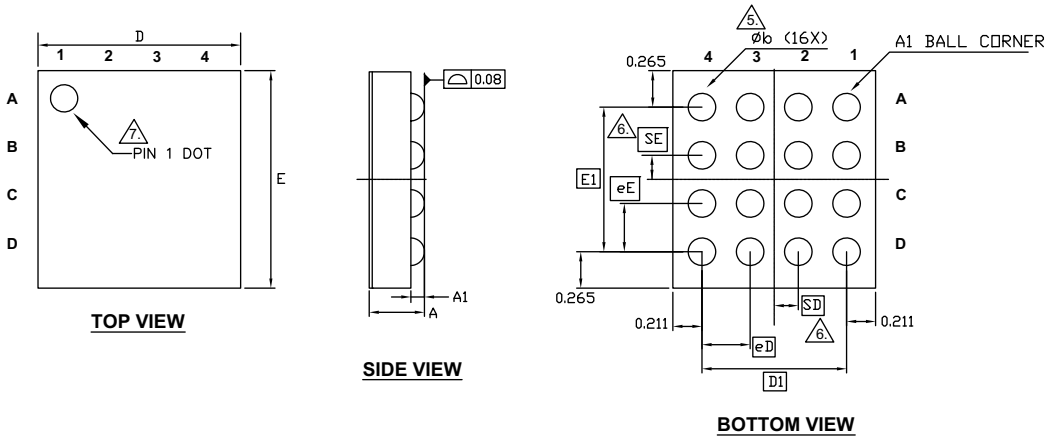
1. DIMENSIONS IN INCHES[MM] MIN.
   MAX.
2. PIN 1 ID IS OPTIONAL,
   ROUND ON SINGLE LEADFRAME
   RECTANGULAR ON MATRIX LEADFRAME
3. REFERENCE JEDEC MS-012
4. PACKAGE WEIGHT 0.07gms

PART #	
S08.15	STANDARD PKG
SZ08.15	LEAD FREE PKG
SW8.15	LEAD FREE PKG



51-85066 *H

Figure 16. 16-Ball WLCSP 1.47 × 1.58 × 0.4 mm



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	0.42
A1	0.089	0.099	0.109
D	1.447	1.472	1.497
E	1.554	1.579	1.604
D1	1.05 BSC		
E1	1.05 BSC		
MD	4		
ME	4		
N	16		
Ø b	0.17	0.20	0.23
eD	0.35 BSC		
eE	0.35 BSC		
SD	0.18 BSC		
SE	0.18 BSC		

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
7. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.
9. JEDEC SPECIFICATION NO. REF. : N/A.

002-18598 **

Table 31. Acronyms Used in this Document *(continued)*

Acronym	Description
PC	program counter
PCB	printed circuit board
PGA	programmable gain amplifier
PHUB	peripheral hub
PHY	physical layer
PICU	port interrupt control unit
PLA	programmable logic array
PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration data sheet
POR	power-on reset
PRES	precise power-on reset
PRS	pseudo random sequence
PS	port read data register
PSoC®	Programmable System-on-Chip™
PSRR	power supply rejection ratio
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I^2C serial clock
SDA	I^2C serial data
S/H	sample and hold
SINAD	signal to noise and distortion ratio
SIO	special input/output, GPIO with advanced features. See GPIO.
SOC	start of conversion
SOF	start of frame
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory
SRES	software reset
SWD	serial wire debug, a test protocol

Table 31. Acronyms Used in this Document *(continued)*

Acronym	Description
SWV	single-wire viewer
TD	transaction descriptor, see also DMA
THD	total harmonic distortion
TIA	transimpedance amplifier
TRM	technical reference manual
TTL	transistor-transistor logic
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UDB	universal digital block
USB	Universal Serial Bus
USBIO	USB input/output, PSoC pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset I/O pin
XTAL	crystal

Revision History

Description Title: PSoC® 4: PSoC 4000 Family Datasheet Programmable System-on-Chip (PSoC®) Document Number: 001-89638				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*B	4348760	WKA	05/16/2014	New PSoC 4000 datasheet.
*C	4514139	WKA	10/27/2014	Added 28-pin SSOP pin and package details. Updated V_{REF} spec values. Updated conditions for SID174. Updated SID.CSD#15 values and description. Added spec SID339.
*D	4617283	WKA	01/09/2015	Corrected Development Kits information and PSoC Creator Example Project figure. Corrected typo in the ordering information table. Updated 28-pin SSOP package diagram.
*E	4735762	WKA	05/26/2015	Added 16-ball WLCSP pin and package details.
*F	5466193	WKA	10/07/2016	Updated Table 30. Updated 8-pin SOIC package diagram. Updated the template.
*G	5685079	TSEN	04/05/2017	Updated 16-ball WLCSP package details.

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