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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	16MHz
Connectivity	I <sup>2</sup> C
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	12
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	D/A 1x7b, 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-SOIC (0.154", 3.90mm Width)
Supplier Device Package	16-SOIC
Purchase URL	<a href="https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4013sxi-411">https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4013sxi-411</a>

## More Information

Cypress provides a wealth of data at [www.cypress.com](http://www.cypress.com) to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article [KBA86521, How to Design with PSoC 3, PSoC 4, and PSoC 5LP](#). Following is an abbreviated list for PSoC 4:

- Overview: [PSoC Portfolio](#), [PSoC Roadmap](#)
- Product Selectors: [PSoC 1](#), [PSoC 3](#), [PSoC 4](#), [PSoC 5LP](#)  
In addition, PSoC Creator includes a device selection tool.
- Application notes: Cypress offers a large number of PSoC application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with PSoC 4 are:
  - [AN79953](#): Getting Started With PSoC 4
  - [AN88619](#): PSoC 4 Hardware Design Considerations
  - [AN86439](#): Using PSoC 4 GPIO Pins
  - [AN57821](#): Mixed Signal Circuit Board Layout
  - [AN81623](#): Digital Design Best Practices
  - [AN73854](#): Introduction To Bootloaders
  - [AN89610](#): ARM Cortex Code Optimization
- Technical Reference Manual (TRM) is in two documents:
  - [Architecture TRM](#) details each PSoC 4 functional block.
  - [Registers TRM](#) describes each of the PSoC 4 registers.
- Development Kits:
  - CY8CKIT-040, PSoC 4000 Pioneer Kit, is an easy-to-use and inexpensive development platform with debugging capability. This kit includes connectors for Arduino<sup>™</sup> compatible shields and Digilent<sup>®</sup> Pmod<sup>™</sup> daughter cards.
  - The MiniProg3 device provides an interface for flash programming and debug.

## PSoC Creator

[PSoC Creator](#) is a free Windows-based Integrated Design Environment (IDE). It enables concurrent hardware and firmware design of PSoC 3, PSoC 4, and PSoC 5LP based systems. Create designs using classic, familiar schematic capture supported by over 100 pre-verified, production-ready PSoC Components; see the [list of component datasheets](#). With PSoC Creator, you can:

1. Drag and drop component icons to build your hardware system design in the main design workspace
2. Codesign your application firmware with the PSoC hardware, using the PSoC Creator IDE C compiler
3. Configure components using the configuration tools
4. Explore the library of 100+ components
5. Review component datasheets

Figure 1. CapSense Example Project in PSoC Creator

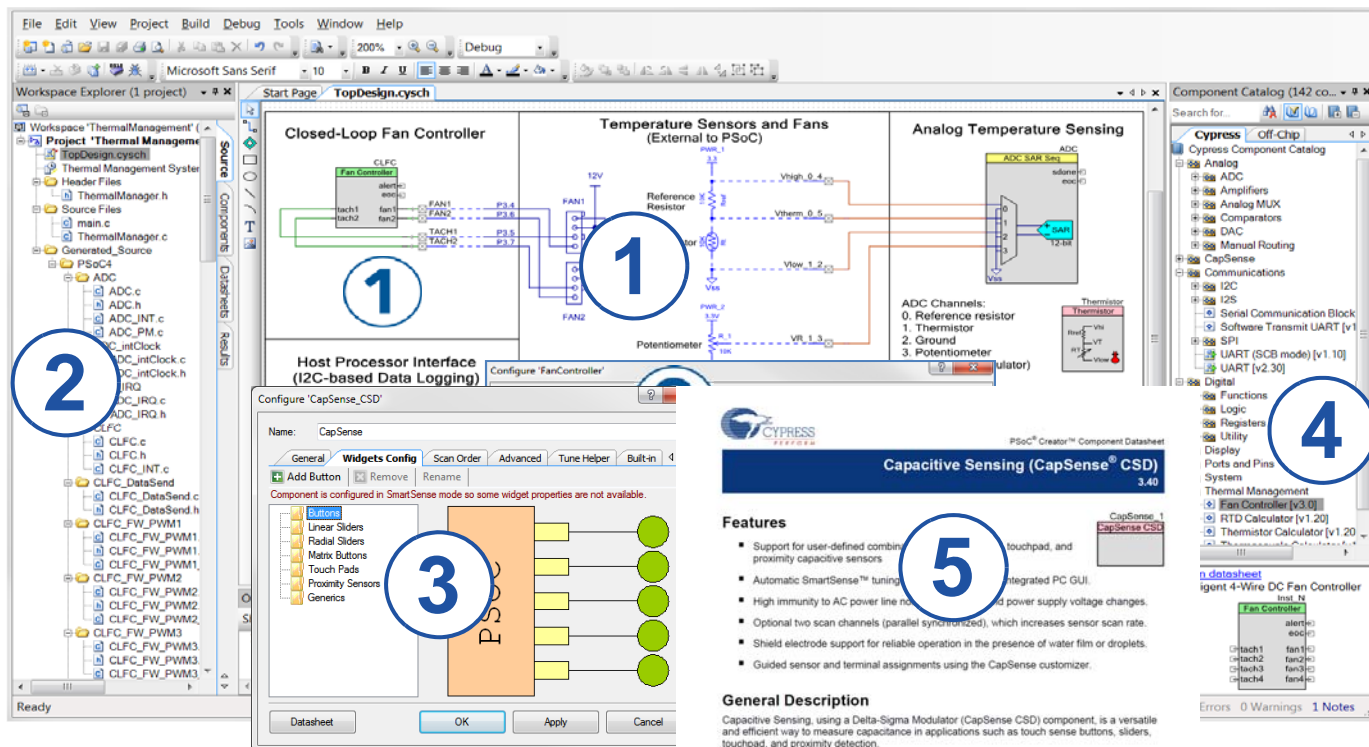
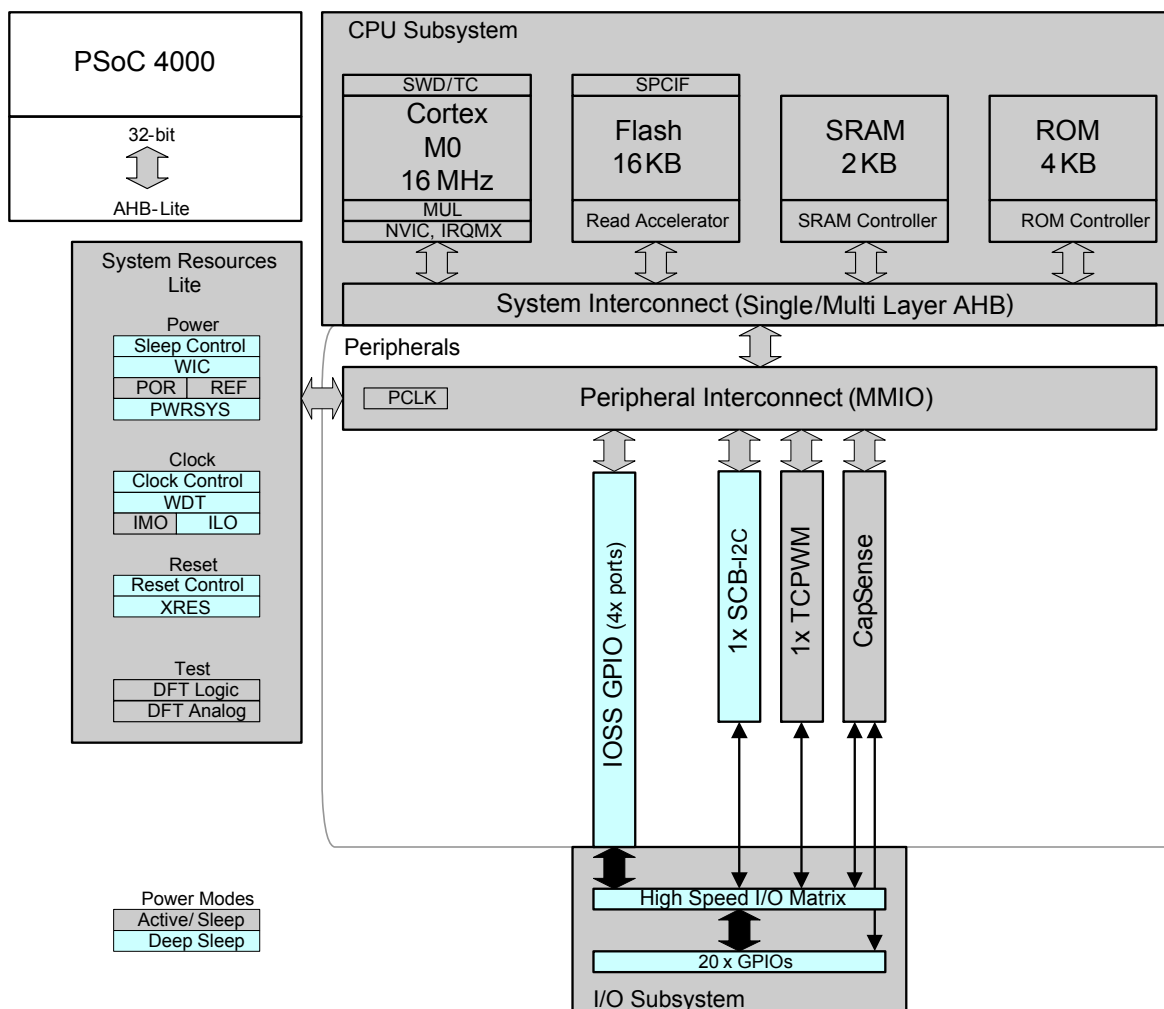


Figure 2. Block Diagram



PSoC 4000 devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware.

The ARM Serial-Wire Debug (SWD) interface supports all programming and debug features of the device.

Complete debug-on-chip functionality enables full-device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC Creator IDE provides fully integrated programming and debug support for the PSoC 4000 devices. The SWD interface is fully compatible with industry-standard third-party tools. The PSoC 4000 family provides a level of security not possible with multi-chip application solutions or with microcontrollers. It has the following advantages:

- Allows disabling of debug features
- Robust flash protection
- Allows customer-proprietary functionality to be implemented in on-chip programmable blocks

The debug circuits are enabled by default and can only be disabled in firmware. If they are not enabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables debugging.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. All programming, debug, and test interfaces are disabled when maximum device security is enabled. Therefore, PSoC 4000, with device security enabled, may not be returned for failure analysis. This is a trade-off the PSoC 4000 allows the customer to make.

## Analog Blocks

### Low-power Comparators

The PSoC 4000 has a low-power comparator, which uses the built-in voltage reference. Any one of up to 16 pins can be used as a comparator input and the output of the comparator can be brought out to a pin. The selected comparator input is connected to the minus input of the comparator with the plus input always connected to the 1.2-V voltage reference. This comparator is also used for CapSense purposes and is not available during CapSense operation.

### Current DACs

The PSoC 4000 has two IDACs, which can drive any of up to 16 pins on the chip. These IDACs have programmable current ranges.

### Analog Multiplexed Buses

The PSoC 4000 has two concentric independent buses that go around the periphery of the chip. These buses (called amux buses) are connected to firmware-programmable analog switches that allow the chip's internal resources (IDACs, comparator) to connect to any pin on Ports 0, 1, and 2.

## Fixed Function Digital

### Timer/Counter/PWM (TCPWM) Block

The TCPWM block consists of a 16-bit counter with user-programmable period length. There is a capture register to record the count value at the time of an event (which may be an I/O event), a period register that is used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals that are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow use as dead-band programmable complementary PWM outputs. It also has a Kill input to force outputs to a predetermined state; for example, this is used in motor drive systems when an over-current state is indicated and the PWM driving the FETs needs to be shut off immediately with no time for software intervention.

### Serial Communication Block (SCB)

The PSoC 4000 has a serial communication block, which implements a multi-master I<sup>2</sup>C interface.

**I<sup>2</sup>C Mode:** The hardware I<sup>2</sup>C block implements a full multi-master and slave interface (it is capable of multi-master arbitration). This block is capable of operating at speeds of up to 400 kbps (Fast Mode) and has flexible buffering options to reduce interrupt overhead and latency for the CPU. It also supports EZI<sup>2</sup>C that creates a mailbox address range in the memory of the PSoC 4000 and effectively reduces I<sup>2</sup>C communication to reading from and writing to an array in memory. In addition, the block supports an 8-deep FIFO for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduces the need for clock stretching caused by the CPU not having read data on time.

The I<sup>2</sup>C peripheral is compatible with the I<sup>2</sup>C Standard-mode and Fast-mode devices as defined in the NXP I<sup>2</sup>C-bus specification and user manual (UM10204). The I<sup>2</sup>C bus I/O is implemented with GPIO in open-drain modes.

The PSoC 4000 is not completely compliant with the I<sup>2</sup>C spec in the following respect:

- GPIO cells are not overvoltage tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I<sup>2</sup>C system.
- Fast-mode minimum fall time is not met in Fast Strong mode; Slow Strong mode can help meet this spec depending on the Bus Load.

## GPIO

The PSoC 4000 has up to 20 GPIOs. The GPIO block implements the following:

- Eight drive modes:
  - Analog input mode (input and output buffers disabled)
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTTL).
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes
- Selectable slew rates for dV/dt related noise control to improve EMI

The pins are organized in logical entities called ports, which are 8-bit in width (less for Ports 2 and 3). During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin.

Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves.

Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it (4 for PSoC 4000).

The 28-pin and 24-pin packages have 20 GPIOs. The 16-pin SOIC has 13 GPIOs. The 16-pin QFN and the 16-ball WLCSP have 12 GPIOs. The 8-pin SOIC has 5 GPIOs.

## Special Function Peripherals

### CapSense

CapSense is supported in the PSoC 4000 through a CSD block that can be connected to up to 16 pins through an analog mux bus via an analog switch (pins on Port 3 are not available for CapSense purposes). CapSense function can thus be provided on any available pin or group of pins in a system under software control. A PSoC Creator component is provided for the CapSense block to make it easy for the user.

Shield voltage can be driven on another mux bus to provide water-tolerance capability. Water tolerance is provided by driving the shield electrode in phase with the sense electrode to keep the shield capacitance from attenuating the sensed input. Proximity sensing can also be implemented.

The CapSense block has two IDACs, which can be used for general purposes if CapSense is not being used (both IDACs are available in that case) or if CapSense is used without water tolerance (one IDAC is available).

**Table 1. Pin Descriptions** *(continued)*

28-Pin SSOP		24-Pin QFN		16-Pin QFN		16-Pin SOIC		8-Pin SOIC		TCPWM Signals	Alternate Functions
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name		
11	VSS										
12	No Connect (NC) <sup>[2]</sup>										
13	P1.7/MATCH/EXT_CLK	19	P1.7/MATCH/EXT_CLK	13	P1.7/MATCH/EXT_CLK	15	P1.7/MATCH/EXT_CLK			MATCH: Match Out	External Clock
14	P2.0	20	P2.0			16	P2.0				
15	VSS										
16	P3.0/SDA/SWD_IO	21	P3.0/SDA/SWD_IO	14	P3.0/SDA/SWD_IO	1	P3.0/SDA/SWD_IO	8	P3.0/SDA/SWD_IO		I2C Data, SWD I/O
17	P3.1/SCL/SWD_CLK	22	P3.1/SCL/SWD_CLK	15	P3.1/SCL/SWD_CLK	2	P3.1/SCL/SWD_CLK	1	P3.1/SCL/SWD_CLK		I2C Clock, SWD Clock
18	P3.2	23	P3.2	16	P3.2					OUT0:PWM OUT 0	
19	XRES	24	XRES								XRES: External Reset

**Descriptions of the Pin functions are as follows:**

**VDD:** Power supply for both analog and digital sections.

**VDDIO:** Where available, this pin provides a separate voltage domain (see the [Power](#) section for details).

**VSS:** Ground pin.

**VCCD:** Regulated digital supply (1.8 V ±5%).

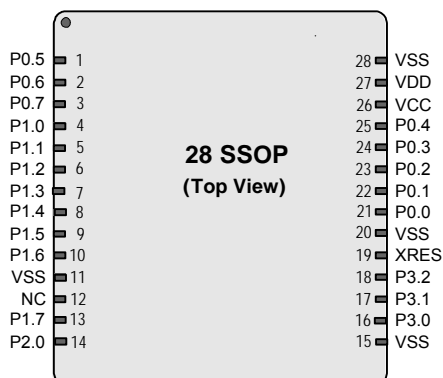
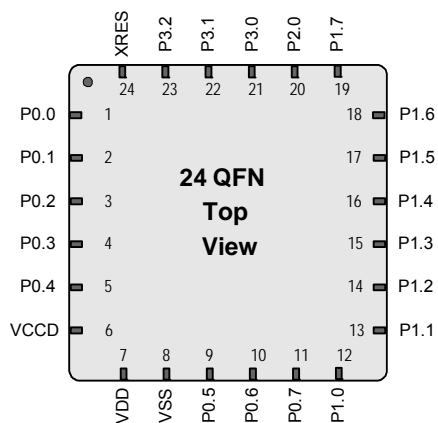
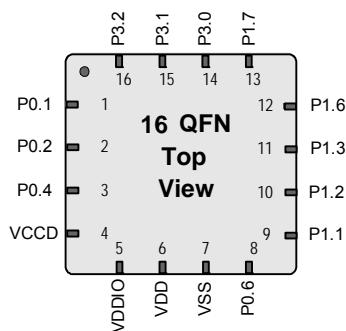
Pins belonging to Ports 0, 1, and 2 can all be used as CSD sense or shield pins connected to AMUXBUS A or B. They can also be used as GPIO pins that can be driven by the firmware, in addition to their alternate functions listed in the [Table 1](#).

Pins on Port 3 can be used as GPIO, in addition to their alternate functions listed above.

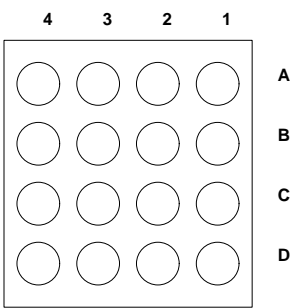
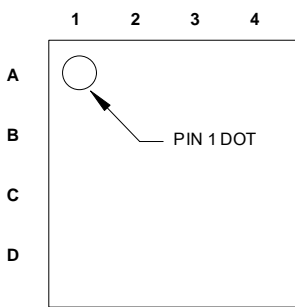
The following packages are provided: 28-pin SSOP, 24-pin QFN, 16-pin QFN, 16-pin SOIC, and 8-pin SOIC.

**Note**

2. This pin is not to be used; it must be left floating.

**Figure 4. 28-Pin SSOP Pinout**

**Figure 5. 24-pin QFN Pinout**

**Figure 6. 16-Pin QFN Pinout**


**Table 2. 16-ball WLCSP Pin Descriptions and Diagram**

Pin	Name	TCPWM Signal	Alternate Functions	Pin Diagram
B4	P3.2	OUT0:PWMOUT0	—	<div>Bottom View</div>  <div>Top View</div> 
C3	P0.2/TRIN2	TRIN2:Trigger Input 2	—	
C4	P0.4/TRIN4/CMPO_0/ EXT_CLK	TRIN4:Trigger Input 4	CMPO_0: Sense Comp Out, Ext. Clock, CMOD Cap	
D4	VCCD	—	—	
D3	VDD	—	—	
D2	VSS	—	—	
C2	VDDIO	—	—	
D1	P0.6	—	—	
C1	P1.1/OUT0	OUT0:PWMOUT0	—	
B1	P1.2/SCL	—	I <sup>2</sup> C Clock	
A1	P1.3/SDA	—	I <sup>2</sup> C Data	
A2	P1.6/OVF0/UND0/nO UT0/CMPO_0	nOUT0:Complement of OUT0, UND0, OVF0	CMPO_0: Sense Comp Out, Internal Reset function <sup>[3]</sup>	
B2	P1.7/MATCH/ EXT_CLK	MATCH: Match Out	External Clock	
A3	P2.0	—	—	
B3	P3.0/SDA/SWD_IO	—	I <sup>2</sup> C Data, SWD I/O	
A4	P3.1/SCL/SWD_CLK	—	I <sup>2</sup> C Clock, SWD Clock	

**Note**

3. Must not have load to ground during POR (should be an output).



## Development Support

The PSoC 4000 family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit [www.cypress.com/go/psoc4](http://www.cypress.com/go/psoc4) to find out more.

### Documentation

A suite of documentation supports the PSoC 4000 family to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

**Software User Guide:** A step-by-step guide for using PSoC Creator. The software user guide shows you how the PSoC Creator build process works in detail, how to use source control with PSoC Creator, and much more.

**Component Datasheets:** The flexibility of PSoC allows the creation of new peripherals (components) long after the device has gone into production. Component data sheets provide all of the information needed to select and use a particular component, including a functional description, API documentation, example code, and AC/DC specifications.

**Application Notes:** PSoC application notes discuss a particular application of PSoC in depth; examples include brushless DC motor control and on-chip filtering. Application notes often include example projects in addition to the application note document.

**Technical Reference Manual:** The Technical Reference Manual (TRM) contains all the technical detail you need to use a PSoC device, including a complete description of all PSoC registers. The TRM is available in the Documentation section at [www.cypress.com/psoc4](http://www.cypress.com/psoc4).

### Online

In addition to print documentation, the Cypress PSoC forums connect you with fellow PSoC users and experts in PSoC from around the world, 24 hours a day, 7 days a week.

### Tools

With industry standard cores, programming, and debugging interfaces, the PSoC 4000 family is part of a development tool ecosystem. Visit us at [www.cypress.com/go/psoccreator](http://www.cypress.com/go/psoccreator) for the latest information on the revolutionary, easy to use PSoC Creator IDE, supported third party compilers, programmers, debuggers, and development kits.



## Electrical Specifications

### Absolute Maximum Ratings

**Table 3. Absolute Maximum Ratings**<sup>[4]</sup>

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID1	V <sub>DD_ABS</sub>	Digital supply relative to V <sub>SS</sub>	-0.5	—	6	V	
SID2	V <sub>CCD_ABS</sub>	Direct digital core voltage input relative to V <sub>SS</sub>	-0.5	—	1.95	V	
SID3	V <sub>GPIO_ABS</sub>	GPIO voltage	-0.5	—	V <sub>DD</sub> +0.5	V	
SID4	I <sub>GPIO_ABS</sub>	Maximum current per GPIO	-25	—	25	mA	
SID5	I <sub>GPIO_injection</sub>	GPIO injection current, Max for V <sub>IH</sub> > V <sub>DD</sub> , and Min for V <sub>IL</sub> < V <sub>SS</sub>	-0.5	—	0.5	mA	Current injected per pin
BID44	ESD_HBM	Electrostatic discharge human body model	2200	—	—	V	
BID45	ESD_CDM	Electrostatic discharge charged device model	500	—	—	V	
BID46	LU	Pin current for latch-up	-140	—	140	mA	

### Device Level Specifications

All specifications are valid for -40 °C ≤ T<sub>A</sub> ≤ 85 °C and T<sub>J</sub> ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

**Table 4. DC Specifications**

Typical values measured at V<sub>DD</sub> = 3.3 V and 25 °C.

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID53	V <sub>DD</sub>	Power supply input voltage	1.8	—	5.5	V	With regulator enabled
SID255	V <sub>DD</sub>	Power supply input voltage (V <sub>CCD</sub> = V <sub>DD</sub> )	1.71	—	1.89	V	Internally unregulated supply
SID54	V <sub>DDIO</sub>	V <sub>DDIO</sub> domain supply	1.71	—	V <sub>DD</sub>	V	
SID55	C <sub>EFC</sub>	External regulator voltage bypass	—	0.1	—	μF	X5R ceramic or better
SID56	C <sub>EXC</sub>	Power supply bypass capacitor	—	1	—	μF	X5R ceramic or better
<b>Active Mode, V<sub>DD</sub> = 1.8 to 5.5 V</b>							
SID9	I <sub>DD5</sub>	Execute from flash; CPU at 6 MHz	—	2.0	2.85	mA	
SID12	I <sub>DD8</sub>	Execute from flash; CPU at 12 MHz	—	3.2	3.75	mA	
SID16	I <sub>DD11</sub>	Execute from flash; CPU at 16 MHz	—	4.0	4.5	mA	
<b>Sleep Mode, V<sub>DD</sub> = 1.71 to 5.5 V</b>							
SID25	I <sub>DD20</sub>	I <sup>2</sup> C wakeup, WDT on. 6 MHz	—	1.1	—	mA	
SID25A	I <sub>DD20A</sub>	I <sup>2</sup> C wakeup, WDT on. 12 MHz	—	1.4	—	mA	
<b>Deep Sleep Mode, V<sub>DD</sub> = 1.8 to 3.6 V (Regulator on)</b>							
SID31	I <sub>DD26</sub>	I <sup>2</sup> C wakeup and WDT on	—	2.5	8.2	μA	

#### Note

4. Usage above the absolute maximum conditions listed in Table 1 may cause permanent damage to the device. Exposure to Absolute Maximum conditions for extended periods of time may affect device reliability. The Maximum Storage Temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below Absolute Maximum conditions but above normal operating conditions, the device may not operate to specification.

**Table 4. DC Specifications (continued)**

 Typical values measured at  $V_{DD} = 3.3 \text{ V}$  and  $25^\circ\text{C}$ .

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
<b>Deep Sleep Mode, <math>V_{DD} = 3.6</math> to <math>5.5 \text{ V}</math> (Regulator on)</b>							
SID34	$I_{DD29}$	I <sup>2</sup> C wakeup and WDT on	–	2.5	12	μA	
<b>Deep Sleep Mode, <math>V_{DD} = V_{CCD} = 1.71</math> to <math>1.89 \text{ V}</math> (Regulator bypassed)</b>							
SID37	$I_{DD32}$	I <sup>2</sup> C wakeup and WDT on	–	2.5	9.2	μA	
<b>XRES Current</b>							
SID307	$I_{DD\_XR}$	Supply current while XRES asserted	–	2	5	mA	

**Table 5. AC Specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID48	$F_{CPU}$	CPU frequency	DC	–	16	MHz	$1.71 \leq V_{DD} \leq 5.5$
SID49 <sup>[5]</sup>	$T_{SLEEP}$	Wakeup from Sleep mode	–	0	–	μs	
SID50 <sup>[5]</sup>	$T_{DEEPSLEEP}$	Wakeup from Deep Sleep mode	–	35	–	μs	

#### GPIO

**Table 6. GPIO DC Specifications (referenced to  $V_{DDIO}$  for 16-Pin QFN  $V_{DDIO}$  pins)**

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID57	$V_{IH}$ <sup>[6]</sup>	Input voltage high threshold	$0.7 \times V_{DD}$	–	–	V	CMOS Input
SID58	$V_{IL}$	Input voltage low threshold	–	–	$0.3 \times V_{DD}$	V	CMOS Input
SID241	$V_{IH}$ <sup>[6]</sup>	LVTTL input, $V_{DD} < 2.7 \text{ V}$	$0.7 \times V_{DD}$	–	–	V	
SID242	$V_{IL}$	LVTTL input, $V_{DD} < 2.7 \text{ V}$	–	–	$0.3 \times V_{DD}$	V	
SID243	$V_{IH}$ <sup>[6]</sup>	LVTTL input, $V_{DD} \geq 2.7 \text{ V}$	2.0	–	–	V	
SID244	$V_{IL}$	LVTTL input, $V_{DD} \geq 2.7 \text{ V}$	–	–	0.8	V	
SID59	$V_{OH}$	Output voltage high level	$V_{DD} - 0.6$	–	–	V	$I_{OH} = 4 \text{ mA}$ at $3 \text{ V } V_{DD}$
SID60	$V_{OH}$	Output voltage high level	$V_{DD} - 0.5$	–	–	V	$I_{OH} = 1 \text{ mA}$ at $1.8 \text{ V } V_{DD}$
SID61	$V_{OL}$	Output voltage low level	–	–	0.6	V	$I_{OL} = 4 \text{ mA}$ at $1.8 \text{ V } V_{DD}$
SID62	$V_{OL}$	Output voltage low level	–	–	0.6	V	$I_{OL} = 10 \text{ mA}$ at $3 \text{ V } V_{DD}$
SID62A	$V_{OL}$	Output voltage low level	–	–	0.4	V	$I_{OL} = 3 \text{ mA}$ at $3 \text{ V } V_{DD}$
SID63	$R_{PULLUP}$	Pull-up resistor	3.5	5.6	8.5	kΩ	
SID64	$R_{PULLDOWN}$	Pull-down resistor	3.5	5.6	8.5	kΩ	
SID65	$I_{IL}$	Input leakage current (absolute value)	–	–	2	nA	$25^\circ\text{C}$ , $V_{DD} = 3.0 \text{ V}$
SID66	$C_{IN}$	Input capacitance	–	3	7	pF	

#### Notes

5. Guaranteed by characterization.
6.  $V_{IH}$  must not exceed  $V_{DD} + 0.2 \text{ V}$ .

**Table 6. GPIO DC Specifications (referenced to  $V_{DDIO}$  for 16-Pin QFN  $V_{DDIO}$  pins) (continued)**

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID67 <sup>[7]</sup>	$V_{HYSTTL}$	Input hysteresis LVTTL	15	40	—	mV	$V_{DD} \geq 2.7 \text{ V}$
SID68 <sup>[7]</sup>	$V_{HYSCMOS}$	Input hysteresis CMOS	$0.05 \times V_{DD}$	—	—	mV	$V_{DD} < 4.5 \text{ V}$
SID68A <sup>[7]</sup>	$V_{HYSCMOS5V5}$	Input hysteresis CMOS	200	—	—	mV	$V_{DD} > 4.5 \text{ V}$
SID69 <sup>[7]</sup>	$I_{DIODE}$	Current through protection diode to $V_{DD}/V_{SS}$	—	—	100	$\mu\text{A}$	
SID69A <sup>[7]</sup>	$I_{TOT\_GPIO}$	Maximum total source or sink chip current	—	—	85	mA	

**Table 7. GPIO AC Specifications**

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID70	$T_{RISEF}$	Rise time in fast strong mode	2	—	12	ns	3.3 V $V_{DD}$ , Cload = 25 pF
SID71	$T_{FALLF}$	Fall time in fast strong mode	2	—	12	ns	3.3 V $V_{DD}$ , Cload = 25 pF
SID72	$T_{RISES}$	Rise time in slow strong mode	10	—	60	—	3.3 V $V_{DD}$ , Cload = 25 pF
SID73	$T_{FALLS}$	Fall time in slow strong mode	10	—	60	—	3.3 V $V_{DD}$ , Cload = 25 pF
SID74	$F_{GPIOUT1}$	GPIO $F_{OUT}$ ; 3.3 V $\leq V_{DD} \leq 5.5 \text{ V}$ . Fast strong mode.	—	—	16	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID75	$F_{GPIOUT2}$	GPIO $F_{OUT}$ ; 1.71 V $\leq V_{DD} \leq 3.3 \text{ V}$ . Fast strong mode.	—	—	16	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID76	$F_{GPIOUT3}$	GPIO $F_{OUT}$ ; 3.3 V $\leq V_{DD} \leq 5.5 \text{ V}$ . Slow strong mode.	—	—	7	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID245	$F_{GPIOUT4}$	GPIO $F_{OUT}$ ; 1.71 V $\leq V_{DD} \leq 3.3 \text{ V}$ . Slow strong mode.	—	—	3.5	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID246	$F_{GPIOIN}$	GPIO input operating frequency; 1.71 V $\leq V_{DD} \leq 5.5 \text{ V}$	—	—	16	MHz	90/10% $V_{IO}$

**Note**

7. Guaranteed by characterization.

## XRES

**Table 8. XRES DC Specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID77	$V_{IH}$	Input voltage high threshold	$0.7 \times V_{DD}$	–	–	V	CMOS Input
SID78	$V_{IL}$	Input voltage low threshold	–	–	$0.3 \times V_{DD}$	V	CMOS Input
SID79	$R_{PULLUP}$	Pull-up resistor	3.5	5.6	8.5	k $\Omega$	
SID80	$C_{IN}$	Input capacitance	–	3	7	pF	
SID81 <sup>[8]</sup>	$V_{HYSXRES}$	Input voltage hysteresis	–	$0.05 \times V_{DD}$	–	mV	Typical hysteresis is 200 mV for $V_{DD} > 4.5V$

**Table 9. XRES AC Specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID83 <sup>[8]</sup>	$T_{RESETWIDTH}$	Reset pulse width	5	–	–	$\mu s$	
BID#194 <sup>[8]</sup>	$T_{RESETWAKE}$	Wake-up time from reset release	–	–	3	ms	

## Analog Peripherals

### Comparator

**Table 10. Comparator DC Specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID330 <sup>[8]</sup>	$I_{CMP1}$	Block current, High Bandwidth mode	–	–	110	$\mu A$	
SID331 <sup>[8]</sup>	$I_{CMP2}$	Block current, Low Power mode	–	–	85	$\mu A$	
SID332 <sup>[8]</sup>	$V_{OFFSET1}$	Offset voltage, High Bandwidth mode	–	10	30	mV	
SID333 <sup>[8]</sup>	$V_{OFFSET2}$	Offset voltage, Low Power mode	–	10	30	mV	
SID334 <sup>[8]</sup>	$Z_{CMP}$	DC input impedance of comparator	35	–	–	M $\Omega$	
SID338 <sup>[8]</sup>	VINP_COMP	Comparator input range	0	–	3.6	V	Max input voltage is lower of 3.6 V or $V_{DD}$
SID339	VREF_COMP	Comparator internal voltage reference	1.188	1.2	1.212	V	

**Note**

8. Guaranteed by characterization.

**Table 11. Comparator AC Specifications (Guaranteed by Characterization)**

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID336 <sup>[8]</sup>	T <sub>COMP1</sub>	Response Time High Bandwidth mode, 50-mV overdrive	–	–	90	ns	
SID337 <sup>[8]</sup>	T <sub>COMP2</sub>	Response Time Low Power mode, 50-mV overdrive	–	–	110	ns	

**CSD**
**Table 12. CSD and IDAC Block Specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
<b>CSD and IDAC Specifications</b>							
SYS.PER#3	VDD_RIPPLE	Max allowed ripple on power supply, DC to 10 MHz	–	–	±50	mV	VDD > 2V (with ripple), 25 °C T <sub>A</sub> , Sensitivity = 0.1 pF
SYS.PER#16	VDD_RIPPLE_1.8	Max allowed ripple on power supply, DC to 10 MHz	–	–	±25	mV	VDD > 1.75V (with ripple), 25 °C T <sub>A</sub> , Parasitic Capacitance (C <sub>P</sub> ) < 20 pF, Sensitivity ≥ 0.4 pF
SID.CSD#15	VREFHI	Reference Buffer Output	1.1	1.2	1.3	V	
SID.CSD#16	IDAC1IDD	IDAC1 (8-bits) block current	–	–	1125	µA	
SID.CSD#17	IDAC2IDD	IDAC2 (7-bits) block current	–	–	1125	µA	
SID308	V <sub>CSD</sub>	Voltage range of operation	1.71	–	5.5	V	1.8 V ±5% or 1.8 V to 5.5 V
SID308A	VCOMPIDAC	Voltage compliance range of IDAC	0.8	–	V <sub>DD</sub> – 0.8	V	
SID309	IDAC1 <sub>DNL</sub>	DNL for 8-bit resolution	–1	–	1	LSB	
SID310	IDAC1 <sub>INL</sub>	INL for 8-bit resolution	–3	–	3	LSB	
SID311	IDAC2 <sub>DNL</sub>	DNL for 7-bit resolution	–1	–	1	LSB	
SID312	IDAC2 <sub>INL</sub>	INL for 7-bit resolution	–3	–	3	LSB	
SID313	SNR	Ratio of counts of finger to noise. Guaranteed by characterization	5	–	–	Ratio	Capacitance range of 9 to 35 pF, 0.1 pF sensitivity
SID314	IDAC1 <sub>CRT1</sub>	Output current of IDAC1 (8 bits) in high range	–	612	–	µA	
SID314A	IDAC1 <sub>CRT2</sub>	Output current of IDAC1(8 bits) in low range	–	306	–	µA	
SID315	IDAC2 <sub>CRT1</sub>	Output current of IDAC2 (7 bits) in high range	–	304.8	–	µA	
SID315A	IDAC2 <sub>CRT2</sub>	Output current of IDAC2 (7 bits) in low range	–	152.4	–	µA	
SID320	IDAC <sub>OFFSET</sub>	All zeroes input	–	–	±1	LSB	
SID321	IDAC <sub>GAIN</sub>	Full-scale error less offset	–	–	±10	%	
SID322	IDAC <sub>MISMATCH</sub>	Mismatch between IDACs	–	–	7	LSB	
SID323	IDAC <sub>SET8</sub>	Settling time to 0.5 LSB for 8-bit IDAC	–	–	10	µs	Full-scale transition. No external load.
SID324	IDAC <sub>SET7</sub>	Settling time to 0.5 LSB for 7-bit IDAC	–	–	10	µs	Full-scale transition. No external load.
SID325	CMOD	External modulator capacitor.	–	2.2	–	nF	5-V rating, X7R or NP0 cap.

### SWD Interface

**Table 20. SWD Interface Specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID213	F_SWDCCLK1	$3.3\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	–	–	14	MHz	SWDCCLK $\leq$ 1/3 CPU clock frequency
SID214	F_SWDCCLK2	$1.71\text{ V} \leq V_{DD} \leq 3.3\text{ V}$	–	–	7	MHz	SWDCCLK $\leq$ 1/3 CPU clock frequency
SID215 <sup>[13]</sup>	T_SWDI_SETUP	$T = 1/f\text{ SWDCCLK}$	$0.25 \cdot T$	–	–	ns	
SID216 <sup>[13]</sup>	T_SWDI_HOLD	$T = 1/f\text{ SWDCCLK}$	$0.25 \cdot T$	–	–	ns	
SID217 <sup>[13]</sup>	T_SWDO_VALID	$T = 1/f\text{ SWDCCLK}$	–	–	$0.5 \cdot T$	ns	
SID217A <sup>[13]</sup>	T_SWDO_HOLD	$T = 1/f\text{ SWDCCLK}$	1	–	–	ns	

### Internal Main Oscillator

**Table 21. IMO DC Specifications**

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID218	I <sub>IMO1</sub>	IMO operating current at 48 MHz	–	–	250	μA	
SID219	I <sub>IMO2</sub>	IMO operating current at 24 MHz	–	–	180	μA	

**Table 22. IMO AC Specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID223	F <sub>IMOTOL1</sub>	Frequency variation at 24 and 32 MHz (trimmed)	–	–	±2	%	$2\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ , and $-25\text{ °C} \leq T_A \leq 85\text{ °C}$
SID223A	F <sub>IMOTOLVCCD</sub>	Frequency variation at 24 and 32 MHz (trimmed)	–	–	±4	%	All other conditions
SID226	T <sub>STARTIMO</sub>	IMO startup time	–	–	7	μs	
SID228	T <sub>JITRMSIMO2</sub>	RMS jitter at 24 MHz	–	145	–	ps	

### Internal Low-Speed Oscillator

**Table 23. ILO DC Specifications**

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID231 <sup>[13]</sup>	I <sub>ILO1</sub>	ILO operating current	–	0.3	1.05	μA	
SID233 <sup>[13]</sup>	I <sub>ILOLEAK</sub>	ILO leakage current	–	2	15	nA	

**Table 24. ILO AC Specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID234 <sup>[13]</sup>	T <sub>STARTILO1</sub>	ILO startup time	–	–	2	ms	
SID236 <sup>[13]</sup>	T <sub>ILODUTY</sub>	ILO duty cycle	40	50	60	%	
SID237	F <sub>ILOTRIM1</sub>	ILO frequency range	20	40	80	kHz	

**Note**

13. Guaranteed by characterization.

**Table 25. External Clock Specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID305 <sup>[14]</sup>	ExtClkFreq	External clock input frequency	0	–	16	MHz	
SID306 <sup>[14]</sup>	ExtClkDuty	Duty cycle; measured at $V_{DD}/2$	45	–	55	%	

**Table 26. Block Specs**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID262 <sup>[14]</sup>	T <sub>CLKSWITCH</sub>	System clock source switching time	3	–	4	Periods	

**Note**

14. Guaranteed by characterization.



## Ordering Information

The PSoC 4000 part numbers and features are listed in the following table. All package types are available in Tape and Reel.

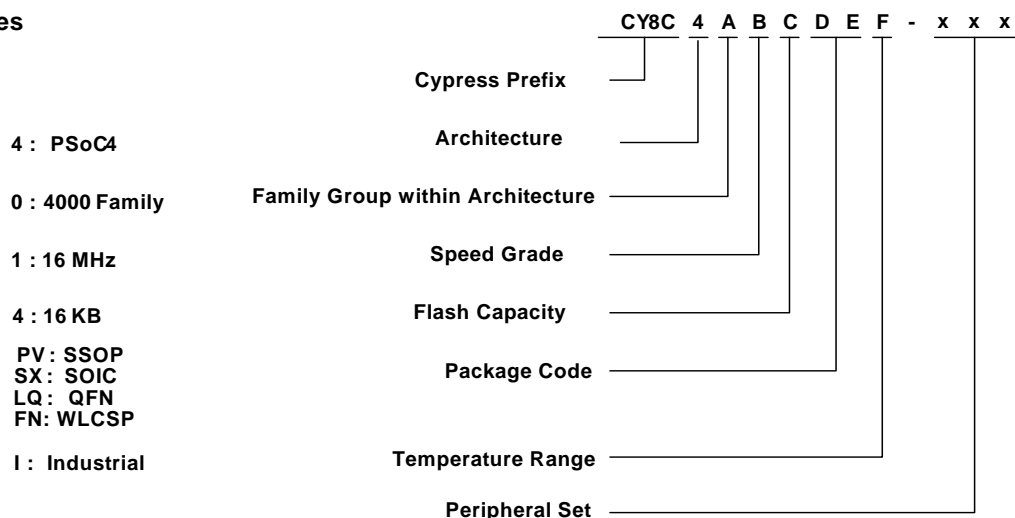
Category	MPN	Feature									Package					
		Max CPU Speed (MHz)	Flash (KB)	SRAM (KB)	CapSense	7-bit IDAC	8-bit IDAC	Comparators	TCPWM Blocks	I2C	16 - WLCSP	8-SOIC	16-SOIC	16-QFN	24-QFN	28-SSOP
CY8C4013	CY8C4013SXI-400	16	8	2	–	–	–	–	1	1	–	✓	–	–	–	–
	CY8C4013SXI-410	16	8	2	–	1	1	1	1	1	–	✓	–	–	–	–
	CY8C4013SXI-411	16	8	2	–	1	1	1	1	1	–	–	✓	–	–	–
	CY8C4013LQI-411	16	8	2	–	1	1	1	1	1	–	–	–	✓	–	–
CY8C4014	CY8C4014SXI-420	16	16	2	✓	1	1	1	1	1	–	✓	–	–	–	–
	CY8C4014SXI-411	16	16	2	–	1	1	1	1	1	–	–	✓	–	–	–
	CY8C4014SXI-421	16	16	2	✓	1	1	1	1	1	–	–	✓	–	–	–
	CY8C4014LQI-421	16	16	2	✓	1	1	1	1	1	–	–	–	✓	–	–
	CY8C4014LQI-412	16	16	2	–	1	1	1	1	1	–	–	–	–	✓	–
	CY8C4014LQI-422	16	16	2	✓	1	1	1	1	1	–	–	–	–	✓	–
	CY8C4014PVI-412	16	16	2	–	1	1	1	1	1	–	–	–	–	–	✓
	CY8C4014PVI-422	16	16	2	✓	1	1	1	1	1	–	–	–	–	–	✓
	CY8C4014FNI-421	16	16	2	✓	1	1	1	1	1	✓	–	–	–	–	–
Other	CY8C4014LQI-SLT1	16	16	2	✓	1	1	1	1	1	–	–	–	✓	–	–
	CY8C4014LQI-SLT2	16	16	2	✓	1	1	1	1	1	–	–	–	–	✓	–

## Part Numbering Conventions

PSoC 4 devices follow the part numbering convention described in the following table. All fields are single-character alphanumeric (0, 1, 2, ..., 9, A, B, ..., Z) unless stated otherwise.

The part numbers are of the form CY8C4ABCDEF-XYZ where the fields are defined as follows.

### Examples



## Packaging

**Table 27. Package List**

Spec ID#	Package	Description
BID#47A	28-Pin SSOP	28-pin 5 × 10 × 1.65mm SSOP with 0.65-mm pitch
BID#26	24-Pin QFN	24-pin 4 × 4 × 0.6 mm QFN with 0.5-mm pitch
BID#33	16-Pin QFN	16-pin 3 × 3 × 0.6 mm QFN with 0.5-mm pitch
BID#40	16-Pin SOIC	16-pin (150 Mil) SOIC
BID#47	8-Pin SOIC	8-pin (150 Mil) SOIC
BID#147A	16-Ball WLCSP	16-Ball 1.47 × 1.58 × 0.4 mm

**Table 28. Package Characteristics**

Parameter	Description	Conditions	Min	Typ	Max	Units
T <sub>A</sub>	Operating ambient temperature		−40	25	85	°C
T <sub>J</sub>	Operating junction temperature		−40	–	100	°C
T <sub>JA</sub>	Package θ <sub>JA</sub> (28-pin SSOP)		–	66.6	–	°C/Watt
T <sub>JC</sub>	Package θ <sub>JC</sub> (28-pin SSOP)		–	34	–	°C/Watt
T <sub>JA</sub>	Package θ <sub>JA</sub> (24-pin QFN)		–	38	–	°C/Watt
T <sub>JC</sub>	Package θ <sub>JC</sub> (24-pin QFN)		–	5.6	–	°C/Watt
T <sub>JA</sub>	Package θ <sub>JA</sub> (16-pin QFN)		–	49.6	–	°C/Watt
T <sub>JC</sub>	Package θ <sub>JC</sub> (16-pin QFN)		–	5.9	–	°C/Watt
T <sub>JA</sub>	Package θ <sub>JA</sub> (16-pin SOIC)		–	142	–	°C/Watt
T <sub>JC</sub>	Package θ <sub>JC</sub> (16-pin SOIC)		–	49.8	–	°C/Watt
T <sub>JA</sub>	Package θ <sub>JA</sub> (16-ball WLCSP)		–	90	–	°C/Watt
T <sub>JC</sub>	Package θ <sub>JC</sub> (16-ball WLCSP)		–	0.9	–	°C/Watt
T <sub>JA</sub>	Package θ <sub>JA</sub> (8-pin SOIC)		–	198	–	°C/Watt
T <sub>JC</sub>	Package θ <sub>JC</sub> (8-pin SOIC)		–	56.9	–	°C/Watt

**Table 29. Solder Reflow Peak Temperature**

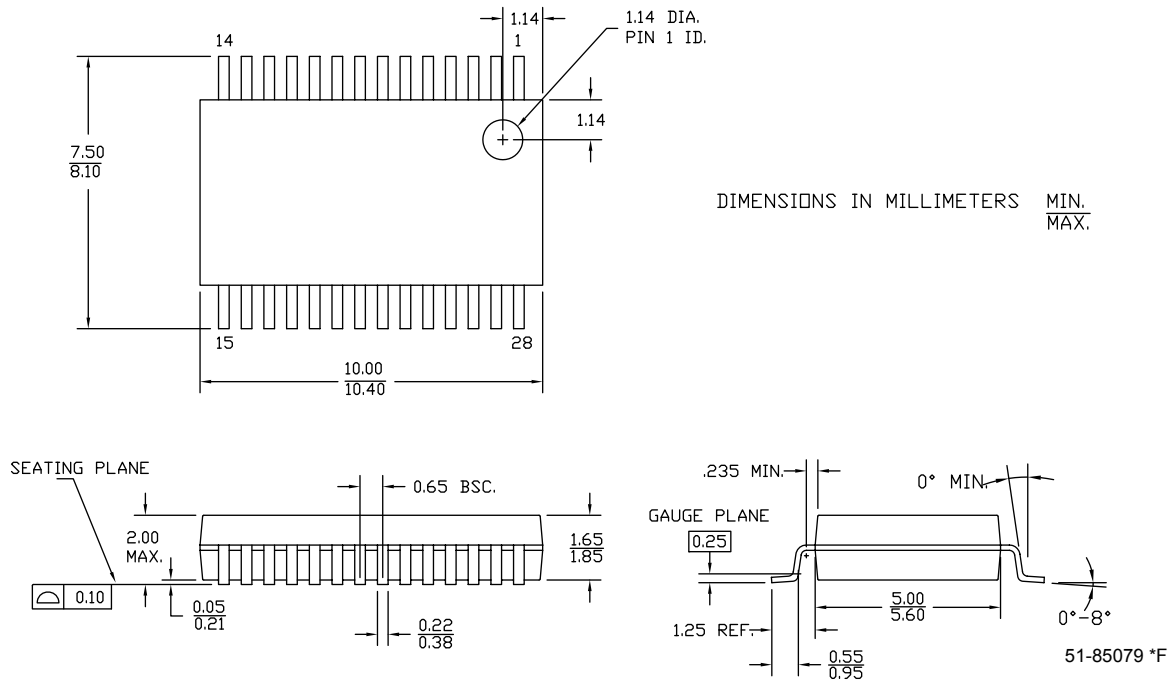
Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
All	260 °C	30 seconds

**Table 30. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-020**

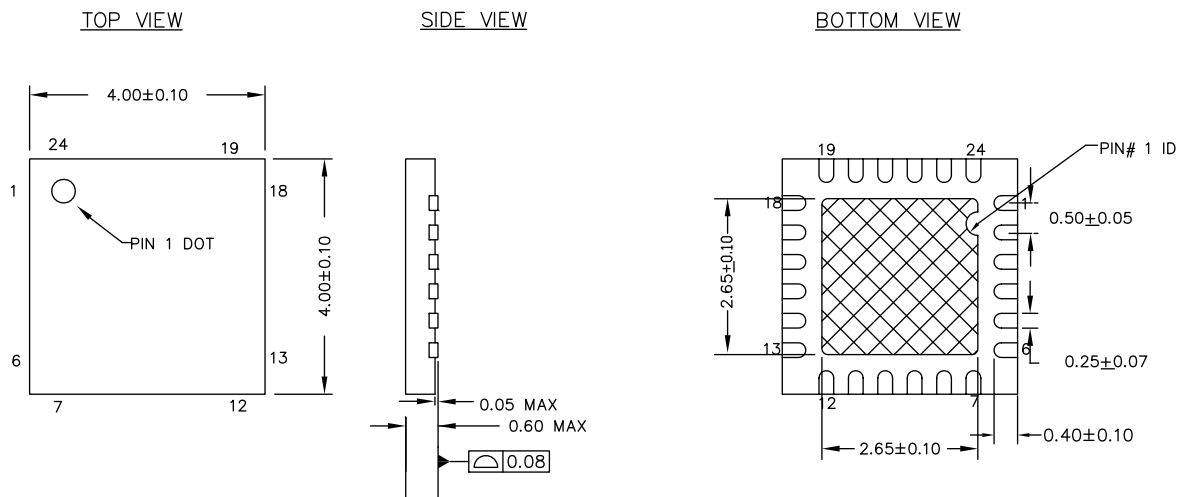
Package	MSL
All except WLCSP	MSL 3
16-ball WLCSP	MSL1

## Package Outline Drawings

**Figure 11. 28-Pin SSOP Package Outline**



**Figure 12. 24-pin QFN EPAD (Sawn) Package Outline**



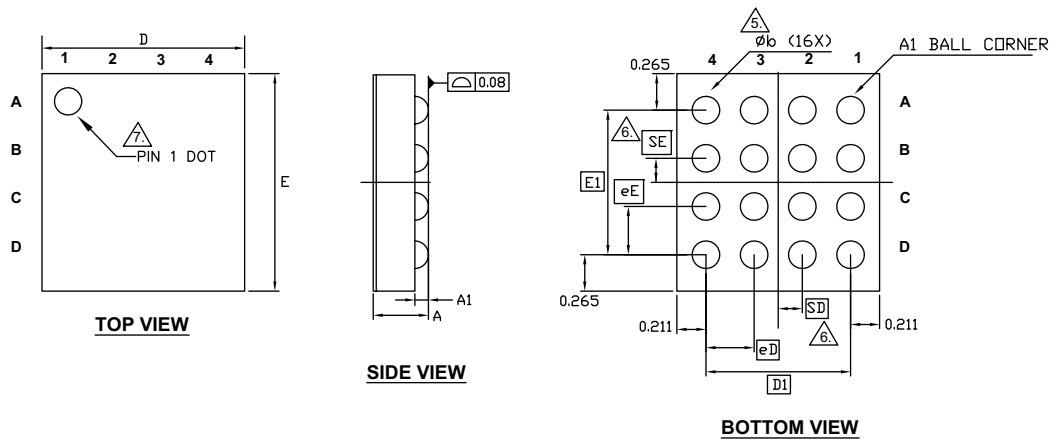
### NOTES :

1. HATCH IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC # MO-248
3. PACKAGE WEIGHT : 29 ± 3 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-13937 °F

### Note

15. Dimensions of the QFN package drawings are in millimeters.

**Figure 16. 16-Ball WLCSP 1.47 x 1.58 x 0.4 mm**


SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	0.42
A1	0.089	0.099	0.109
D	1.447	1.472	1.497
E	1.554	1.579	1.604
D1	1.05 BSC		
E1	1.05 BSC		
MD	4		
ME	4		
N	16		
Ø b	0.17	0.20	0.23
eD	0.35 BSC		
eE	0.35 BSC		
SD	0.18 BSC		
SE	0.18 BSC		

**NOTES:**

- ALL DIMENSIONS ARE IN MILLIMETERS.
- SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
- "e" REPRESENTS THE SOLDER BALL GRID PITCH.
- SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION. N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
- DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
- "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0. WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
- A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
- "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.
- JEDEC SPECIFICATION NO. REF. : N/A.

002-18598 \*\*

**Table 31. Acronyms Used in this Document** *(continued)*

Acronym	Description
PC	program counter
PCB	printed circuit board
PGA	programmable gain amplifier
PHUB	peripheral hub
PHY	physical layer
PICU	port interrupt control unit
PLA	programmable logic array
PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration data sheet
POR	power-on reset
PRES	precise power-on reset
PRS	pseudo random sequence
PS	port read data register
PSoC®	Programmable System-on-Chip™
PSRR	power supply rejection ratio
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I <sup>2</sup> C serial clock
SDA	I <sup>2</sup> C serial data
S/H	sample and hold
SINAD	signal to noise and distortion ratio
SIO	special input/output, GPIO with advanced features. See GPIO.
SOC	start of conversion
SOF	start of frame
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory
SRES	software reset
SWD	serial wire debug, a test protocol

**Table 31. Acronyms Used in this Document** *(continued)*

Acronym	Description
SWV	single-wire viewer
TD	transaction descriptor, see also DMA
THD	total harmonic distortion
TIA	transimpedance amplifier
TRM	technical reference manual
TTL	transistor-transistor logic
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UDB	universal digital block
USB	Universal Serial Bus
USBIO	USB input/output, PSoC pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset I/O pin
XTAL	crystal

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