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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	16MHz
Connectivity	I²C
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	12
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	D/A 1x7b, 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-SOIC (0.154", 3.90mm Width)
Supplier Device Package	16-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4013sxi-411t

More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article [KBA86521, How to Design with PSoC 3, PSoC 4, and PSoC 5LP](#). Following is an abbreviated list for PSoC 4:

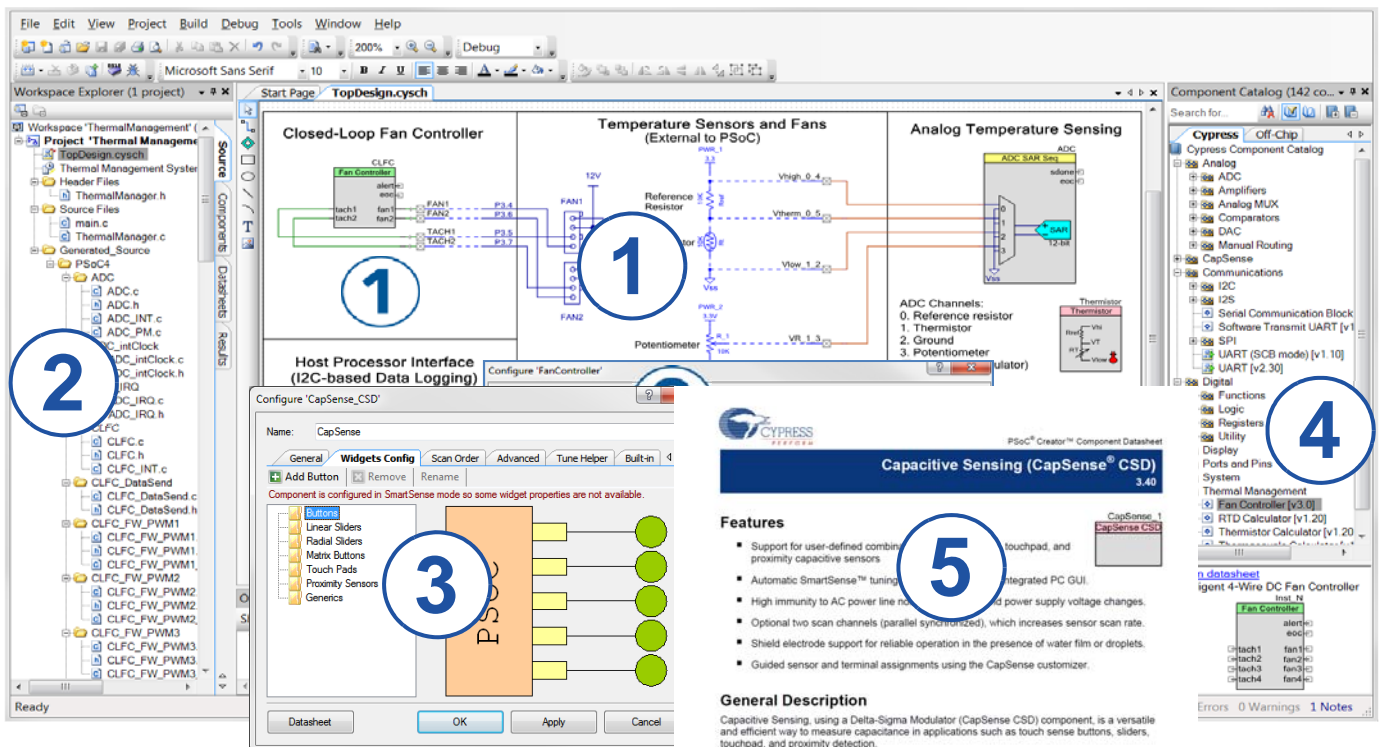
- Overview: [PSoC Portfolio](#), [PSoC Roadmap](#)
- Product Selectors: [PSoC 1](#), [PSoC 3](#), [PSoC 4](#), [PSoC 5LP](#)
In addition, PSoC Creator includes a device selection tool.
- Application notes: Cypress offers a large number of PSoC application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with PSoC 4 are:
 - [AN79953](#): Getting Started With PSoC 4
 - [AN88619](#): PSoC 4 Hardware Design Considerations
 - [AN86439](#): Using PSoC 4 GPIO Pins
 - [AN57821](#): Mixed Signal Circuit Board Layout
 - [AN81623](#): Digital Design Best Practices
 - [AN73854](#): Introduction To Bootloaders
 - [AN89610](#): ARM Cortex Code Optimization
- Technical Reference Manual (TRM) is in two documents:
 - [Architecture TRM](#) details each PSoC 4 functional block.
 - [Registers TRM](#) describes each of the PSoC 4 registers.
- Development Kits:
 - CY8CKIT-040, PSoC 4000 Pioneer Kit, is an easy-to-use and inexpensive development platform with debugging capability. This kit includes connectors for Arduino[™] compatible shields and Digilent[®] Pmod[™] daughter cards.
 - The MiniProg3 device provides an interface for flash programming and debug.

PSoC Creator

[PSoC Creator](#) is a free Windows-based Integrated Design Environment (IDE). It enables concurrent hardware and firmware design of PSoC 3, PSoC 4, and PSoC 5LP based systems. Create designs using classic, familiar schematic capture supported by over 100 pre-verified, production-ready PSoC Components; see the [list of component datasheets](#). With PSoC Creator, you can:

1. Drag and drop component icons to build your hardware system design in the main design workspace
2. Codesign your application firmware with the PSoC hardware, using the PSoC Creator IDE C compiler
3. Configure components using the configuration tools
4. Explore the library of 100+ components
5. Review component datasheets

Figure 1. CapSense Example Project in PSoC Creator



Functional Definition

CPU and Memory Subsystem

CPU

The Cortex-M0 CPU in the PSoC 4000 is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. Most instructions are 16 bits in length and the CPU executes a subset of the Thumb-2 instruction set. This enables fully compatible, binary, upward migration of the code to higher performance processors, such as the Cortex-M3 and M4. It includes a nested vectored interrupt controller (NVIC) block with eight interrupt inputs and also includes a Wakeup Interrupt Controller (WIC). The WIC can wake the processor from the Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in the Deep Sleep mode. The CPU subsystem also includes a 24-bit timer called SYSTICK, which can generate an interrupt.

The CPU also includes a debug interface, the serial wire debug (SWD) interface, which is a 2-wire form of JTAG. The debug configuration used for PSoC 4000 has four breakpoint (address) comparators and two watchpoint (data) comparators.

Flash

The PSoC 4000 device has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The low-power flash block is designed to deliver zero wait-state (WS) access time at 16 MHz.

SRAM

Two KB of SRAM are provided with zero wait-state access at 16 MHz.

SROM

A supervisory ROM that contains boot and configuration routines is provided.

System Resources

Power System

The power system is described in detail in the section on [Power on page 12](#). It provides an assurance that voltage levels are as required for each respective mode and either delays mode entry (for example, on power-on reset (POR)) until voltage levels are as required for proper functionality, or generates resets (for example, on brown-out detection). The PSoC 4000 operates with a single external supply over the range of either 1.8 V \pm 5% (externally regulated) or 1.8 to 5.5 V (internally regulated) and has three different power modes, transitions between which are managed by the power system. The PSoC 4000 provides Active, Sleep, and Deep Sleep low-power modes.

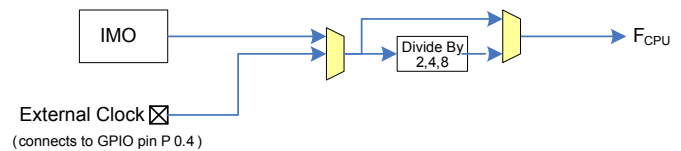
All subsystems are operational in Active mode. The CPU subsystem (CPU, flash, and SRAM) is clock-gated off in Sleep mode, while all peripherals and interrupts are active with instantaneous wake-up on a wake-up event. In Deep Sleep mode, the high-speed clock and associated circuitry is switched off; wake-up from this mode takes 35 μ S.

Clock System

The PSoC 4000 clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that there are no metastable conditions.

The clock system for the PSoC 4000 consists of the internal main oscillator (IMO) and the internal low-frequency oscillator (ILO) and provision for an external clock.

Figure 3. PSoC 4000 MCU Clocking Architecture



The F_{CPU} signal can be divided down to generate synchronous clocks for the analog and digital peripherals. There are four clock dividers for the PSoC 4000, each with 16-bit divide capability. The 16-bit capability allows flexible generation of fine-grained frequency values and is fully supported in PSoC Creator.

IMO Clock Source

The IMO is the primary source of internal clocking in the PSoC 4000. It is trimmed during testing to achieve the specified accuracy. The IMO default frequency is 24 MHz and it can be adjusted from 24 to 48 MHz in steps of 4 MHz. The IMO tolerance with Cypress-provided calibration settings is \pm 2% (24 and 32 MHz).

ILO Clock Source

The ILO is a very low power, 40-kHz oscillator, which is primarily used to generate clocks for the watchdog timer (WDT) and peripheral operation in Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy.

Watchdog Timer

A watchdog timer is implemented in the clock block running from the ILO; this allows watchdog operation during Deep Sleep and generates a watchdog reset if not serviced before the set timeout occurs. The watchdog reset is recorded in a Reset Cause register, which is firmware readable.

Reset

The PSoC 4000 can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through reset and allows software to determine the cause of the reset. An XRES pin is reserved for external reset on the 24-pin package. An internal POR is provided on the 16-pin and 8-pin packages. The XRES pin has an internal pull-up resistor that is always enabled. Reset is Active Low.

Voltage Reference

The PSoC 4000 reference system generates all internally required references. A 1.2-V voltage reference is provided for the comparator. The IDACs are based on a \pm 5% reference.

Analog Blocks

Low-power Comparators

The PSoC 4000 has a low-power comparator, which uses the built-in voltage reference. Any one of up to 16 pins can be used as a comparator input and the output of the comparator can be brought out to a pin. The selected comparator input is connected to the minus input of the comparator with the plus input always connected to the 1.2-V voltage reference. This comparator is also used for CapSense purposes and is not available during CapSense operation.

Current DACs

The PSoC 4000 has two IDACs, which can drive any of up to 16 pins on the chip. These IDACs have programmable current ranges.

Analog Multiplexed Buses

The PSoC 4000 has two concentric independent buses that go around the periphery of the chip. These buses (called amux buses) are connected to firmware-programmable analog switches that allow the chip's internal resources (IDACs, comparator) to connect to any pin on Ports 0, 1, and 2.

Fixed Function Digital

Timer/Counter/PWM (TCPWM) Block

The TCPWM block consists of a 16-bit counter with user-programmable period length. There is a capture register to record the count value at the time of an event (which may be an I/O event), a period register that is used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals that are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow use as dead-band programmable complementary PWM outputs. It also has a Kill input to force outputs to a predetermined state; for example, this is used in motor drive systems when an over-current state is indicated and the PWM driving the FETs needs to be shut off immediately with no time for software intervention.

Serial Communication Block (SCB)

The PSoC 4000 has a serial communication block, which implements a multi-master I²C interface.

I²C Mode: The hardware I²C block implements a full multi-master and slave interface (it is capable of multi-master arbitration). This block is capable of operating at speeds of up to 400 kbps (Fast Mode) and has flexible buffering options to reduce interrupt overhead and latency for the CPU. It also supports EZI²C that creates a mailbox address range in the memory of the PSoC 4000 and effectively reduces I²C communication to reading from and writing to an array in memory. In addition, the block supports an 8-deep FIFO for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduces the need for clock stretching caused by the CPU not having read data on time.

The I²C peripheral is compatible with the I²C Standard-mode and Fast-mode devices as defined in the NXP I²C-bus specification and user manual (UM10204). The I²C bus I/O is implemented with GPIO in open-drain modes.

The PSoC 4000 is not completely compliant with the I²C spec in the following respect:

- GPIO cells are not overvoltage tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I²C system.
- Fast-mode minimum fall time is not met in Fast Strong mode; Slow Strong mode can help meet this spec depending on the Bus Load.

GPIO

The PSoC 4000 has up to 20 GPIOs. The GPIO block implements the following:

- Eight drive modes:
 - Analog input mode (input and output buffers disabled)
 - Input only
 - Weak pull-up with strong pull-down
 - Strong pull-up with weak pull-down
 - Open drain with strong pull-down
 - Open drain with strong pull-up
 - Strong pull-up with strong pull-down
 - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTTL).
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes
- Selectable slew rates for dV/dt related noise control to improve EMI

The pins are organized in logical entities called ports, which are 8-bit in width (less for Ports 2 and 3). During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin.

Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves.

Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it (4 for PSoC 4000).

The 28-pin and 24-pin packages have 20 GPIOs. The 16-pin SOIC has 13 GPIOs. The 16-pin QFN and the 16-ball WLCSP have 12 GPIOs. The 8-pin SOIC has 5 GPIOs.

Special Function Peripherals

CapSense

CapSense is supported in the PSoC 4000 through a CSD block that can be connected to up to 16 pins through an analog mux bus via an analog switch (pins on Port 3 are not available for CapSense purposes). CapSense function can thus be provided on any available pin or group of pins in a system under software control. A PSoC Creator component is provided for the CapSense block to make it easy for the user.

Shield voltage can be driven on another mux bus to provide water-tolerance capability. Water tolerance is provided by driving the shield electrode in phase with the sense electrode to keep the shield capacitance from attenuating the sensed input. Proximity sensing can also be implemented.

The CapSense block has two IDACs, which can be used for general purposes if CapSense is not being used (both IDACs are available in that case) or if CapSense is used without water tolerance (one IDAC is available).

Pinouts

All port pins support GPIO. Ports 0, 1, and 2 support CSD CapSense and analog multiplexed bus connections. TCPWM functions and Alternate Functions are multiplexed with port pins as follows for the five PSoC 4000 packages.

Table 1. Pin Descriptions

28-Pin SSOP		24-Pin QFN		16-Pin QFN		16-Pin SOIC		8-Pin SOIC		TCPWM Signals	Alternate Functions
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name		
20	VSS										
21	P0.0/TRIN0	1	P0.0/TRIN0							TRIN0: Trigger Input 0	
22	P0.1/TRIN1/CMPO_0	2	P0.1/TRIN1/CMPO_0	1	P0.1/TRIN1/CMPO_0	3	P0.1/TRIN1/CMPO_0			TRIN1: Trigger Input 1	CMPO_0: Sense Comp Out
23	P0.2/TRIN2	3	P0.2/TRIN2	2	P0.2/TRIN2	4	P0.2/TRIN2			TRIN2: Trigger Input 2	
24	P0.3/TRIN3	4	P0.3/TRIN3							TRIN3: Trigger Input 3	
25	P0.4/TRIN4/CMPO_0/EXT_CLK	5	P0.4/TRIN4/CMPO_0/EXT_CLK	3	P0.4/TRIN4/CMPO_0/EXT_CLK	5	P0.4/TRIN4/CMPO_0/EXT_CLK	2	P0.4/TRIN4/CMPO_0/EXT_CLK	TRIN4: Trigger Input 4	CMPO_0: Sense Comp Out, External Clock, CMOD Cap
26	VCC	6	VCC	4	VCC	6	VCC	3	VCC		
27	VDD	7	VDD	6	VDD	7	VDD	4	VDD		
28	VSS	8	VSS	7	VSS	8	VSS	5	VSS		
1	P0.5	9	P0.5	5	VDDIO	9	P0.5				
2	P0.6	10	P0.6	8	P0.6	10	P0.6				
3	P0.7	11	P0.7								
4	P1.0	12	P1.0								
5	P1.1/OUT0	13	P1.1/OUT0	9	P1.1/OUT0	11	P1.1/OUT0	6	P1.1/OUT0	OUT0: PWM OUT 0	
6	P1.2/SCL	14	P1.2/SCL	10	P1.2/SCL	12	P1.2/SCL				I2C Clock
7	P1.3/SDA	15	P1.3/SDA	11	P1.3/SDA	13	P1.3/SDA				I2C Data
8	P1.4/UND0	16	P1.4/UND0							UND0: Underflow Out	
9	P1.5/OVF0	17	P1.5/OVF0							OVF0: Overflow Out	
10	P1.6/OVF0/UND0/nOUT0/CMPO_0	18	P1.6/OVF0/UND0/nOUT0/CMPO_0	12	P1.6/OVF0/UND0/nOUT0/CMPO_0	14	P1.6/OVF0/UND0/nOUT0/CMPO_0	7	P1.6/OVF0/UND0/nOUT0/CMPO_0	nOUT0: Complement of OUT0, UND0, OVF0 as above	CMPO_0: Sense Comp Out, Internal Reset function ^[1]

Note

1. Must not have load to ground during POR (should be an output).

Figure 7. 16-Pin SOIC Pinout

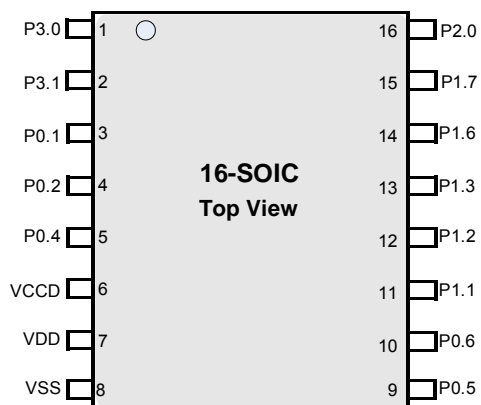
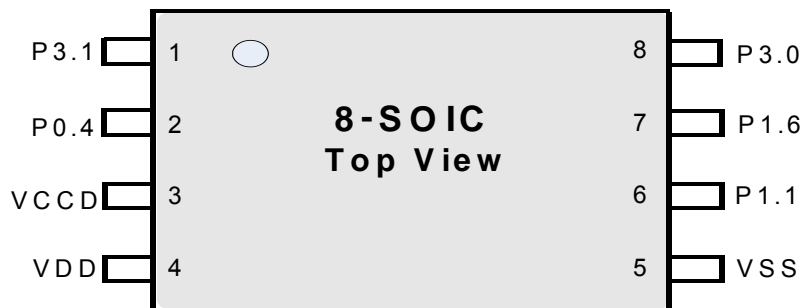


Figure 8. 8-Pin SOIC Pinout



Power

The following power system diagrams (Figure 9 and Figure 10) show the set of power supply pins as implemented for the PSoC 4000. The system has one regulator in Active mode for the digital circuitry. There is no analog regulator; the analog circuits run directly from the V_{DD} input. There is a separate regulator for the Deep Sleep mode. The supply voltage range is either 1.8 V \pm 5% (externally regulated) or 1.8 V to 5.5 V (unregulated externally; regulated internally) with all functions and circuits operating over that range.

The V_{DDIO} pin, available in the 16-pin QFN package, provides a separate voltage domain for the following pins: P3.0, P3.1, and P3.2. P3.0 and P3.1 can be I²C pins and the chip can thus communicate with an I²C system, running at a different voltage (where $V_{DDIO} \leq V_{DD}$). For example, V_{DD} can be 3.3 V and V_{DDIO} can be 1.8 V.

The PSoC 4000 family allows two distinct modes of power supply operation: Unregulated External Supply and Regulated External Supply.

Unregulated External Supply

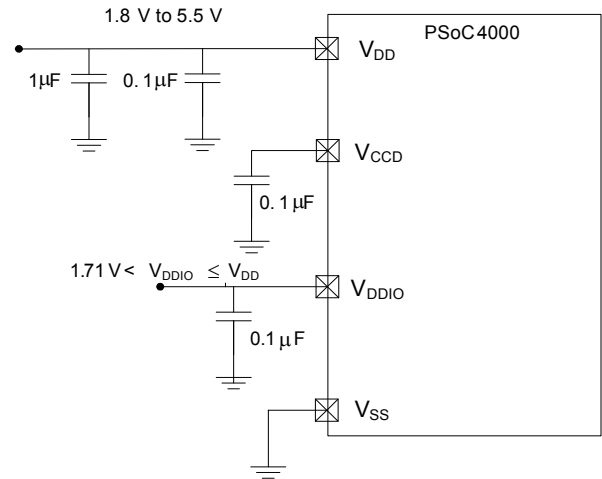
In this mode, the PSoC 4000 is powered by an external power supply that can be anywhere in the range of 1.8 to 5.5 V. This range is also designed for battery-powered operation. For example, the chip can be powered from a battery system that starts at 3.5 V and works down to 1.8 V. In this mode, the internal regulator of the PSoC 4000 supplies the internal logic and the V_{CCD} output of the PSoC 4000 must be bypassed to ground via an external capacitor (0.1 μ F; X5R ceramic or better).

Bypass capacitors must be used from V_{DD} to ground. The typical practice for systems in this frequency range is to use a capacitor in the 1- μ F range, in parallel with a smaller capacitor (0.1 μ F, for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

An example of a bypass scheme follows (V_{DDIO} is available on the 16-QFN package).

Figure 9. 16-pin QFN Bypass Scheme Example - Unregulated External Supply

Power supply connections when $1.8 \leq V_{DD} \leq 5.5$ V



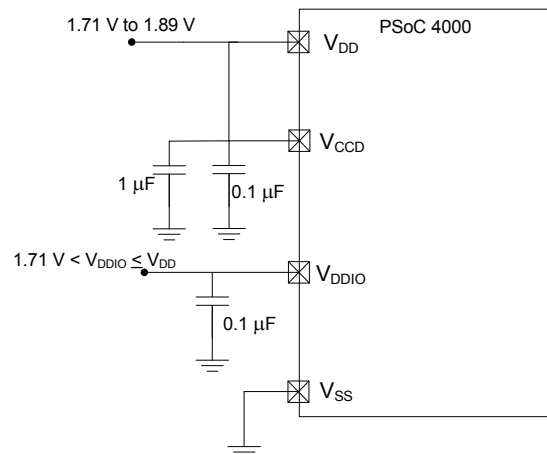
Regulated External Supply

In this mode, the PSoC 4000 is powered by an external power supply that must be within the range of 1.71 to 1.89 V; note that this range needs to include the power supply ripple too. In this mode, the V_{DD} and V_{CCD} pins are shorted together and bypassed. The internal regulator should be disabled in the firmware. Note that in this mode V_{DD} (V_{CCD}) should never exceed 1.89 in any condition, including flash programming.

An example of a bypass scheme follows (V_{DDIO} is available on the 16-QFN package).

Figure 10. 16-pin QFN Bypass Scheme Example - Regulated External Supply

Power supply connections when $1.71 \leq V_{DD} \leq 1.89$ V



Development Support

The PSoC 4000 family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit www.cypress.com/go/psoc4 to find out more.

Documentation

A suite of documentation supports the PSoC 4000 family to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

Software User Guide: A step-by-step guide for using PSoC Creator. The software user guide shows you how the PSoC Creator build process works in detail, how to use source control with PSoC Creator, and much more.

Component Datasheets: The flexibility of PSoC allows the creation of new peripherals (components) long after the device has gone into production. Component data sheets provide all of the information needed to select and use a particular component, including a functional description, API documentation, example code, and AC/DC specifications.

Application Notes: PSoC application notes discuss a particular application of PSoC in depth; examples include brushless DC motor control and on-chip filtering. Application notes often include example projects in addition to the application note document.

Technical Reference Manual: The Technical Reference Manual (TRM) contains all the technical detail you need to use a PSoC device, including a complete description of all PSoC registers. The TRM is available in the Documentation section at www.cypress.com/psoc4.

Online

In addition to print documentation, the Cypress PSoC forums connect you with fellow PSoC users and experts in PSoC from around the world, 24 hours a day, 7 days a week.

Tools

With industry standard cores, programming, and debugging interfaces, the PSoC 4000 family is part of a development tool ecosystem. Visit us at www.cypress.com/go/psoccreator for the latest information on the revolutionary, easy to use PSoC Creator IDE, supported third party compilers, programmers, debuggers, and development kits.

Electrical Specifications

Absolute Maximum Ratings

Table 3. Absolute Maximum Ratings^[4]

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID1	V _{DD_ABS}	Digital supply relative to V _{SS}	-0.5	—	6	V	
SID2	V _{CCD_ABS}	Direct digital core voltage input relative to V _{SS}	-0.5	—	1.95	V	
SID3	V _{GPIO_ABS}	GPIO voltage	-0.5	—	V _{DD} +0.5	V	
SID4	I _{GPIO_ABS}	Maximum current per GPIO	-25	—	25	mA	
SID5	I _{GPIO_injection}	GPIO injection current, Max for V _{IH} > V _{DD} , and Min for V _{IL} < V _{SS}	-0.5	—	0.5	mA	Current injected per pin
BID44	ESD_HBM	Electrostatic discharge human body model	2200	—	—	V	
BID45	ESD_CDM	Electrostatic discharge charged device model	500	—	—	V	
BID46	LU	Pin current for latch-up	-140	—	140	mA	

Device Level Specifications

All specifications are valid for -40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

Table 4. DC Specifications

Typical values measured at V_{DD} = 3.3 V and 25 °C.

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID53	V _{DD}	Power supply input voltage	1.8	—	5.5	V	With regulator enabled
SID255	V _{DD}	Power supply input voltage (V _{CCD} = V _{DD})	1.71	—	1.89	V	Internally unregulated supply
SID54	V _{DDIO}	V _{DDIO} domain supply	1.71	—	V _{DD}	V	
SID55	C _{EFC}	External regulator voltage bypass	—	0.1	—	μF	X5R ceramic or better
SID56	C _{EXC}	Power supply bypass capacitor	—	1	—	μF	X5R ceramic or better
Active Mode, V_{DD} = 1.8 to 5.5 V							
SID9	I _{DD5}	Execute from flash; CPU at 6 MHz	—	2.0	2.85	mA	
SID12	I _{DD8}	Execute from flash; CPU at 12 MHz	—	3.2	3.75	mA	
SID16	I _{DD11}	Execute from flash; CPU at 16 MHz	—	4.0	4.5	mA	
Sleep Mode, V_{DD} = 1.71 to 5.5 V							
SID25	I _{DD20}	I ² C wakeup, WDT on. 6 MHz	—	1.1	—	mA	
SID25A	I _{DD20A}	I ² C wakeup, WDT on. 12 MHz	—	1.4	—	mA	
Deep Sleep Mode, V_{DD} = 1.8 to 3.6 V (Regulator on)							
SID31	I _{DD26}	I ² C wakeup and WDT on	—	2.5	8.2	μA	

Note

4. Usage above the absolute maximum conditions listed in Table 1 may cause permanent damage to the device. Exposure to Absolute Maximum conditions for extended periods of time may affect device reliability. The Maximum Storage Temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below Absolute Maximum conditions but above normal operating conditions, the device may not operate to specification.

Table 6. GPIO DC Specifications (referenced to V_{DDIO} for 16-Pin QFN V_{DDIO} pins) (continued)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID67 ^[7]	V_{HYSTTL}	Input hysteresis LVTTL	15	40	—	mV	$V_{DD} \geq 2.7 \text{ V}$
SID68 ^[7]	$V_{HYSCMOS}$	Input hysteresis CMOS	$0.05 \times V_{DD}$	—	—	mV	$V_{DD} < 4.5 \text{ V}$
SID68A ^[7]	$V_{HYSCMOS5V5}$	Input hysteresis CMOS	200	—	—	mV	$V_{DD} > 4.5 \text{ V}$
SID69 ^[7]	I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	—	—	100	μA	
SID69A ^[7]	I_{TOT_GPIO}	Maximum total source or sink chip current	—	—	85	mA	

Table 7. GPIO AC Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID70	T_{RISEF}	Rise time in fast strong mode	2	—	12	ns	3.3 V V_{DD} , Cload = 25 pF
SID71	T_{FALLF}	Fall time in fast strong mode	2	—	12	ns	3.3 V V_{DD} , Cload = 25 pF
SID72	T_{RISES}	Rise time in slow strong mode	10	—	60	—	3.3 V V_{DD} , Cload = 25 pF
SID73	T_{FALLS}	Fall time in slow strong mode	10	—	60	—	3.3 V V_{DD} , Cload = 25 pF
SID74	$F_{GPIOUT1}$	GPIO F_{OUT} ; 3.3 V $\leq V_{DD} \leq 5.5 \text{ V}$. Fast strong mode.	—	—	16	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID75	$F_{GPIOUT2}$	GPIO F_{OUT} ; 1.71 V $\leq V_{DD} \leq 3.3 \text{ V}$. Fast strong mode.	—	—	16	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID76	$F_{GPIOUT3}$	GPIO F_{OUT} ; 3.3 V $\leq V_{DD} \leq 5.5 \text{ V}$. Slow strong mode.	—	—	7	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID245	$F_{GPIOUT4}$	GPIO F_{OUT} ; 1.71 V $\leq V_{DD} \leq 3.3 \text{ V}$. Slow strong mode.	—	—	3.5	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID246	F_{GPIOIN}	GPIO input operating frequency; 1.71 V $\leq V_{DD} \leq 5.5 \text{ V}$	—	—	16	MHz	90/10% V_{IO}

Note

7. Guaranteed by characterization.

Table 11. Comparator AC Specifications (Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID336 ^[8]	T _{COMP1}	Response Time High Bandwidth mode, 50-mV overdrive	–	–	90	ns	
SID337 ^[8]	T _{COMP2}	Response Time Low Power mode, 50-mV overdrive	–	–	110	ns	

CSD

Table 12. CSD and IDAC Block Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
CSD and IDAC Specifications							
SYS.PER#3	VDD_RIPPLE	Max allowed ripple on power supply, DC to 10 MHz	–	–	±50	mV	VDD > 2V (with ripple), 25 °C T _A , Sensitivity = 0.1 pF
SYS.PER#16	VDD_RIPPLE_1.8	Max allowed ripple on power supply, DC to 10 MHz	–	–	±25	mV	VDD > 1.75V (with ripple), 25 °C T _A , Parasitic Capacitance (C _P) < 20 pF, Sensitivity ≥ 0.4 pF
SID.CSD#15	VREFHI	Reference Buffer Output	1.1	1.2	1.3	V	
SID.CSD#16	IDAC1IDD	IDAC1 (8-bits) block current	–	–	1125	µA	
SID.CSD#17	IDAC2IDD	IDAC2 (7-bits) block current	–	–	1125	µA	
SID308	V _{CSD}	Voltage range of operation	1.71	–	5.5	V	1.8 V ±5% or 1.8 V to 5.5 V
SID308A	VCOMPIDAC	Voltage compliance range of IDAC	0.8	–	V _{DD} – 0.8	V	
SID309	IDAC1 _{DNL}	DNL for 8-bit resolution	–1	–	1	LSB	
SID310	IDAC1 _{INL}	INL for 8-bit resolution	–3	–	3	LSB	
SID311	IDAC2 _{DNL}	DNL for 7-bit resolution	–1	–	1	LSB	
SID312	IDAC2 _{INL}	INL for 7-bit resolution	–3	–	3	LSB	
SID313	SNR	Ratio of counts of finger to noise. Guaranteed by characterization	5	–	–	Ratio	Capacitance range of 9 to 35 pF, 0.1 pF sensitivity
SID314	IDAC1 _{CRT1}	Output current of IDAC1 (8 bits) in high range	–	612	–	µA	
SID314A	IDAC1 _{CRT2}	Output current of IDAC1(8 bits) in low range	–	306	–	µA	
SID315	IDAC2 _{CRT1}	Output current of IDAC2 (7 bits) in high range	–	304.8	–	µA	
SID315A	IDAC2 _{CRT2}	Output current of IDAC2 (7 bits) in low range	–	152.4	–	µA	
SID320	IDAC _{OFFSET}	All zeroes input	–	–	±1	LSB	
SID321	IDAC _{GAIN}	Full-scale error less offset	–	–	±10	%	
SID322	IDAC _{MISMATCH}	Mismatch between IDACs	–	–	7	LSB	
SID323	IDAC _{SET8}	Settling time to 0.5 LSB for 8-bit IDAC	–	–	10	µs	Full-scale transition. No external load.
SID324	IDAC _{SET7}	Settling time to 0.5 LSB for 7-bit IDAC	–	–	10	µs	Full-scale transition. No external load.
SID325	CMOD	External modulator capacitor.	–	2.2	–	nF	5-V rating, X7R or NP0 cap.

Digital Peripherals

Timer Counter Pulse-Width Modulator (TCPWM)

Table 13. TCPWM Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.TCPWM.1	ITCPWM1	Block current consumption at 3 MHz	–	–	45	μA	All modes (TCPWM)
SID.TCPWM.2	ITCPWM2	Block current consumption at 8 MHz	–	–	145	μA	All modes (TCPWM)
SID.TCPWM.2A	ITCPWM3	Block current consumption at 16 MHz	–	–	160	μA	All modes (TCPWM)
SID.TCPWM.3	TCPWM _{FREQ}	Operating frequency	–	–	F _c	MHz	F _c max = CLK_SYS. Maximum = 16 MHz
SID.TCPWM.4	TPWM _{ENEXT}	Input trigger pulse width	2/F _c	–	–	ns	For all trigger events ^[9]
SID.TCPWM.5	TPWM _{EXT}	Output trigger pulse widths	2/F _c	–	–	ns	Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) outputs
SID.TCPWM.5A	TC _{RES}	Resolution of counter	1/F _c	–	–	ns	Minimum time between successive counts
SID.TCPWM.5B	PWM _{RES}	PWM resolution	1/F _c	–	–	ns	Minimum pulse width of PWM Output
SID.TCPWM.5C	Q _{RES}	Quadrature inputs resolution	1/F _c	–	–	ns	Minimum pulse width between Quadrature phase inputs.

²C

Table 14. Fixed I²C DC Specifications^[10]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID149	I _{I2C1}	Block current consumption at 100 kHz	–	–	25	μA	
SID150	I _{I2C2}	Block current consumption at 400 kHz	–	–	135	μA	
SID.PWR#5	ISBI2C	I ² C enabled in Deep Sleep mode	–	–	2.5	μA	

Table 15. Fixed I²C AC Specifications^[10]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID153	F _{I2C1}	Bit rate	–	–	400	Kbps	

Note

9. Trigger events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected.

10. Guaranteed by characterization.

Memory

Table 16. Flash DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID173	V _{PE}	Erase and program voltage	1.71	–	5.5	V	

Table 17. Flash AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID174	T _{ROWWRITE} ^[11]	Row (block) write time (erase and program)	–	–	20	ms	Row (block) = 64 bytes
SID175	T _{ROWERASE} ^[11]	Row erase time	–	–	13	ms	
SID176	T _{ROWPROGRAM} ^[11]	Row program time after erase	–	–	7	ms	
SID178	T _{BULKERASE} ^[11]	Bulk erase time (16 KB)	–	–	15	ms	
SID180 ^[12]	T _{DEVPROG} ^[11]	Total device program time	–	–	7.5	seconds	
SID181 ^[12]	F _{END}	Flash endurance	100 K	–	–	cycles	
SID182 ^[12]	F _{RET}	Flash retention. T _A ≤ 55 °C, 100 K P/E cycles	20	–	–	years	
SID182A ^[12]		Flash retention. T _A ≤ 85 °C, 10 K P/E cycles	10	–	–	years	

System Resources

Power-on Reset (POR)

Table 18. Power On Reset (PRES)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.CLK#6	SR_POWER_UP	Power supply slew rate	1	–	67	V/ms	At power-up
SID185 ^[12]	V _{RISEIPOR}	Rising trip voltage	0.80	–	1.5	V	
SID186 ^[12]	V _{FALLIPOR}	Falling trip voltage	0.70	–	1.4	V	

Table 19. Brown-out Detect (BOD) for V_{CCD}

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID190 ^[12]	V _{FALLPPOR}	BOD trip voltage in active and sleep modes	1.48	–	1.62	V	
SID192 ^[12]	V _{FALLDPSLP}	BOD trip voltage in Deep Sleep	1.11	–	1.5	V	

Notes

11. It can take as much as 20 milliseconds to write to Flash. During this time the device should not be Reset, or Flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.

12. Guaranteed by characterization.

SWD Interface

Table 20. SWD Interface Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID213	F_SWDCCLK1	$3.3\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	–	–	14	MHz	SWDCCLK \leq 1/3 CPU clock frequency
SID214	F_SWDCCLK2	$1.71\text{ V} \leq V_{DD} \leq 3.3\text{ V}$	–	–	7	MHz	SWDCCLK \leq 1/3 CPU clock frequency
SID215 ^[13]	T_SWDI_SETUP	$T = 1/f\text{ SWDCCLK}$	$0.25 \cdot T$	–	–	ns	
SID216 ^[13]	T_SWDI_HOLD	$T = 1/f\text{ SWDCCLK}$	$0.25 \cdot T$	–	–	ns	
SID217 ^[13]	T_SWDO_VALID	$T = 1/f\text{ SWDCCLK}$	–	–	$0.5 \cdot T$	ns	
SID217A ^[13]	T_SWDO_HOLD	$T = 1/f\text{ SWDCCLK}$	1	–	–	ns	

Internal Main Oscillator

Table 21. IMO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID218	I _{IMO1}	IMO operating current at 48 MHz	–	–	250	μA	
SID219	I _{IMO2}	IMO operating current at 24 MHz	–	–	180	μA	

Table 22. IMO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID223	F _{IMOTOL1}	Frequency variation at 24 and 32 MHz (trimmed)	–	–	±2	%	$2\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, and $-25\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$
SID223A	F _{IMOTOLVCCD}	Frequency variation at 24 and 32 MHz (trimmed)	–	–	±4	%	All other conditions
SID226	T _{STARTIMO}	IMO startup time	–	–	7	μs	
SID228	T _{JITRMSIMO2}	RMS jitter at 24 MHz	–	145	–	ps	

Internal Low-Speed Oscillator

Table 23. ILO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID231 ^[13]	I _{ILO1}	ILO operating current	–	0.3	1.05	μA	
SID233 ^[13]	I _{ILOLEAK}	ILO leakage current	–	2	15	nA	

Table 24. ILO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID234 ^[13]	T _{STARTILO1}	ILO startup time	–	–	2	ms	
SID236 ^[13]	T _{ILODUTY}	ILO duty cycle	40	50	60	%	
SID237	F _{ILOTRIM1}	ILO frequency range	20	40	80	kHz	

Note

13. Guaranteed by characterization.

Table 25. External Clock Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID305 ^[14]	ExtClkFreq	External clock input frequency	0	–	16	MHz	
SID306 ^[14]	ExtClkDuty	Duty cycle; measured at $V_{DD}/2$	45	–	55	%	

Table 26. Block Specs

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID262 ^[14]	T _{CLKSWITCH}	System clock source switching time	3	–	4	Periods	

Note

14. Guaranteed by characterization.



The PSoC 4000 part numbers and features are listed in the following table. All package types are available in Tape and Reel.

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Package Outline Drawings

Figure 11. 28-Pin SSOP Package Outline

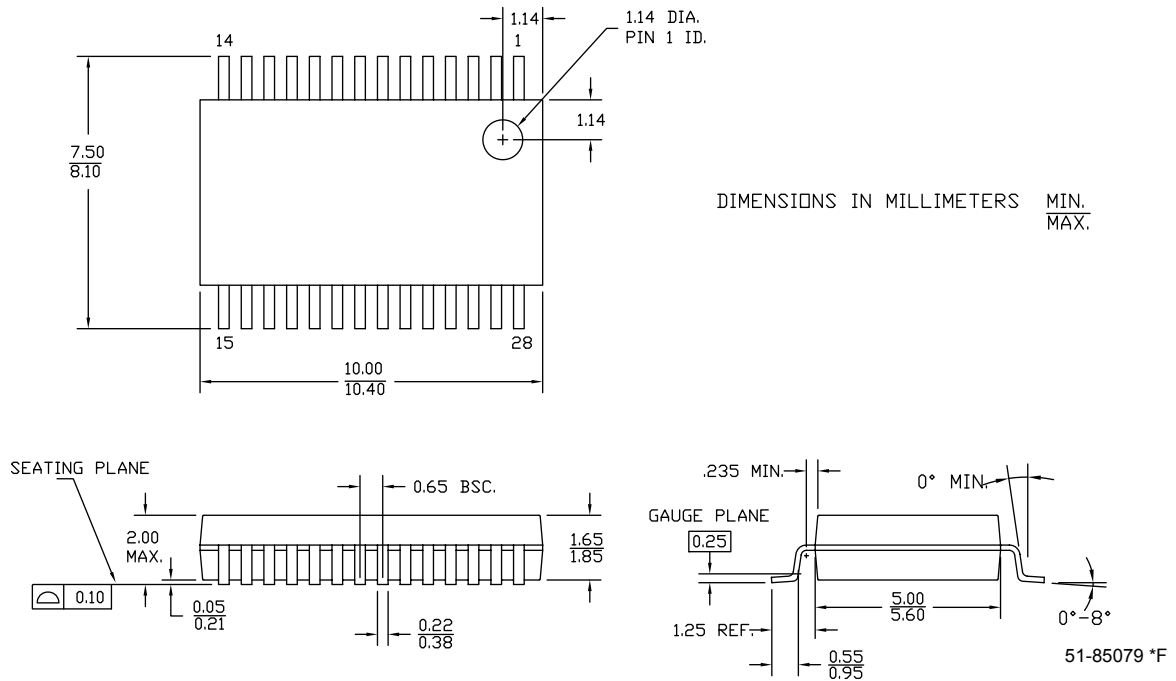
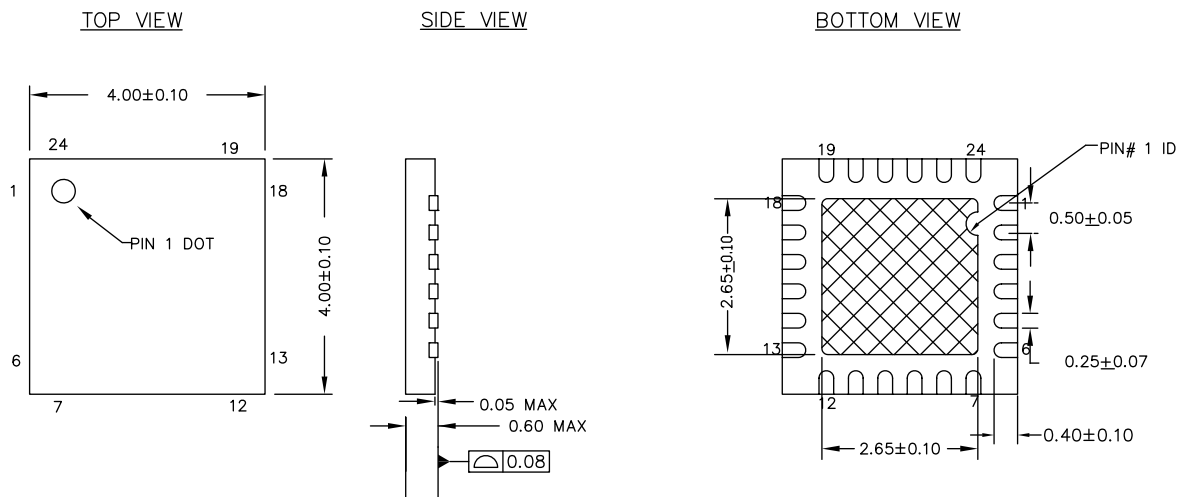



Figure 12. 24-pin QFN EPAD (Sawn) Package Outline



NOTES :

1.  HATCH IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC # MO-248
3. PACKAGE WEIGHT : 29 ± 3 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

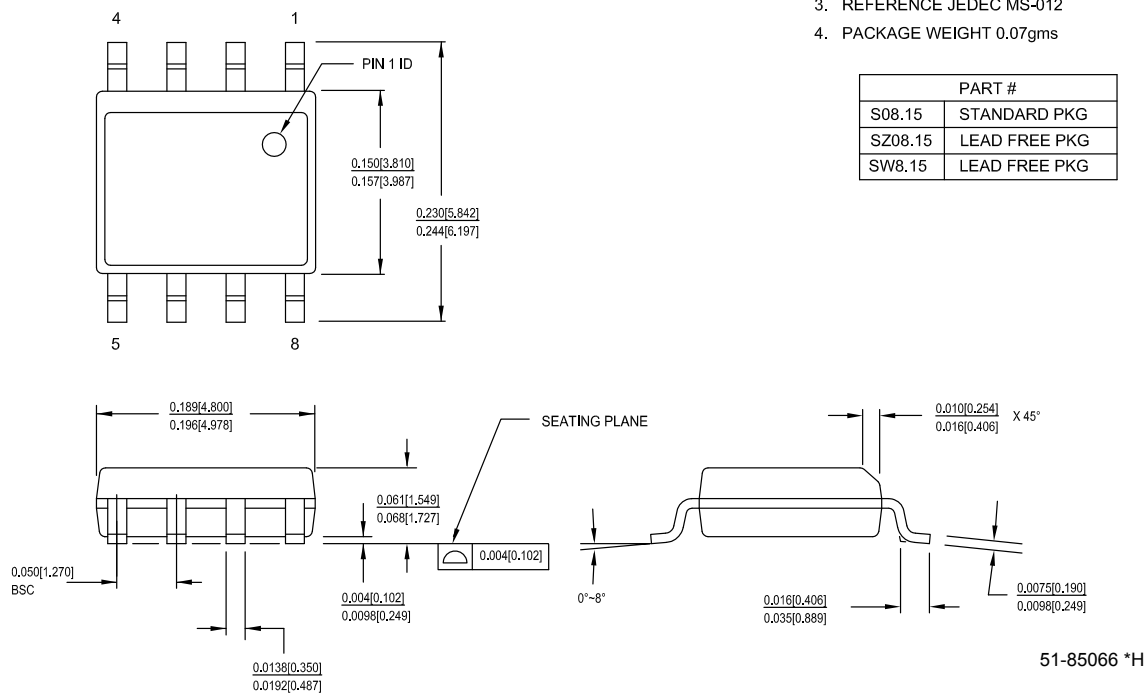
001-13937 *F

Note

15. Dimensions of the QFN package drawings are in millimeters.

Figure 15. 8-pin (150-mil) SOIC Package Outline

1. DIMENSIONS IN INCHES[MM] MIN.
MAX.
2. PIN 1 ID IS OPTIONAL.
ROUND ON SINGLE LEADFRAME
RECTANGULAR ON MATRIX LEADFRAME
3. REFERENCE JEDEC MS-012
4. PACKAGE WEIGHT 0.07gms



Acronyms

Table 31. Acronyms Used in this Document

Acronym	Description
abus	analog local bus
ADC	analog-to-digital converter
AG	analog global
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an ARM data transfer bus
ALU	arithmetic logic unit
AMUXBUS	analog multiplexer bus
API	application programming interface
APSR	application program status register
ARM®	advanced RISC machine, a CPU architecture
ATM	automatic thump mode
BW	bandwidth
CAN	Controller Area Network, a communications protocol
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
DAC	digital-to-analog converter, see also IDAC, VDAC
DFB	digital filter block
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DMIPS	Dhrystone million instructions per second
DMA	direct memory access, see also TD
DNL	differential nonlinearity, see also INL
DNU	do not use
DR	port write data registers
DSI	digital system interconnect
DWT	data watchpoint and trace
ECC	error correcting code
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
EMIF	external memory interface
EOC	end of conversion
EOF	end of frame
EPSR	execution program status register
ESD	electrostatic discharge

Table 31. Acronyms Used in this Document *(continued)*

Acronym	Description
ETM	embedded trace macrocell
FIR	finite impulse response, see also IIR
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output, applies to a PSoC pin
HVI	high-voltage interrupt, see also LVI, LVD
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
I ² C, or IIC	Inter-Integrated Circuit, a communications protocol
IIR	infinite impulse response, see also FIR
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
I/O	input/output, see also GPIO, DIO, SIO, USBIO
IPOR	initial power-on reset
IPSR	interrupt program status register
IRQ	interrupt request
ITM	instrumentation trace macrocell
LCD	liquid crystal display
LIN	Local Interconnect Network, a communications protocol.
LR	link register
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVI	low-voltage interrupt, see also HVI
LVTTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit
MISO	master-in slave-out
NC	no connect
NMI	nonmaskable interrupt
NRZ	non-return-to-zero
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL
opamp	operational amplifier
PAL	programmable array logic, see also PLD

Document Conventions

Units of Measure

Table 32. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
dB	decibel
fF	femto farad
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohour
kHz	kilohertz
kΩ	kilo ohm
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
μA	microampere
μF	microfarad
μH	microhenry
μs	microsecond
μV	microvolt
μW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
sqrtHz	square root of hertz
V	volt

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