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#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	16MHz
Connectivity	I <sup>2</sup> C
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	12
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	D/A 1x7b, 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-XFBGA, WLCSP
Supplier Device Package	16-WLCSP (1.45x1.56)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4014fni-421at

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



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Figure 2. Block Diagram

PSoC 4000 devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware.

The ARM Serial-Wire Debug (SWD) interface supports all programming and debug features of the device.

Complete debug-on-chip functionality enables full-device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC Creator IDE provides fully integrated programming and debug support for the PSoC 4000 devices. The SWD interface is fully compatible with industry-standard third-party tools. The PSoC 4000 family provides a level of security not possible with multi-chip application solutions or with microcontrollers. It has the following advantages:

- Allows disabling of debug features
- Robust flash protection
- Allows customer-proprietary functionality to be implemented in on-chip programmable blocks

The debug circuits are enabled by default and can only be disabled in firmware. If they are not enabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables debugging.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. All programming, debug, and test interfaces are disabled when maximum device security is enabled. Therefore, PSoC 4000, with device security enabled, may not be returned for failure analysis. This is a trade-off the PSoC 4000 allows the customer to make.



# **Functional Definition**

#### **CPU and Memory Subsystem**

#### CPU

The Cortex-M0 CPU in the PSoC 4000 is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. Most instructions are 16 bits in length and the CPU executes a subset of the Thumb-2 instruction set. This enables fully compatible, binary, upward migration of the code to higher performance processors, such as the Cortex-M3 and M4. It includes a nested vectored interrupt controller (NVIC) block with eight interrupt inputs and also includes a Wakeup Interrupt Controller (WIC). The WIC can wake the processor from the Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in the Deep Sleep mode. The CPU subsystem also includes a 24-bit timer called SYSTICK, which can generate an interrupt.

The CPU also includes a debug interface, the serial wire debug (SWD) interface, which is a 2-wire form of JTAG. The debug configuration used for PSoC 4000 has four breakpoint (address) comparators and two watchpoint (data) comparators.

#### Flash

The PSoC 4000 device has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The low-power flash block is designed to deliver zero wait-state (WS) access time at 16 MHz.

SRAM

Two KB of SRAM are provided with zero wait-state access at 16 MHz.

#### SROM

A supervisory ROM that contains boot and configuration routines is provided.

#### System Resources

#### Power System

The power system is described in detail in the section on Power on page 12. It provides an assurance that voltage levels are as required for each respective mode and either delays mode entry (for example, on power-on reset (POR)) until voltage levels are as required for proper functionality, or generates resets (for example, on brown-out detection). The PSoC 4000 operates with a single external supply over the range of either 1.8 V  $\pm$ 5% (externally regulated) or 1.8 to 5.5 V (internally regulated) and has three different power modes, transitions between which are managed by the power system. The PSoC 4000 provides Active, Sleep, and Deep Sleep low-power modes.

All subsystems are operational in Active mode. The CPU subsystem (CPU, flash, and SRAM) is clock-gated off in Sleep mode, while all peripherals and interrupts are active with instantaneous wake-up on a wake-up event. In Deep Sleep mode, the high-speed clock and associated circuitry is switched off; wake-up from this mode takes 35  $\mu$ S.

#### Clock System

The PSoC 4000 clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that there are no metastable conditions.

The clock system for the PSoC 4000 consists of the internal main oscillator (IMO) and the internal low-frequency oscillator (ILO) and provision for an external clock.

#### Figure 3. PSoC 4000 MCU Clocking Architecture



The  $F_{CPU}$  signal can be divided down to generate synchronous clocks for the analog and digital peripherals. There are four clock dividers for the PSoC 4000, each with 16-bit divide capability The 16-bit capability allows flexible generation of fine-grained frequency values and is fully supported in PSoC Creator.

#### IMO Clock Source

The IMO is the primary source of internal clocking in the PSoC 4000. It is trimmed during testing to achieve the specified accuracy. The IMO default frequency is 24 MHz and it can be adjusted from 24 to 48 MHz in steps of 4 MHz. The IMO tolerance with Cypress-provided calibration settings is  $\pm 2\%$  (24 and 32 MHz).

#### ILO Clock Source

The ILO is a very low power, 40-kHz oscillator, which is primarily used to generate clocks for the watchdog timer (WDT) and peripheral operation in Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy.

#### Watchdog Timer

A watchdog timer is implemented in the clock block running from the ILO; this allows watchdog operation during Deep Sleep and generates a watchdog reset if not serviced before the set timeout occurs. The watchdog reset is recorded in a Reset Cause register, which is firmware readable.

#### Reset

The PSoC 4000 can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through reset and allows software to determine the cause of the reset. An XRES pin is reserved for external reset on the 24-pin package. An internal POR is provided on the 16-pin and 8-pin packages. The XRES pin has an internal pull-up resistor that is always enabled. Reset is Active Low.

#### Voltage Reference

The PSoC 4000 reference system generates all internally required references. A 1.2-V voltage reference is provided for the comparator. The IDACs are based on a  $\pm 5\%$  reference.



Table 1.	Pin	Descriptions	(continued)
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	28-Pin SSOP		24-Pin QFN		16-Pin QFN		16-Pin SOIC	8-Pin SOIC			
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	TCPWM Signals	Alternate Functions
11	VSS										
12	No Connect (NC) <sup>[2]</sup>										
13	P1.7/MATCH/EXT_ CLK	19	P1.7/MATCH/EXT_ CLK	13	P1.7/MATCH/EXT_ CLK	15	P1.7/MATCH/EXT_ CLK			MATCH: Match Out	External Clock
14	P2.0	20	P2.0			16	P2.0				
15	VSS										
16	P3.0/SDA/SWD_IO	21	P3.0/SDA/SWD_IO	14	P3.0/SDA/SWD_IO	1	P3.0/SDA/SWD_IO	8	P3.0/SDA/SWD_IO		I2C Data, SWD I/O
17	P3.1/SCL/SWD_CL K	22	P3.1/SCL/SWD_CL K	15	P3.1/SCL/SWD_CL K	2	P3.1/SCL/SWD_CL K	1	P3.1/SCL/SWD_CL K		I2C Clock, SWD Clock
18	P3.2	23	P3.2	16	P3.2					OUT0:PWM OUT 0	
19	XRES	24	XRES								XRES: External Reset

#### Descriptions of the Pin functions are as follows:

**VDD**: Power supply for both analog and digital sections.

VDDIO: Where available, this pin provides a separate voltage domain (see the Power section for details).

VSS: Ground pin.

VCCD: Regulated digital supply (1.8 V ±5%).

Pins belonging to Ports 0, 1, and 2 can all be used as CSD sense or shield pins connected to AMUXBUS A or B. They can also be used as GPIO pins that can be driven by the firmware, in addition to their alternate functions listed in the Table 1.

Pins on Port 3 can be used as GPIO, in addition to their alternate functions listed above.

The following packages are provided: 28-pin SSOP, 24-pin QFN, 16-pin QFN, 16-pin SOIC, and 8-pin SOIC.

2. This pin is not to be used; it must be left floating.



#### Figure 4. 28-Pin SSOP Pinout







#### Figure 6. 16-Pin QFN Pinout





Figure 7. 16-Pin SOIC Pinout









Pin	Name	TCPWM Signal	Alternate Functions	Pin Diagram
B4	P3.2	OUT0:PWMOUT0	-	Bottom View
C3	P0.2/TRIN2	TRIN2:Trigger Input 2	-	4 3 2 1
C4	P0.4/TRIN4/CMPO_0/ EXT_CLK	TRIN4: Trigger Input 4	CMPO_0: Sense Comp Out, Ext. Clock, CMOD Cap	A
D4	VCCD	-	-	
D3	VDD	-	-	
D2	VSS	-	-	
C2	VDDIO	-	-	
D1	P0.6	-	-	
C1	P1.1/OUT0	OUT0:PWMOUT0	-	
B1	P1.2/SCL	-	I <sup>2</sup> C Clock	
A1	P1.3/SDA	-	l <sup>2</sup> C Data	1 2 3 4
A2	P1.6/OVF0/UND0/nO UT0/CMPO_0	nOUT0:Complement of OUT0, UND0, OVF0	CMPO_0: Sense Comp Out, Internal Reset function <sup>[3]</sup>	
B2	P1.7/MATCH/ EXT_CLK	MATCH: Match Out	External Clock	c
A3	P2.0	_	-	
B3	P3.0/SDA/SWD_IO	-	I <sup>2</sup> C Data, SWD I/O	D
A4	P3.1/SCL/SWD_CLK	_	I <sup>2</sup> C Clock, SWD Clock	

#### Table 2. 16-ball WLCSP Pin Descriptions and Diagram



### Power

The following power system diagrams (Figure 9 and Figure 10) show the set of power supply pins as implemented for the PSoC 4000. The system has one regulator in Active mode for the digital circuitry. There is no analog regulator; the analog circuits run directly from the  $V_{DD}$  input. There is a separate regulator for the Deep Sleep mode. The supply voltage range is either 1.8 V ±5% (externally regulated) or 1.8 V to 5.5 V (unregulated externally; regulated internally) with all functions and circuits operating over that range.

The V<sub>DDIO</sub> pin, available in the 16-pin QFN package, provides a separate voltage domain for the following pins: P3.0, P3.1, and P3.2. P3.0 and P3.1 can be I<sup>2</sup>C pins and the chip can thus communicate with an I<sup>2</sup>C system, running at a different voltage (where V<sub>DDIO</sub>  $\leq$  V<sub>DD</sub>). For example, V<sub>DD</sub> can be 3.3 V and V<sub>DDIO</sub> can be 1.8 V.

The PSoC 4000 family allows two distinct modes of power supply operation: Unregulated External Supply and Regulated External Supply.

#### **Unregulated External Supply**

In this mode, the PSoC 4000 is powered by an external power supply that can be anywhere in the range of 1.8 to 5.5 V. This range is also designed for battery-powered operation. For example, the chip can be powered from a battery system that starts at 3.5 V and works down to 1.8 V. In this mode, the internal regulator of the PSoC 4000 supplies the internal logic and the V<sub>CCD</sub> output of the PSoC 4000 must be bypassed to ground via an external capacitor (0.1  $\mu$ F; X5R ceramic or better).

Bypass capacitors must be used from V<sub>DD</sub> to ground. The typical practice for systems in this frequency range is to use a capacitor in the 1-µF range, in parallel with a smaller capacitor (0.1 µF, for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

An example of a bypass scheme follows (V\_{DDIO} is available on the 16-QFN package).

# Figure 9. 16-pin QFN Bypass Scheme Example - Unregulated External Supply

Power supply connections when  $1.8 \leq V_{\text{DD}} \leq ~5.5\,\text{V}$ 



#### **Regulated External Supply**

In this mode, the PSoC 4000 is powered by an external power supply that must be within the range of 1.71 to 1.89 V; note that this range needs to include the power supply ripple too. In this mode, the  $V_{DD}$  and  $V_{CCD}$  pins are shorted together and bypassed. The internal regulator should be disabled in the firmware. Note that in this mode VDD (VCCD) should never exceed 1.89 in any condition, including flash programming.

An example of a bypass scheme follows ( $V_{\mbox{\scriptsize DDIO}}$  is available on the 16-QFN package).

# Figure 10. 16-pin QFN Bypass Scheme Example - Regulated External Supply

Power supply connections when  $1.71 \leq V_{\text{DD}} \leq 1.89 \; V$ 





## **Electrical Specifications**

#### **Absolute Maximum Ratings**

#### Table 3. Absolute Maximum Ratings<sup>[4]</sup>

Spec ID#	Parameter	Description	Min	Тур	Max	Units	Details/ Conditions
SID1	V <sub>DD_ABS</sub>	Digital supply relative to V <sub>SS</sub>	-0.5	-	6	V	
SID2	V <sub>CCD_ABS</sub>	Direct digital core voltage input relative to $V_{SS}$	-0.5	-	1.95	V	
SID3	V <sub>GPIO_ABS</sub>	GPIO voltage	-0.5	_	V <sub>DD</sub> +0.5	V	
SID4	I <sub>GPIO_ABS</sub>	Maximum current per GPIO	-25	-	25	mA	
SID5	I <sub>GPIO_injection</sub>	GPIO injection current, Max for V <sub>IH</sub> > V <sub>DD</sub> , and Min for V <sub>IL</sub> < V <sub>SS</sub>	-0.5	-	0.5	mA	Current injected per pin
BID44	ESD_HBM	Electrostatic discharge human body model	2200	-	_	V	
BID45	ESD_CDM	Electrostatic discharge charged device model	500	-	-	V	
BID46	LU	Pin current for latch-up	-140	_	140	mA	

#### **Device Level Specifications**

All specifications are valid for –40 °C  $\leq$  T<sub>A</sub>  $\leq$  85 °C and T<sub>J</sub>  $\leq$  100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

#### Table 4. DC Specifications

Typical values measured at V<sub>DD</sub> = 3.3 V and 25 °C.

Spec ID#	Parameter	Description	Min	Тур	Мах	Units	Details/ Conditions	
SID53	V <sub>DD</sub>	Power supply input voltage	1.8	-	5.5	V	With regulator enabled	
SID255	V <sub>DD</sub>	Power supply input voltage ( $V_{CCD}$ = $V_{DD}$ )	1.71	-	1.89	V	Internally unreg- ulated supply	
SID54	V <sub>DDIO</sub>	V <sub>DDIO</sub> domain supply	1.71	-	V <sub>DD</sub>	V		
SID55	C <sub>EFC</sub>	External regulator voltage bypass	-	0.1	-	μF	X5R ceramic or better	
SID56	C <sub>EXC</sub>	Power supply bypass capacitor	-	1	-	μF	X5R ceramic or better	
Active Mode,	V <sub>DD</sub> = 1.8 to 5.5	V						
SID9	I <sub>DD5</sub>	Execute from flash; CPU at 6 MHz	-	2.0	2.85	mA		
SID12	I <sub>DD8</sub>	Execute from flash; CPU at 12 MHz	-	3.2	3.75	mA		
SID16	I <sub>DD11</sub>	Execute from flash; CPU at 16 MHz	-	4.0	4.5	mA		
Sleep Mode, V	/ <sub>DD</sub> = 1.71 to 5.5	V						
SID25	I <sub>DD20</sub>	I <sup>2</sup> C wakeup, WDT on. 6 MHz	-	1.1	-	mA		
SID25A	I <sub>DD20A</sub>	I <sup>2</sup> C wakeup, WDT on. 12 MHz	-	1.4	-	mA		
Deep Sleep Mode, V <sub>DD</sub> = 1.8 to 3.6 V (Regulator on)								
SID31	I <sub>DD26</sub>	I <sup>2</sup> C wakeup and WDT on	-	2.5	8.2	μA		

#### Note

<sup>4.</sup> Usage above the absolute maximum conditions listed in Table 1 may cause permanent damage to the device. Exposure to Absolute Maximum conditions for extended periods of time may affect device reliability. The Maximum Storage Temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below Absolute Maximum conditions but above normal operating conditions, the device may not operate to specification.



#### Table 4. DC Specifications (continued)

Typical values measured at V\_DD = 3.3 V and 25  $^\circ\text{C}.$ 

Spec ID#	Parameter	Description	Min	Тур	Max	Units	Details/ Conditions				
Deep Sleep M	Deep Sleep Mode, V <sub>DD</sub> = 3.6 to 5.5 V (Regulator on)										
SID34	I <sub>DD29</sub>	I <sup>2</sup> C wakeup and WDT on	-	2.5	12	μA					
Deep Sleep M	Deep Sleep Mode, V <sub>DD</sub> = V <sub>CCD</sub> = 1.71 to 1.89 V (Regulator bypassed)										
SID37	I <sub>DD32</sub>	I <sup>2</sup> C wakeup and WDT on	-	2.5	9.2	μA					
XRES Current											
SID307	I <sub>DD_XR</sub>	Supply current while XRES asserted	_	2	5	mA					

#### Table 5. AC Specifications

Spec ID#	Parameter	Description	Min	Тур	Max	Units	Details/ Conditions
SID48	F <sub>CPU</sub>	CPU frequency	DC	Ι	16	MHz	$1.71 \leq V_{DD} \leq 5.5$
SID49 <sup>[5]</sup>	T <sub>SLEEP</sub>	Wakeup from Sleep mode	-	0	_	μs	
SID50 <sup>[5]</sup>	T <sub>DEEPSLEEP</sub>	Wakeup from Deep Sleep mode	-	35	_	μs	

GPIO

#### Table 6. GPIO DC Specifications (referenced to $V_{DDIO}$ for 16-Pin QFN $V_{DDIO}$ pins)

Spec ID#	Parameter	Description	Min	Тур	Max	Units	Details/ Conditions
SID57	V <sub>IH</sub> <sup>[6]</sup>	Input voltage high threshold	$0.7 \times V_{DD}$	-	-	V	CMOS Input
SID58	V <sub>IL</sub>	Input voltage low threshold	-	-	$0.3 \times V_{DD}$	V	CMOS Input
SID241	V <sub>IH</sub> <sup>[6]</sup>	LVTTL input, V <sub>DD</sub> < 2.7 V	$0.7 \times V_{DD}$	-	-	V	
SID242	V <sub>IL</sub>	LVTTL input, V <sub>DD</sub> < 2.7 V	-	-	$0.3 \times V_{DD}$	V	
SID243	V <sub>IH</sub> <sup>[6]</sup>	LVTTL input, $V_{DD} \ge 2.7 V$	2.0	-	-	V	
SID244	V <sub>IL</sub>	LVTTL input, $V_{DD} \ge 2.7 V$	-	-	0.8	V	
SID59	V <sub>OH</sub>	Output voltage high level	V <sub>DD</sub> –0.6	_	-	V	I <sub>OH</sub> = 4 mA at 3 V V <sub>DD</sub>
SID60	V <sub>OH</sub>	Output voltage high level	V <sub>DD</sub> –0.5	l	-	V	I <sub>OH</sub> = 1 mA at 1.8 V V <sub>DD</sub>
SID61	V <sub>OL</sub>	Output voltage low level	_	-	0.6	V	I <sub>OL</sub> = 4 mA at 1.8 V V <sub>DD</sub>
SID62	V <sub>OL</sub>	Output voltage low level	_	Ι	0.6	V	I <sub>OL</sub> = 10 mA at 3 V V <sub>DD</sub>
SID62A	V <sub>OL</sub>	Output voltage low level	-	-	0.4	V	I <sub>OL</sub> = 3 mA at 3 V V <sub>DD</sub>
SID63	R <sub>PULLUP</sub>	Pull-up resistor	3.5	5.6	8.5	kΩ	
SID64	R <sub>PULLDOWN</sub>	Pull-down resistor	3.5	5.6	8.5	kΩ	
SID65	IIL	Input leakage current (absolute value)	-	-	2	nA	25 °C, V <sub>DD</sub> = 3.0 V
SID66	C <sub>IN</sub>	Input capacitance	-	3	7	pF	

#### Notes

Guaranteed by characterization.
 V<sub>IH</sub> must not exceed V<sub>DD</sub> + 0.2 V.





Spec ID#	Parameter	Description	Min	Тур	Max	Units	Details/ Conditions
SID67 <sup>[7]</sup>	V <sub>HYSTTL</sub>	Input hysteresis LVTTL	15	40	-	mV	$V_{DD} \geq 2.7 \ V$
SID68 <sup>[7]</sup>	V <sub>HYSCMOS</sub>	Input hysteresis CMOS	0.05 × V <sub>DD</sub>	Ι	_	mV	V <sub>DD</sub> < 4.5 V
SID68A <sup>[7]</sup>	V <sub>HYSCMOS5V5</sub>	Input hysteresis CMOS	200	-	_	mV	V <sub>DD</sub> > 4.5 V
SID69 <sup>[7]</sup>	IDIODE	Current through protection diode to $V_{DD}/V_{SS}$	-	-	100	μA	
SID69A <sup>[7]</sup>	I <sub>TOT_GPIO</sub>	Maximum total source or sink chip current	-	-	85	mA	

#### Table 6. GPIO DC Specifications (referenced to $V_{DDIO}$ for 16-Pin QFN $V_{DDIO}$ pins) (continued)

#### Table 7. GPIO AC Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Тур	Мах	Units	Details/ Conditions
SID70	T <sub>RISEF</sub>	Rise time in fast strong mode	2	-	12	ns	3.3 V V <sub>DD</sub> , Cload = 25 pF
SID71	T <sub>FALLF</sub>	Fall time in fast strong mode	2	-	12	ns	3.3 V V <sub>DD</sub> , Cload = 25 pF
SID72	T <sub>RISES</sub>	Rise time in slow strong mode	10	-	60	-	3.3 V V <sub>DD</sub> , Cload = 25 pF
SID73	T <sub>FALLS</sub>	Fall time in slow strong mode	10	-	60	-	3.3 V V <sub>DD</sub> , Cload = 25 pF
SID74	F <sub>GPIOUT1</sub>	GPIO $F_{OUT}$ ; 3.3 V $\leq$ V <sub>DD</sub> $\leq$ 5.5 V. Fast strong mode.	-	-	16	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID75	F <sub>GPIOUT2</sub>	GPIO $F_{OUT}$ ; 1.71 V $\leq V_{DD} \leq 3.3$ V. Fast strong mode.	-	-	16	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID76	F <sub>GPIOUT3</sub>	GPIO $F_{OUT}$ ; 3.3 V $\leq$ V <sub>DD</sub> $\leq$ 5.5 V. Slow strong mode.	-	-	7	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID245	F <sub>GPIOUT4</sub>	GPIO $F_{OUT}$ ; 1.71 V $\leq$ V <sub>DD</sub> $\leq$ 3.3 V. Slow strong mode.	-	-	3.5	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID246	F <sub>GPIOIN</sub>	GPIO input operating frequency; 1.71 V $\leq$ V <sub>DD</sub> $\leq$ 5.5 V	-	_	16	MHz	90/10% V <sub>IO</sub>



#### XRES

#### Table 8. XRES DC Specifications

Spec ID#	Parameter	Description	Min	Тур	Max	Units	Details/ Conditions
SID77	V <sub>IH</sub>	Input voltage high threshold	0.7 × V <sub>DD</sub>	-	-	V	CMOS Input
SID78	V <sub>IL</sub>	Input voltage low threshold	-	-	0.3 × V <sub>DD</sub>	V	CMOS Input
SID79	R <sub>PULLUP</sub>	Pull-up resistor	3.5	5.6	8.5	kΩ	
SID80	C <sub>IN</sub>	Input capacitance	-	3	7	pF	
SID81 <sup>[8]</sup>	V <sub>HYSXRES</sub>	Input voltage hysteresis	-	0.05* V <sub>DD</sub>	-	mV	Typical hysteresis is 200 mV for V <sub>DD</sub> > 4.5V

#### Table 9. XRES AC Specifications

Spec ID#	Parameter	Description	Min	Тур	Max	Units	Details/ Conditions
SID83 <sup>[8]</sup>	TRESETWIDTH	Reset pulse width	5	-	-	μs	
BID#194 <sup>[8]</sup>	TRESETWAKE	Wake-up time from reset release	-	-	3	ms	

#### Analog Peripherals

Comparator

#### Table 10. Comparator DC Specifications

Spec ID#	Parameter	Description	Min	Тур	Max	Units	Details/ Conditions
SID330 <sup>[8]</sup>	I <sub>CMP1</sub>	Block current, High Bandwidth mode	-	_	110	μA	
SID331 <sup>[8]</sup>	I <sub>CMP2</sub>	Block current, Low Power mode	-	-	85	μA	
SID332 <sup>[8]</sup>	V <sub>OFFSET1</sub>	Offset voltage, High Bandwidth mode	-	10	30	mV	
SID333 <sup>[8]</sup>	V <sub>OFFSET2</sub>	Offset voltage, Low Power mode	_	10	30	mV	
SID334 <sup>[8]</sup>	Z <sub>CMP</sub>	DC input impedance of comparator	35	-	-	MΩ	
SID338 <sup>[8]</sup>	VINP_COMP	Comparator input range	0	-	3.6	V	Max input voltage is lower of 3.6 V or V <sub>DD</sub>
SID339	VREF_COMP	Comparator internal voltage reference	1.188	1.2	1.212	V	



#### Memory

#### Table 16. Flash DC Specifications

Spec ID	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID173	V <sub>PE</sub>	Erase and program voltage	1.71	_	5.5	V	

#### Table 17. Flash AC Specifications

Spec ID	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID174	T <sub>ROWWRITE</sub> <sup>[11]</sup>	Row (block) write time (erase and program)	_	_	20	ms	Row (block) = 64 bytes
SID175	T <sub>ROWERASE</sub> <sup>[11]</sup>	Row erase time	-	_	13	ms	
SID176	T <sub>ROWPROGRAM</sub> <sup>[11]</sup>	Row program time after erase	-	-	7	ms	
SID178	T <sub>BULKERASE</sub> <sup>[11]</sup>	Bulk erase time (16 KB)	-	-	15	ms	
SID180 <sup>[12]</sup>	T <sub>DEVPROG</sub> <sup>[11]</sup>	Total device program time	-	-	7.5	seconds	
SID181 <sup>[12]</sup>	F <sub>END</sub>	Flash endurance	100 K	-	-	cycles	
SID182 <sup>[12]</sup>	F <sub>RET</sub>	Flash retention. $T_A \le 55 \degree$ C, 100 K P/E cycles	20	-	-	years	
SID182A <sup>[12]</sup>		Flash retention. $T_A \le 85 \text{ °C}$ , 10 K P/E cycles	10	-	_	years	

#### System Resources

Power-on Reset (POR)

#### Table 18. Power On Reset (PRES)

Spec ID	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID.CLK#6	SR_POWER_UP	Power supply slew rate	1	-	67	V/ms	At power-up
SID185 <sup>[12]</sup>	V <sub>RISEIPOR</sub>	Rising trip voltage	0.80	-	1.5	V	
SID186 <sup>[12]</sup>	V <sub>FALLIPOR</sub>	Falling trip voltage	0.70	_	1.4	V	

#### Table 19. Brown-out Detect (BOD) for V<sub>CCD</sub>

Spec ID	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID190 <sup>[12]</sup>	V <sub>FALLPPOR</sub>	BOD trip voltage in active and sleep modes	1.48	-	1.62	V	
SID192 <sup>[12]</sup>	V <sub>FALLDPSLP</sub>	BOD trip voltage in Deep Sleep	1.11	-	1.5	V	

Notes 11. It can take as much as 20 milliseconds to write to Flash. During this time the device should not be Reset, or Flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.



#### SWD Interface

#### Table 20. SWD Interface Specifications

Spec ID	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID213	F_SWDCLK1	$3.3~V \leq V_{DD} \leq 5.5~V$	-	-	14	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID214	F_SWDCLK2	$1.71~V \leq V_{DD} \leq 3.3~V$	-	-	7	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID215 <sup>[13]</sup>	T_SWDI_SETUP	T = 1/f SWDCLK	0.25*T	-	-	ns	
SID216 <sup>[13]</sup>	T_SWDI_HOLD	T = 1/f SWDCLK	0.25*T	-	-	ns	
SID217 <sup>[13]</sup>	T_SWDO_VALID	T = 1/f SWDCLK	1	-	0.5*T	ns	
SID217A <sup>[13]</sup>	T_SWDO_HOLD	T = 1/f SWDCLK	1	-	_	ns	

Internal Main Oscillator

#### Table 21. IMO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID218	I <sub>IMO1</sub>	IMO operating current at 48 MHz	-	-	250	μA	
SID219	I <sub>IMO2</sub>	IMO operating current at 24 MHz	-	-	180	μA	

#### Table 22. IMO AC Specifications

Spec ID	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID223	F <sub>IMOTOL1</sub>	Frequency variation at 24 and 32 MHz (trimmed)	-	-	±2	%	2 V $\leq$ V $_{DD}$ $\leq$ 5.5 V, and –25 $^\circ\text{C}$ $\leq$ T $_A$ $\leq$ 85 $^\circ\text{C}$
SID223A	FIMOTOLVCCD	Frequency variation at 24 and 32 MHz (trimmed)	-	-	±4	%	All other conditions
SID226	T <sub>STARTIMO</sub>	IMO startup time	-	-	7	μs	
SID228	T <sub>JITRMSIMO2</sub>	RMS jitter at 24 MHz	-	145	-	ps	

#### Internal Low-Speed Oscillator

#### Table 23. ILO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID231 <sup>[13]</sup>	I <sub>ILO1</sub>	ILO operating current	-	0.3	1.05	μA	
SID233 <sup>[13]</sup>	I <sub>ILOLEAK</sub>	ILO leakage current	-	2	15	nA	

#### Table 24. ILO AC Specifications

Spec ID	Parameter	Description	Min	Тур	Max	Units	<b>Details/Conditions</b>
SID234 <sup>[13]</sup>	T <sub>STARTILO1</sub>	ILO startup time	-	-	2	ms	
SID236 <sup>[13]</sup>	T <sub>ILODUTY</sub>	ILO duty cycle	40	50	60	%	
SID237	F <sub>ILOTRIM1</sub>	ILO frequency range	20	40	80	kHz	

Note 13. Guaranteed by characterization.



The Field Values are listed in the following table:

Field	Description	Values	Meaning
CY8C	Cypress prefix		
4	Architecture	4	PSoC 4
Α	Family	0	4000 Family
В	CPU speed	1	16 MHz
		4	48 MHz
С	Flash capacity	3	8 KB
		4	16 KB
		5	32 KB
		6	64 KB
		7	128 KB
DE	Package code	SX	SOIC
		LQ	QFN
		PV	SSOP
		FN	WLCSP
F	Temperature range	I	Industrial
XYZ	Attributes code	000-999	Code of feature set in specific family



# Packaging

#### Table 27. Package List

Spec ID#	Package	Description
BID#47A	28-Pin SSOP	28-pin 5 × 10 × 1.65mm SSOP with 0.65-mm pitch
BID#26	24-Pin QFN	24-pin 4 × 4 × 0.6 mm QFN with 0.5-mm pitch
BID#33	16-Pin QFN	16-pin 3 × 3 × 0.6 mm QFN with 0.5-mm pitch
BID#40	16-Pin SOIC	16-pin (150 Mil) SOIC
BID#47	8-Pin SOIC	8-pin (150 Mil) SOIC
BID#147A	16-Ball WLCSP	16-Ball 1.47 × 1.58 × 0.4 mm

#### Table 28. Package Characteristics

Parameter	Description	Conditions	Min	Тур	Max	Units
T <sub>A</sub>	Operating ambient temperature		-40	25	85	°C
TJ	Operating junction temperature		-40	-	100	°C
T <sub>JA</sub>	Package θ <sub>JA</sub> (28-pin SSOP)		-	66.6	-	°C/Watt
T <sub>JC</sub>	Package $\theta_{JC}$ (28-pin SSOP)		-	34	-	°C/Watt
T <sub>JA</sub>	Package θ <sub>JA</sub> (24-pin QFN)		-	38	-	°C/Watt
T <sub>JC</sub>	Package $\theta_{JC}$ (24-pin QFN)		-	5.6	-	°C/Watt
T <sub>JA</sub>	Package θ <sub>JA</sub> (16-pin QFN)		-	49.6	-	°C/Watt
T <sub>JC</sub>	Package θ <sub>JC</sub> (16-pin QFN)		-	5.9	-	°C/Watt
T <sub>JA</sub>	Package θ <sub>JA</sub> (16-pin SOIC)		-	142	-	°C/Watt
T <sub>JC</sub>	Package θ <sub>JC</sub> (16-pin SOIC)		-	49.8	-	°C/Watt
T <sub>JA</sub>	Package $\theta_{JA}$ (16-ball WLCSP)		-	90	-	°C/Watt
T <sub>JC</sub>	Package $\theta_{JC}$ (16-ball WLCSP)		-	0.9	-	°C/Watt
T <sub>JA</sub>	Package θ <sub>JA</sub> (8-pin SOIC)		-	198	-	°C/Watt
T <sub>JC</sub>	Package θ <sub>JC</sub> (8-pin SOIC)		-	56.9	-	°C/Watt

#### Table 29. Solder Reflow Peak Temperature

Package Maximum Peak Temperature		Maximum Time at Peak Temperature		
All	260 °C	30 seconds		

#### Table 30. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-020

Package	MSL
All except WLCSP	MSL 3
16-ball WLCSP	MSL1



#### Package Outline Drawings



#### Note

15. Dimensions of the QFN package drawings are in millimeters.



#### Figure 16. 16-Ball WLCSP 1.47 × 1.58 × 0.4 mm



0/4/001	DIMENSIONS				
SYMBOL	MIN.	NOM.	MAX.		
A	-	-	0.42		
A1	0.089	0.099	0.109		
D	1.447	1.472	1.497		
E	1.554	1.579	1.604		
D1	1.05 BSC				
E1	1.05 BSC				
MD	4				
ME	4				
N	16				
ØÞ	0.17	0.20	0.23		
eD	0.35 BSC				
eE	0.35 BSC				
SD	0.18 BSC				
SE	0.18 BSC				

#### NOTES:

- 1. ALL DIMENSIONS ARE IN MILLIMETERS.
- 2. SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
- 3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
- 4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION. N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
- AIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
- \*SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0.
  - WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
- A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
- 8. \*\*\* INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.
- 9. JEDEC SPECIFICATION NO. REF. : N/A.

002-18598 \*\*



# **Document Conventions**

#### Units of Measure

#### Table 32. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
dB	decibel
fF	femto farad
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohour
kHz	kilohertz
kΩ	kilo ohm
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
μA	microampere
μF	microfarad
μH	microhenry
μs	microsecond
μV	microvolt
μW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
S	second
sps	samples per second
sqrtHz	square root of hertz
V	volt



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