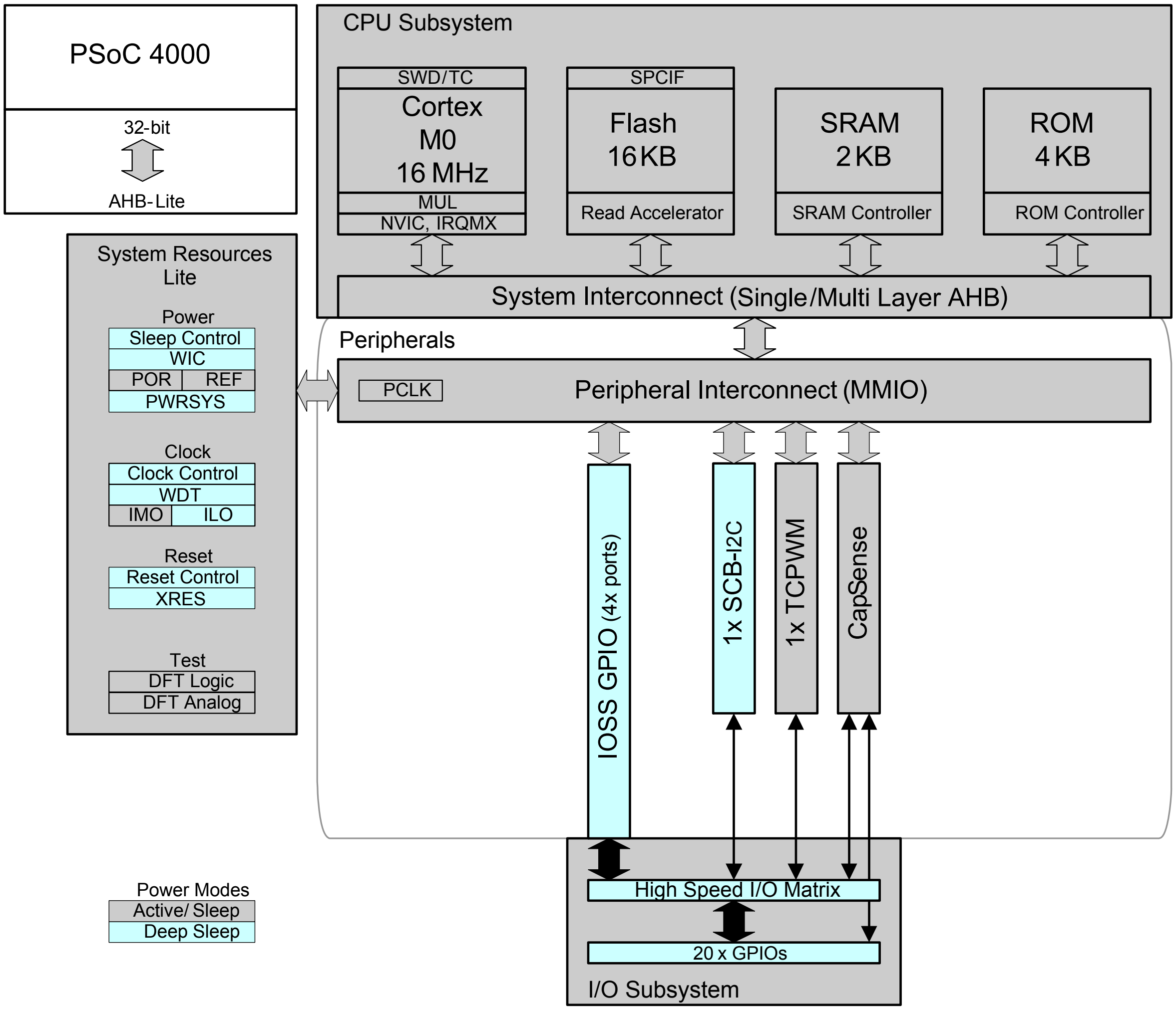
Infineon Technologies - CY8C4014SXI-420 Datasheet

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	16MHz
Connectivity	I²C
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	5
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	D/A 1x7b, 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.154", 3.90mm Width)
Supplier Device Package	8-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4014sxi-420

Contents

Figure 2. Block Diagram



PSoC 4000 devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware.

The ARM Serial-Wire Debug (SWD) interface supports all programming and debug features of the device.

Complete debug-on-chip functionality enables full-device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC Creator IDE provides fully integrated programming and debug support for the PSoC 4000 devices. The SWD interface is fully compatible with industry-standard third-party tools. The PSoC 4000 family provides a level of security not possible with multi-chip application solutions or with microcontrollers. It has the following advantages:

- Allows disabling of debug features
- Robust flash protection
- Allows customer-proprietary functionality to be implemented in on-chip programmable blocks

The debug circuits are enabled by default and can only be disabled in firmware. If they are not enabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables debugging.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. All programming, debug, and test interfaces are disabled when maximum device security is enabled. Therefore, PSoC 4000, with device security enabled, may not be returned for failure analysis. This is a trade-off the PSoC 4000 allows the customer to make.

Functional Definition

CPU and Memory Subsystem

CPU

The Cortex-M0 CPU in the PSoC 4000 is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. Most instructions are 16 bits in length and the CPU executes a subset of the Thumb-2 instruction set. This enables fully compatible, binary, upward migration of the code to higher performance processors, such as the Cortex-M3 and M4. It includes a nested vectored interrupt controller (NVIC) block with eight interrupt inputs and also includes a Wakeup Interrupt Controller (WIC). The WIC can wake the processor from the Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in the Deep Sleep mode. The CPU subsystem also includes a 24-bit timer called SYSTICK, which can generate an interrupt.

The CPU also includes a debug interface, the serial wire debug (SWD) interface, which is a 2-wire form of JTAG. The debug configuration used for PSoC 4000 has four breakpoint (address) comparators and two watchpoint (data) comparators.

Flash

The PSoC 4000 device has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The low-power flash block is designed to deliver zero wait-state (WS) access time at 16 MHz.

SRAM

Two KB of SRAM are provided with zero wait-state access at 16 MHz.

SROM

A supervisory ROM that contains boot and configuration routines is provided.

System Resources

Power System

The power system is described in detail in the section on Power on page 12. It provides an assurance that voltage levels are as required for each respective mode and either delays mode entry (for example, on power-on reset (POR)) until voltage levels are as required for proper functionality, or generates resets (for example, on brown-out detection). The PSoC 4000 operates with a single external supply over the range of either 1.8 V ±5% (externally regulated) or 1.8 to 5.5 V (internally regulated) and has three different power modes, transitions between which are managed by the power system. The PSoC 4000 provides Active, Sleep, and Deep Sleep low-power modes.

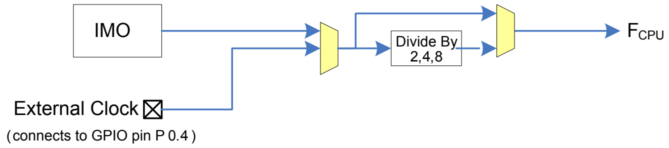
All subsystems are operational in Active mode. The CPU subsystem (CPU, flash, and SRAM) is clock-gated off in Sleep mode, while all peripherals and interrupts are active with instantaneous wake-up on a wake-up event. In Deep Sleep mode, the high-speed clock and associated circuitry is switched off; wake-up from this mode takes 35 µS.

Clock System

The PSoC 4000 clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that there are no metastable conditions.

The clock system for the PSoC 4000 consists of the internal main oscillator (IMO) and the internal low-frequency oscillator (ILO) and provision for an external clock.

Figure 3. PSoC 4000 MCU Clocking Architecture



The F_{CPU} signal can be divided down to generate synchronous clocks for the analog and digital peripherals. There are four clock dividers for the PSoC 4000, each with 16-bit divide capability The 16-bit capability allows flexible generation of fine-grained frequency values and is fully supported in PSoC Creator.

IMO Clock Source

The IMO is the primary source of internal clocking in the PSoC 4000. It is trimmed during testing to achieve the specified accuracy.The IMO default frequency is 24 MHz and it can be adjusted from 24 to 48 MHz in steps of 4 MHz. The IMO tolerance with Cypress-provided calibration settings is ±2% (24 and 32 MHz).

ILO Clock Source

The ILO is a very low power, 40-kHz oscillator, which is primarily used to generate clocks for the watchdog timer (WDT) and peripheral operation in Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy.

Watchdog Timer

A watchdog timer is implemented in the clock block running from the ILO; this allows watchdog operation during Deep Sleep and generates a watchdog reset if not serviced before the set timeout occurs. The watchdog reset is recorded in a Reset Cause register, which is firmware readable.

Reset

The PSoC 4000 can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through reset and allows software to determine the cause of the reset. An XRES pin is reserved for external reset on the 24-pin package. An internal POR is provided on the 16-pin and 8-pin packages. The XRES pin has an internal pull-up resistor that is always enabled. Reset is Active Low.

Voltage Reference

The PSoC 4000 reference system generates all internally required references. A 1.2-V voltage reference is provided for the comparator. The IDACs are based on a ±5% reference.

Analog Blocks

Low-power Comparators

The PSoC 4000 has a low-power comparator, which uses the built-in voltage reference. Any one of up to 16 pins can be used as a comparator input and the output of the comparator can be brought out to a pin. The selected comparator input is connected to the minus input of the comparator with the plus input always connected to the 1.2-V voltage reference. This comparator is also used for CapSense purposes and is not available during CapSense operation.

Current DACs

The PSoC 4000 has two IDACs, which can drive any of up to 16 pins on the chip. These IDACs have programmable current ranges.

Analog Multiplexed Buses

The PSoC 4000 has two concentric independent buses that go around the periphery of the chip. These buses (called amux buses) are connected to firmware-programmable analog switches that allow the chip's internal resources (IDACs, comparator) to connect to any pin on Ports 0, 1, and 2.

Fixed Function Digital

Timer/Counter/PWM (TCPWM) Block

The TCPWM block consists of a 16-bit counter with user-programmable period length. There is a capture register to record the count value at the time of an event (which may be an I/O event), a period register that is used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals that are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow use as dead-band programmable complementary PWM outputs. It also has a Kill input to force outputs to a predetermined state; for example, this is used in motor drive systems when an over-current state is indicated and the PWM driving the FETs needs to be shut off immediately with no time for software intervention.

Serial Communication Block (SCB)

The PSoC 4000 has a serial communication block, which implements a multi-master I^{2}C interface.

I^{2}C Mode: The hardware I^{2}C block implements a full multi-master and slave interface (it is capable of multi-master arbitration). This block is capable of operating at speeds of up to 400 kbps (Fast Mode) and has flexible buffering options to reduce interrupt overhead and latency for the CPU. It also supports EZI2C that creates a mailbox address range in the memory of the PSoC 4000 and effectively reduces I^{2}C communication to reading from and writing to an array in memory. In addition, the block supports an 8-deep FIFO for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduces the need for clock stretching caused by the CPU not having read data on time.

The I^{2}C peripheral is compatible with the I^{2}C Standard-mode and Fast-mode devices as defined in the NXP I^{2}C-bus specification and user manual (UM10204). The I^{2}C bus I/O is implemented with GPIO in open-drain modes.

The PSoC 4000 is not completely compliant with the I^{2}C spec in the following respect:

- GPIO cells are not overvoltage tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I^{2}C system.
- Fast-mode minimum fall time is not met in Fast Strong mode; Slow Strong mode can help meet this spec depending on the Bus Load.

GPIO

The PSoC 4000 has up to 20 GPIOs. The GPIO block implements the following:

- Eight drive modes:
  - Analog input mode (input and output buffers disabled)
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL).
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes
- Selectable slew rates for dV/dt related noise control to improve EMI

The pins are organized in logical entities called ports, which are 8-bit in width (less for Ports 2 and 3). During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin.

Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves.

Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it (4 for PSoC 4000).

The 28-pin and 24-pin packages have 20 GPIOs. The 16-pin SOIC has 13 GPIOs. The 16-pin QFN and the 16-ball WLCSP have 12 GPIOs. The 8-pin SOIC has 5 GPIOs.

Special Function Peripherals

CapSense

CapSense is supported in the PSoC 4000 through a CSD block that can be connected to up to 16 pins through an analog mux bus via an analog switch (pins on Port 3 are not available for CapSense purposes). CapSense function can thus be provided on any available pin or group of pins in a system under software control. A PSoC Creator component is provided for the CapSense block to make it easy for the user.

Shield voltage can be driven on another mux bus to provide water-tolerance capability. Water tolerance is provided by driving the shield electrode in phase with the sense electrode to keep the shield capacitance from attenuating the sensed input. Proximity sensing can also be implemented.

The CapSense block has two IDACs, which can be used for general purposes if CapSense is not being used (both IDACs are available in that case) or if CapSense is used without water tolerance (one IDAC is available).

Pinouts

All port pins support GPIO. Ports 0, 1, and 2 support CSD CapSense and analog multiplexed bus connections. TCPWM functions and Alternate Functions are multiplexed with port pins as follows for the five PSoC 4000 packages.

Table 1. Pin Descriptions

28-Pin SSOP		24-Pin QFN		16-Pin QFN		16-Pin SOIC		8-Pin SOIC			
Pin	**Name**	**Pin**	**Name**	**Pin**	**Name**	**Pin**	**Name**	**Pin**	**Name**	**TCPWM Signals**	**Alternate Functions**
20	VSS										
21	P0.0/TRIN0	1	P0.0/TRIN0							TRIN0: Trigger Input 0	
22	P0.1/TRIN1/CMPO_0	2	P0.1/TRIN1/CMPO_0	1	P0.1/TRIN1/CMPO_0	3	P0.1/TRIN1/CMPO_0			TRIN1: Trigger Input 1	CMPO_0: Sense Comp Out
23	P0.2/TRIN2	3	P0.2/TRIN2	2	P0.2/TRIN2	4	P0.2/TRIN2			TRIN2: Trigger Input 2	
24	P0.3/TRIN3	4	P0.3/TRIN3							TRIN3: Trigger Input 3	
25	P0.4/TRIN4/CMPO_0/EXT_CLK	5	P0.4/TRIN4/CMPO_0/EXT_CLK	3	P0.4/TRIN4/CMPO_0/EXT_CLK	5	P0.4/TRIN4/CMPO_0/EXT_CLK	2	P0.4/TRIN4/CMPO_0/EXT_CLK	TRIN4: Trigger Input 4	CMPO_0: Sense Comp Out, External Clock, CMOD Cap
26	VCC	6	VCC	4	VCC	6	VCC	3	VCC		
27	VDD	7	VDD	6	VDD	7	VDD	4	VDD		
28	VSS	8	VSS	7	VSS	8	VSS	5	VSS		
1	P0.5	9	P0.5	5	VDDIO	9	P0.5				
2	P0.6	10	P0.6	8	P0.6	10	P0.6				
3	P0.7	11	P0.7								
4	P1.0	12	P1.0								
5	P1.1/OUT0	13	P1.1/OUT0	9	P1.1/OUT0	11	P1.1/OUT0	6	P1.1/OUT0	OUT0: PWM OUT 0	
6	P1.2/SCL	14	P1.2/SCL	10	P1.2/SCL	12	P1.2/SCL				I2C Clock
7	P1.3/SDA	15	P1.3/SDA	11	P1.3/SDA	13	P1.3/SDA				I2C Data
8	P1.4/UND0	16	P1.4/UND0							UND0: Underflow Out	
9	P1.5/OVF0	17	P1.5/OVF0							OVF0: Overflow Out	
10	P1.6/OVF0/UND0/nOUT0/CMPO_0	18	P1.6/OVF0/UND0/nOUT0/CMPO_0	12	P1.6/OVF0/UND0/nOUT0/CMPO_0	14	P1.6/OVF0/UND0/nOUT0/CMPO_0	7	P1.6/OVF0/UND0/nOUT0/CMPO_0	nOUT0: Complement of OUT0, UND0, OVF0 as above	CMPO_0: Sense Comp Out, Internal Reset function[1]

Note

1. Must not have load to ground during POR (should be an output).

Table 1. Pin Descriptions *(continued)*

28-Pin SSOP		24-Pin QFN		16-Pin QFN		16-Pin SOIC		8-Pin SOIC			
Pin	**Name**	**Pin**	**Name**	**Pin**	**Name**	**Pin**	**Name**	**Pin**	**Name**	**TCPWM Signals**	**Alternate Functions**
11	VSS										
12	No Connect (NC)[2]										
13	P1.7/MATCH/EXT_CLK	19	P1.7/MATCH/EXT_CLK	13	P1.7/MATCH/EXT_CLK	15	P1.7/MATCH/EXT_CLK			MATCH: Match Out	External Clock
14	P2.0	20	P2.0			16	P2.0				
15	VSS										
16	P3.0/SDA/SWD_IO	21	P3.0/SDA/SWD_IO	14	P3.0/SDA/SWD_IO	1	P3.0/SDA/SWD_IO	8	P3.0/SDA/SWD_IO		I2C Data, SWD I/O
17	P3.1/SCL/SWD_CLK	22	P3.1/SCL/SWD_CLK	15	P3.1/SCL/SWD_CLK	2	P3.1/SCL/SWD_CLK	1	P3.1/SCL/SWD_CLK		I2C Clock, SWD Clock
18	P3.2	23	P3.2	16	P3.2					OUT0:PWM OUT 0	
19	XRES	24	XRES								XRES: External Reset

Descriptions of the Pin functions are as follows:

VDD: Power supply for both analog and digital sections.

VDDIO: Where available, this pin provides a separate voltage domain (see the Power section for details).

VSS: Ground pin.

VCCD: Regulated digital supply (1.8 V ±5%).

Pins belonging to Ports 0, 1, and 2 can all be used as CSD sense or shield pins connected to AMUXBUS A or B. They can also be used as GPIO pins that can be driven by the firmware, in addition to their alternate functions listed in the Table 1.

Pins on Port 3 can be used as GPIO, in addition to their alternate functions listed above.

The following packages are provided: 28-pin SSOP, 24-pin QFN, 16-pin QFN, 16-pin SOIC, and 8-pin SOIC.

Note

[2] This pin is not to be used; it must be left floating.

Figure 4. 28-Pin SSOP Pinout

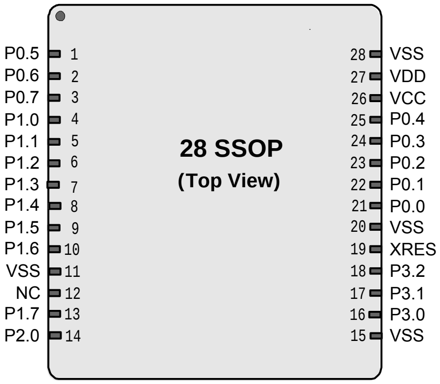


Figure 5. 24-pin QFN Pinout

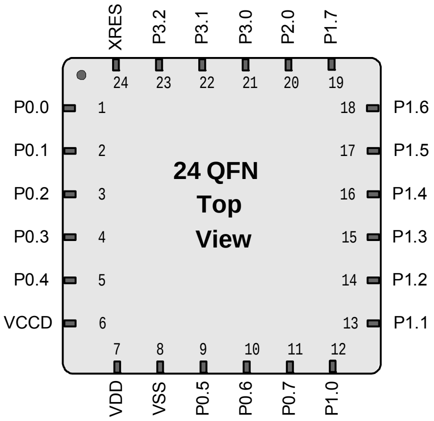


Figure 6. 16-Pin QFN Pinout

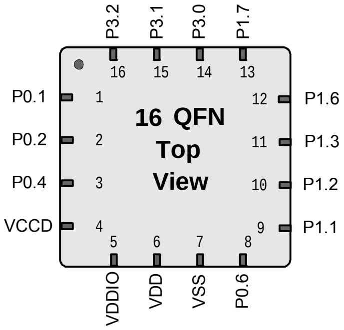


Figure 7. 16-Pin SOIC Pinout

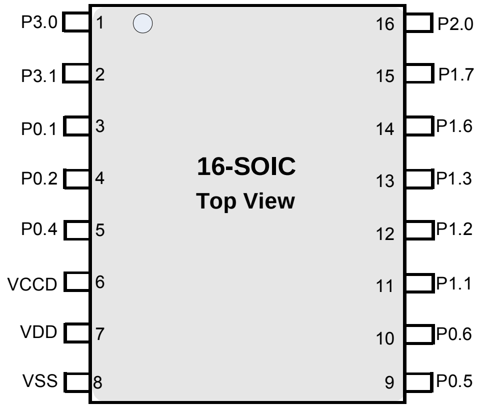
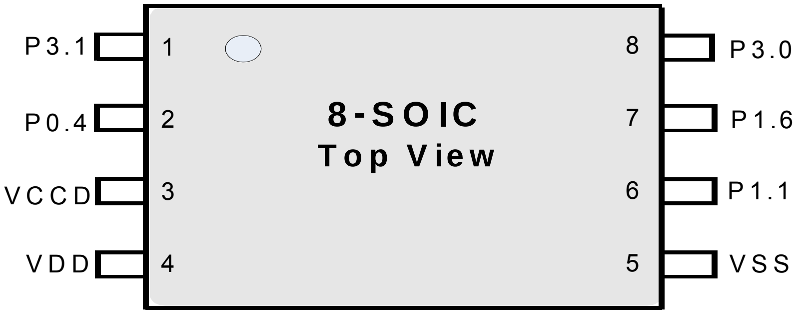


Figure 8. 8-Pin SOIC Pinout



Power

The following power system diagrams (Figure 9 and Figure 10) show the set of power supply pins as implemented for the PSoC 4000. The system has one regulator in Active mode for the digital circuitry. There is no analog regulator; the analog circuits run directly from the V_{DD} input. There is a separate regulator for the Deep Sleep mode. The supply voltage range is either 1.8 V ±5% (externally regulated) or 1.8 V to 5.5 V (unregulated externally; regulated internally) with all functions and circuits operating over that range.

The V_{DDIO} pin, available in the 16-pin QFN package, provides a separate voltage domain for the following pins: P3.0, P3.1, and P3.2. P3.0 and P3.1 can be I^2C pins and the chip can thus communicate with an I^2C system, running at a different voltage (where $V_{DDIO} \leq V_{DD}$). For example, V_{DD} can be 3.3 V and V_{DDIO} can be 1.8 V.

The PSoC 4000 family allows two distinct modes of power supply operation: Unregulated External Supply and Regulated External Supply.

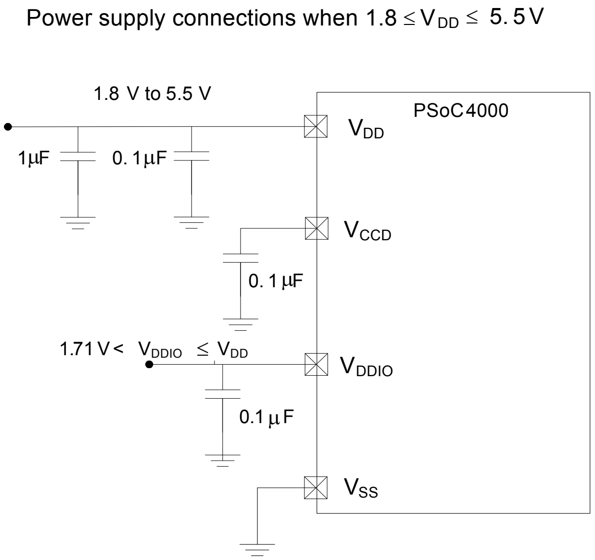
Unregulated External Supply

In this mode, the PSoC 4000 is powered by an external power supply that can be anywhere in the range of 1.8 to 5.5 V. This range is also designed for battery-powered operation. For example, the chip can be powered from a battery system that starts at 3.5 V and works down to 1.8 V. In this mode, the internal regulator of the PSoC 4000 supplies the internal logic and the V_{CCD} output of the PSoC 4000 must be bypassed to ground via an external capacitor (0.1 µF; X5R ceramic or better).

Bypass capacitors must be used from V_{DD} to ground. The typical practice for systems in this frequency range is to use a capacitor in the 1-µF range, in parallel with a smaller capacitor (0.1 µF, for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

An example of a bypass scheme follows (V_{DDIO} is available on the 16-QFN package).

Figure 9. 16-pin QFN Bypass Scheme Example - Unregulated External Supply

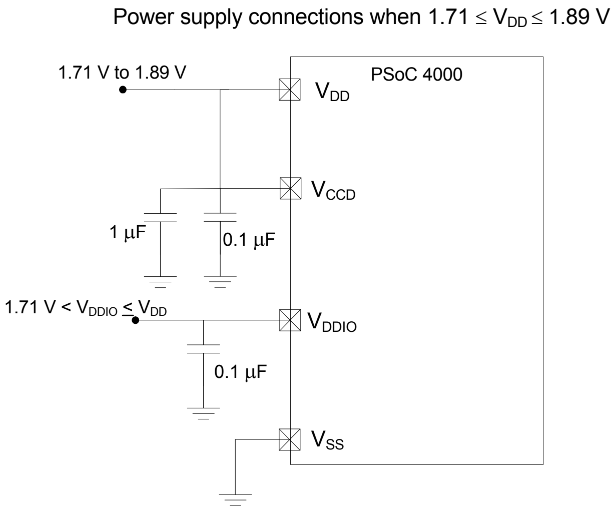


Regulated External Supply

In this mode, the PSoC 4000 is powered by an external power supply that must be within the range of 1.71 to 1.89 V; note that this range needs to include the power supply ripple too. In this mode, the V_{DD} and V_{CCD} pins are shorted together and bypassed. The internal regulator should be disabled in the firmware. Note that in this mode VDD (VCCD) should never exceed 1.89 in any condition, including flash programming.

An example of a bypass scheme follows (V_{DDIO} is available on the 16-QFN package).

Figure 10. 16-pin QFN Bypass Scheme Example - Regulated External Supply



Electrical Specifications

Absolute Maximum Ratings

Table 3. Absolute Maximum Ratings[4]

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID1	V_{DD_ABS}	Digital supply relative to V_{SS}	–0.5	–	6	V	
SID2	V_{CCD_ABS}	Direct digital core voltage input relative to V_{SS}	–0.5	–	1.95	V	
SID3	V_{GPIO_ABS}	GPIO voltage	–0.5	–	V_{DD}+0.5	V	
SID4	I_{GPIO_ABS}	Maximum current per GPIO	–25	–	25	mA	
SID5	$I_{GPIO\_injection}$	GPIO injection current, Max for $V_{IH} > V_{DD}$, and Min for $V_{IL} < V_{SS}$	–0.5	–	0.5	mA	Current injected per pin
BID44	ESD_HBM	Electrostatic discharge human body model	2200	–	–	V	
BID45	ESD_CDM	Electrostatic discharge charged device model	500	–	–	V	
BID46	LU	Pin current for latch-up	–140	–	140	mA	

Device Level Specifications

All specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

Table 4. DC Specifications

Typical values measured at V_{DD} = 3.3 V and 25 °C.

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID53	V_{DD}	Power supply input voltage	1.8	–	5.5	V	With regulator enabled
SID255	V_{DD}	Power supply input voltage ($V_{CCD} = V_{DD}$)	1.71	–	1.89	V	Internally unregulated supply
SID54	V_{DDIO}	V_{DDIO} domain supply	1.71	–	V_{DD}	V	
SID55	C_{EFC}	External regulator voltage bypass	–	0.1	–	µF	X5R ceramic or better
SID56	C_{EXC}	Power supply bypass capacitor	–	1	–	µF	X5R ceramic or better
Active Mode, V_{DD} = 1.8 to 5.5 V							
SID9	I_{DD5}	Execute from flash; CPU at 6 MHz	–	2.0	2.85	mA	
SID12	I_{DD8}	Execute from flash; CPU at 12 MHz	–	3.2	3.75	mA	
SID16	I_{DD11}	Execute from flash; CPU at 16 MHz	–	4.0	4.5	mA	
Sleep Mode, V_{DD} = 1.71 to 5.5 V							
SID25	I_{DD20}	I^2C wakeup, WDT on. 6 MHz	–	1.1	–	mA	
SID25A	I_{DD20A}	I^2C wakeup, WDT on. 12 MHz	–	1.4	–	mA	
Deep Sleep Mode, V_{DD} = 1.8 to 3.6 V (Regulator on)							
SID31	I_{DD26}	I^2C wakeup and WDT on	–	2.5	8.2	µA	

Note

[4] Usage above the absolute maximum conditions listed in Table 1 may cause permanent damage to the device. Exposure to Absolute Maximum conditions for extended periods of time may affect device reliability. The Maximum Storage Temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below Absolute Maximum conditions but above normal operating conditions, the device may not operate to specification.

XRES

Table 8. XRES DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID77	V_{IH}	Input voltage high threshold	0.7 × V_{DD}	–	–	V	CMOS Input
SID78	V_{IL}	Input voltage low threshold	–	–	0.3 × V_{DD}	V	CMOS Input
SID79	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	
SID80	C_{IN}	Input capacitance	–	3	7	pF	
SID81[8]	$V_{HYSXRES}$	Input voltage hysteresis	–	0.05* V_{DD}	–	mV	Typical hysteresis is 200 mV for V_{DD} > 4.5V

Table 9. XRES AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID83[8]	$T_{RESETWIDTH}$	Reset pulse width	5	–	–	µs	
BID#194[8]	$T_{RESETWAKE}$	Wake-up time from reset release	–	–	3	ms	

Analog Peripherals

Comparator

Table 10. Comparator DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID330[8]	I_{CMP1}	Block current, High Bandwidth mode	–	–	110	µA	
SID331[8]	I_{CMP2}	Block current, Low Power mode	–	–	85	µA	
SID332[8]	$V_{OFFSET1}$	Offset voltage, High Bandwidth mode	–	10	30	mV	
SID333[8]	$V_{OFFSET2}$	Offset voltage, Low Power mode	–	10	30	mV	
SID334[8]	Z_{CMP}	DC input impedance of comparator	35	–	–	MΩ	
SID338[8]	VINP_COMP	Comparator input range	0	–	3.6	V	Max input voltage is lower of 3.6 V or V_{DD}
SID339	VREF_COMP	Comparator internal voltage reference	1.188	1.2	1.212	V	

Note

[8] Guaranteed by characterization.

Memory

Table 16. Flash DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID173	V_{PE}	Erase and program voltage	1.71	–	5.5	V	

Table 17. Flash AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID174	$T_{ROWWRITE}$[11]	Row (block) write time (erase and program)	–	–	20	ms	Row (block) = 64 bytes
SID175	$T_{ROWERASE}$[11]	Row erase time	–	–	13	ms	
SID176	$T_{ROWPROGRAM}$[11]	Row program time after erase	–	–	7	ms	
SID178	$T_{BULKERASE}$[11]	Bulk erase time (16 KB)	–	–	15	ms	
SID180[12]	$T_{DEVPROG}$[11]	Total device program time	–	–	7.5	seconds	
SID181[12]	F_{END}	Flash endurance	100 K	–	–	cycles	
SID182[12]	F_{RET}	Flash retention. $T_A \leq 55$ °C, 100 K P/E cycles	20	–	–	years	
SID182A[12]		Flash retention. $T_A \leq 85$ °C, 10 K P/E cycles	10	–	–	years	

System Resources

Power-on Reset (POR)

Table 18. Power On Reset (PRES)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.CLK#6	SR_POWER_UP	Power supply slew rate	1	–	67	V/ms	At power-up
SID185[12]	$V_{RISEIPOR}$	Rising trip voltage	0.80	–	1.5	V	
SID186[12]	$V_{FALLIPOR}$	Falling trip voltage	0.70	–	1.4	V	

Table 19. Brown-out Detect (BOD) for V_{CCD}

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID190[12]	$V_{FALLPPOR}$	BOD trip voltage in active and sleep modes	1.48	–	1.62	V	
SID192[12]	$V_{FALLDPSLP}$	BOD trip voltage in Deep Sleep	1.11	–	1.5	V	

Notes

[11] It can take as much as 20 milliseconds to write to Flash. During this time the device should not be Reset, or Flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.

[12] Guaranteed by characterization.

Ordering Information

The PSoC 4000 part numbers and features are listed in the following table. All package types are available in Tape and Reel.

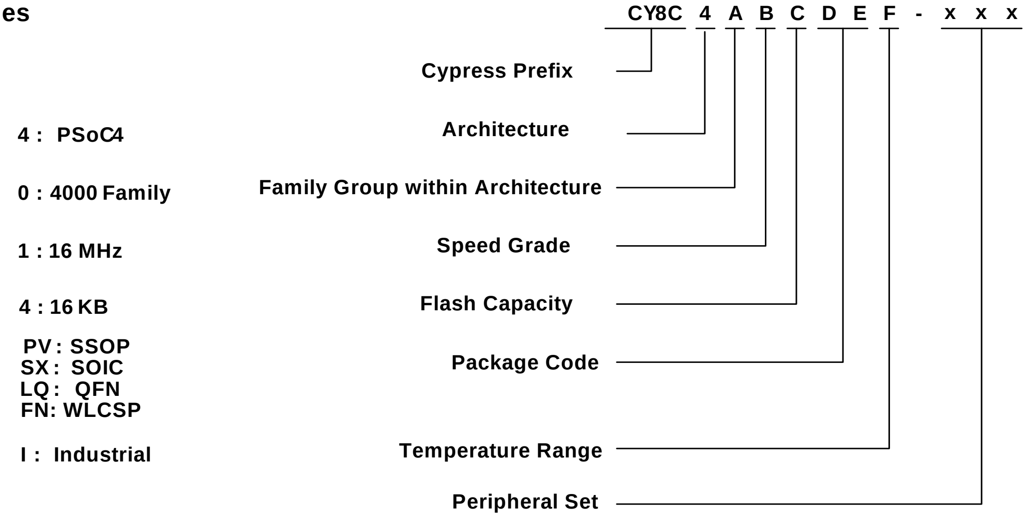
Category	MPN	Feature									Package					
		Max CPU Speed (MHz)	Flash (KB)	SRAM (KB)	CapSense	7-bit IDAC	8-bit IDAC	Comparators	TCPWM Blocks	I2C	16 -WLCSP	8-SOIC	16-SOIC	16-QFN	24-QFN	28-SSOP
CY8C4013	CY8C4013SXI-400	16	8	2	–	–	–	–	1	1	–	✔	–	–	–	–
	CY8C4013SXI-410	16	8	2	–	1	1	1	1	1	–	✔	–	–	–	–
	CY8C4013SXI-411	16	8	2	–	1	1	1	1	1	–	–	✔	–	–	–
	CY8C4013LQI-411	16	8	2	–	1	1	1	1	1	–	–	–	✔	–	–
CY8C4014	CY8C4014SXI-420	16	16	2	✔	1	1	1	1	1	–	✔	–	–	–	–
	CY8C4014SXI-411	16	16	2	–	1	1	1	1	1	–	–	✔	–	–	–
	CY8C4014SXI-421	16	16	2	✔	1	1	1	1	1	–	–	✔	–	–	–
	CY8C4014LQI-421	16	16	2	✔	1	1	1	1	1	–	–	–	✔	–	–
	CY8C4014LQI-412	16	16	2	–	1	1	1	1	1	–	–	–	–	✔	–
	CY8C4014LQI-422	16	16	2	✔	1	1	1	1	1	–	–	–	–	✔	–
	CY8C4014PVI-412	16	16	2	–	1	1	1	1	1	–	–	–	–	–	✔
	CY8C4014PVI-422	16	16	2	✔	1	1	1	1	1	–	–	–	–	–	✔
	CY8C4014FNI-421	16	16	2	✔	1	1	1	1	1	✔	–	–	–	–	–
Other	CY8C4014LQI-SLT1	16	16	2	✔	1	1	1	1	1	–	–	–	✔	–	–
	CY8C4014LQI-SLT2	16	16	2	✔	1	1	1	1	1	–	–	–	–	✔	–

Part Numbering Conventions

PSoC 4 devices follow the part numbering convention described in the following table. All fields are single-character alphanumeric (0, 1, 2, …, 9, A,B, …, Z) unless stated otherwise.

The part numbers are of the form CY8C4ABCDEF-XYZ where the fields are defined as follows.

Examples



The Field Values are listed in the following table:

Field	Description	Values	Meaning
CY8C	Cypress prefix		
4	Architecture	4	PSoC 4
A	Family	0	4000 Family
B	CPU speed	1	16 MHz
		4	48 MHz
C	Flash capacity	3	8 KB
		4	16 KB
		5	32 KB
		6	64 KB
		7	128 KB
DE	Package code	SX	SOIC
		LQ	QFN
		PV	SSOP
		FN	WLCSP
F	Temperature range	I	Industrial
XYZ	Attributes code	000-999	Code of feature set in specific family

Packaging

Table 27. Package List

Spec ID#	Package	Description
BID#47A	28-Pin SSOP	28-pin 5 × 10 × 1.65mm SSOP with 0.65-mm pitch
BID#26	24-Pin QFN	24-pin 4 × 4 × 0.6 mm QFN with 0.5-mm pitch
BID#33	16-Pin QFN	16-pin 3 × 3 × 0.6 mm QFN with 0.5-mm pitch
BID#40	16-Pin SOIC	16-pin (150 Mil) SOIC
BID#47	8-Pin SOIC	8-pin (150 Mil) SOIC
BID#147A	16-Ball WLCSP	16-Ball 1.47 × 1.58 × 0.4 mm

Table 28. Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
T_A	Operating ambient temperature		–40	25	85	°C
T_J	Operating junction temperature		–40	–	100	°C
T_{JA}	Package θ_{JA} (28-pin SSOP)		–	66.6	–	°C/Watt
T_{JC}	Package θ_{JC} (28-pin SSOP)		–	34	–	°C/Watt
T_{JA}	Package θ_{JA} (24-pin QFN)		–	38	–	°C/Watt
T_{JC}	Package θ_{JC} (24-pin QFN)		–	5.6	–	°C/Watt
T_{JA}	Package θ_{JA} (16-pin QFN)		–	49.6	–	°C/Watt
T_{JC}	Package θ_{JC} (16-pin QFN)		–	5.9	–	°C/Watt
T_{JA}	Package θ_{JA} (16-pin SOIC)		–	142	–	°C/Watt
T_{JC}	Package θ_{JC} (16-pin SOIC)		–	49.8	–	°C/Watt
T_{JA}	Package θ_{JA} (16-ball WLCSP)		–	90	–	°C/Watt
T_{JC}	Package θ_{JC} (16-ball WLCSP)		–	0.9	–	°C/Watt
T_{JA}	Package θ_{JA} (8-pin SOIC)		–	198	–	°C/Watt
T_{JC}	Package θ_{JC} (8-pin SOIC)		–	56.9	–	°C/Watt

Table 29. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
All	260 °C	30 seconds

Table 30. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-020

Package	MSL
All except WLCSP	MSL 3
16-ball WLCSP	MSL1

Package Outline Drawings

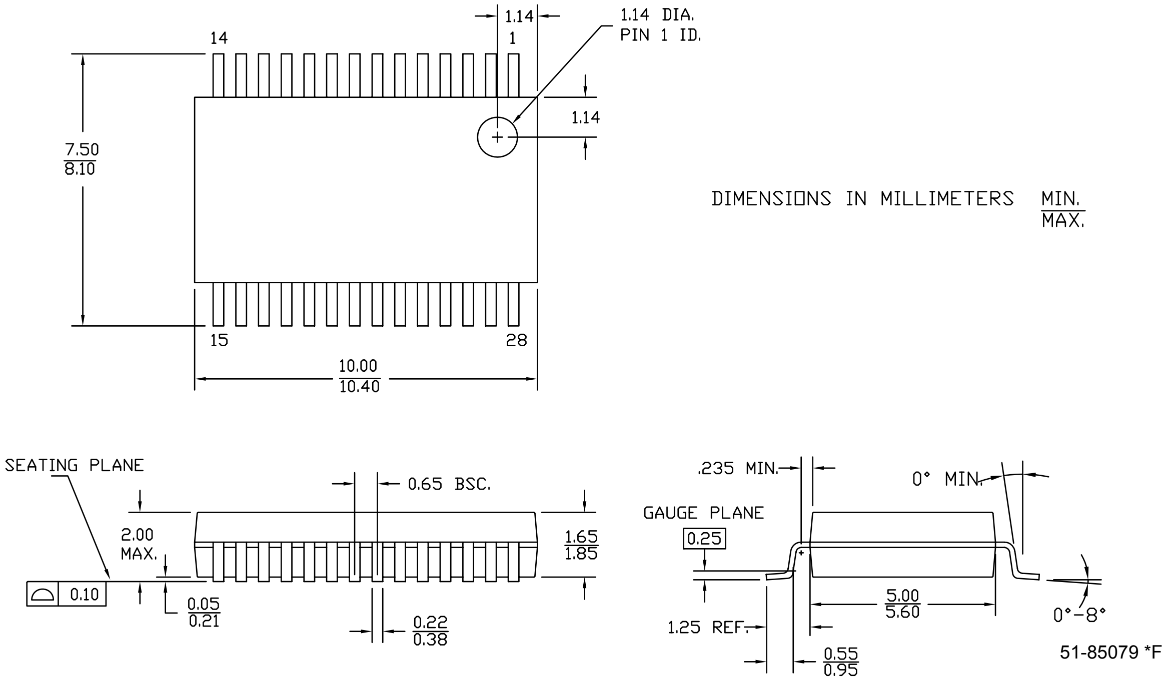


Figure 11. 28-Pin SSOP Package Outline

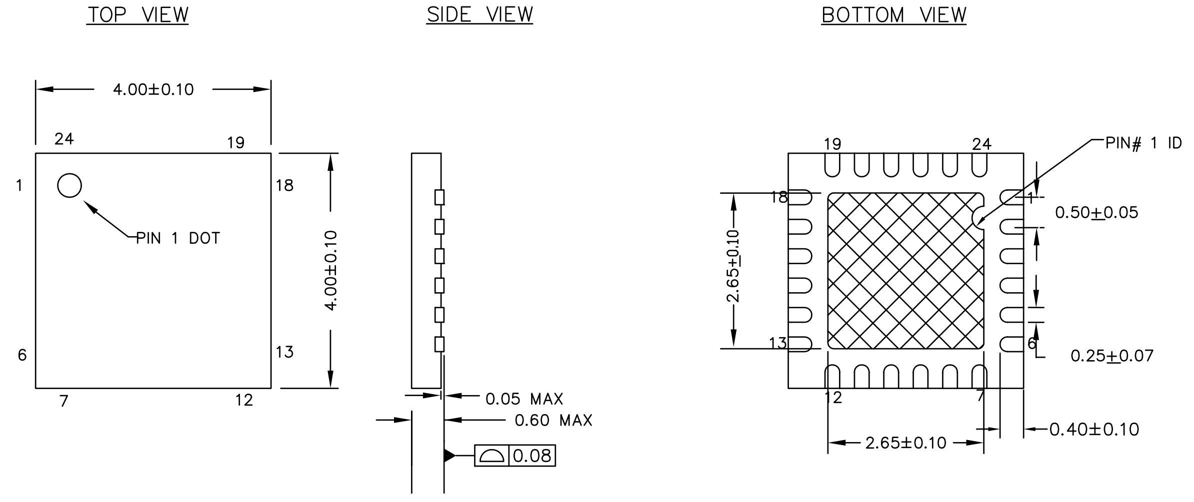


Figure 12. 24-pin QFN EPAD (Sawn) Package Outline

NOTES :

1. ▨ HATCH IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC # MO-248
3. PACKAGE WEIGHT : 29 ± 3 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

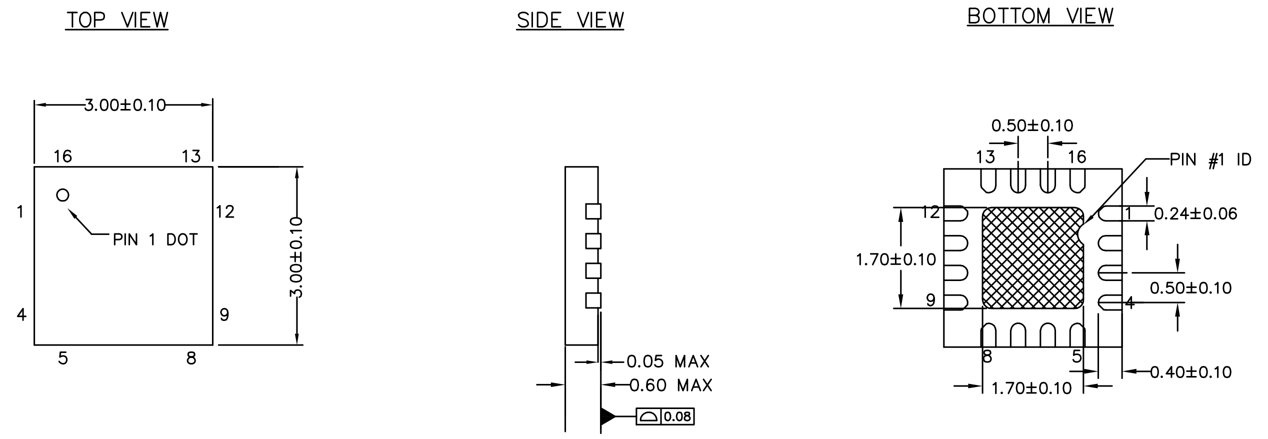
001-13937 *F

Note

15. Dimensions of the QFN package drawings are in millimeters.

The center pad on the QFN package should be connected to ground (VSS) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floating and not connected to any other signal.

Figure 13. 16-pin QFN Package EPAD (Sawn)

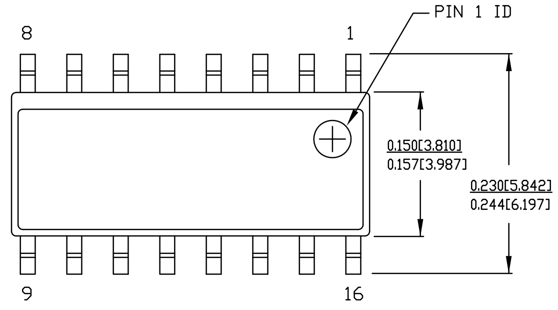


NOTES

1. ▨ HATCH AREA IS SOLDERABLE EXPOSED PAD
2. REFERENCE JEDEC # MO-248
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web

001-87187 *A

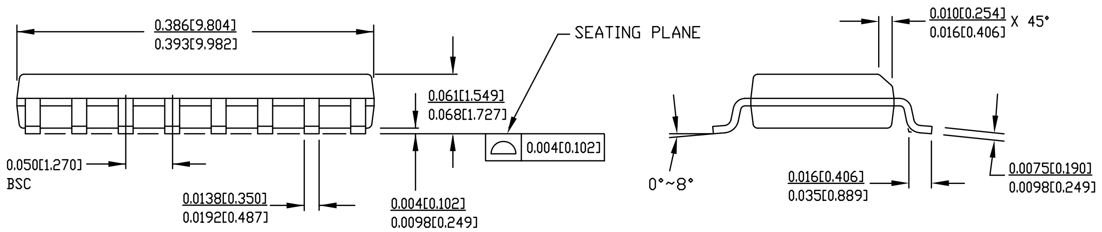
Figure 14. 16-pin (150-mil) SOIC Package Outline



NOTE:

1. DIMENSIONS IN INCHES[MM] MIN. MAX.
2. REFERENCE JEDEC MS-012
3. PACKAGE WEIGHT : refer to PMDD spec. 001-04308

PART #	
S16.15	STANDARD PKG.
SZ16.15	LEAD FREE PKG.



51-85068 *E

Note

16. Dimensions of the QFN package drawings are in inches [millimeters].

Acronyms

Table 31. Acronyms Used in this Document

Acronym	Description
abus	analog local bus
ADC	analog-to-digital converter
AG	analog global
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an ARM data transfer bus
ALU	arithmetic logic unit
AMUXBUS	analog multiplexer bus
API	application programming interface
APSR	application program status register
ARM®	advanced RISC machine, a CPU architecture
ATM	automatic thump mode
BW	bandwidth
CAN	Controller Area Network, a communications protocol
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
DAC	digital-to-analog converter, see also IDAC, VDAC
DFB	digital filter block
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DMIPS	Dhrystone million instructions per second
DMA	direct memory access, see also TD
DNL	differential nonlinearity, see also INL
DNU	do not use
DR	port write data registers
DSI	digital system interconnect
DWT	data watchpoint and trace
ECC	error correcting code
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
EMIF	external memory interface
EOC	end of conversion
EOF	end of frame
EPSR	execution program status register
ESD	electrostatic discharge

Table 31. Acronyms Used in this Document *(continued)*

Acronym	Description
ETM	embedded trace macrocell
FIR	finite impulse response, see also IIR
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output, applies to a PSoC pin
HVI	high-voltage interrupt, see also LVI, LVD
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
IIR	infinite impulse response, see also FIR
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
I/O	input/output, see also GPIO, DIO, SIO, USBIO
IPOR	initial power-on reset
IPSR	interrupt program status register
IRQ	interrupt request
ITM	instrumentation trace macrocell
LCD	liquid crystal display
LIN	Local Interconnect Network, a communications protocol.
LR	link register
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVI	low-voltage interrupt, see also HVI
LVTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit
MISO	master-in slave-out
NC	no connect
NMI	nonmaskable interrupt
NRZ	non-return-to-zero
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL
opamp	operational amplifier
PAL	programmable array logic, see also PLD

Table 31. Acronyms Used in this Document *(continued)*

Acronym	Description
PC	program counter
PCB	printed circuit board
PGA	programmable gain amplifier
PHUB	peripheral hub
PHY	physical layer
PICU	port interrupt control unit
PLA	programmable logic array
PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration data sheet
POR	power-on reset
PRES	precise power-on reset
PRS	pseudo random sequence
PS	port read data register
PSoC®	Programmable System-on-Chip™
PSRR	power supply rejection ratio
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I^2C serial clock
SDA	I^2C serial data
S/H	sample and hold
SINAD	signal to noise and distortion ratio
SIO	special input/output, GPIO with advanced features. See GPIO.
SOC	start of conversion
SOF	start of frame
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory
SRES	software reset
SWD	serial wire debug, a test protocol
SWV	single-wire viewer
TD	transaction descriptor, see also DMA
THD	total harmonic distortion
TIA	transimpedance amplifier
TRM	technical reference manual
TTL	transistor-transistor logic
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UDB	universal digital block
USB	Universal Serial Bus
USBIO	USB input/output, PSoC pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset I/O pin
XTAL	crystal

Revision History

Description Title: PSoC® 4: PSoC 4000 Family Datasheet Programmable System-on-Chip (PSoC®) Document Number: 001-89638				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*B	4348760	WKA	05/16/2014	New PSoC 4000 datasheet.
*C	4514139	WKA	10/27/2014	Added 28-pin SSOP pin and package details. Updated V_{REF} spec values. Updated conditions for SID174. Updated SID.CSD#15 values and description. Added spec SID339.
*D	4617283	WKA	01/09/2015	Corrected Development Kits information and PSoC Creator Example Project figure. Corrected typo in the ordering information table. Updated 28-pin SSOP package diagram.
*E	4735762	WKA	05/26/2015	Added 16-ball WLCSP pin and package details.
*F	5466193	WKA	10/07/2016	Updated Table 30. Updated 8-pin SOIC package diagram. Updated the template.
*G	5685079	TSEN	04/05/2017	Updated 16-ball WLCSP package details.