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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	RF4CE, Remote Control
Core Processor	ARM® Cortex®-M3
Program Memory Type	FLASH (128kB)
Controller Series	STM32W
RAM Size	8K x 8
Interface	I²C, SPI, UART/USART
Number of I/O	24
Voltage - Supply	1.18V ~ 3.6V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-VFQFPN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32w108cbu63tr

1.2 Overview

1.2.1 Functional description

The STM32W108xx radio receiver is a low-IF, super-heterodyne receiver. The architecture has been chosen to optimize co-existence with other devices in the 2.4 GHz band (namely, WIFI and Bluetooth), and to minimize power consumption. The receiver uses differential signal paths to reduce sensitivity to noise interference. Following RF amplification, the signal is downconverted by an image-rejecting mixer, filtered, and then digitized by an ADC.

The radio transmitter uses an efficient architecture in which the data stream directly modulates the VCO frequency. An integrated power amplifier (PA) provides the output power. Digital logic controls Tx path and output power calibration. If the STM32W108xx is to be used with an external PA, use the TX_ACTIVE or nTX_ACTIVE signal to control the timing of the external switching logic.

The integrated 4.8 GHz VCO and loop filter minimize off-chip circuitry. Only a 24 MHz crystal with its loading capacitors is required to establish the PLL local oscillator signal.

The MAC interfaces the on-chip RAM to the Rx and Tx baseband modules. The MAC provides hardware-based IEEE 802.15.4 packet-level filtering. It supplies an accurate symbol time base that minimizes the synchronization effort of the software stack and meets the protocol timing requirements. In addition, it provides timer and synchronization assistance for the IEEE 802.15.4 CSMA-CA algorithm.

The STM32W108xx integrates an ARM® Cortex®-M3 microprocessor, revision r1p1. This industry-leading core provides 32 bit performance and is very power efficient. It has excellent code density using the ARM® Thumb 2 instruction set. The processor can be operated at 12 MHz or 24 MHz when using the crystal oscillator, or at 6 MHz or 12 MHz when using the integrated high frequency RC oscillator.

The STM32W108xx has 128/192/256 Kbyte of Flash memory, 8/12/16 Kbyte of SRAM on-chip, and the ARM configurable memory protection unit (MPU).

The STM32W108xx contains 24 GPIO pins shared with other peripheral or alternate functions. Because of flexible routing within the STM32W108xx, external devices can use the alternate functions on a variety of different GPIOs. The integrated Serial Controller SC1 can be configured for SPI (master or slave), I^2C (master-only), or UART operation, and the Serial Controller SC2 can be configured for SPI (master or slave) or I^2C (master-only) operation.

The STM32W108xx has a general purpose ADC which can sample analog signals from six GPIO pins in single-ended or differential modes. It can also sample the regulated supply VDD_PADSA, the voltage reference VREF, and GND. The ADC has two selectable voltage ranges: 0 V to 1.2 V for the low voltage (input buffer disabled) and 0.1 V to VDD_PADS minus 0.1 V for the high voltage supply (input buffer enabled). The ADC has a DMA mode to capture samples and automatically transfer them into RAM. The integrated voltage reference for the ADC, VREF, can be made available to external circuitry. An external voltage reference can also be driven into the ADC.

The STM32W108xx contains four oscillators: a high frequency 24 MHz external crystal oscillator (24 MHz HSE OSC), a high frequency 12 MHz internal RC oscillator (12 MHz HSI RC), an optional low frequency 32.768 kHz external crystal oscillator (32 kHz HSE OSC), and a 10 kHz internal RC oscillator (10 kHz LSI RC).

Figure 3. 40-pin VFQFPN pinout

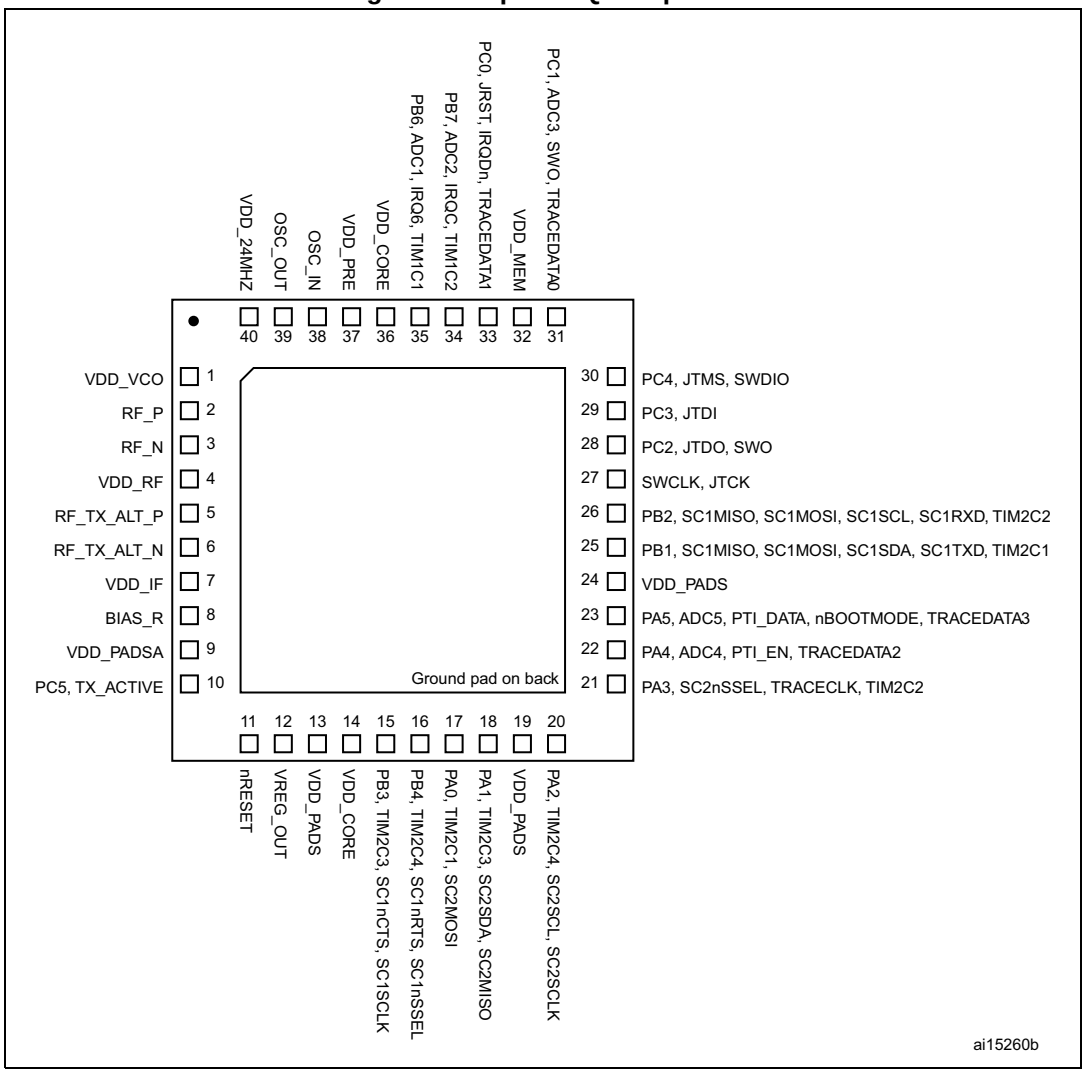


Table 2. Pin descriptions

48-Pin Package Pin no.	40-Pin Package Pin no.	Signal	Direction	Description
1	40	VDD_24MHZ	Power	1.8V high-frequency oscillator supply
2	1	VDD_VCO	Power	1.8V VCO supply
3	2	RF_P	I/O	Differential (with RF_N) receiver input/transmitter output
4	3	RF_N	I/O	Differential (with RF_P) receiver input/transmitter output
5	4	VDD_RF	Power	1.8V RF supply (LNA and PA)
6	5	RF_TX_ALT_P	O	Differential (with RF_TX_ALT_N) transmitter output (optional)
7	6	RF_TX_ALT_N	O	Differential (with RF_TX_ALT_P) transmitter output (optional)
8	7	VDD_IF	Power	1.8V IF supply (mixers and filters)
9	8	BIAS_R	I	Bias setting resistor

Table 2. Pin descriptions (continued)

48-Pin Package Pin no.	40-Pin Package Pin no.	Signal	Direction	Description
19	15	PB3	I/O	Digital I/O
		TIM2_CH3 (see Pin 22)	O	Timer 2 channel 3 output Enable remap with TIM2_OR[6] Enable timer output in TIM2_CCER Select alternate output function with GPIOB_CRL[15:12]
			I	Timer 2 channel 3 input. Enable remap with TIM2_OR[6].
		UART_CTS	I	UART CTS handshake of Serial Controller 1 Enable with SC1_UARTCR[5] Select UART with SC1_CR
		SC1SCLK	O	SPI master clock of Serial Controller 1 Either disable timer output in TIM2_CCER or disable remap with TIM2_OR[6] Enable master with SC1_SPICR[4] Select SPI with SC1_CR Select alternate output function with GPIOB_CRL[15:12]
			I	SPI slave clock of Serial Controller 1 Enable slave with SC1_SPICR[4] Select SPI with SC1_CR
20	16	PB4	I/O	Digital I/O
		TIM2_CH4 (see also Pin 24)	O	Timer 2 channel 4 output Enable remap with TIM2_OR[7] Enable timer output in TIM2_CCER Select alternate output function with GPIOB_CRH[3:0]
			I	Timer 2 channel 4 input. Enable remap with TIM2_OR[7].
		UART_RTS	O	UART RTS handshake of Serial Controller 1 Either disable timer output in TIM2_CCER or disable remap with TIM2_OR[7] Enable with SC1_UARTCR[5] Select UART with SC1_CR Select alternate output function with GPIOB_CRH[3:0]
		SC1nSSEL	I	SPI slave select of Serial Controller 1 Enable slave with SC1_SPICR[4] Select SPI with SC1_CR

4 Embedded memory

4.1 Memory organization and memory map

The bytes are coded in the memory in Little Endian format. The lowest numbered byte in a word is considered the word's least significant byte and the highest numbered byte the most significant.

For detailed mapping of peripheral registers, please refer to the relevant section.

All the memory areas that are not allocated to on-chip memories and peripherals are considered "Reserved").

Refer to *Figure 4: STM32W108xB memory mapping, Figure 5: STM32W108CC and STM32W108CZ memory mapping,* and *Table 3: STM32W108xx peripheral register boundary addresses* for the register boundary addresses of the peripherals available in all STM32W108xx devices.

6.1 Power domains

The STM32W108xx contains three power domains:

- An "always on domain" containing all logic and analog cells required to manage the STM32W108xx's power modes, including the GPIO controller and sleep timer. This domain must remain powered.
- A "core domain" containing the CPU, Nested Vectored Interrupt Controller (NVIC), and peripherals. To save power, this domain can be powered down using a mode called deep sleep.
- A "memory domain" containing the RAM and Flash memories. This domain is managed by the power management controller. When in deep sleep, the RAM portion of this domain is powered from the always-on domain supply to retain the RAM contents while the regulators are disabled. During deep sleep the Flash portion is completely powered down.

6.1.1 Internally regulated power

The preferred and recommended power configuration is to use the internal regulated power supplies to provide power to the core and memory domains. The internal regulators (VREG_1V25 and VREG_1V8) generate nominal 1.25 V and 1.8 V supplies. The 1.25 V supply is internally routed to the core domain and to an external pin. The 1.8 V supply is routed to an external pin where it can be externally routed back into the chip to supply the memory domain. The internal regulators are described in *Section 7: Integrated voltage regulator on page 90*.

When using the internal regulators, the always-on domain must be powered between 2.1 V and 3.6 V at all four VDD_PADS pins.

When using the internal regulators, the VREG_1V8 regulator output pin (VREG_OUT) must be connected to the VDD_MEM, VDD_PADSA, VDD_VCO, VDD_RF, VDD_IF, VDD_PRE, and VDD_SYNTH pins.

When using the internal regulators, the VREG_1V25 regulator output and supply requires a connection between both VDD_CORE pins.

6.1.2 Externally regulated power

Optionally, the on-chip regulators may be left unused, and the core and memory domains may instead be powered from external supplies. For simplicity, the voltage for the core domain can be raised to nominal 1.8 V, requiring only one external regulator. Note that if the core domain is powered at a higher voltage (1.8 V instead of 1.25 V) then power consumption increases. A regulator enable signal, REG_EN, is provided for control of external regulators. This is an open-drain signal that requires an external pull-up resistor. If REG_EN is not required to control external regulators it can be disabled (see *Section 8.1.3: Forced functions on page 95*).

Using an external regulator requires the always-on domain to be powered between 1.8 V and 3.6 V at all four VDD_PADS pins.

When using an external regulator, the VREG_1V8 regulator output pin (VREG_OUT) must be left unconnected.

When using an external regulator, this external nominal 1.8 V supply has to be connected to both VDD_CORE pins and to the VDD_MEM, VDD_PADSA, VDD_VCO, VDD_RF, VDD_IF, VDD_PRE and VDD_SYNTH pins.

Sleep timer force interrupt register (SLPTMR_IFR)

Address: 0x4000 A020
Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved													CMPB	CMPA	WRAP
													rw	rw	rw

Bits 31:3 Reserved, must be kept at reset value

Bit 2 CMPB: Force sleep timer compare B interrupt

Bit 1 CMPA: Force sleep timer compare A interrupt

Bit 0 WRAP: Force sleep timer wrap interrupt

Sleep timer interrupt enable register (SLPTMR_IER)

Address: 0x4000 A054
Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved													CMPB	CMPA	WRAP
													rw	rw	rw

Bits 31:3 Reserved, must be kept at reset value

Bit 2 CMPB: Sleep timer compare B

Bit 1 CMPA: Sleep timer compare A

Bit 0 WRAP: Sleep timer wrap

8.5.9 External interrupt x configuration register (EXTIx_CR)

Address offset: 0xBC14 (EXTIC_CR) and 0xBC18 (EXTID_CR)
Reset value: 0x0000 000F (EXTIC_CR) and 0x0000 0010 (EXTID_CR)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											GPIO_SEL[4:0]				
											rw	rw	rw	rw	rw

Bits 31:5 Reserved, must be kept at reset value

Bits 4:0 GPIO_SEL[4:0]: Pin assigned to EXTIx

0x00: PA0
0x01: PA1
0x02: PA2
0x03: PA3
0x04: PA4
0x05: PA5
0x06: PA6
0x07: PA7
0x08: PB0
0x09: PB1
0x0A: PB2
0x0B: PB3
0x0C: PB4
0x0D: PB5
0x0E: PB6
0x0F: PB7
0x10: PC0
0x11: PC1
0x12: PC2
0x13: PC3
0x14: PC4
0x15: PC5
0x16: PC6
0x17: PC7
0x18 - 0x1F: Reserved, must be kept at reset value

8.5.10 PC TRACE or debug select register (GPIO_PCTRACECR)

Address offset: 0x4000 4028
Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															SEL
															rws

Bits 31:1 Reserved, must be kept at reset value

Bit 0 SEL: Channel encoding
1: PC trace
0: BB debug

9.6.1 Setup and configuration

The UART baud rate clock is produced by a programmable baud generator starting from the 24 Hz clock:

$$baud = \frac{24MHz}{2N + F}$$

The integer portion of the divisor, N, is written to the SC1_UARTBRR1 register and the fractional part, F, to the SC1_UARTBRR2 register. *Table 29* shows the values used to generate some common baud rates and their associated clock frequency error. The UART requires an internal clock that is at least eight times the baud rate clock, so the minimum allowable setting for SC1_UARTBRR1 is '8'.

Table 29. UART baud rate divisors for common baud rates

Baud rate (bits/sec)	SC1_UARTBRR1	SC1_UARTBRR2	Baud rate error (%)
300	40000	0	0
2400	5000	0	0
4800	2500	0	0
9600	1250	0	0
19200	625	0	0
38400	312	1	0
57600	208	1	- 0.08
115200	104	0	+ 0.16
230400	52	0	+ 0.16
460800	26	0	+ 0.16
921600	13	0	+ 0.16

Note: The UART may receive corrupt bytes if the interbyte gap is long or there is a baud rate mismatch between receive and transmit. The UART may detect a parity and/or framing error on the corrupt byte, but there will not necessarily be any error detected. As a result, the device should be operated in systems where the other side of the communication link also uses a crystal as its timing reference, and baud rates should be selected to minimize the baud rate mismatch to the crystal tolerance. UART protocols should contain some form of error checking (e.g. CRC) at the packet level to detect, and retry in the event of errors.

The UART character frame format is determined by three bits in the SC1_UARTCR register:

- STOP selects the number of stop bits in transmitted characters. (Only one stop bit is ever required in received characters.) If this bit is clear, characters are transmitted with one stop bit; if set, characters are transmitted with two stop bits.
- PCE controls whether or not received and transmitted characters include a parity bit. If PCE is clear, characters do not contain a parity bit, otherwise, characters do contain a parity bit.
- PS specifies whether transmitted and received parity bits contain odd or even parity. If this bit is clear, the parity bit is even, and if set, the parity bit is odd. Even parity is the exclusive-or of all of the data bits, and odd parity is the inverse of the even parity value. PS has no effect if PCE is clear.

9.9.2 Serial controller SPI control register (SCx_SPICR)

Address offset: 0xC858 (SC1_SPICR) and 0xC058 (SC2_SPICR)
Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										RX MODE	MSTR	RP TEN	LSB FIRST	CPHA	CPOL
										rw	rw	rw	rw	rw	rw

Bits 31:6 Reserved, must be kept at reset value

Bit 5 RXMODE: Receiver-driven mode selection bit (SPI master mode only)
0: Initiate transactions when transmit data is available.
1: Initiate transactions when the receive buffer (FIFO or DMA) has space. Force immediate transmission of busy token or resend last byte (depending on **RPTEN**) and receive data into FIFO until the FIFO is full.

Bit 4 MSTR: Master selection
0: Slave configuration
1: Master configuration

Bit 3 RPTEN: Repeat enable
This bit controls behavior on a transmit buffer underrun condition in slave mode. Clear this bit to send the BUSY token (0xFF) and set this bit to repeat the last byte. Changes to this bit take effect when the transmit FIFO is empty and the transmit serializer is idle.

Bit 2 LSBFIRST: Frame format
0: Most significant bit transmitted first
1: Least significant bit transmitted first

Bit 1 CPHA: Clock phase
0: The first clock transition is the first data capture edge
1: The second clock transition is the first data capture edge

Bit 0 CPOL: Clock polarity
0: CK to 0 when idle
1: CK to 1 when idle

Table 31. SC1/SC2 register map and reset values (continued)

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0xC80C	SC1_DMARX ENDADDBR	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	ADD[12:0]												
	Reset value																				0	0	0	0	0	0	0	0	0	0	0	0	0
0xC810	SC1_DMATX BEGADDAR	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	ADD[12:0]												
	Reset value																				0	0	0	0	0	0	0	0	0	0	0	0	0
0xC814	SC1_DMATX ENDADDAR	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	ADD[12:0]												
	Reset value																				0	0	0	0	0	0	0	0	0	0	0	0	0
0xC818	SC1_DMATX BEGADDBR	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	ADD[12:0]												
	Reset value																				0	0	0	0	0	0	0	0	0	0	0	0	0
0xC81C	SC1_DMATX ENDADDBR	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	ADD[12:0]												
	Reset value																				0	0	0	0	0	0	0	0	0	0	0	0	0
0xC820	SC1_DMARX CNTAR	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	CNT[12:0]												
	Reset value																				0	0	0	0	0	0	0	0	0	0	0	0	0
0xC824	SC1_DMARX CNTBR	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	CNT[12:0]												
	Reset value																				0	0	0	0	0	0	0	0	0	0	0	0	0
0xC828	SC1_DMATX CNTR	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	CNT[12:0]												
	Reset value																				0	0	0	0	0	0	0	0	0	0	0	0	0
0xC82C	SC1_DMASR	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	NSSS [2:0]			FEB	FEA	PEB	PEA	OVRB	OVRA	TXBACK	TXAACK	RXBACK	RXAACK
	Reset value																				0	0	0	0	0	0	0	0	0	0	0	0	0
0xC830	SC1_DMACR	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	TXRST	RXRST	TXLODB	TXLODA	RXLODB	RXLODA
	Reset value																											0	0	0	0	0	0
0xC834	SC1_DMARX ERRAR	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	ADD[12:0]												
	Reset value																				0	0	0	0	0	0	0	0	0	0	0	0	0
0xC838	SC1_DMARX ERRBR	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	ADD[12:0]												
	Reset value																				0	0	0	0	0	0	0	0	0	0	0	0	0
0xC870	SC1_DMARX CNTSAVEDR	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	CNT[12:0]												
	Reset value																				0	0	0	0	0	0	0	0	0	0	0	0	0
0xA80C	SC2_ISR	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	PE	FE	TXULODB	TXULODA	RXULODB	RXULODA	NACK	CMDFIN	BTF	BRF	UDR	OVR	IDLE	TXE	RXNE
	Reset value																		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0xA84C	SC2_IER	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	PEIE	FEIE	TXULODRIE	TXULODAIE	RXULODBIE	RXULODAIE	NACKIE	CMDFINIE	BTFIE	BRFIE	UDRIE	OVRIE	IDLEIE	TXEIE	RXNEIE
	Reset value																		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

10.1.3 Clock selection

The counter clock can be provided by the following clock sources:

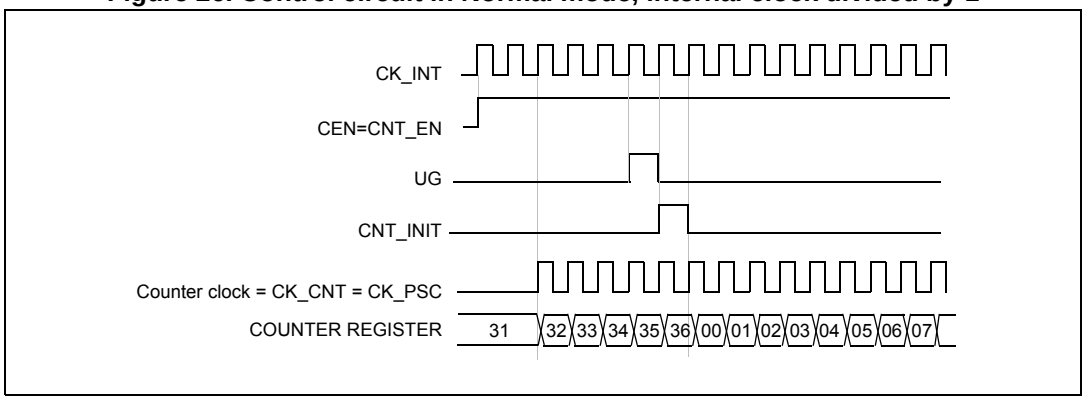
- Internal clock (PCLK)
- External clock mode 1: external input pin (TIy)
- External clock mode 2: external trigger input (ETR)
- Internal trigger input (ITR0): using the other timer as prescaler. Refer to the *Using one timer as prescaler for the other timer* for more details.

Internal clock source (CK_INT)

The internal clock is selected when the slave mode controller is disabled (SMS = 000 in the TIMx_SMCR register). In this mode, the CEN, DIR (in the TIMx_CR1 register), and UG bits (in the TIMx_EGR register) are actual control bits and can be changed only by software, except for UG, which remains cleared automatically. As soon as the CEN bit is written to 1, the prescaler is clocked by the internal clock CK_INT.

Figure 26 shows the behavior of the control circuit and the up-counter in normal mode, without prescaling.

Figure 26. Control circuit in Normal mode, internal clock divided by 1

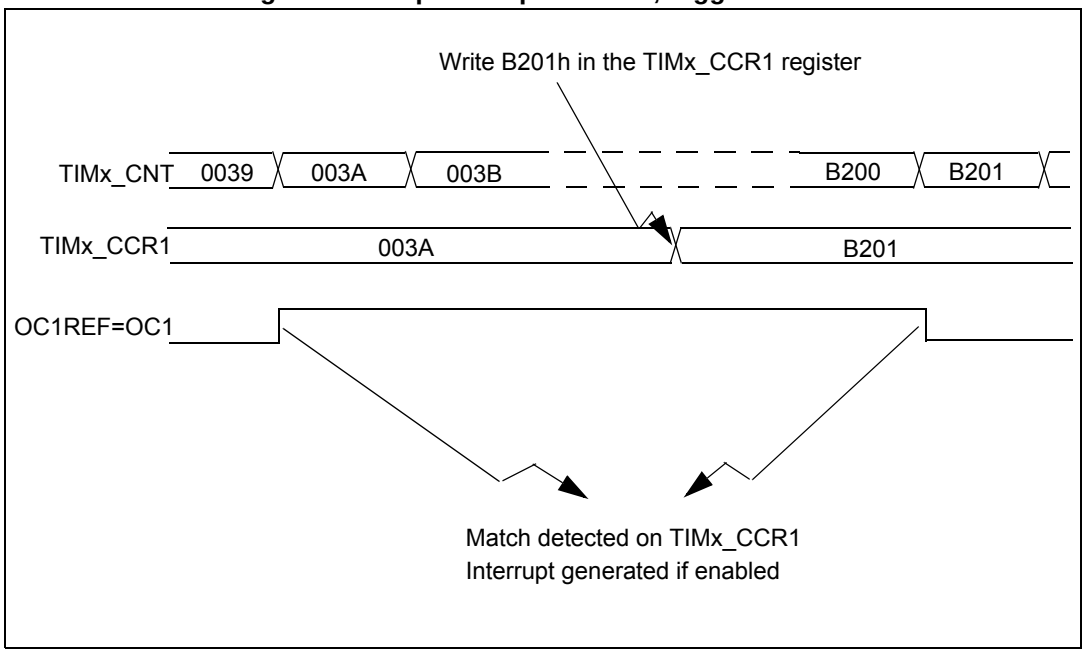


External clock source mode 1

This mode is selected when SMS = 111 in the TIMx_SMCR register. The counter can count at each rising or falling edge on a selected input.

To control the output waveform, software can update the TIMx_CCRy register at any time, provided that the buffer register is not enabled (OCyPE = 0). Otherwise TIMx_CCRy shadow register is updated only at the next update event. An example is given in *Figure 35*.

Figure 35. Output compare mode, toggle on OC1



10.1.9 PWM mode

Pulse width modulation mode allows you to generate a signal with a frequency determined by the value of the TIMx_ARR register, and a duty cycle determined by the value of the TIMx_CCRy register.

PWM mode can be selected independently on each channel (one PWM per OCy output) by writing 110 (PWM mode 1) or 111 (PWM mode 2) in the OCyM bits in the TIMx_CCMR1 register. The corresponding buffer register must be enabled by setting the OCyPE bit in the TIMx_CCMR1 register. Finally, in up-counting or center-aligned mode the auto-reload buffer register must be enabled by setting the ARPE bit in the TIMx_CR1 register.

Because the buffer registers are only transferred to the shadow registers when an update event occurs, before starting the counter initialize all the registers by setting the UG bit in the TIMx_EGR register.

OCy polarity is software programmable using the CCyP bit in the TIMx_CCER register. It can be programmed as active high or active low. OCy output is enabled by the CCyE bit in the TIMx_CCER register. Refer to the TIMx_CCER register description in the Registers section for more details.

In PWM mode (1 or 2), TIMx_CNT and TIMx_CCRy are always compared to determine whether TIMx_CCRy ≤TIMx_CNT or TIMx_CNT ≤TIMx_CCRy,depending on the direction of the counter. The OCyREF signal is asserted only:

- When the result of the comparison changes, or
- When the output compare mode (OCyM bits in the TIMx_CCMR1 register) switches from the "frozen" configuration (no comparison, OCyM = 000) to one of the PWM modes (OCyM = 110 or 111).

This allows software to force a PWM output to a particular state while the timer is running.

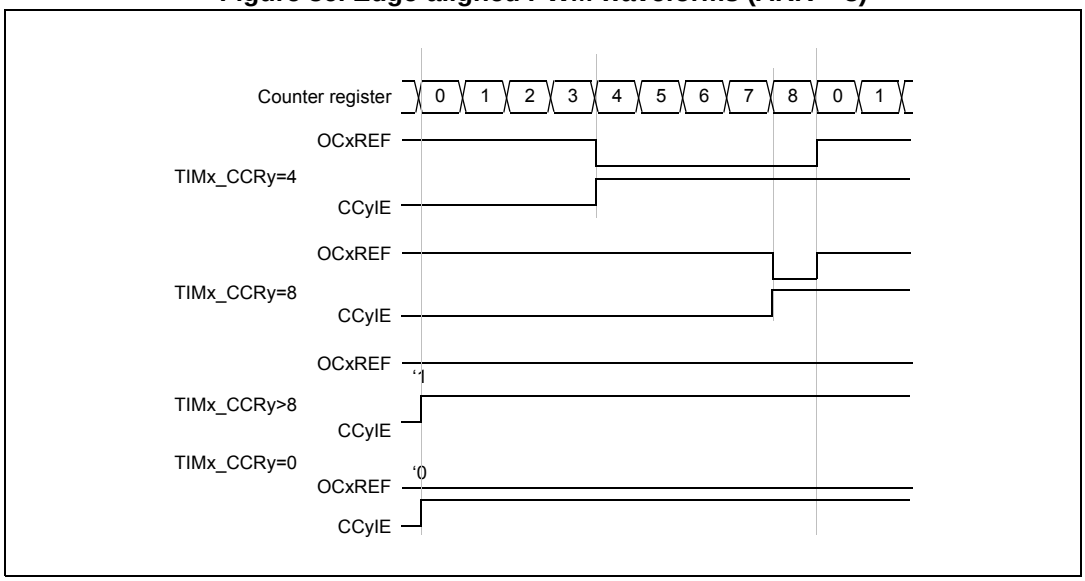
The timer is able to generate PWM in edge-aligned mode or center-aligned mode depending on the CMS bits in the TIMx_CR1 register.

PWM edge-aligned mode: up-counting configuration

Up-counting is active when the DIR bit in the TIMx_CR1 register is low. Refer to *Up-counting mode on page 164*.

The following example uses PWM mode 1. The reference PWM signal OCyREF is high as long as TIMx_CNT < TIMx_CCRy, otherwise it becomes low. If the compare value in TIMx_CCRy is greater than the auto-reload value in TIMx_ARR, then OCyREF is held at 1. If the compare value is 0, then OCyREF is held at 0. *Figure 36* shows some edge-aligned PWM waveforms in an example, where TIMx_ARR = 8.

Figure 36. Edge-aligned PWM waveforms (ARR = 8)



PWM edge-aligned mode: down-counting configuration

Down-counting is active when the DIR bit in the TIMx_CR1 register is high. Refer to *Down-counting mode on page 166* for more information.

In PWM mode 1, the reference signal OCyREF is low as long as TIMx_CNT > TIMx_CCRy, otherwise it becomes high. If the compare value in TIMx_CCRy is greater than the auto-reload value in TIMx_ARR, then OCyREF is held at 1. Zero-percent PWM is not possible in this mode.

PWM center-aligned mode

Center-aligned mode is active except when the CMS bits in the TIMx_CR1 register are 00 (all configurations where CMS is non-zero have the same effect on the OCyREF/OCy signals). The compare flag is set when the counter counts up, when it counts down, or when it counts up and down, depending on the CMS bits configuration. The direction bit (DIR) in the TIMx_CR1 register is updated by hardware and must not be changed by software. Refer to *Center-aligned mode (up/down counting) on page 167* for more information.

10.3.8 Timer x capture/compare mode register 1 (TIMx_CCMR1)

Address offset: 0xE018 (TIM1) and 0xF018 (TIM2)
Reset value: 0x0000 0000

The timer channels can be programmed as inputs (capture mode) or outputs (compare mode). The direction of a channel “y” is defined by configuring the corresponding CCyS bits in this register. All other bits have different functions in input and in output mode. For a given bit:

- OCxy describes its function when the channel is configured as an output (CCyS = 0)
- ICxy describes its function when the channel is configured as an input (CCyS > 0)

In short, the same bit can have a different meaning for the input stage and for the output stage. Care should be taken.

Output compare mode

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	OC2M[2:0]			OC2PE	OC2FE	CC2S[1:0]		Reserved	OC1M[2:0]			OC1PE	OC1FE	CC1S[1:0]	
	rw	rw	rw	rw	rw	rw	rw		rw	rw	rw	rw	rw	rw	rw

Bits 31:15 Reserved, must be kept at reset value

Bits 14:12 OC2M[2:0]: Output Compare 2 Mode

Defines the behavior of the output reference signal OC2REF from which OC2 derives. OC2REF is active high whereas OC2"s active level depends on the CC2P bit.
000: Frozen - The comparison between the output compare register TIMx_CCR2 and the counter TIMx_CNT has no effect on the outputs.
001: Set OC2REF to active on match. The OC2REF signal is forced high when the counter TIMx_CNT matches the capture/compare register 2 (TIMx_CCR2).
010: Set OC2REF to inactive on match. OC2REF signal is forced low when the counter TIMx_CNT matches the capture/compare register 2 (TIMx_CCR2).
011: Toggle - OC2REF toggles when TIMx_CNT = TIMx_CCR2
100: Force OC2REF inactive
101: Force OC2REF active
110: PWM mode 1 - In up-counting, OC2REF is active as long as TIMx_CNT < TIMx_CCR2, otherwise OC2REF is inactive. In down-counting, OC2REF is inactive if TIMx_CNT > TIMx_CCR2, otherwise OC2REF is active.
111: PWM mode 2 - In up-counting, OC2REF is inactive if TIMx_CNT < TIMx_CCR2, otherwise OC2REF is active. In down-counting, OC2REF is active if TIMx_CNT > TIMx_CCR2, otherwise it is inactive.
Note: In PWM mode 1 or 2, the OC2REF level changes only when the result of the comparison changes or when the output compare mode switches from “frozen” mode to “PWM” mode.

Bit 11 OC4PE: Output Compare 4 Preload Enable

0: Buffer register for TIMx_CCR4 is disabled. TIMx_CCR4 can be written at anytime, the new value is used by the shadow register immediately.

1: Buffer register for TIMx_CCR4 is enabled. Read/write operations access the buffer register. TIMx_CCR4 buffer value is loaded in the shadow register at each update event.

Note: The PWM mode can be used without enabling the buffer register only in one pulse mode (OPM bit set in the TIMx_CR2 register), otherwise the behavior is undefined.

Bit 10 OC4FE: Output Compare 4 Fast Enable

This bit speeds the effect of an event on the trigger in input on the OC4 output.

0: OC4 behaves normally depending on the counter and CCR4 values even when the trigger is ON. The minimum delay to activate OC4 when an edge occurs on the trigger input is 5 clock cycles.

1: An active edge on the trigger input acts like a compare match on the OC4 output. OC4 is set to the compare level independently from the result of the comparison. Delay to sample the trigger input and to activate OC4 output is reduced to 3 clock cycles. OC4FE acts only if the channel is configured in PWM 1 or PWM 2 mode.

Bits 9:8 CC4S[1:0]: Capture / Compare 1 Selection

This configures the channel as an output or an input. If an input, it selects the input source.

00: Channel is an output

01: Channel is an input and is mapped to TI4

10: Channel is an input and is mapped to TI3

11: Channel is an input and is mapped to TRGI. This mode requires an internal trigger input selected by the TS bit in the TIMx_SMCR register.

Note: CC2S may be written only when the channel is off (CC2E = 0 in the TIMx_CCER register).

Bit 7 Reserved, must be kept at reset value

Bits 6:4 OC3M[2:0]: Output Compare 1 Mode

See OC4M description above

Bit 3 OC3PE: Output Compare 3 Preload Enable

See OC4PE description above

Bit 2 OC3FE: Output Compare 3 Fast Enable

See OC4FE description above

Bits 1:0 CC3S[1:0]: Capture / Compare 3 Selection

This configures the channel as an output or an input. If an input, it selects the input source.

00: Channel is an output

01: Channel is an input and is mapped to TI3

10: Channel is an input and is mapped to TI4

11: Channel is an input and is mapped to TRGI. This requires an internal trigger input selected by the TS bit in the TIMx_SMCR register.

Note: CC3S may be written only when the channel is off (CC3E = 0 in the TIMx_CCER register).

Input capture mode

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IC4F[3:0]				IC4PSC[1:0]		CC4S[1:0]		IC3F[3:0]				IC3PSC[1:0]		CC3S[1:0]	
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bits 31:16 Reserved, must be kept at reset value

Bits 15:12 IC4F[3:0]: Input Capture 1 Filter

This defines the frequency used to sample the TI4 input, $f_{Sampling}$, and the length of the digital filter applied to TI4. The digital filter requires N consecutive samples in the same state before being output.

0000: $f_{Sampling}$ = PCLK, no filtering
0001: $f_{Sampling}$ = PCLK, N=2
0010: $f_{Sampling}$ = PCLK, N=4
0011: $f_{Sampling}$ = PCLK, N=8
0100: $f_{Sampling}$ = PCLK/2, N=6
0101: $f_{Sampling}$ = PCLK/2, N=8
0110: $f_{Sampling}$ = PCLK/4, N=6
0111: $f_{Sampling}$ = PCLK/4, N=8
1000: $f_{Sampling}$ = PCLK/8, N=6
1001: $f_{Sampling}$ = PCLK/8, N=8
1010: $f_{Sampling}$ = PCLK/16, N=5
1011: $f_{Sampling}$ = PCLK/16, N=6
1100: $f_{Sampling}$ = PCLK/16, N=8.
1101: $f_{Sampling}$ = PCLK/32, N=5
1110: $f_{Sampling}$ = PCLK/32, N=6
1111: $f_{Sampling}$ = PCLK/32, N=8

Note: PCLK is 12 MHz when using the 24 MHz HSE OSC, and 6 MHz using the 12 MHz HSI RC oscillator.

Bits 11:10 IC4PSC[1:0]: Input Capture 1 Prescaler

00: No prescaling, capture each time an edge is detected on the capture input
01: Capture once every 2 events
10: Capture once every 4 events
11: Capture once every 6 events

Bits 9:8 CC4S[1:0]: Capture / Compare 1 Selection

This configures the channel as an output or an input. If an input, it selects the input source.
00: Channel is an output
01: Channel is an input and is mapped to TI4
10: Channel is an input and is mapped to TI3
11: Channel is an input and is mapped to TRGI. This mode requires an internal trigger input selected by the TS bit in the TIMx_SMCR register.

Note: CC2S may be written only when the channel is off (CC2E = 0 in the TIMx_CCER register).

10.3.17 Timer *x* capture/compare 4 register (TIMx_CCR4)

Address offset: 0xE040 (TIM1) and 0xF040 (TIM2)
Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCR[15:0]															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bits 31:16 Reserved, must be kept at reset value

Bits 15:0 See description in the TIMx_CCR1 register

10.3.18 Timer 1 option register (TIM1_OR)

Address offset: 0xE050
Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												OR RSVD	CLK MSKEN	EXTRIGSEL[1:0]	
												rw	rw	rw	rw

Bits 31:4 Reserved, must be kept at reset value

Bit 3 ORRSVD

Reserved: this bit must always be set to 0

Bit 2 CLKMSKEN

Enables TIM1MSK when TIM1CLK is selected as the external trigger: 0 = TIM1MSK not used, 1 = TIM1CLK is ANDed with the TIM1MSK input.

Bits 1:0 EXTRIGSEL[1:0]:

Selects the external trigger used in external clock mode 2: 0 = PCLK, 1 = calibrated 1 kHz clock, 2 = 32 kHz reference clock (if available), 3 = TIM1CLK pin.

Table 59 lists other specifications for the ADC not covered in *Table 56*, *Table 57*, and *Table 58*.

Table 59. ADC characteristics

Parameter	Min.	Typ.	Max.	Units
VREF	1.17	1.2	1.35	V
VREF output current	–	–	1	mA
VREF load capacitance	–	–	10	nF
External VREF voltage range	1.1	1.2	1.3	V
External VREF input impedance	1	–	–	MΩ
Minimum input voltage Input buffer disabled Input buffer enabled	 0 0.1	 – –	 – –	V
Maximum input voltage Input buffer disabled Input buffer enabled	 – –	 – –	 VREF VDD_PADS - 0.1	V
Single-ended signal range Input buffer disabled Input buffer enabled	 0 0.1	 – –	 VREF VDD_PADS – 0.1	V
Differential signal range Input buffer disabled Input buffer enabled	 -VREF -VDD_PADS + 0.1	 – –	 +VREF +VDD_PADS - 0.1	V
Common mode range Input buffer disabled Input buffer enabled	 - 0	 - VDD_PADS/2	 - VREF	V
Input referred ADC offset	-10	–	10	mV
Input Impedance 1 MHz sample clock 6 MHz sample clock Not sampling	 1 0.5 10	 – – –	 – – –	MΩ

Note: The signal-ended ADC measurements are limited in their range and only guaranteed for accuracy within the limits shown in this table. The ADC internal design allows for measurements outside of this range (±200 mV) when the input buffer is disabled, but the accuracy of such measurements is not guaranteed. The maximum input voltage is of more interest to the differential sampling where a differential measurement might be small, but a common mode can push the actual input voltage on one of the signals towards the upper voltage limit.

16 Ordering information scheme

Example: STM32 W 108 C B U 6 x

Device family

STM32 = ARM®-based 32-bit microcontroller

Product type

W = wireless system-on-chip

Sub-family

108 = IEEE 802.15.4 specification

Pin count

H = 40 pins
C = 48 pins

Code size

B = 128 Kbyte of Flash memory

C = 256 Kbyte of Flash memory

Z = 192 Kbyte of Flash memory

Package

U = FQFPN

Temperature range

6 = –40 °C to +85 °C

7 = –40 °C to +105 °C

Enabled protocol stack

"Blank" = Development sample platform (1)

1 = Ember ZigBee stack(2)

3 = RF4CE stack

4 = IEEE 802.15.4 media access control

1. This P/N is under specific ordering conditions. Please refer to your nearest ST sales office.
2. The Ember ZigBee stack is available on 128 Kbyte devices only.