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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	I²C, FlexIO, SPI, UART/USART, USB
Peripherals	DMA, I²S, PWM, WDT
Number of I/O	82
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 24x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mkl28z512vll7

- 32–40 kHz, or 3–32 MHz crystal oscillator
- 1 kHz LPO clock
- 8/2 MHz slow internal reference clock (SIRC)
- Peripheral Clock Control (PCC) module that supports asynchronous clocking and clock divide options for peripherals.

Human-machine interface

- General-purpose input/output up to 97
- Low-power hardware touch sensor interface (TSI)

- Secure Real time clock
- 56-bit software time stamp timer at 1 MHz

Security and integrity modules

- 80-bit unique identification number per chip
- MMCAU supports acceleration of the DES, 3DES, AES, MD5, SHA-1, and SHA-256 algorithms
- True Random Number Generator (TRNG)

Operating Characteristics

- Voltage range: 1.71 to 3.6 V
- Temperature range: –40 to 105 °C

NOTE

The 121-pin packages for this product is not yet available. However, it is included in a Package Your Way program for Kinetis MCUs. Visit nxp.com/KPYW for more details.

Ordering Information [1]

Part Number	Memory		Package		IO and ADC channels		
	Flash (KB)	SRAM (KB)	Pin count	Package	GPIOs	GPIOs (INT/HD)	ADC channels (SE/DP)
MKL28Z512VLL7	512	128	100	LQFP	82	82/8	27/4
MKL28Z512VDC7[2]	512	128	121	XFBGA	97	97/8	27/4

1. To confirm current availability of ordererable part numbers, go to http://www.nxp.com and perform a part number search.
2. Package Your Way.

Related Resources

Type	Description	Resource
Selector Guide	The NXP Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector.	Solution Advisor
Product Brief	The Product Brief contains concise overview/summary information to enable quick evaluation of a device for design suitability.	KL2XPB[1]
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	MKL28ZRM[1]
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	MKL28Z512Vxx7[1]
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.	KINETIS_L_1N52N[1]
Package drawing	Package dimensions are provided in package drawings.	• 121-XFBGA: 98ASA00595D[1] • 100-LQFP: 98ASS23308W[1]

1. To find the associated resource, go to http://www.nxp.com and perform a search using this term.

1.4 Voltage and current operating ratings

Table 4. Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	–0.3	3.8	V
I_{DD}	Digital supply current	—	120	mA
V_{IO}	IO pin input voltage	–0.3	V_{DD} + 0.3	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	–25	25	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.3	V_{DD} + 0.3	V
V_{USB_DP}	USB_DP input voltage	–0.3	3.63	V
V_{USB_DM}	USB_DM input voltage	–0.3	3.63	V
V_{REGIN}	USB regulator input	–0.3	6.0	V

2 General

2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

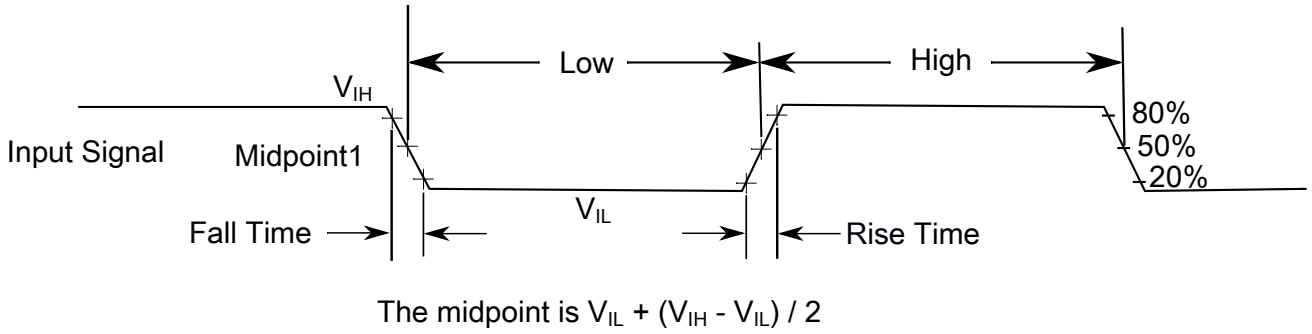


Figure 2. Input signal measurement reference

All digital I/O switching characteristics, unless otherwise specified, assume that the output pins have the following characteristics.

- C_L=30 pF loads
- Slew rate disabled
- Normal drive strength

Table 6. V_{DD} supply LVD, HVD, and POR operating requirements (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{LVDH}	Falling low-voltage detect threshold — high range (LVDV = 01)	2.48	2.56	2.64	V	—
	Low-voltage warning thresholds — high range					1
V_{LVW1H}	• Level 1 falling (LVWV = 00)	2.62	2.70	2.78	V	
V_{LVW2H}	• Level 2 falling (LVWV = 01)	2.72	2.80	2.88	V	
V_{LVW3H}	• Level 3 falling (LVWV = 10)	2.82	2.90	2.98	V	
V_{LVW4H}	• Level 4 falling (LVWV = 11)	2.92	3.00	3.08	V	
V_{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	±60	—	mV	—
V_{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	—
	Low-voltage warning thresholds — low range					1
V_{LVW1L}	• Level 1 falling (LVWV = 00)	1.74	1.80	1.86	V	
V_{LVW2L}	• Level 2 falling (LVWV = 01)	1.84	1.90	1.96	V	
V_{LVW3L}	• Level 3 falling (LVWV = 10)	1.94	2.00	2.06	V	
V_{LVW4L}	• Level 4 falling (LVWV = 11)	2.04	2.10	2.16	V	
V_{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	±40	—	mV	—
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	—
t_{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	µs	—
V_{HVDL}	High voltage detect threshold — low range (HVDV=0) — Rising	3.4	3.5	3.6	V	2
	High voltage detect threshold — low range (HVDV=0) — Falling	3.35	3.45	3.55		
V_{HVDH}	High voltage detect threshold — high range (HVDV=1) — Rising	3.65	3.75	3.85	V	2
	High voltage detect threshold — high range (HVDV=1) — Falling	3.6	3.7	3.8		
V_{HYSH}	High voltage detect hysteresis — low range (HVDV=0)	—	50	—	mV	—
	High voltage detect hysteresis — high range (HVDV=1)	—	50	—		

1. Rising thresholds are falling threshold + hysteresis voltage
2. The selection of high voltage detect trip voltage is controlled by PMC_HVDSC1[HVDV].

2.2.3 Voltage and current operating behaviors

Table 7. Voltage and current operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{OH}	Output high voltage — Normal drive pad • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = –5 mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = –2.5 mA	 V_{DD} – 0.5 V_{DD} – 0.5		 — —	 V V	1
V_{OH}	Output high voltage — High drive pad • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = –20 mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = –10 mA	 V_{DD} – 0.5 V_{DD} – 0.5		 — —	 V V	1
I_{OHT}	Output high current total for all ports	—		100	mA	
V_{OL}	Output low voltage — Normal drive pad • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 5 mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 2.5 mA	 — —		 0.5 0.5	 V V	1
V_{OL}	Output low voltage — High drive pad • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 20 mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 10 mA	 — —		 0.5 0.5	 V V	1
I_{OLT}	Output low current total for all ports	—		100	mA	
I_{IN}	Input leakage current (per pin) for full temperature range	—		1	µA	2
I_{IN}	Input leakage current (per pin) at 25 °C	—		0.025	µA	2
I_{IN}	Input leakage current (total all pins) for full temperature range	—		41	µA	2
I_{OZ}	Hi-Z (off-state) leakage current (per pin)	—		1	µA	
R_{PU}	Internal pullup resistors	20		50	kΩ	3

1. PTB0, PTB1, PTC3, PTC4, PTD4, PTD5, PTD6 and PTD7 I/O have both high drive and normal drive capability selected by the associated PORTx_PCRn[DSE] control bit. All other GPIOs are normal drive only. PTD4, PTD5, PTD6, PTD7, PTE20, PTE21, PTE22, and PTE23 are also fast pins.
2. Measured at V_{DD} = 3.6 V
3. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{SS}

2.2.4 Power mode transition operating behaviors

All specifications in the following table assume this clock configuration in Run mode:

- CPU and system clocks = 48 MHz
- Bus and flash clock = 24 MHz
- SCG configured in FIRC mode; peripheral functional clocks from FIRCDIV3_CLK and USB clock from FIRCDIV1_CLK

xxDIV3, xxDIV2, and xxDIV1 in SCG_SIRCDIV register. PLL, SOSC, and FIRC disabled by clearing SCG_SPLLCSR[SPLLEN], SCG_SOSCCSR[SOSCEN], and SCG_FIRCCSR[FIRCEN].

12. No brownout

Table 10. Low power mode peripheral adders — typical value

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
$I_{EREFSTEN8MHz}$	External 8 MHz crystal clock adder with System OSC. Measured by entering VLPS mode with the crystal enabled (SCG_SOSCCFG[RANGE] = 10, SCG_SOSCCFG[HGO] = 0, SCG_SOSCCFG[EREFS] = 1, and SC2P/SC4P/SC8P = 0).	402.9	462.1	477.5	492	506.2	530.4	uA
$I_{EREFSTEN32KHz}$	External 32 kHz crystal clock adder with System OSC by means of SCG_SOSCCFG[RANGE] = 01, SCG_SOSCCFG[HGO] = 0, SCG_SOSCCFG[EREFS] = 1, and SC2P/SC4P/SC8P = 0. Measured by entering all the following modes with the crystal enabled:							nA
	• VLLS1	373.9	539.2	612.3	644.9	523.7	1000	
	• VLLS3	568.4	552.6	650.8	757.9	995.6	1400	
	• LLS3	582.8	565.0	615.5	797.1	968.5	1700	
	• VLPS	472.4	635.2	776.9	425.6	1500	2800	
	• STOP	528.0	534.1	636.6	9600	20300	40900	
I_{LPTMR}	LPTMR peripheral adder measured by placing the device in VLLS1 mode with LPTMR enabled using LPO clock.	151.0	7.7	21.8	7.6	174.0	31.0	nA
I_{CMP}	CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.	18.8	19.6	19.9	20.0	20.4	20.5	µA
I_{RTC}	RTC peripheral adder measured by placing the device in VLLS1 mode and the RTC ALARM set for 1 minute. Includes selected clock source power consumption.							
	• OSC32KCLK (32KHz external crystal)	116.0	1400	1400	1500	1500	120.0	nA
	• LPO (internal 1K Hz Low Power Oscillator)	35.0	1400	1400	1600	1400	120.0	
I_{LPUART}	LPUART peripheral adder measured by placing the device in STOP mode with selected clock source waiting for RX data at 115200 baud rate. Includes							

Table continues on the next page...

Table 10. Low power mode peripheral adders — typical value (continued)

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
I_{WDOG}	WDOG peripheral adder measured by placing the device in STOP mode, WDOG is configured to time out at 1 second. Includes selected clock source power consumption. • Slow IRC clock from SCG (8 MHz internal reference clock) • OSCERCLK (8 MHz external crystal) • LPO (internal 1 kHz Lower Power Oscillator)	68.8 11.2 56.0	68.5 10.1 57.1	69.2 10.1 58.6	69.9 10.2 58.5	71.7 10.5 58.6	72.6 10.7 60.0	µA
I_{SIRC_8MHz}	SIRC adder when SIRC is configured to 8 MHz. Measured by entering VLPS mode with 8 MHz IRC enabled, and SIRCDIV1, SIRCDIV2, SIRCDIV3 =000.	67.2	63.0	63.3	63.2	63.3	63.6	µA
I_{SIRC_2MHz}	SIRC adder when SIRC is configured to 2 MHz. Measured by entering STOP or VLPS mode with 2 MHz IRC enabled, and SIRCDIV1, SIRCDIV2, SIRCDIV3 =000.	22.3	21.2	21.4	21.5	21.7	21.4	µA

2.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- SCG is configured as SPLL mode with SOSC as the clock source for RUN mode current measurement, and as SIRC mode for VLPR mode current measurement
- USB regulator disabled
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA
- For the ALLON curve, all peripheral clocks are enabled as specified in notes of Power consumption operating behaviors.

Table 20. System PLL Specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
J_{acc_pll}	PLL accumilated jitter over 1 µs (RMS) • f_{vco} = 180 MHz • f_{vco} = 288 MHz	 — —	 600 300	 — —	 ps	2
D_{unl}	Lock exit frequency tolerance	±4.47	—	±5.97	%	
t_{pll_lock}	Lock detector detection time	—	—	150×10^{-6} + 1075(1/ f_{pll_ref})	s	3

1. Excludes any oscillator currents that are also consuming power while PLL is in operation.
2. This specification was obtained using a Freescale developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
3. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled to PLL enabled. If a crystal/resonator is being used as the reference, this specification assumes it is already running.

3.3.2 Oscillator electrical specifications

3.3.2.1 Oscillator DC electrical specifications

Table 21. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	
I_{DDOSC}	Supply current — low-power mode (HGO=0)					1
	• 32 kHz	—	500	—	nA	
	• 4 MHz	—	200	—	µA	
	• 8 MHz (RANGE=01)	—	300	—	µA	
	• 16 MHz	—	950	—	µA	
	• 24 MHz	—	1.2	—	mA	
	• 32 MHz	—	1.5	—	mA	
I_{DDOSC}	Supply current — high gain mode (HGO=1)					1
	• 32 kHz	—	25	—	µA	
	• 4 MHz	—	400	—	µA	
	• 8 MHz (RANGE=01)	—	500	—	µA	
	• 16 MHz	—	2.5	—	mA	
	• 24 MHz	—	3	—	mA	
	• 32 MHz	—	4	—	mA	

Table continues on the next page...

3.3.2.2 Oscillator frequency specifications

Table 22. Oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal or resonator frequency — low-frequency range (SCG_SOSCCFG[RANGE]=01)	32	—	40	kHz	
$f_{osc\_hi\_1}$	Oscillator crystal or resonator frequency — medium frequency range (SCG_SOSCCFG[RANGE]=10)	1	—	8	MHz	
$f_{osc\_hi\_2}$	Oscillator crystal or resonator frequency — high frequency range (SCG_SOSCCFG[RANGE]=11)	8	—	32	MHz	
f_{ec_extal}	Input clock frequency (external clock mode)	—	—	48	MHz	1, 2
t_{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t_{cst}	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—	750	—	ms	3, 4, 5
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	—	250	—	ms	
	Crystal startup time — 8 MHz medium frequency (SCG_SOSCCFG[RANGE]=11), low-power mode (HGO=0)	—	0.6	—	ms	
	Crystal startup time — 8 MHz medium frequency (SCG_SOSCCFG[RANGE]=10), high-gain mode (HGO=1)	—	1	—	ms	

1. Other frequency limits may apply when external clock is being used as a reference for the PLL.
2. When transitioning to system PLL mode, restrict the frequency of the input clock so that, when it is divided by PREDIV, it remains within the limits of the PLL reference input clock frequency.
3. Proper PC board layout procedures must be followed to achieve specifications.
4. Crystal startup time is defined as the time between the oscillator being enabled and the SCG_SOSCCSR[SOSCVLD] being set.
5. Crystal startup time is dependent on external crystal and/or resonator and loading capacitance as well as series resistance.

3.4 Memories and memory interfaces

3.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

3.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

3.4.1.4 Reliability specifications

Table 26. NVM reliability specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
Program Flash						
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	—
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	—
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	2

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at –40 °C ≤ T_j ≤ 125 °C.

3.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

3.6 Analog

3.6.1 ADC electrical specifications

3.6.1.1 16-bit ADC operating conditions

Table 27. 16-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
V_{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	—
ΔV_{DDA}	Supply voltage	Delta to V_{DD} (V_{DD} – V_{DDA})	-100	0	+100	mV	2
ΔV_{SSA}	Ground voltage	Delta to V_{SS} (V_{SS} – V_{SSA})	-100	0	+100	mV	2
V_{ADIN}	Input voltage	• 16-bit differential mode • All other modes	VREFL VREFL	— —	31/32 × VREFH VREFH	V	—
C_{ADIN}	Input capacitance	• 16-bit mode • 8-bit / 10-bit / 12-bit modes	— —	8 4	10 5	pF	—
R_{ADIN}	Input series resistance		—	2	5	kΩ	—
R_{AS}	Analog source resistance	16-bit modes • f_{ADCK} > 8 MHz	— —	— —	 0.5	 kΩ	3, 4

Table continues on the next page...

4. 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
6. Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
7. Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.
8. ADC conversion clock < 3 MHz

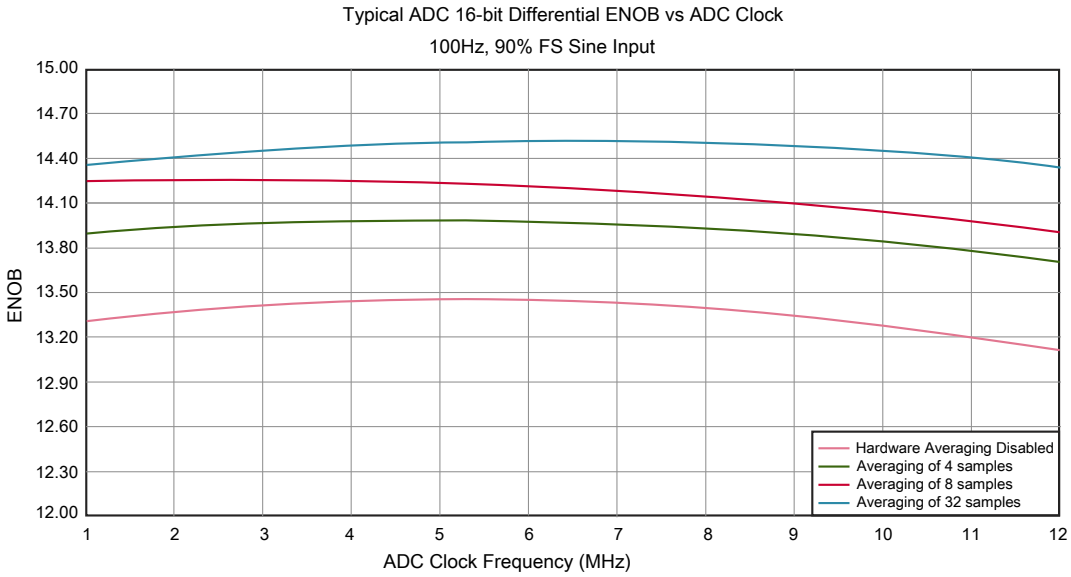


Figure 8. Typical ENOB vs. ADC_CLK for 16-bit differential mode

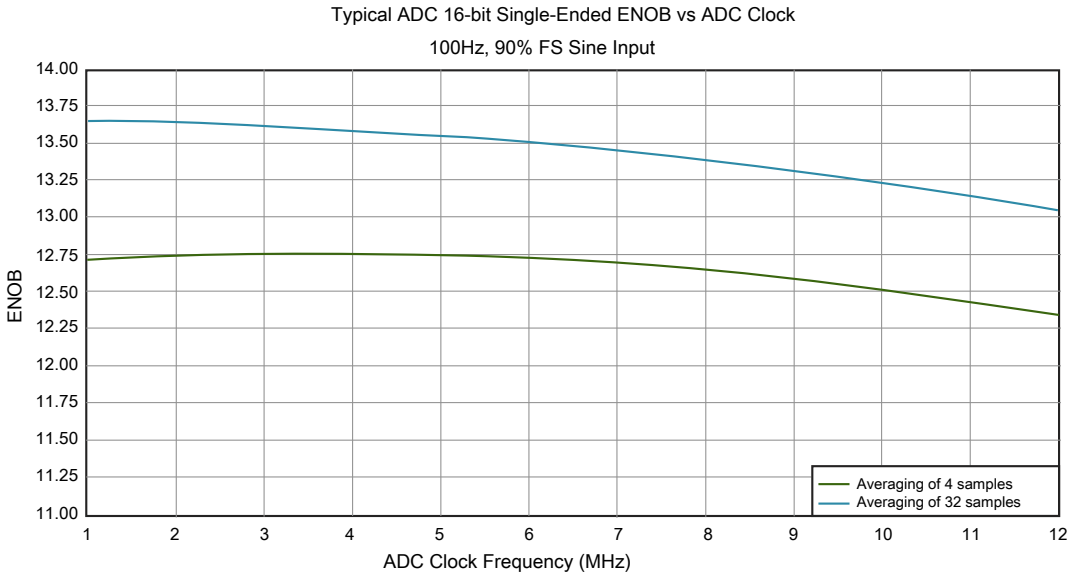


Figure 9. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode

3.6.2 Voltage reference electrical specifications

3.6.4.2 12-bit DAC operating behaviors

Table 35. 12-bit DAC operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA_DACLP}	Supply current — low-power mode	—	—	250	μA	
I_{DDA_DACHP}	Supply current — high-speed mode	—	—	900	μA	
t_{DACLP}	Full-scale settling time (0x080 to 0xF7F) — low-power mode	—	100	200	μs	1
t_{DACHP}	Full-scale settling time (0x080 to 0xF7F) — high-power mode	—	15	30	μs	1
$t_{CCDACLP}$	Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode	—	0.7	1	μs	1
$V_{dacoutl}$	DAC output voltage range low — high-speed mode, no load, DAC set to 0x000	—	—	100	mV	
$V_{dacouth}$	DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFF	V_{DACR} −100	—	V_{DACR}	mV	
INL	Integral non-linearity error — high speed mode	—	—	±8	LSB	2
DNL	Differential non-linearity error — V_{DACR} > 2 V	—	—	±1	LSB	3
DNL	Differential non-linearity error — V_{DACR} = VREF_OUT	—	—	±1	LSB	4
V_{OFFSET}	Offset error	—	±0.4	±0.8	%FSR	5
E_G	Gain error	—	±0.1	±0.6	%FSR	5
PSRR	Power supply rejection ratio, V_{DDA} ≥ 2.4 V	60	—	90	dB	
T_{CO}	Temperature coefficient offset voltage	—	3.7	—	μV/C	6
T_{GE}	Temperature coefficient gain error	—	0.000421	—	%FSR/C	
Rop	Output resistance (load = 3 kΩ)	—	—	250	Ω	
SR	Slew rate -80h→ F7Fh→ 80h • High power (SP_{HP}) • Low power (SP_{LP})	 1.2 0.05	 1.7 0.12	 — —	V/μs	
BW	3dB bandwidth • High power (SP_{HP}) • Low power (SP_{LP})	 550 40	 — —	 — —	kHz	

1. Settling within ±1 LSB
2. The INL is measured for 0 + 100 mV to V_{DACR} −100 mV
3. The DNL is measured for 0 + 100 mV to V_{DACR} −100 mV
4. The DNL is measured for 0 + 100 mV to V_{DACR} −100 mV with V_{DDA} > 2.4 V
5. Calculated by a best fit curve from V_{SS} + 100 mV to V_{DACR} − 100 mV
6. V_{DDA} = 3.0 V, reference select set for V_{DDA} (DACx_CO:DACRFS = 1), high power mode (DACx_C0:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device

The interface is designed to be used with synchronous Smart cards, meaning the EMV SIM module provides the clock used by the Smart card. The clock frequency is typically 372 times the Tx/Rx data rate; however, the EMV SIM module can also work with CLK frequencies of 16 times the Tx/Rx data rate.

There is no timing relationship between the clock and the data. The clock that the EMV SIM module provides to the Smart card is used by the Smart card to recover the clock from the data in the same manner as standard UART data exchanges. All five signals of the EMV SIM module are asynchronous with each other.

There are no required timing relationships between signals in normal mode. The smart card is initiated by the interface device; the Smart card responds with Answer to Reset. Although the EMV SIM interface has no defined requirements, the ISO/IEC 7816 defines reset and power-down sequences (for detailed information see ISO/IEC 7816).

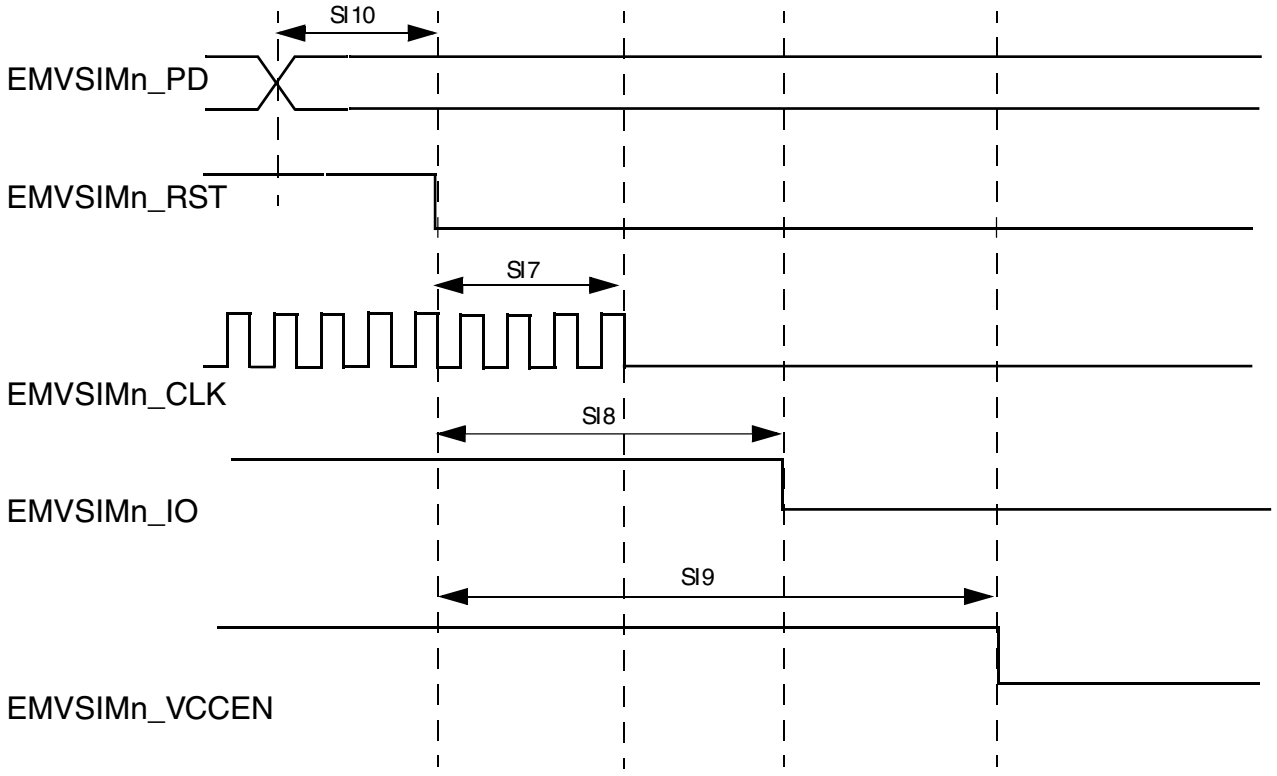
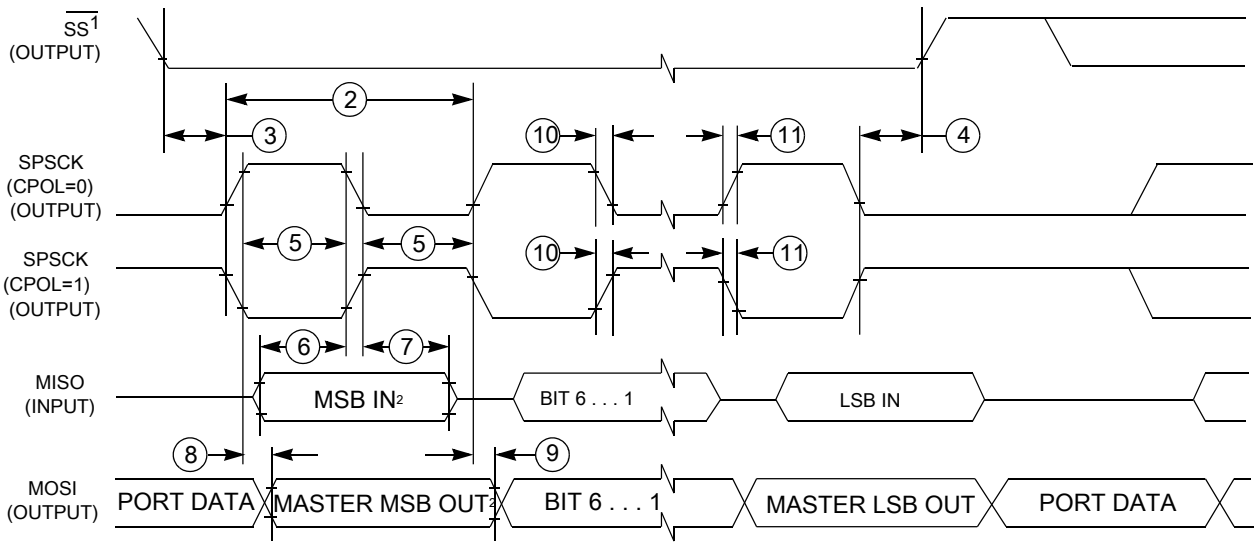


Figure 14. EMV SIM Clock Timing Diagram



1.If configured as output

2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 19. LPSPI master mode timing (CPHA = 1)

Table 43. LPSPI slave mode timing on slew rate disabled pads

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	0	$f_{periph}/4$	Hz	1
2	t_{SPSCK}	SPSCK period	4 x t_{periph}	—	ns	2
3	t_{Lead}	Enable lead time	1	—	t_{periph}	—
4	t_{Lag}	Enable lag time	1	—	t_{periph}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{periph} - 30	—	ns	—
6	t_{SU}	Data setup time (inputs)	2.5	—	ns	—
7	t_{HI}	Data hold time (inputs)	3.5	—	ns	—
8	t_a	Slave access time	—	t_{periph}	ns	3
9	t_{dis}	Slave MISO disable time	—	t_{periph}	ns	4
10	t_v	Data valid (after SPSCK edge)	—	31	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—
12	t_{RI}	Rise time input	—	t_{periph} - 25	ns	—
	t_{FI}	Fall time input				
13	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				

1. f_{periph} is the LPSPI peripheral functional clock
2. $t_{periph} = 1/f_{periph}$
3. Time to data active from high-impedance state
4. Hold time to high-impedance state

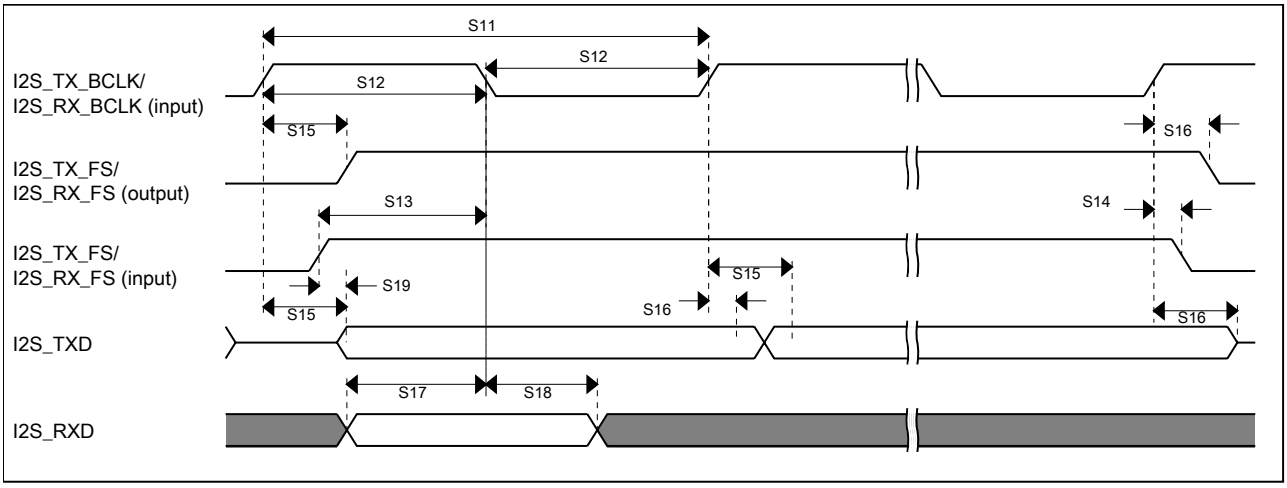


Figure 23. I2S/SAI timing — slave modes

3.8.7.2 VLPR, VLPW, and VLPS mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in VLPR, VLPW, and VLPS modes.

Table 48. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	62.5	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	250	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	45	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid		—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	45	ns
S8	I2S_TX_BCLK to I2S_TXD invalid		—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK		—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

6.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to **nxp.com** and perform a part number search for the following device numbers: PKL28Z and MKL28Z

7 Design considerations

7.1 Hardware design considerations

This device contains protective circuitry to guard against damage due to high static voltage or electric fields. However, take normal precautions to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit.

7.1.1 Printed circuit board recommendations

- Place connectors or cables on one edge of the board and do not place digital circuits between connectors.
- Drivers and filters for I/O functions must be placed as close to the connectors as possible. Connect TVS devices at the connector to a good ground. Connect filter capacitors at the connector to a good ground.
- Physically isolate analog circuits from digital circuits if possible.
- Place input filter capacitors as close to the MCU as possible.
- For best EMC performance, route signals as transmission lines; use a ground plane directly under LQFP/MAPBGA packages.

7.1.2 Power delivery system

Consider the following items in the power delivery system:

- Use a plane for ground.
- Use a plane for MCU VDD supply if possible.
- Always route ground first, as a plane or continuous surface, and never as sequential segments.
- Route power next, as a plane or traces that are parallel to ground traces.
- Place bulk capacitance, 10 µF or more, at the entrance of the power plane.
- Place bypass capacitors for MCU power domain as close as possible to each VDD/VSS pair, including VDDA/VSSA and VREFH/VREFL.

- The minimum bypass requirement is to place 0.1 µF capacitors positioned as near as possible to the package supply pins.
- The VREG_IN voltage range is 2.7 V to 5.5 V. Typically, 5.0V is applied here. If USB module is used, this pin must be powered to make the USB transceiver also powered. It is recommended to include a filter circuit with one bulk capacitor (no less than 2.2 µF) and one 0.1 µF capacitor to VREG_IN at this pin to improve USB performance. Total capacitors on VBUS should be less than 10 µF.
- Take special care to minimize noise levels on the VREFH/VREFL inputs. An option is to use the internal reference voltage (output 1.2 V or 2.1 V typically) as the ADC reference.

NOTE

The internal reference voltage output (VREF_OUT) is bonded to the VREFH pin. When the VREF_OUT output is used, a 0.1 µF capacitor is required as a filter. Do not connect any other supply voltage to the pin that has VREF_OUT activated.

7.1.3 Analog design

Each ADC input must have an RC filter as shown in the following figure. The maximum value of R must be smaller than RAS max if high resolution is required. The value of C must be chosen to ensure that the RC time constant is very small compared to the sample period. See AN4373: Cookbook for SAR ADC Measurements for how to select proper RC values.

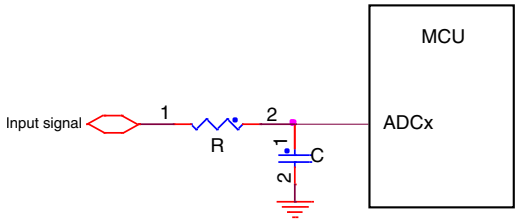


Figure 28. RC circuit for ADC input

High voltage measurement circuits require voltage division, current limiting, and overvoltage protection as shown the following figure. The voltage divider formed by R1 – R4 must yield a voltage less than or equal to VREFH. Typically, VREFH is connected to VDDA. The current must be limited to less than the negative injection current limit. Since the ADC pins do not have diodes to VDD, external clamp diodes must be included to protect against transient over-voltages.

The RESET_b pin is an open-drain I/O pin that has an internal pullup resistor. An external RC circuit is recommended to filter noise as shown in the following figure. The resistor value must be in the range of 4.7 kΩ to 10 kΩ; the recommended capacitance value is 0.1 µF. The RESET_b pin also has a selectable digital filter to reject spurious noise.

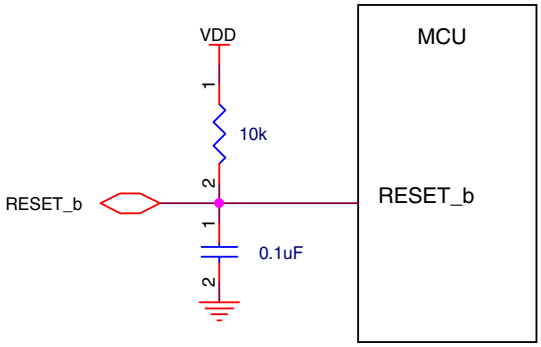


Figure 30. Reset circuit

When an external supervisor chip is connected to the RESET_b pin, a series resistor must be used to avoid damaging the supervisor chip or the RESET_b pin, as shown in the following figure. The series resistor value (RS below) must be in the range of 100 Ω to 1 kΩ depending on the external reset chip drive strength. The supervisor chip must have an active high, open-drain output.

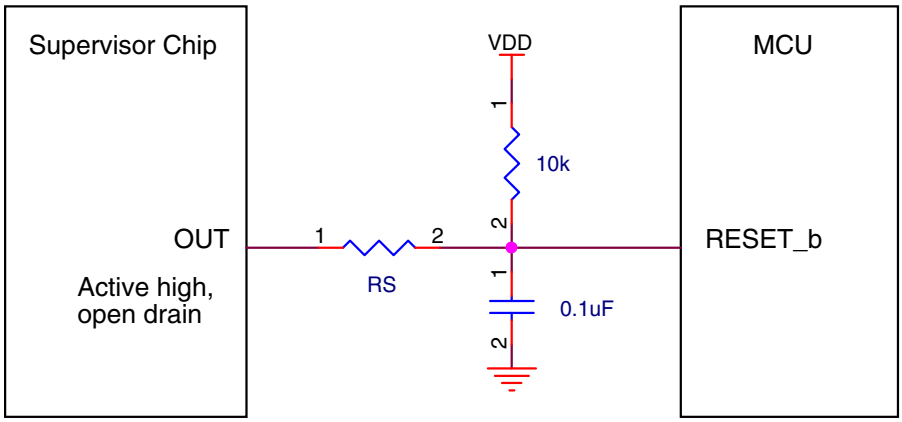


Figure 31. Reset signal connection to external reset chip

- NMI pin

Connect the pull up resistor to VDD_MCU for the pins like RESET and NMI. For other pull up resistor, do not use VDD_MCU.

7.1.5 Crystal oscillator

When using an external crystal or ceramic resonator as the frequency reference for the MCU clock system, refer to the following table and diagrams.

The feedback resistor, RF, is incorporated internally with the low power oscillators. An external feedback is required when using high gain (HGO=1) mode. In harsh EMC environment, it is recommended to use high gain mode. For low frequency (32 to 40 kHz), switching between high gain and low power is not supported.

The series resistor, RS, is used to limit current to external crystal or resonator to avoid overdrive, and is required in high gain (HGO=1) mode when the crystal or resonator frequency is below 2 MHz. The low power oscillator (HGO=0) must not have any series resistor RS.

Internal load capacitors (Cx, Cy) are provided in the low frequency (32.786kHz) mode. Use the SCxP bits in the SCG_SOSCCFG register to adjust the load capacitance for the crystal. Typically, values of 10 pf to 16 pF are sufficient for 32.768 kHz crystals that have a 12.5 pF CL specification. The internal load capacitor selection must not be used for high frequency crystals and resonators. See crystal or resonator manufacturer's recommendation for parameters about load capacitance and RF.

Table 51. External crystal/resonator connections

Oscillator mode	Diagram
Low frequency (32 kHz-40 kHz), low power	Diagram 1
Low frequency (32 kHz-40 kHz), high gain	Diagram 2, Diagram 4
High/Medium frequency (1-32 MHz), low power	Diagram 3
High/Medium frequency (1-32MHz), high gain	Diagram 4

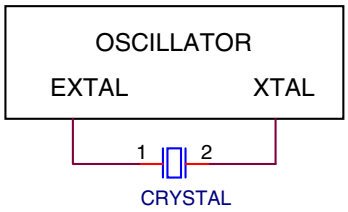


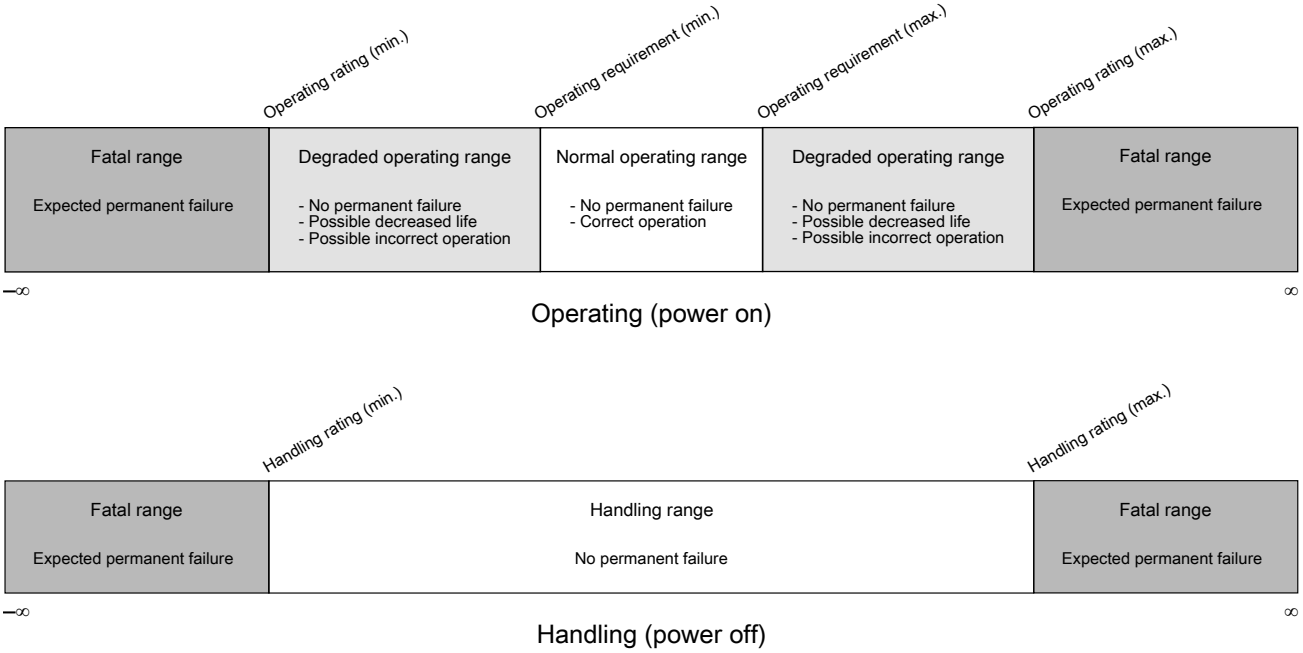
Figure 35. Crystal connection – Diagram 1

9.3 Typical-value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	Supply voltage	3.3	V

9.4 Relationship between ratings and operating requirements



9.5 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

10 Revision History

The following table provides a revision history for this document.

Table 53. Revision History

Rev. No.	Date	Substantial Changes
0	08/2015	Initial release

1	10/2015	• Removed "Ready Play module (RPM)" from the features list
		• Added "96 MHz high speed mode" to the features list under "Core"
		• Updated the values in the following sections:
		  • Voltage and current operating requirements
		  • Power mode transition operating behaviors
		  • EMC radiated emissions operating behaviors
		  • General switching specifications
		  • Oscillator frequency specifications
		  • 16-bit ADC operating conditions
		  • LPSPI switching specifications
		  • LPI2C specifications
		• Created new table for topic "Power consumption operating behaviors"
		• Updated the pinouts
		• Updated the "Terminology and guidelines" section to a new format

2	04/2016	• Removed 64-pin package information and marked 121-pin package information as "Package Your Way"
		• Updated the values in Power mode transition operating behaviors
		• Updated values and resolved TBDs in Power consumption operating behaviors
		• In section Diagram: Typical IDD_RUN operating behavior :
		  • Added "For the ALLON curve, all peripheral clocks are enabled as specified in notes of Table 9."
		  • Updated figures
		• Updated table in Slow IRC (SIRC) specifications
		• Removed section "Specification Test Methods"
		• In table VREF full-range operating behaviors, removed the user trim values and updated the factory trim values

2.1	06/2016	• In table Table 10 Low power mode peripheral adders — typical value, removed I_{USB_Alive}