# Infineon Technologies - CY8C3665AXI-010 Datasheet

**Welcome to E-XFL.COM**

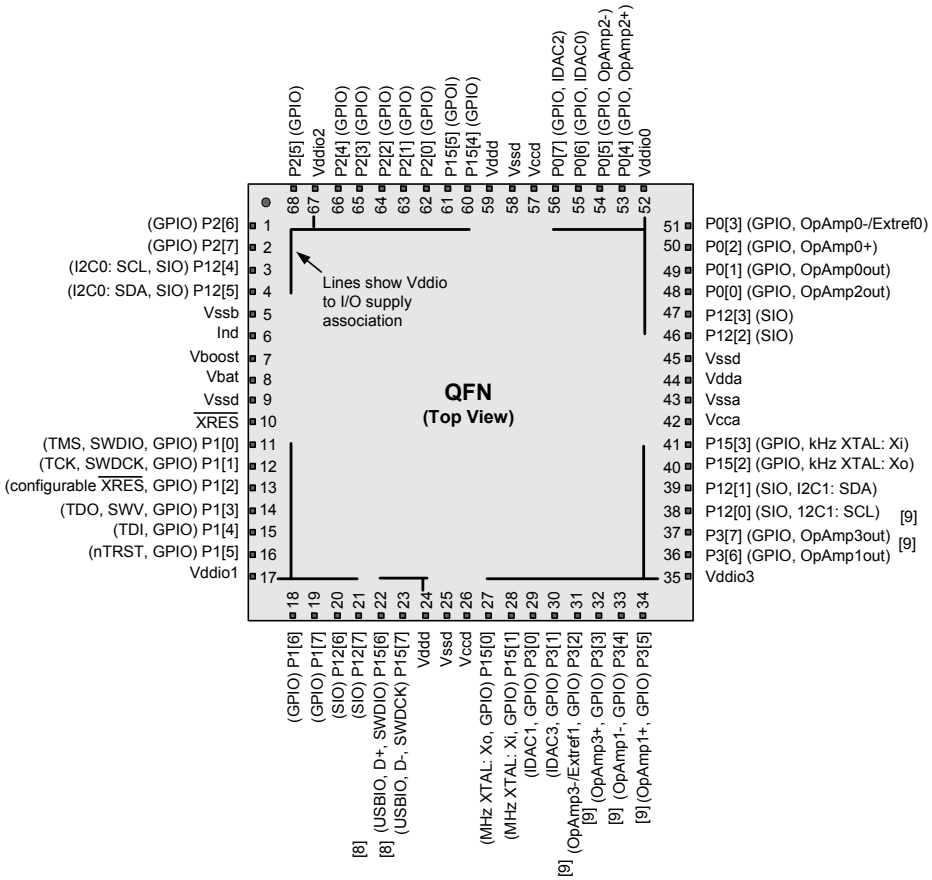
## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | 8051 |
| Core Size | 8-Bit |
| Speed | 67MHz |
| Connectivity | EBI/EMI, I²C, LINbus, SPI, UART/USART |
| Peripherals | CapSense, DMA, POR, PWM, WDT |
| Number of I/O | 62 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 1K x 8 |
| RAM Size | 4K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.71V ~ 5.5V |
| Data Converters | A/D 16x12b; D/A 4x8b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP |
| Supplier Device Package | 100-TQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3665axi-010 |

**Figure 2-3. 68-pin QFN Part Pinout**[10]




**Notes**
8. Pins are Do Not Use (DNU) on devices without USB. The pin must be left floating.
9. This feature on select devices only. See Ordering Information on page 99 for details.
10. The center pad on the QFN package should be connected to digital ground (Vssd) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floated and not connected to any other signal.

**Table 4-2. Logical Instructions** *(continued)*

| Mnemonic | Description | Bytes | Cycles |
|---|---|---|---|
| ORL A,#data | OR immediate data to accumulator | 2 | 2 |
| ORL Direct, A | OR accumulator to direct byte | 2 | 3 |
| ORL Direct, #data | OR immediate data to direct byte | 3 | 3 |
| XRL A,Rn | XOR register to accumulator | 1 | 1 |
| XRL A,Direct | XOR direct byte to accumulator | 2 | 2 |
| XRL A,@Ri | XOR indirect RAM to accumulator | 1 | 2 |
| XRL A,#data | XOR immediate data to accumulator | 2 | 2 |
| XRL Direct, A | XOR accumulator to direct byte | 2 | 3 |
| XRL Direct, #data | XOR immediate data to direct byte | 3 | 3 |
| CLR A | Clear accumulator | 1 | 1 |
| CPL A | Complement accumulator | 1 | 1 |
| RL A | Rotate accumulator left | 1 | 1 |
| RLC A | Rotate accumulator left through carry | 1 | 1 |
| RR A | Rotate accumulator right | 1 | 1 |
| RRC A | Rotate accumulator right though carry | 1 | 1 |
| SWAP A | Swap nibbles within accumulator | 1 | 1 |

#### *4.3.1.3 Data Transfer Instructions*

The data transfer instructions are of three types: the core RAM, xdata RAM, and the lookup tables. The core RAM transfer includes transfer between any two core RAM locations or SFRs. These instructions can use direct, indirect, register, and immediate addressing. The xdata RAM transfer includes only the transfer between the accumulator and the xdata RAM location. It can use only indirect addressing. The lookup tables involve nothing but the read of program memory using the Indexed addressing mode. Table 4-3 lists the various data transfer instructions available.

#### *4.3.1.4 Boolean Instructions*

The 8051 core has a separate bit-addressable memory location. It has 128 bits of bit addressable RAM and a set of SFRs that are bit addressable. The instruction set includes the whole menu of bit operations such as move, set, clear, toggle, OR, and AND instructions and the conditional jump instructions. Table 4-4 on page 14 lists the available Boolean instructions.

**Table 4-3. Data Transfer Instructions**

| Mnemonic | Description | Bytes | Cycles |
|---|---|---|---|
| MOV A,Rn | Move register to accumulator | 1 | 1 |
| MOV A,Direct | Move direct byte to accumulator | 2 | 2 |
| MOV A,@Ri | Move indirect RAM to accumulator | 1 | 2 |
| MOV A,#data | Move immediate data to accumulator | 2 | 2 |
| MOV Rn,A | Move accumulator to register | 1 | 1 |
| MOV Rn,Direct | Move direct byte to register | 2 | 3 |
| MOV Rn, #data | Move immediate data to register | 2 | 2 |
| MOV Direct, A | Move accumulator to direct byte | 2 | 2 |
| MOV Direct, Rn | Move register to direct byte | 2 | 2 |
| MOV Direct, Direct | Move direct byte to direct byte | 3 | 3 |
| MOV Direct, @Ri | Move indirect RAM to direct byte | 2 | 3 |
| MOV Direct, #data | Move immediate data to direct byte | 3 | 3 |
| MOV @Ri, A | Move accumulator to indirect RAM | 1 | 2 |

## 4.5 Interrupt Controller

The interrupt controller provides a mechanism for hardware resources to change program execution to a new address, independent of the current task being executed by the main code. The interrupt controller provides enhanced features not found on original 8051 interrupt controllers:

- Thirty-two interrupt vectors
- Jumps directly to ISR anywhere in code space with dynamic vector addresses
- Multiple sources for each vector
- Flexible interrupt to vector matching
- Each interrupt vector is independently enabled or disabled
- Each interrupt can be dynamically assigned one of eight priorities
- Eight level nestable interrupts
- Multiple I/O interrupt vectors
- Software can send interrupts
- Software can clear pending interrupts

When an interrupt is pending, the current instruction is completed and the program counter is pushed onto the stack. Code execution then jumps to the program address provided by the vector. After the ISR is completed, a RETI instruction is executed and returns execution to the instruction following the previously interrupted instruction. To do this the RETI instruction pops the program counter from the stack.

If the same priority level is assigned to two or more interrupts, the interrupt with the lower vector number is executed first. Each interrupt vector may choose from three interrupt sources: Fixed Function, DMA, and UDB. The fixed function interrupts are direct connections to the most common interrupt sources and provide the lowest resource cost connection. The DMA interrupt sources provide direct connections to the two DMA interrupt sources provided per DMA channel. The third interrupt source for vectors is from the UDB digital routing array. This allows any digital signal available to the UDB array to be used as an interrupt source. Fixed function interrupts and all interrupt sources may be routed to any interrupt vector using the UDB interrupt source connections.

**Table 4-8. Interrupt Vector Table**

| # | Fixed Function | DMA | UDB |
|---|---|---|---|
| 0 | LVD | phub_termout0[0] | udb_intr[0] |
| 1 | ECC | phub_termout0[1] | udb_intr[1] |
| 2 | Reserved | phub_termout0[2] | udb_intr[2] |
| 3 | Sleep (Pwr Mgr) | phub_termout0[3] | udb_intr[3] |
| 4 | PICU[0] | phub_termout0[4] | udb_intr[4] |
| 5 | PICU[1] | phub_termout0[5] | udb_intr[5] |
| 6 | PICU[2] | phub_termout0[6] | udb_intr[6] |
| 7 | PICU[3] | phub_termout0[7] | udb_intr[7] |
| 8 | PICU[4] | phub_termout0[8] | udb_intr[8] |
| 9 | PICU[5] | phub_termout0[9] | udb_intr[9] |
| 10 | PICU[6] | phub_termout0[10] | udb_intr[10] |
| 11 | PICU[12] | phub_termout0[11] | udb_intr[11] |
| 12 | PICU[15] | phub_termout0[12] | udb_intr[12] |
| 13 | Comparators Combined | phub_termout0[13] | udb_intr[13] |
| 14 | Switched Caps Combined | phub_termout0[14] | udb_intr[14] |
| 15 | $I^2C$ | phub_termout0[15] | udb_intr[15] |
| 16 | CAN | phub_termout1[0] | udb_intr[16] |
| 17 | Timer/Counter0 | phub_termout1[1] | udb_intr[17] |
| 18 | Timer/Counter1 | phub_termout1[2] | udb_intr[18] |
| 19 | Timer/Counter2 | phub_termout1[3] | udb_intr[19] |
| 20 | Timer/Counter3 | phub_termout1[4] | udb_intr[20] |
| 21 | USB SOF Int | phub_termout1[5] | udb_intr[21] |
| 22 | USB Arb Int | phub_termout1[6] | udb_intr[22] |
| 23 | USB Bus Int | phub_termout1[7] | udb_intr[23] |
| 24 | USB Endpoint[0] | phub_termout1[8] | udb_intr[24] |
| 25 | USB Endpoint Data | phub_termout1[9] | udb_intr[25] |
| 26 | Reserved | phub_termout1[10] | udb_intr[26] |
| 27 | Reserved | phub_termout1[11] | udb_intr[27] |
| 28 | DFB Int | phub_termout1[12] | udb_intr[28] |
| 29 | Decimator Int | phub_termout1[13] | udb_intr[29] |
| 30 | PHUB Error Int | phub_termout1[14] | udb_intr[30] |
| 31 | EEPROM Fault Int | phub_termout1[15] | udb_intr[31] |

# 5. Memory

## 5.1 Static RAM

CY8C36 Static RAM (SRAM) is used for temporary data storage. Up to 8 KB of SRAM is provided and can be accessed by the 8051 or the DMA controller. See Memory Map on page 19. Simultaneous access of SRAM by the 8051 and the DMA controller is possible if different 4-KB blocks are accessed.

## 5.2 Flash Program Memory

Flash memory in PSoC devices provides nonvolatile storage for user firmware, user configuration data, bulk data storage, and optional ECC data. The main flash memory area contains up to 64 KB of user program space.

Up to an additional 8 KB of flash space is available for ECC. If ECC is not used this space can store device configuration data and bulk user data. User code may not be run out of the ECC flash memory section. ECC can correct one bit error and detect two bit errors per 8 bytes of firmware memory; an interrupt can be generated when an error is detected.

Flash is read in units of rows; each row is 9 bytes wide with 8 bytes of data and 1 byte of ECC data. When a row is read, the data bytes are copied into an 8-byte instruction buffer. The CPU fetches its instructions from this buffer, for improved CPU performance.

Flash programming is performed through a special interface and preempts code execution out of flash. The flash programming interface performs flash erasing, programming and setting code protection levels. Flash in-system serial programming (ISSP), typically used for production programming, is possible through both the SWD and JTAG interfaces. In-system programming, typically used for bootloaders, is also possible using serial interfaces such as $I^2C$, USB, UART, and SPI, or any communications protocol.

## 5.3 Flash Security

All PSoC devices include a flexible flash-protection model that prevents access and visibility to on-chip flash memory. This prevents duplication or reverse engineering of proprietary code. Flash memory is organized in blocks, where each block contains 256 bytes of program or data and 32 bytes of ECC or configuration data. A total of up to 256 blocks is provided on 64-KB flash devices.

The device offers the ability to assign one of four protection levels to each row of flash. Table 5-1 lists the protection modes available. Flash protection levels can only be changed by performing a complete flash erase. The Full Protection and Field Upgrade settings disable external access (through a debugging tool such as PSoC Creator, for example). If your application requires code update through a boot loader, then use the Field Upgrade setting. Use the Unprotected setting only when no security is needed in your application. The PSoC device also offers an advanced security feature called Device Security which permanently disables all test, programming, and debug ports, protecting your application from external access (see Device Security on page 56). For more information about how to take full advantage of the security features in PSoC, see the PSoC 3 TRM.

**Table 5-1. Flash Protection**

| Protection Setting | Allowed | Not Allowed |
|---|---|---|
| Unprotected | External read and write + internal read and write | – |
| Factory Upgrade | External write + internal read and write | External read |
| Field Upgrade | Internal read and write | External read and write |
| Full Protection | Internal read | External read and write + internal write |

**Disclaimer**

Note the following details of the flash code protection features on Cypress devices.

Cypress products meet the specifications contained in their particular Cypress datasheets. Cypress believes that its family of products is one of the most secure families of its kind on the market today, regardless of how they are used. There may be methods, unknown to Cypress, that can breach the code protection features. Any of these methods, to our knowledge, would be dishonest and possibly illegal. Neither Cypress nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

Cypress is willing to work with the customer who is concerned about the integrity of their code. Code protection is constantly evolving. We at Cypress are committed to continuously improving the code protection features of our products.

## 5.4 EEPROM

PSoC EEPROM memory is a byte-addressable nonvolatile memory. The CY8C36 has up to 2 KB of EEPROM memory to store user data. Reads from EEPROM are random access at the byte level. Reads are done directly; writes are done by sending write commands to an EEPROM programming interface. CPU code execution can continue from flash during EEPROM writes. EEPROM is erasable and writeable at the row level. The EEPROM is divided into 128 rows of 16 bytes each.

The CPU can not execute out of EEPROM. There is no ECC hardware associated with EEPROM. If ECC is required it must be handled in firmware.

## 5.5 External Memory Interface

CY8C36 provides an external memory interface (EMIF) for connecting to external memory devices. The connection allows read and write accesses to external memories. The EMIF operates in conjunction with UDBs, I/O ports, and other hardware to generate external memory address and control signals. At 33 MHz, each memory access cycle takes four bus clock cycles.

Figure 5-1 is the EMIF block diagram. The EMIF supports synchronous and asynchronous memories. The CY8C36 supports only one type of external memory device at a time.

External memory can be accessed through the 8051 xdata space; up to 24 address bits can be used. See xdata Space on page 21. The memory can be 8 or 16 bits wide.

**Figure 6-9. SIO Input/Output Block Diagram**

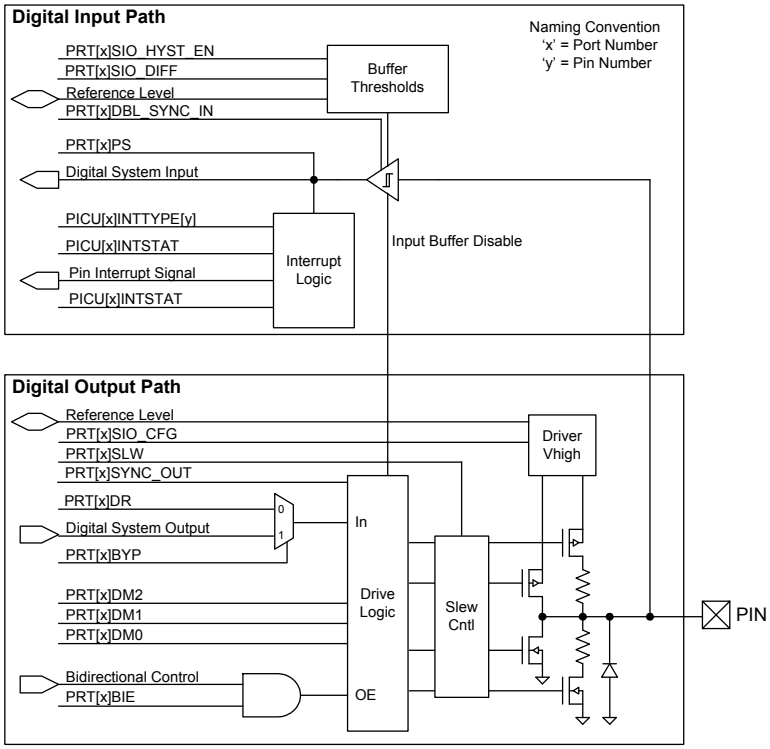
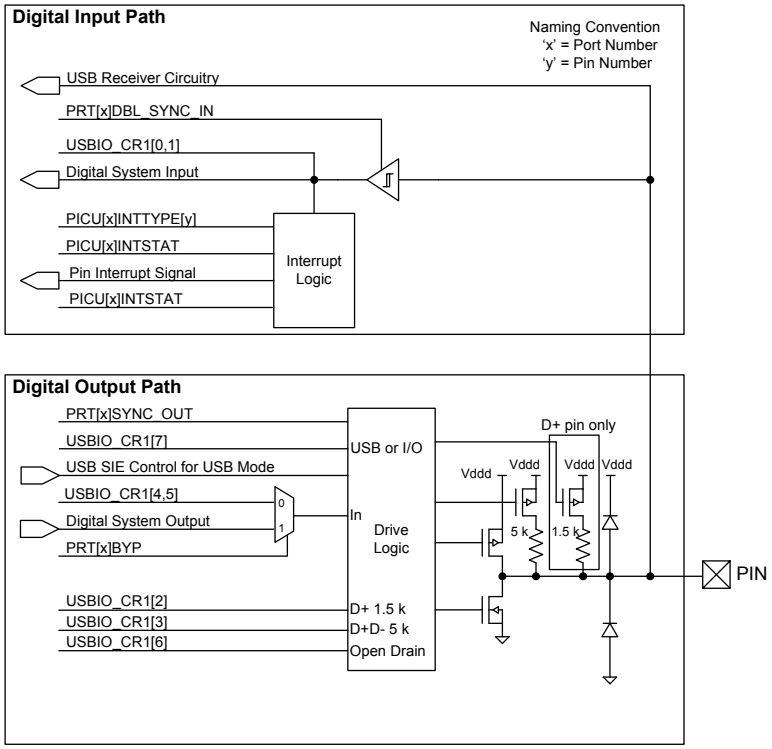



**Figure 6-10. USBIO Block Diagram**



- High Impedance Analog

  The default reset state with both the output driver and digital input buffer turned off. This prevents any current from flowing in the I/O's digital input buffer due to a floating voltage. This state is recommended for pins that are floating or that support an analog voltage. High impedance analog pins do not provide digital input functionality.

  To achieve the lowest chip current in sleep modes, all I/Os must either be configured to the high impedance analog mode, or have their pins driven to a power supply rail by the PSoC device or by external circuitry.

- High Impedance Digital

  The input buffer is enabled for digital signal input. This is the standard high impedance (HiZ) state recommended for digital inputs.

- Resistive pull-up or resistive pull-down

  Resistive pull-up or pull-down, respectively, provides a series resistance in one of the data states and strong drive in the other. Pins can be used for digital input and output in these modes. Interfacing to mechanical switches is a common application for these modes. Resistive pull-up and pull-down are not available with SIO in regulated output mode.

- Open Drain, Drives High and Open Drain, Drives Low

  Open drain modes provide high impedance in one of the data states and strong drive in the other. Pins can be used for digital input and output in these modes. A common application for these modes is driving the $I^2C$ bus signal lines.

- Strong Drive

  Provides a strong CMOS output drive in either high or low state. This is the standard output mode for pins. Strong Drive mode pins must not be used as inputs under normal circumstances. This mode is often used to drive digital output signals or external FETs.

- Resistive pull-up and pull-down

  Similar to the resistive pull-up and resistive pull-down modes except the pin is always in series with a resistor. The high data state is pull-up while the low data state is pull-down. This mode is most often used when other signals that may cause shorts can drive the bus. Resistive pull-up and pull-down are not available with SIO in regulated output mode.

### *6.4.2 Pin Registers*

Registers to configure and interact with pins come in two forms that may be used interchangeably.

All I/O registers are available in the standard port form, where each bit of the register corresponds to one of the port pins. This register form is efficient for quickly reconfiguring multiple port pins at the same time.

I/O registers are also available in pin form, which combines the eight most commonly used port register bits into a single register for each pin. This enables very fast configuration changes to individual pins with a single register write.

### *6.4.3 Bidirectional Mode*

High speed bidirectional capability allows pins to provide both the high impedance digital drive mode for input signals and a second user selected drive mode such as strong drive (set using PRT×DM[2:0] registers) for output signals on the same pin, based on the state of an auxiliary control bus signal. The bidirectional capability is useful for processor busses and communications interfaces such as the SPI Slave MISO pin that requires dynamic hardware control of the output buffer.

The auxiliary control bus routes up to 16 UDB or digital peripheral generated output enable signals to one or more pins.

### *6.4.4 Slew Rate Limited Mode*

GPIO and SIO pins have fast and slow output slew rate options for strong and open drain drive modes, not resistive drive modes. Because it results in reduced EMI, the slow edge rate option is recommended for signals that are not speed critical, generally less than 1 MHz. The fast slew rate is for signals between 1 MHz and 33 MHz. The slew rate is individually configurable for each pin, and is set by the PRT×SLW registers.

### *6.4.5 Pin Interrupts*

All GPIO and SIO pins are able to generate interrupts to the system. All eight pins in each port interface to their own Port Interrupt Control Unit (PICU) and associated interrupt vector. Each pin of the port is independently configurable to detect rising edge, falling edge, both edge interrupts, or to not generate an interrupt.

Depending on the configured mode for each pin, each time an interrupt event occurs on a pin, its corresponding status bit of the interrupt status register is set to "1" and an interrupt request is sent to the interrupt controller. Each PICU has its own interrupt vector in the interrupt controller and the pin status register providing easy determination of the interrupt source down to the pin level.

Port pin interrupts remain active in all sleep modes allowing the PSoC device to wake from an externally generated interrupt.

While level sensitive interrupts are not directly supported; universal digital blocks (UDB) provide this functionality to the system when needed.

### *6.4.6 Input Buffer Mode*

GPIO and SIO input buffers can be configured at the port level for the default CMOS input thresholds or the optional LVTTL input thresholds. All input buffers incorporate Schmitt triggers for input hysteresis. Additionally, individual pin input buffers can be disabled in any drive mode.

### *6.4.7 I/O Power Supplies*

Up to four I/O pin power supplies are provided depending on the device and package. Each I/O supply must be less than or equal to the voltage on the chip's analog ($V_{DDA}$) pin. This feature allows users to provide different I/O voltage levels for different pins on the device. Refer to the specific device package pinout to determine Vddio capability for a given port and pin.

The SIO port pins support an additional regulated high output capability, as described in Adjustable Output Level.

### *6.4.8 Analog Connections*

These connections apply only to GPIO pins. All GPIO pins may be used as analog inputs or outputs. The analog voltage present on the pin must not exceed the Vddio supply voltage to which the GPIO belongs. Each GPIO may connect to one of the analog

global busses or to one of the analog mux buses to connect any pin to any internal analog resource such as ADC or comparators. In addition, select pins provide direct connections to specific analog features such as the high current DACs or uncommitted opamps.

### 6.4.9 CapSense

This section applies only to GPIO pins. All GPIO pins may be used to create CapSense buttons and sliders[19]. See the "CapSense" section on page 53 for more information.

### 6.4.10 LCD Segment Drive

This section applies only to GPIO pins. All GPIO pins may be used to generate Segment and Common drive signals for direct glass drive of LCD glass. See the "LCD Direct Drive" section on page 52 for details.

### 6.4.11 Adjustable Output Level

This section applies only to SIO pins. SIO port pins support the ability to provide a regulated high output level for interface to external signals that are lower in voltage than the SIO's respective Vddio. SIO pins are individually configurable to output either the standard Vddio level or the regulated output, which is based on an internally generated reference. Typically a voltage DAC (VDAC) is used to generate the reference (see Figure 6-12). The "DAC" section on page 53 has more details on VDAC use and reference routing to the SIO pins. Resistive pull-up and pull-down drive modes are not available with SIO in regulated output mode.

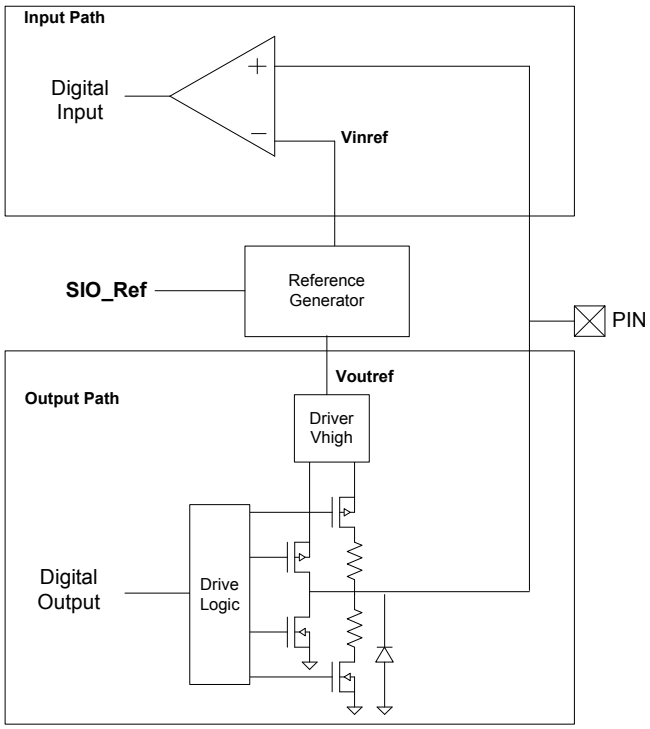
### 6.4.12 Adjustable Input Level

This section applies only to SIO pins. SIO pins by default support the standard CMOS and LVTTL input levels but also support a differential mode with programmable levels. SIO pins are grouped into pairs. Each pair shares a reference generator block which, is used to set the digital input buffer reference level for interface to external signals that differ in voltage from Vddio. The reference sets the pins voltage threshold for a high logic level (see Figure 6-12). Available input thresholds are:

- 0.5 × Vddio
- 0.4 × Vddio
- 0.5 × $V_{REF}$
- $V_{REF}$

Typically a voltage DAC (VDAC) generates the $V_{REF}$ reference. "DAC" section on page 53 has more details on VDAC use and reference routing to the SIO pins.

**Figure 6-12. SIO Reference for Input and Output**




### 6.4.13 SIO as Comparator

This section applies only to SIO pins. The adjustable input level feature of the SIOs as explained in the Adjustable Input Level section can be used to construct a comparator. The threshold for the comparator is provided by the SIO's reference generator. The reference generator has the option to set the analog signal routed through the analog global line as threshold for the comparator. Note that a pair of SIO pins share the same threshold.

The digital input path in Figure 6-9 on page 30 illustrates this functionality. In the figure, 'Reference level' is the analog signal routed through the analog global. The hysteresis feature can also be enabled for the input buffer of the SIO, which increases noise immunity for the comparator.

### 6.4.14 Hot Swap

This section applies only to SIO pins. SIO pins support 'hot swap' capability to plug into an application without loading the signals that are connected to the SIO pins even when no power is applied to the PSoC device. This allows the unpowered PSoC to maintain a high impedance load to the external device while also preventing the PSoC from being powered through a GPIO pin's protection diode.

**Note**
19. GPIOs with opamp outputs are not recommended for use with CapSense

## 7.1 Example Peripherals

The flexibility of the CY8C36 family's Universal Digital Blocks (UDBs) and Analog Blocks allow the user to create a wide range of components (peripherals). The most common peripherals were built and characterized by Cypress and are shown in the PSoC Creator component catalog, however, users may also create their own custom components using PSoC Creator. Using PSoC Creator, users may also create their own components for reuse within their organization, for example sensor interfaces, proprietary algorithms, and display interfaces.

The number of components available through PSoC Creator is too numerous to list in the datasheet, and the list is always growing. An example of a component available for use in CY8C36 family, but, not explicitly called out in this datasheet is the UART component.

### *7.1.1 Example Digital Components*

The following is a sample of the digital components available in PSoC Creator for the CY8C36 family. The exact amount of hardware resources (UDBs, routing, RAM, flash) used by a component varies with the features selected in PSoC Creator for the component.

- Communications
  - $I^2C$
  - UART
  - SPI
- Functions
  - EMIF
  - PWMs
  - Timers
  - Counters
- Logic
  - NOT
  - OR
  - XOR
  - AND

### *7.1.2 Example Analog Components*

The following is a sample of the analog components available in PSoC Creator for the CY8C36 family. The exact amount of hardware resources (SC/CT blocks, routing, RAM, flash) used by a component varies with the features selected in PSoC Creator for the component.

- Amplifiers
  - TIA
  - PGA
  - opamp
- ADC
  - Delta-Sigma
- DACs
  - Current
  - Voltage
  - PWM
- Comparators
- Mixers

### *7.1.3 Example System Function Components*

The following is a sample of the system function components available in PSoC Creator for the CY8C36 family. The exact amount of hardware resources (UDBs, DFB taps, SC/CT blocks, routing, RAM, flash) used by a component varies with the features selected in PSoC Creator for the component.

- CapSense
- LCD Drive
- LCD Control
- Filters

### *7.1.4 Designing with PSoC Creator*

#### *7.1.4.1 More Than a Typical IDE*

A successful design tool allows for the rapid development and deployment of both simple and complex designs. It reduces or eliminates any learning curve. It makes the integration of a new design into the production stream straightforward.

PSoC Creator is that design tool.

PSoC Creator is a full featured Integrated Development Environment (IDE) for hardware and software design. It is optimized specifically for PSoC devices and combines a modern, powerful software development platform with a sophisticated graphical design tool. This unique combination of tools makes PSoC Creator the most flexible embedded design platform available.

Graphical design entry simplifies the task of configuring a particular part. You can select the required functionality from an extensive catalog of components and place it in your design. All components are parameterized and have an editor dialog that allows you to tailor functionality to your needs.

PSoC Creator automatically configures clocks and routes the I/O to the selected pins and then generates APIs to give the application complete control over the hardware. Changing the PSoC device configuration is as simple as adding a new component, setting its parameters, and rebuilding the project.

At any stage of development you are free to change the hardware configuration and even the target processor. To retarget your application (hardware and software) to new devices, even from 8- to 32-bit families, just select the new device and rebuild.

You also have the ability to change the C compiler and evaluate an alternative. Components are designed for portability and are validated against all devices, from all families, and against all supported tool chains. Switching compilers is as easy as editing the from the project options and rebuilding the application with no errors from the generated APIs or boot code.

## 7.7 Timers, Counters, and PWMs

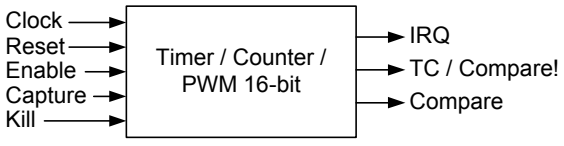
The Timer/Counter/PWM peripheral is a 16-bit dedicated peripheral providing three of the most common embedded peripheral features. As almost all embedded systems use some combination of timers, counters, and PWMs. Four of them have been included on this PSoC device family. Additional and more advanced functionality timers, counters, and PWMs can also be instantiated in Universal Digital Blocks (UDBs) as required. PSoC Creator allows you to choose the timer, counter, and PWM features that they require. The tool set utilizes the most optimal resources available.

The Timer/Counter/PWM peripheral can select from multiple clock sources, with input and output signals connected through the DSI routing. DSI routing allows input and output connections to any device pin and any internal digital signal accessible through the DSI. Each of the four instances has a compare output, terminal count output (optional complementary compare output), and programmable interrupt request line. The Timer/Counter/PWMs are configurable as free running, one shot, or Enable input controlled. The peripheral has timer reset and capture inputs, and a kill input for control of the comparator outputs. The peripheral supports full 16-bit capture.

Timer/Counter/PWM features include:

- 16-bit Timer/Counter/PWM (down count only)
- Selectable clock source
- PWM comparator (configurable for LT, LTE, EQ, GTE, GT)
- Period reload on start, reset, and terminal count
- Interrupt on terminal count, compare true, or capture
- Dynamic counter reads
- Timer capture mode
- Count while enable signal is asserted mode
- Free run mode
- One Shot mode (stop at end of period)
- Complementary PWM outputs with deadband
- PWM output kill

**Figure 7-21. Timer/Counter/PWM**




## 7.8 I²C

The I²C peripheral provides a synchronous two wire interface designed to interface the PSoC device with a two wire I²C serial communication bus. The bus is compliant with Philips 'The I²C Specification' version 2.1. Additional I²C interfaces can be instantiated using Universal Digital Blocks (UDBs) in PSoC Creator, as required.

To eliminate the need for excessive CPU intervention and overhead, I²C specific support is provided for status detection and generation of framing bits. I²C operates as a slave, a master, or multimaster (Slave and Master). In slave mode, the unit always listens for a start condition to begin sending or receiving data. Master mode supplies the ability to generate the Start and Stop conditions and initiate transactions. Multimaster mode provides clock synchronization and arbitration to allow multiple masters on the same bus. If Master mode is enabled and Slave mode is not enabled, the block does not generate interrupts on externally generated Start conditions. I²C interfaces through the DSI routing and allows direct connections to any GPIO or SIO pins.

I²C provides hardware address detect of a 7-bit address without CPU intervention. Additionally the device can wake from low-power modes on a 7-bit hardware address match. If wakeup functionality is required, I²C pin connections are limited to the two special sets of SIO pins.

I²C features include:

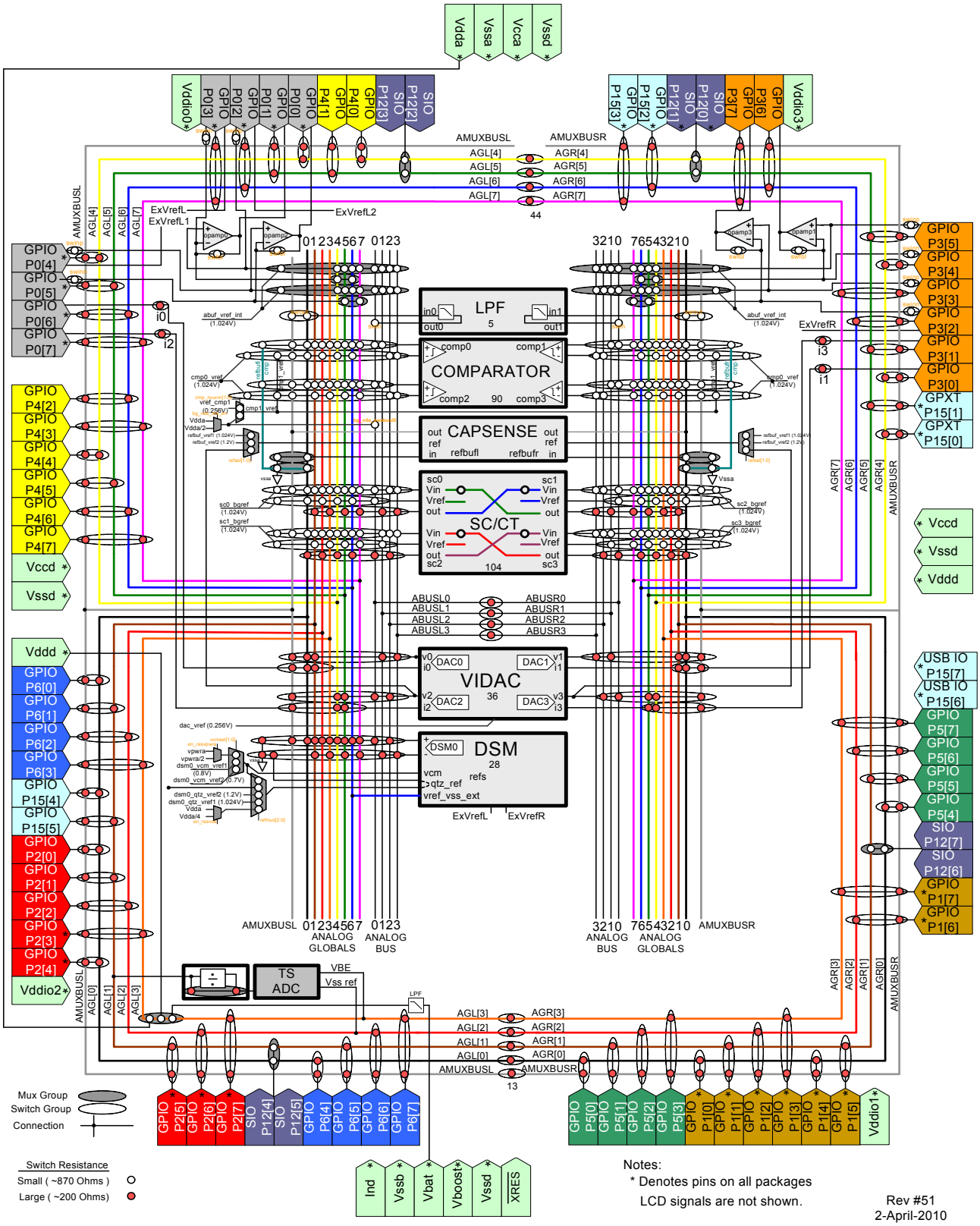
- Slave and master, transmitter, and receiver operation
- Byte processing for low CPU overhead
- Interrupt or polling CPU interface
- Support for bus speeds up to 1 Mbps (3.4 Mbps in UDBs)
- 7 or 10-bit addressing (10-bit addressing requires firmware support)
- SMBus operation (through firmware support – SMBus supported in hardware in UDBs)
- 7-bit hardware address compare
- Wake from low-power modes on address match

## 7.9 Digital Filter Block

Some devices in the CY8C36 family of devices have a dedicated HW accelerator block used for digital filtering. The DFB has a dedicated multiplier and accumulator that calculates a 24-bit by 24-bit multiply accumulate in one system clock cycle. This enables the mapping of a direct form FIR filter that approaches a computation rate of one FIR tap for each clock cycle. The MCU can implement any of the functions performed by this block, but at a slower rate that consumes MCU bandwidth.

The PSoC Creator interface provides a wizard to implement FIR and IIR digital filters with coefficients for LPF, BPF, HPF, Notch and arbitrary shape filters. 64 pairs of data and coefficients are stored. This enables a 64 tap FIR filter or up to 4 16 tap filters of either FIR or IIR formulation.

**Figure 8-2. CY8C36 Analog Interconnect**



first three conversions prime the decimator. The ADC result is valid and available after the fourth conversion, at which time the EoC signal is generated. To detect the end of conversion, the system may poll a control register for status or configure the external EoC signal to generate an interrupt or invoke a DMA request. When the transfer is done the ADC reenters the standby state where it stays until another SoC event.

#### 8.2.2.2 Continuous

Continuous sample mode is used to take multiple successive samples of a single input signal. Multiplexing multiple inputs should not be done with this mode. There is a latency of three conversion times before the first conversion result is available. This is the time required to prime the decimator. After the first result, successive conversions are available at the selected sample rate.

#### 8.2.2.3 Multi Sample

Multi sample mode is similar to continuous mode except that the ADC is reset between samples. This mode is useful when the input is switched between multiple signals. The decimator is re-primed between each sample so that previous samples do not affect the current conversion. Upon completion of a sample, the next sample is automatically initiated. The results can be transferred using either firmware polling, interrupt, or DMA.

More information on output formats is provided in the Technical Reference Manual.

### 8.2.3 Start of Conversion Input

The SoC signal is used to start an ADC conversion. A digital clock or UDB output can be used to drive this input. It can be used when the sampling period must be longer than the ADC conversion time or when the ADC must be synchronized to other hardware. This signal is optional and does not need to be connected if ADC is running in a continuous mode.

### 8.2.4 End of Conversion Output

The EoC signal goes high at the end of each ADC conversion. This signal may be used to trigger either an interrupt or DMA request.

## 8.3 Comparators

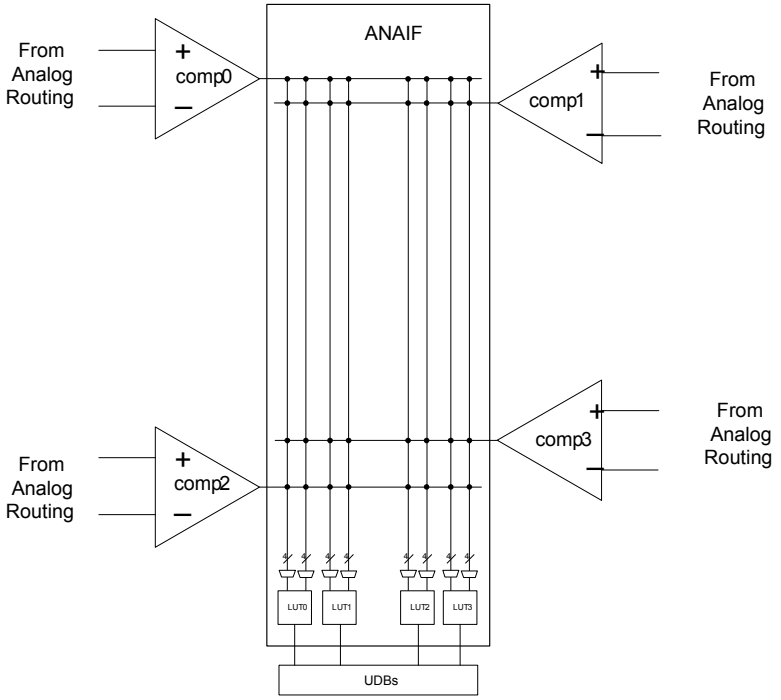
The CY8C36 family of devices contains four comparators in a device. Comparators have these features:

- Input offset factory trimmed to less than 5 mV
- Rail-to-rail common mode input range ($V_{SSA}$ to $V_{DDA}$)
- Speed and power can be traded off by using one of three modes: fast, slow, or ultra low-power
- Comparator outputs can be routed to lookup tables to perform simple logic functions and then can also be routed to digital blocks
- The positive input of the comparators may be optionally passed through a low pass filter. Two filters are provided
- Comparator inputs can be connections to GPIO, DAC outputs and SC block outputs

### 8.3.1 Input and Output Interface

The positive and negative inputs to the comparators come from the analog global buses, the analog mux line, the analog local bus and precision reference through multiplexers. The output from each comparator could be routed to any of the two input LUTs. The output of that LUT is routed to the UDB Digital System Interface.

**Figure 8-6. Analog Comparator**



# 11. Electrical Specifications

Specifications are valid for –40 °C ≤ $T_A$ ≤ 85 °C and $T_J$ ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted. The unique flexibility of the PSoC UDBs and analog blocks enable many functions to be implemented in PSoC Creator components, see the component datasheets for full AC/DC specifications of individual functions. See the "Example Peripherals" section on page 35 for further explanation of PSoC Creator components.

## 11.1 Absolute Maximum Ratings

**Table 11-1. Absolute Maximum Ratings DC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $T_{STG}$ | Storage temperature | Higher storage temperatures reduce NVL data retention time. Recommended storage temperature is +25 °C ±25 °C. Extended duration storage temperatures above 85 °C degrade reliability. | –55 | 25 | 100 | °C |
| $V_{DDA}$ | Analog supply voltage relative to $V_{SSA}$ | | –0.5 | – | 6 | V |
| $V_{DDD}$ | Digital supply voltage relative to $V_{SSD}$ | | –0.5 | – | 6 | V |
| $V_{DDIO}$ | I/O supply voltage relative to $V_{SSD}$ | | –0.5 | – | 6 | V |
| $V_{CCA}$ | Direct analog core voltage input | | –0.5 | – | 1.95 | V |
| $V_{CCD}$ | Direct digital core voltage input | | –0.5 | – | 1.95 | V |
| $V_{SSA}$ | Analog ground voltage | | $V_{SSD}$ – 0.5 | – | $V_{SSD}$ + 0.5 | V |
| $V_{GPIO}$[20] | DC input voltage on GPIO | Includes signals sourced by $V_{DDA}$ and routed internal to the pin | $V_{SSD}$ – 0.5 | – | $V_{DDIO}$ + 0.5 | V |
| $V_{SIO}$ | DC input voltage on SIO | Output disabled | $V_{SSD}$ – 0.5 | – | 7 | V |
| | | Output enabled | $V_{SSD}$ – 0.5 | – | 6 | V |
| $V_{IND}$ | Voltage at boost converter input | | 0.5 | – | 5.5 | V |
| $V_{BAT}$ | Boost converter supply | | $V_{SSD}$ – 0.5 | – | 5.5 | V |
| Ivddio | Current per $V_{DDIO}$ supply pin | | – | – | 100 | mA |
| Vextref | ADC external reference inputs | Pins P0[3], P3[2] | – | – | 2 | V |
| LU | Latch up current[21] | | –140 | – | 140 | mA |
| $ESD_{HBM}$ | Electrostatic discharge voltage | Human body model | 750 | – | – | V |
| $ESD_{CDM}$ | Electrostatic discharge voltage | Charge device model | 500 | – | – | V |

**Note** Usage above the absolute maximum conditions listed in Table 11-1 may cause permanent damage to the device. Exposure to maximum conditions for extended periods of time may affect device reliability. When used below maximum conditions but above normal operating conditions the device may not operate to specification.

**Notes**
20. The $V_{DDIO}$ supply voltage must be greater than the maximum analog voltage on the associated GPIO pins. Maximum analog voltage on GPIO pin ≤ $V_{DDIO}$ ≤ $V_{DDA}$.
21. Meets or exceeds JEDEC Spec EIA/JESD78 IC Latch-up Test.

**Table 11-14. USBIO AC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Tdrate | Full-speed data rate average bit rate | | 12 – 0.25% | 12 | 12 + 0.25% | MHz |
| Tjr1 | Receiver data jitter tolerance to next transition | | –8 | – | 8 | ns |
| Tjr2 | Receiver data jitter tolerance to pair transition | | –5 | – | 5 | ns |
| Tdj1 | Driver differential jitter to next transition | | –3.5 | – | 3.5 | ns |
| Tdj2 | Driver differential jitter to pair transition | | –4 | – | 4 | ns |
| Tfdeop | Source jitter for differential transition to SE0 transition | | –2 | – | 5 | ns |
| Tfeopt | Source SE0 interval of EOP | | 160 | – | 175 | ns |
| Tfeopr | Receiver SE0 interval of EOP | | 82 | – | – | ns |
| Tfst | Width of SE0 interval during differential transition | | – | – | 14 | ns |
| Fgpio_out | GPIO mode output operating frequency | $3\ V \le V_{DDD} \le 5.5\ V$ | – | – | 20 | MHz |
| | | $V_{DDD} = 1.71\ V$ | – | – | 6 | MHz |
| Tr_gpio | Rise time, GPIO mode, 10%/90% $V_{DDD}$ | $V_{DDD} > 3\ V$, 25 pF load | – | – | 12 | ns |
| | | $V_{DDD} = 1.71\ V$, 25 pF load | – | – | 40 | ns |
| Tf_gpio | Fall time, GPIO mode, 90%/10% $V_{DDD}$ | $V_{DDD} > 3\ V$, 25 pF load | – | – | 12 | ns |
| | | $V_{DDD} = 1.71\ V$, 25 pF load | – | – | 40 | ns |

**Table 11-15. USB Driver AC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Tr | Transition rise time | | – | – | 20 | ns |
| Tf | Transition fall time | | – | – | 20 | ns |
| TR | Rise/fall time matching | $V_{USB\_5}$, $V_{USB\_3.3}$, see USB DC Specifications on page 87 | 90% | – | 111% | |
| Vcrs | Output signal crossover voltage | | 1.3 | – | 2 | V |

*11.4.4 XRES*

**Table 11-16. XRES DC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input voltage high threshold | | $0.7 \times V_{DDIO}$ | – | – | V |
| $V_{IL}$ | Input voltage low threshold | | – | – | $0.3 \times V_{DDIO}$ | V |
| Rpullup | Pull-up resistor | | 3.5 | 5.6 | 8.5 | kΩ |
| $C_{IN}$ | Input capacitance[36] | | – | 3 | – | pF |
| $V_H$ | Input voltage hysteresis (Schmitt–Trigger)[36] | | – | 100 | – | mV |
| Idiode | Current through protection diode to $V_{DDIO}$ and $V_{SSIO}$ | | – | – | 100 | µA |

**Table 11-17. XRES AC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $T_{RESET}$ | Reset pulse width | | 1 | – | – | µs |

**Note**
36. Based on device characterization (Not production tested).

**Table 11-21. Delta-sigma ADC AC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| | Startup time | | – | – | 4 | Samples |
| THD | Total harmonic distortion[40] | Buffer gain = 1, 16 bit, Range = ±1.024 V | – | – | 0.0032 | % |
| **12-Bit Resolution Mode** | | | | | | |
| SR12 | Sample rate, continuous, high power[40] | Range = ±1.024 V, unbuffered | 4 | – | 192 | ksps |
| BW12 | Input bandwidth at max sample rate[40] | Range = ±1.024 V, unbuffered | – | 44 | – | kHz |
| SINAD12int | Signal to noise ratio, 12-bit, internal reference[40] | Range = ±1.024 V, unbuffered | 66 | – | – | dB |
| **8-Bit Resolution Mode** | | | | | | |
| SR8 | Sample rate, continuous, high power[40] | Range = ±1.024 V, unbuffered | 8 | – | 384 | ksps |
| BW8 | Input bandwidth at max sample rate[40] | Range = ±1.024 V, unbuffered | – | 88 | – | kHz |
| SINAD8int | Signal to noise ratio, 8-bit, internal reference[40] | Range = ±1.024 V, unbuffered | 43 | – | – | dB |

**Table 11-22. Delta-sigma ADC Sample Rates, Range = ±1.024 V**

| Resolution, Bits | Continuous | | Multi-Sample | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| 8 | 8000 | 384000 | 1911 | 91701 |
| 9 | 6400 | 307200 | 1543 | 74024 |
| 10 | 5566 | 267130 | 1348 | 64673 |
| 11 | 4741 | 227555 | 1154 | 55351 |
| 12 | 4000 | 192000 | 978 | 46900 |

**Figure 11-24. Delta-sigma ADC $I_{DD}$ vs sps, Range = ±1.024 V**

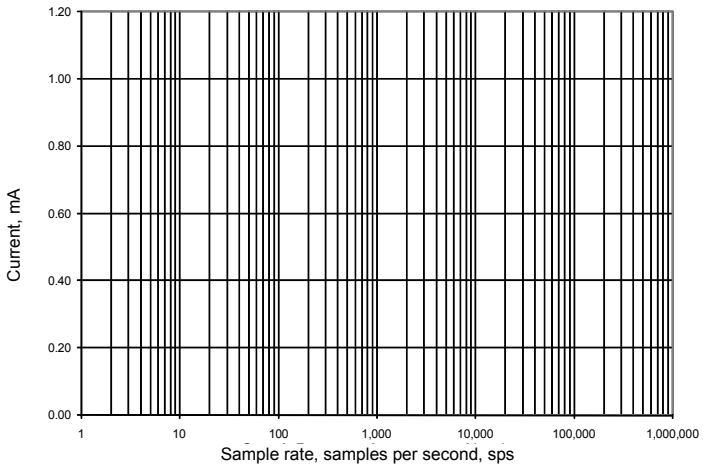
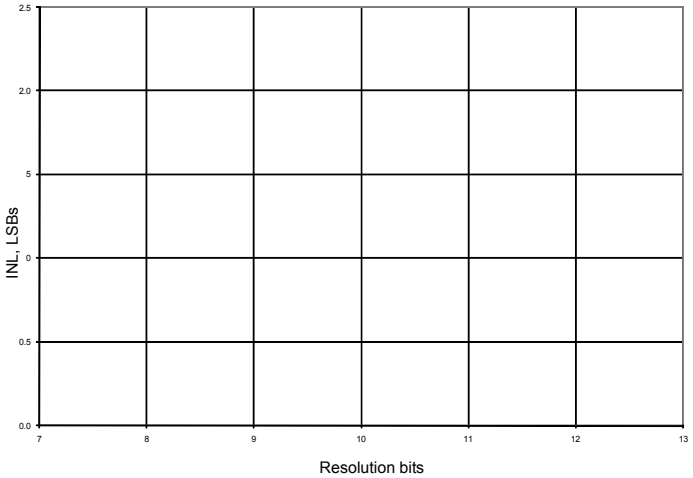



**Figure 11-25. Delta-sigma ADC INL at Maximum Sample Rate**




**Note**
40. Based on device characterization (Not production tested).

### 11.6.3 Pulse Width Modulation

The following specifications apply to the Timer/Counter/PWM peripheral, in PWM mode. PWM components can also be implemented in UDBs; for more information, see the PWM component datasheet in PSoC Creator.

**Table 11-44. PWM DC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| | Block current consumption | 16-bit PWM, at listed input clock frequency | – | – | – | µA |
| | 3 MHz | | – | 15 | – | µA |
| | 12 MHz | | – | 60 | – | µA |
| | 48 MHz | | – | 260 | – | µA |
| | 67 MHz | | – | 350 | – | µA |

**Table 11-45. Pulse Width Modulation (PWM) AC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| | Operating frequency | | DC | – | 67 | MHz |
| | Pulse width | | 15 | – | – | ns |
| | Pulse width (external) | | 30 | – | – | ns |
| | Kill pulse width | | 15 | – | – | ns |
| | Kill pulse width (external) | | 30 | – | – | ns |
| | Enable pulse width | | 15 | – | – | ns |
| | Enable pulse width (external) | | 30 | – | – | ns |
| | Reset pulse width | | 15 | – | – | ns |
| | Reset pulse width (external) | | 30 | – | – | ns |

### 11.6.4 $I^2C$

**Table 11-46. Fixed $I^2C$ DC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| | Block current consumption | Enabled, configured for 100 kbps | – | – | 250 | µA |
| | | Enabled, configured for 400 kbps | – | – | 260 | µA |
| | | Wake from sleep mode | – | – | 30 | µA |

**Table 11-47. Fixed $I^2C$ AC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| | Bit rate | | – | – | 1 | Mbps |

### 11.6.5 Controller Area Network[46]

**Table 11-48. CAN AC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| | Bit rate | Minimum 8 MHz clock | – | – | 1 | Mbit |

**Note**
46. Refer to ISO 11898 specification for details.

### 11.8.3 Interrupt Controller

**Table 11-69. Interrupt Controller AC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| | Delay from interrupt signal input to ISR code execution from ISR code | Includes worse case completion of longest instruction DIV with 6 cycles | – | – | 25 | Tcy CPU |

### 11.8.4 JTAG Interface

**Table 11-70. JTAG Interface AC Specifications[52]**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| f_TCK | TCK frequency | 3.3 V ≤ $V_{DDD}$ ≤ 5 V | – | – | 14[53] | MHz |
| | | 1.71 V ≤ $V_{DDD}$ < 3.3 V | – | – | 7[53] | MHz |
| T_TDI_setup | TDI setup before TCK high | | (T/10) – 5 | – | – | ns |
| T_TMS_setup | TMS setup before TCK high | | T/4 | – | – | |
| T_TDI_hold | TDI, TMS hold after TCK high | T = 1/f_TCK | T/4 | – | – | |
| T_TDO_valid | TCK low to TDO valid | T = 1/f_TCK | 2T/5 | – | – | |
| T_TDO_hold | TDO hold after TCK high | T = 1/f_TCK | T/4 | – | – | |
| | TCK to device outputs valid | | – | – | 2T/5 | |

### 11.8.5 SWD Interface

**Table 11-71. SWD Interface AC Specifications[52]**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| f_SWDCK | SWDCLK frequency | 3.3 V ≤ $V_{DDD}$ ≤ 5 V | – | – | 14[54] | MHz |
| | | 1.71 V ≤ $V_{DDD}$ < 3.3 V | – | – | 7[54] | MHz |
| | | 1.71 V ≤ $V_{DDD}$ < 3.3 V, SWD over USBIO pins | – | – | 5.5[54] | MHz |
| T_SWDI_setup | SWDIO input setup before SWDCK high | T = 1/f_SWDCK | T/4 | – | – | – |
| T_SWDI_hold | SWDIO input hold after SWDCK high | T = 1/f_SWDCK | T/4 | – | – | – |
| T_SWDO_valid | SWDCK low to SWDIO output valid | T = 1/f_SWDCK | 2T/5 | – | – | – |
| T_SWDO_hold | SWDIO output hold after SWDCK high | T = 1/f_SWDCK | T/4 | – | – | – |

### 11.8.6 SWV Interface

**Table 11-72. SWV Interface AC Specifications[52]**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| | SWV mode SWV bit rate | | – | – | 33 | Mbit |

**Notes**
52. Based on device characterization (Not production tested).
53. f_TCK must also be no more than 1/3 CPU clock frequency.
54. f_SWDCK must also be no more than 1/3 CPU clock frequency.

### 11.9.6 Phase-Locked Loop

**Table 11-81. PLL DC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $I_{DD}$ | PLL operating current | In = 3 MHz, Out = 67 MHz | – | 400 | – | µA |
| | | In = 3 MHz, Out = 24 MHz | – | 200 | – | µA |

**Table 11-82. PLL AC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Fpllin | PLL input frequency[57] | | 1 | – | 48 | MHz |
| | PLL intermediate frequency[58] | Output of prescaler | 1 | – | 3 | MHz |
| Fpllout | PLL output frequency[57] | | 24 | – | 67 | MHz |
| | Lock time at startup | | – | – | 250 | µs |
| Jperiod-rms | Jitter (rms)[59] | | – | – | 250 | ps |

**Notes**
57. This specification is guaranteed by testing the PLL across the specified range using the IMO as the source for the PLL.
58. PLL input divider, Q, must be set so that the input frequency is divided down to the intermediate frequency range. Value for Q ranges from 1 to 16.
59. Based on device characterization (Not production tested).

**Figure 13-4. 100-pin TQFP (14 × 14 × 1.4 mm) Package Outline**

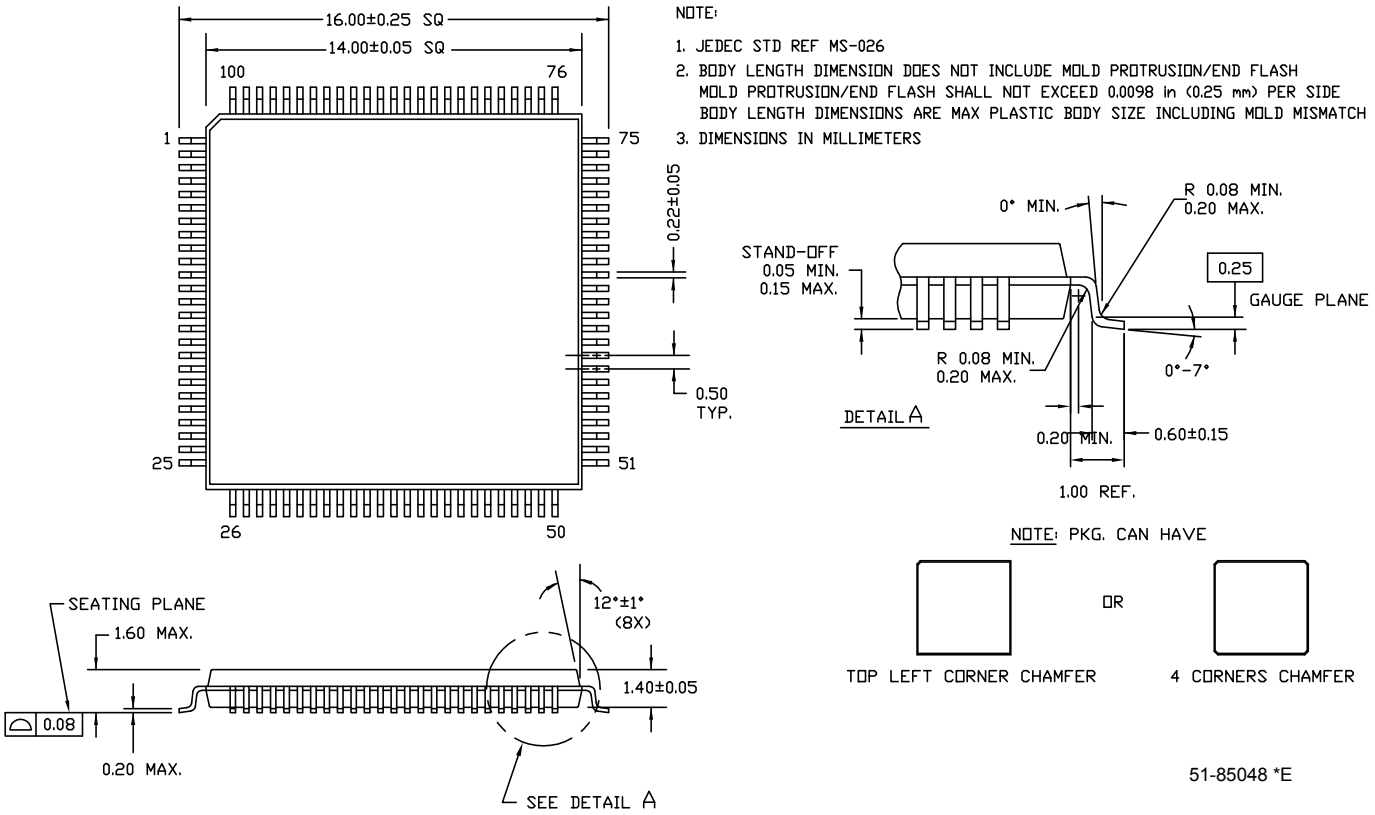


**Table 14-1. Acronyms Used in this Document** *(continued)*

| Acronym | Description |
|---|---|
| PGA | programmable gain amplifier |
| PHUB | peripheral hub |
| PHY | physical layer |
| PICU | port interrupt control unit |
| PLA | programmable logic array |
| PLD | programmable logic device, see also PAL |
| PLL | phase-locked loop |
| PMDD | package material declaration datasheet |
| POR | power-on reset |
| PRES | precise power-on reset |
| PRS | pseudo random sequence |
| PS | port read data register |
| PSoC® | Programmable System-on-Chip™ |
| PSRR | power supply rejection ratio |
| PWM | pulse-width modulator |
| RAM | random-access memory |
| RISC | reduced-instruction-set computing |
| RMS | root-mean-square |
| RTC | real-time clock |
| RTL | register transfer language |
| RTR | remote transmission request |
| RX | receive |
| SAR | successive approximation register |
| SC/CT | switched capacitor/continuous time |
| SCL | $I^2C$ serial clock |
| SDA | $I^2C$ serial data |
| S/H | sample and hold |
| SINAD | signal to noise and distortion ratio |
| SIO | special input/output, GPIO with advanced features. See GPIO. |

**Table 14-1. Acronyms Used in this Document** *(continued)*

| Acronym | Description |
|---|---|
| SOC | start of conversion |
| SOF | start of frame |
| SPI | Serial Peripheral Interface, a communications protocol |
| SR | slew rate |
| SRAM | static random access memory |
| SRES | software reset |
| SWD | serial wire debug, a test protocol |
| SWV | single-wire viewer |
| TD | transaction descriptor, see also DMA |
| THD | total harmonic distortion |
| TIA | transimpedance amplifier |
| TRM | technical reference manual |
| TTL | transistor-transistor logic |
| TX | transmit |
| UART | Universal Asynchronous Transmitter Receiver, a communications protocol |
| UDB | universal digital block |
| USB | Universal Serial Bus |
| USBIO | USB input/output, PSoC pins used to connect to a USB port |
| VDAC | voltage DAC, see also DAC, IDAC |
| WDT | watchdog timer |
| WOL | write once latch, see also NVL |
| WRES | watchdog timer reset |
| XRES | external reset I/O pin |
| XTAL | crystal |

## 15. Reference Documents

*PSoC® 3, PSoC® 5 Architecture TRM*

*PSoC® 3 Registers TRM*

## 17. Revision History

| Description Title: PSoC® 3: CY8C36 Family Datasheet Programmable System-on-Chip (PSoC®)<br>Document Number: 001-53413 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN No.** | **Submission Date** | **Orig. of Change** | **Description of Change** |
| ** | 2714854 | 06/04/09 | PVKV | New datasheet |
| *A | 2758970 | 09/02/09 | MKEA | Updated Part Numbering Conventions<br>Added Section 11.7.5 (EMIF Figures and Tables)<br>Updated GPIO and SIO AC specifications<br>Updated XRES Pin Description and Xdata Address Map specifications<br>Updated DFB and Comparator specifications<br>Updated PHUB features section and RTC in sleep mode<br>Updated IDAC and VDAC DC and Analog Global specifications<br>Updated USBIO AC and Delta Sigma ADC specifications<br>Updated PPOR and Voltage Monitors DC specifications<br>Updated Drive Mode diagram<br>Added 48-QFN Information<br>Updated other electrical specifications |
| *B | 2824546 | 12/09/09 | MKEA | Updated I2C section to reflect 1 Mbps. Updated Table 11-6 and 11-7 (Boost AC and DC specs); also added Shottky Diode specs. Changed current for sleep/hibernate mode to include SIO; Added footnote to analog global specs. Updated Figures 1-1, 6-2, 7-14, and 8-1. Updated Table 6-2 and Table 6-3 (Hibernate and Sleep rows) and Power Modes section. Updated GPIO and SIO AC specifications. Updated Gain error in IDAC and VDAC specifications. Updated description of $V_{DDA}$ spec in Table 11-1 and removed GPIO Clamp Current parameter. Updated number of UDBs on page 1.<br>Moved FILO from ILO DC to AC table.<br>Added PCB Layout and PCB Schematic diagrams.<br>Updated Fgpioout spec (Table 11-9). Added duty cycle frequency in PLL AC spec table. Added note for Sleep and Hibernate modes and Active Mode specs in Table 11-2. Linked URL in Section 10.3 to PSoC Creator site.<br>Updated Ja and Jc values in Table 13-1. Updated Single Sample Mode and Fast FIR Mode sections. Updated Input Resistance specification in Del-Sig ADC table. Added Tio_init parameter. Updated PGA and UGB AC Specs. Removed SPC ADC. Updated Boost Converter section.<br>Added section 'SIO as Comparator'; updated Hysteresis spec (differential mode) in Table 11-10.<br>Updated $V_{BAT}$ condition and deleted Vstart parameter in Table 11-6.<br>Added 'Bytes' column for Tables 4-1 to 4-5. |
| *C | 2873322 | 02/04/10 | MKEA | Changed maximum value of PPOR_TR to '1'. Updated $V_{BIAS}$ specification. Updated PCB Schematic. Updated Figure 8-1 and Figure 6-3. Updated Interrupt Vector table, Updated Sales links. Updated JTAG and SWD specifications. Removed Jp-p and Jperiod from ECO AC Spec table. Added note on sleep timer in Table 11-2. Updated ILO AC and DC specifications. Added Resolution parameter in VDAC and IDAC tables. Updated $I_{OUT}$ typical and maximum values. Changed Temperature Sensor range to –40 °C to +85 °C. Removed Latchup specification from Table 11-1. |