What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details

Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	67MHz
Connectivity	EBI/EMI, I²C, LINbus, SPI, UART/USART, USB
Peripherals	CapSense, DMA, POR, PWM, WDT
Number of I/O	62
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x12b; D/A 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3665axi-016

In addition to the flexibility of the UDB array, PSoC also provides configurable digital blocks targeted at specific functions. For the CY8C36 family these blocks can include four 16-bit timers, counters, and PWM blocks; I²C slave, master, and multi-master; FS USB; and Full CAN 2.0b.

For more details on the peripherals see the "Example Peripherals" section on page 35 of this datasheet. For information on UDBs, DSI, and other digital blocks, see the "Digital Subsystem" section on page 34 of this datasheet.

PSoC's analog subsystem is the second half of its unique configurability. All analog performance is based on a highly accurate absolute voltage reference with less than 0.1-percent error over temperature and voltage. The configurable analog subsystem includes:

■ Analog muxes

■ Comparators

■ Voltage references

■ ADC

■ DACs

■ DFB

All GPIO pins can route analog signals into and out of the device using the internal analog bus. This allows the device to interface up to 62 discrete analog signals. The heart of the analog subsystem is a fast, accurate, configurable delta-sigma ADC with these features:

■ Less than 100 µV offset

■ A gain error of 0.2 percent

■ INL less than ±1 LSB

■ DNL less than ±1 LSB

■ SINAD better than 66 dB

This converter addresses a wide variety of precision analog applications, including some of the most demanding sensors.

The output of the ADC can optionally feed the programmable DFB through the DMA without CPU intervention. You can configure the DFB to perform IIR and FIR digital filters and several user-defined custom functions. The DFB can implement filters with up to 64 taps. It can perform a 48-bit multiply-accumulate (MAC) operation in one clock cycle.

Four high-speed voltage or current DACs support 8-bit output signals at an update rate of up to 8 Msps. They can be routed out of any GPIO pin. You can create higher resolution voltage PWM DAC outputs using the UDB array. This can be used to create a PWM DAC of up to 10 bits, at up to 48 kHz. The digital DACs in each UDB support PWM, PRS, or delta-sigma algorithms with programmable widths.

In addition to the ADC, DACs, and DFB, the analog subsystem provides multiple:

■ Uncommitted opamps

■ Configurable switched capacitor/continuous time (SC/CT) blocks. These support:
  □ Transimpedance amplifiers
  □ Programmable gain amplifiers
  □ Mixers
  □ Other similar analog components

See the "Analog Subsystem" section on page 46 of this datasheet for more details.

PSoC's 8051 CPU subsystem is built around a single-cycle pipelined 8051 8-bit processor running at up to 67 MHz. The CPU subsystem includes a programmable nested vector interrupt controller, DMA controller, and RAM. PSoC's nested vector interrupt controller provides low latency by allowing the CPU to vector directly to the first address of the interrupt service routine, bypassing the jump instruction required by other architectures. The DMA controller enables peripherals to exchange data without CPU involvement. This allows the CPU to run slower (saving power) or use those CPU cycles to improve the performance of firmware algorithms. The single cycle 8051 CPU runs ten times faster than a standard 8051 processor. The processor speed itself is configurable, allowing you to tune active power consumption for specific applications.

PSoC's nonvolatile subsystem consists of flash, byte-writeable EEPROM, and nonvolatile configuration options. It provides up to 64 KB of on-chip flash. The CPU can reprogram individual blocks of flash, enabling bootloaders. You can enable an ECC for high reliability applications. A powerful and flexible protection model secures the user's sensitive information, allowing selective memory block locking for read and write protection. Up to 2 KB of byte-writeable EEPROM is available on-chip to store application data. Additionally, selected configuration options such as boot speed and pin drive mode are stored in nonvolatile memory. This allows settings to activate immediately after POR.

The three types of PSoC I/O are extremely flexible. All I/Os have many drive modes that are set at POR. PSoC also provides up to four I/O voltage domains through the V_{DDIO} pins. Every GPIO has analog I/O, LCD drive[4], CapSense[5], flexible interrupt generation, slew rate control, and digital I/O capability. The SIOs on PSoC allow V_{OH} to be set independently of V_{DDIO} when used as outputs. When SIOs are in input mode they are high impedance. This is true even when the device is not powered or when the pin voltage goes above the supply voltage. This makes the SIO ideally suited for use on an I²C bus where the PSoC may not be powered when other devices on the bus are. The SIO pins also have high current sink capability for applications such as LED drives. The programmable input threshold feature of the SIO can be used to make the SIO function as a general purpose analog comparator. For devices with FS USB the USB physical interface is also provided (USBIO). When not using USB these pins may also be used for limited digital functionality and device programming. All of the features of the PSoC I/Os are covered in detail in the "I/O System and Routing" section on page 28 of this datasheet.

The PSoC device incorporates flexible internal clock generators, designed for high stability and factory trimmed for high accuracy. The internal main oscillator (IMO) is the master clock base for the system, and has 1-percent accuracy at 3 MHz. The IMO can be configured to run from 3 MHz up to 62 MHz. Multiple clock derivatives can be generated from the main clock frequency to meet application needs. The device provides a PLL to generate system clock frequencies up to 67 MHz from the IMO, external crystal, or external reference clock. It also contains a separate, very low-power internal low speed oscillator (ILO) for the sleep and watchdog timers. A 32.768-kHz external watch crystal is also supported for use in RTC applications. The clocks, together with programmable clock dividers, provide the flexibility to integrate most timing requirements.

Figure 2-6. Example PCB Layout for 100-pin TQFP Part for Optimal Analog Performance
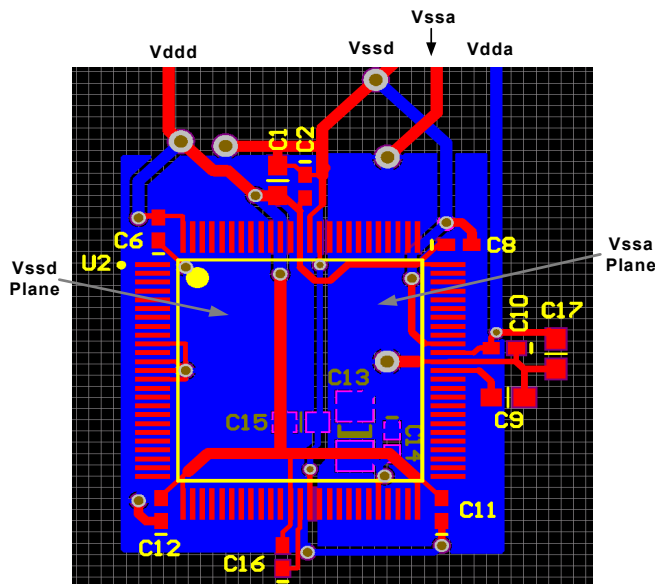
3. Pin Descriptions

IDAC0, IDAC1, IDAC2, IDAC3. Low resistance output pin for high current DACs (IDAC).

OpAmp0out, OpAmp1out[15], OpAmp2out, OpAmp3out[15].

High current output of uncommitted opamp.[14]

Extref0, Extref1. External reference input to the analog system.

OpAmp0–, OpAmp1–[15], OpAmp2–, OpAmp3–[15]. Inverting input to uncommitted opamp.

OpAmp0+, OpAmp1+[15], OpAmp2+, OpAmp3+[15].

Noninverting input to uncommitted opamp.

GPIO. General purpose I/O pin provides interfaces to the CPU, digital peripherals, analog peripherals, interrupts, LCD segment drive, and CapSense.[14]

I2C0: SCL, I2C1: SCL. I2C SCL line providing wake from sleep on an address match. Any I/O pin can be used for I2C SCL if wake from sleep is not required.

I2C0: SDA, I2C1: SDA. I2C SDA line providing wake from sleep on an address match. Any I/O pin can be used for I2C SDA if wake from sleep is not required.

Ind. Inductor connection to boost pump.

kHz XTAL: Xo, kHz XTAL: Xi. 32.768 kHz crystal oscillator pin.

MHz XTAL: Xo, MHz XTAL: Xi. 4 to 33 MHz crystal oscillator pin.

nTRST. Optional JTAG Test Reset programming and debug port connection to reset the JTAG connection.

SIO. Special I/O provides interfaces to the CPU, digital peripherals and interrupts with a programmable high threshold voltage, analog comparator, high sink current, and high impedance state when the device is unpowered.

SWDCK. Serial wire debug clock programming and debug port connection.

SWDIO. Serial wire debug input and output programming and debug port connection.

SWV. Single wire viewer debug output.

TCK. JTAG test clock programming and debug port connection.

TDI. JTAG test data in programming and debug port connection.

TDO. JTAG test data out programming and debug port connection.

TMS. JTAG test mode select programming and debug port connection.

USBIO, D+. Provides D+ connection directly to a USB 2.0 bus. May be used as a digital I/O pin. Pins are Do Not Use (DNU) on devices without USB.

USBIO, D–. Provides D– connection directly to a USB 2.0 bus. May be used as a digital I/O pin. Pins are Do Not Use (DNU) on devices without USB.

Vboost. Power sense connection to boost pump.

Vbat. Battery supply to boost pump.

Vcca. Output of analog core regulator and input to analog core. Requires a 1-µF capacitor to Vssa. Regulator output not for external use.

Notes
14. GPIOs with opamp outputs are not recommended for use with CapSense.
15. This feature on select devices only. See Ordering Information on page 99 for details.

[+] Feedback

Table 4-2. Logical Instructions *(continued)*

Mnemonic	Description	Bytes	Cycles
ORL A,#data	OR immediate data to accumulator	2	2
ORL Direct, A	OR accumulator to direct byte	2	3
ORL Direct, #data	OR immediate data to direct byte	3	3
XRL A,Rn	XOR register to accumulator	1	1
XRL A,Direct	XOR direct byte to accumulator	2	2
XRL A,@Ri	XOR indirect RAM to accumulator	1	2
XRL A,#data	XOR immediate data to accumulator	2	2
XRL Direct, A	XOR accumulator to direct byte	2	3
XRL Direct, #data	XOR immediate data to direct byte	3	3
CLR A	Clear accumulator	1	1
CPL A	Complement accumulator	1	1
RL A	Rotate accumulator left	1	1
RLC A	Rotate accumulator left through carry	1	1
RR A	Rotate accumulator right	1	1
RRC A	Rotate accumulator right though carry	1	1
SWAP A	Swap nibbles within accumulator	1	1

4.3.1.3 Data Transfer Instructions

The data transfer instructions are of three types: the core RAM, xdata RAM, and the lookup tables. The core RAM transfer includes transfer between any two core RAM locations or SFRs. These instructions can use direct, indirect, register, and immediate addressing. The xdata RAM transfer includes only the transfer between the accumulator and the xdata RAM location. It can use only indirect addressing. The lookup tables involve nothing but the read of program memory using the Indexed addressing mode. Table 4-3 lists the various data transfer instructions available.

4.3.1.4 Boolean Instructions

The 8051 core has a separate bit-addressable memory location. It has 128 bits of bit addressable RAM and a set of SFRs that are bit addressable. The instruction set includes the whole menu of bit operations such as move, set, clear, toggle, OR, and AND instructions and the conditional jump instructions. Table 4-4 on page 14 lists the available Boolean instructions.

Table 4-3. Data Transfer Instructions

Mnemonic	Description	Bytes	Cycles
MOV A,Rn	Move register to accumulator	1	1
MOV A,Direct	Move direct byte to accumulator	2	2
MOV A,@Ri	Move indirect RAM to accumulator	1	2
MOV A,#data	Move immediate data to accumulator	2	2
MOV Rn,A	Move accumulator to register	1	1
MOV Rn,Direct	Move direct byte to register	2	3
MOV Rn, #data	Move immediate data to register	2	2
MOV Direct, A	Move accumulator to direct byte	2	2
MOV Direct, Rn	Move register to direct byte	2	2
MOV Direct, Direct	Move direct byte to direct byte	3	3
MOV Direct, @Ri	Move indirect RAM to direct byte	2	3
MOV Direct, #data	Move immediate data to direct byte	3	3
MOV @Ri, A	Move accumulator to indirect RAM	1	2

[+] Feedback

Figure 5-1. EMIF Block Diagram
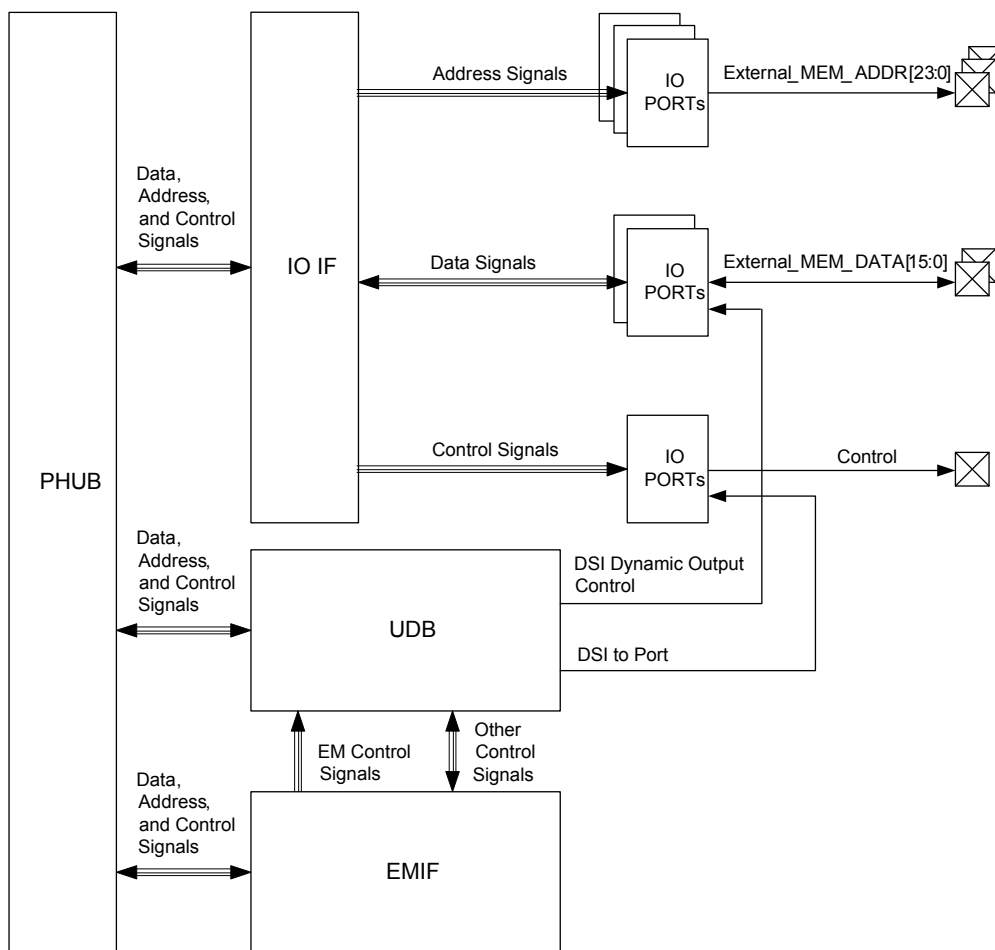
5.6 Memory Map

The CY8C36 8051 memory map is very similar to the MCS-51 memory map.

5.6.1 Code Space

The CY8C36 8051 code space is 64 KB. Only main flash exists in this space. See the "Flash Program Memory" section on page 18.

5.6.2 Internal Data Space

The CY8C36 8051 internal data space is 384 bytes, compressed within a 256-byte space. This space consists of 256 bytes of RAM (in addition to the SRAM mentioned in "Static RAM" on page 18) and a 128-byte space for Special Function Registers (SFRs). See Figure 5-2. The lowest 32 bytes are used for four banks of registers R0-R7. The next 16 bytes are bit-addressable.

Figure 5-2. 8051 Internal Data Space

In addition to the register or bit address modes used with the lower 48 bytes, the lower 128 bytes can be accessed with direct or indirect addressing. With direct addressing mode, the upper 128 bytes map to the SFRs. With indirect addressing mode, the upper 128 bytes map to RAM. Stack operations use indirect addressing; the 8051 stack space is 256 bytes. See the "Addressing Modes" section on page 11.

Figure 6-5. Power Mode Transitions
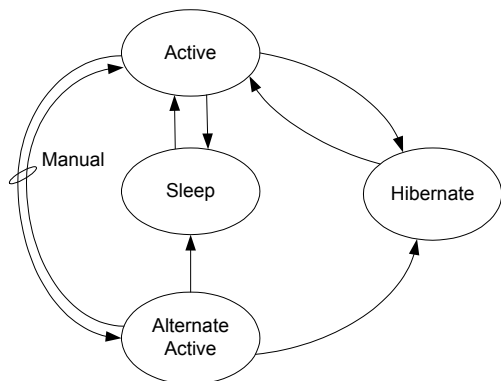
6.2.1.1 Active Mode

Active mode is the primary operating mode of the device. When in active mode, the active configuration template bits control which available resources are enabled or disabled. When a resource is disabled, the digital clocks are gated, analog bias currents are disabled, and leakage currents are reduced as appropriate. User firmware can dynamically control subsystem power by setting and clearing bits in the active configuration template. The CPU can disable itself, in which case the CPU is automatically reenabled at the next wakeup event.

When a wakeup event occurs, the global mode is always returned to active, and the CPU is automatically enabled, regardless of its template settings. Active mode is the default global power mode upon boot.

6.2.1.2 Alternate Active Mode

Alternate Active mode is very similar to Active mode. In alternate active mode, fewer subsystems are enabled, to reduce power consumption. One possible configuration is to turn off the CPU and flash, and run peripherals at full speed.

6.2.1.3 Sleep Mode

Sleep mode reduces power consumption when a resume time of 15 µs is acceptable. The wake time is used to ensure that the regulator outputs are stable enough to directly enter active mode.

6.2.1.4 Hibernate Mode

In hibernate mode nearly all of the internal functions are disabled. Internal voltages are reduced to the minimal level to keep vital systems alive. Configuration state is preserved in hibernate mode and SRAM memory is retained. GPIOs configured as digital outputs maintain their previous values and external GPIO pin interrupt settings are preserved. The device can only return from hibernate mode in response to an external I/O interrupt. The resume time from hibernate mode is less than 100 µs.

6.2.1.5 Wakeup Events

Wakeup events are configurable and can come from an interrupt or device reset. A wakeup event restores the system to active mode. Firmware enabled interrupt sources include internally generated interrupts, power supervisor, central timewheel, and I/O interrupts. Internal interrupt sources can come from a variety of peripherals, such as analog comparators and UDBs. The

central timewheel provides periodic interrupts to allow the system to wake up, poll peripherals, or perform real-time functions. Reset event sources include the external reset I/O pin (XRES), WDT, and precision reset (PRES).
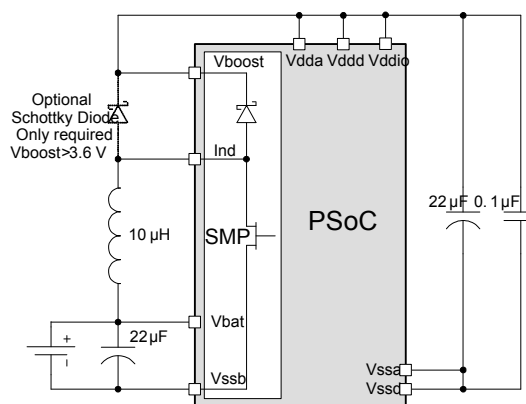
6.2.2 Boost Converter

Applications that use a supply voltage of less than 1.71 V, such as solar or single cell battery supplies, may use the on-chip boost converter. The boost converter may also be used in any system that requires a higher operating voltage than the supply provides. For instance, this includes driving 5.0 V LCD glass in a 3.3 V system. The boost converter accepts an input voltage as low as 0.5 V. With one low cost inductor it produces a selectable output voltage sourcing enough current to operate the PSoC and other on-board components.

The boost converter accepts an input voltage from 0.5 V to 5.5 V (Vbat), and can start up with Vbat as low as 0.5 V. The converter provides a user configurable output voltage of 1.8 to 5.0 V (Vboost). Vbat is typically less than Vboost; if Vbat is greater than or equal to Vboost, then Vboost will be the same as Vbat. The block can deliver up to 50 mA (Iboost) depending on configuration.

Four pins are associated with the boost converter: Vbat, Vssb, Vboost, and Ind. The boosted output voltage is sensed at the Vboost pin and must be connected directly to the chip's supply inputs. An inductor is connected between the Vbat and Ind pins. You can optimize the inductor value to increase the boost converter efficiency based on input voltage, output voltage, current and switching frequency. The external Schottky diode shown in Figure 6-6 is required only in cases when Vboost > 3.6 V.

Figure 6-6. Application for Boost Converter

The switching frequency can be set to 100 kHz, 400 kHz, 2 MHz, or 32 kHz to optimize efficiency and component cost. The 100 kHz, 400 kHz, and 2 MHz switching frequencies are generated using oscillators internal to the boost converter block. When the 32-kHz switching frequency is selected, the clock is derived from a 32 kHz external crystal oscillator. The 32-kHz external clock is primarily intended for boost standby mode.

At 2 MHz the Vboost output is limited to 2 × Vbat, and at 400 kHz Vboost is limited to 4 × Vbat.

The boost converter can be operated in two different modes: active and standby. Active mode is the normal mode of operation

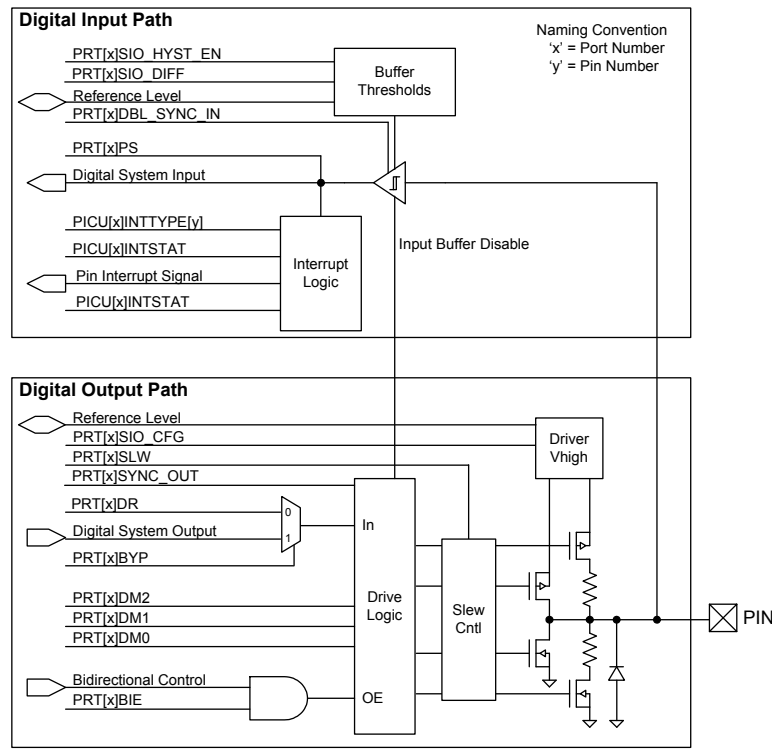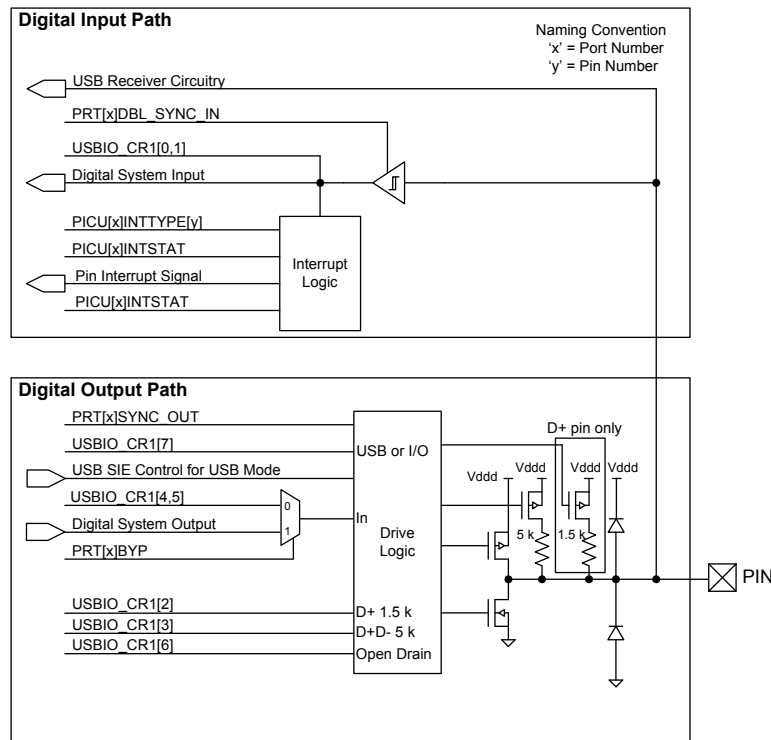**Figure 6-9. SIO Input/Output Block Diagram**

Figure 6-10. USBIO Block Diagram

[+] Feedback

■ High Impedance Analog

The default reset state with both the output driver and digital input buffer turned off. This prevents any current from flowing in the I/O's digital input buffer due to a floating voltage. This state is recommended for pins that are floating or that support an analog voltage. High impedance analog pins do not provide digital input functionality.

To achieve the lowest chip current in sleep modes, all I/Os must either be configured to the high impedance analog mode, or have their pins driven to a power supply rail by the PSoC device or by external circuitry.

■ High Impedance Digital

The input buffer is enabled for digital signal input. This is the standard high impedance (HiZ) state recommended for digital inputs.

■ Resistive pull-up or resistive pull-down

Resistive pull-up or pull-down, respectively, provides a series resistance in one of the data states and strong drive in the other. Pins can be used for digital input and output in these modes. Interfacing to mechanical switches is a common application for these modes. Resistive pull-up and pull-down are not available with SIO in regulated output mode.

■ Open Drain, Drives High and Open Drain, Drives Low

Open drain modes provide high impedance in one of the data states and strong drive in the other. Pins can be used for digital input and output in these modes. A common application for these modes is driving the I^2C bus signal lines.

■ Strong Drive

Provides a strong CMOS output drive in either high or low state. This is the standard output mode for pins. Strong Drive mode pins must not be used as inputs under normal circumstances. This mode is often used to drive digital output signals or external FETs.

■ Resistive pull-up and pull-down

Similar to the resistive pull-up and resistive pull-down modes except the pin is always in series with a resistor. The high data state is pull-up while the low data state is pull-down. This mode is most often used when other signals that may cause shorts can drive the bus. Resistive pull-up and pull-down are not available with SIO in regulated output mode.

6.4.2 Pin Registers

Registers to configure and interact with pins come in two forms that may be used interchangeably.

All I/O registers are available in the standard port form, where each bit of the register corresponds to one of the port pins. This register form is efficient for quickly reconfiguring multiple port pins at the same time.

I/O registers are also available in pin form, which combines the eight most commonly used port register bits into a single register for each pin. This enables very fast configuration changes to individual pins with a single register write.

6.4.3 Bidirectional Mode

High speed bidirectional capability allows pins to provide both the high impedance digital drive mode for input signals and a

second user selected drive mode such as strong drive (set using PRT×DM[2:0] registers) for output signals on the same pin, based on the state of an auxiliary control bus signal. The bidirectional capability is useful for processor busses and communications interfaces such as the SPI Slave MISO pin that requires dynamic hardware control of the output buffer.

The auxiliary control bus routes up to 16 UDB or digital peripheral generated output enable signals to one or more pins.

6.4.4 Slew Rate Limited Mode

GPIO and SIO pins have fast and slow output slew rate options for strong and open drain drive modes, not resistive drive modes. Because it results in reduced EMI, the slow edge rate option is recommended for signals that are not speed critical, generally less than 1 MHz. The fast slew rate is for signals between 1 MHz and 33 MHz. The slew rate is individually configurable for each pin, and is set by the PRT×SLW registers.

6.4.5 Pin Interrupts

All GPIO and SIO pins are able to generate interrupts to the system. All eight pins in each port interface to their own Port Interrupt Control Unit (PICU) and associated interrupt vector. Each pin of the port is independently configurable to detect rising edge, falling edge, both edge interrupts, or to not generate an interrupt.

Depending on the configured mode for each pin, each time an interrupt event occurs on a pin, its corresponding status bit of the interrupt status register is set to "1" and an interrupt request is sent to the interrupt controller. Each PICU has its own interrupt vector in the interrupt controller and the pin status register providing easy determination of the interrupt source down to the pin level.

Port pin interrupts remain active in all sleep modes allowing the PSoC device to wake from an externally generated interrupt.

While level sensitive interrupts are not directly supported; universal digital blocks (UDB) provide this functionality to the system when needed.

6.4.6 Input Buffer Mode

GPIO and SIO input buffers can be configured at the port level for the default CMOS input thresholds or the optional LVTTL input thresholds. All input buffers incorporate Schmitt triggers for input hysteresis. Additionally, individual pin input buffers can be disabled in any drive mode.

6.4.7 I/O Power Supplies

Up to four I/O pin power supplies are provided depending on the device and package. Each I/O supply must be less than or equal to the voltage on the chip's analog (V_{DDA}) pin. This feature allows users to provide different I/O voltage levels for different pins on the device. Refer to the specific device package pinout to determine Vddio capability for a given port and pin.

The SIO port pins support an additional regulated high output capability, as described in Adjustable Output Level.

6.4.8 Analog Connections

These connections apply only to GPIO pins. All GPIO pins may be used as analog inputs or outputs. The analog voltage present on the pin must not exceed the Vddio supply voltage to which the GPIO belongs. Each GPIO may connect to one of the analog

PSoC Creator contains all the tools necessary to complete a design, and then to maintain and extend that design for years to come. All steps of the design flow are carefully integrated and optimized for ease-of-use and to maximize productivity.

7.2 Universal Digital Block

The universal digital block (UDB) represents an evolutionary step to the next generation of PSoC embedded digital peripheral functionality. The architecture in first generation PSoC digital blocks provides coarse programmability in which a few fixed functions with a small number of options are available. The new UDB architecture is the optimal balance between configuration granularity and efficient implementation. A cornerstone of this approach is to provide the ability to customize the devices digital operation to match application requirements.

To achieve this, UDBs consist of a combination of uncommitted logic (PLD), structured logic (Datapath), and a flexible routing scheme to provide interconnect between these elements, I/O connections, and other peripherals. UDB functionality ranges from simple self contained functions that are implemented in one UDB, or even a portion of a UDB (unused resources are available for other functions), to more complex functions that require multiple UDBs. Examples of basic functions are timers, counters, CRC generators, PWMs, dead band generators, and communications functions, such as UARTs, SPI, and I^{2}C. Also, the PLD blocks and connectivity provide full featured general purpose programmable logic within the limits of the available resources.

Figure 7-6. UDB Block Diagram
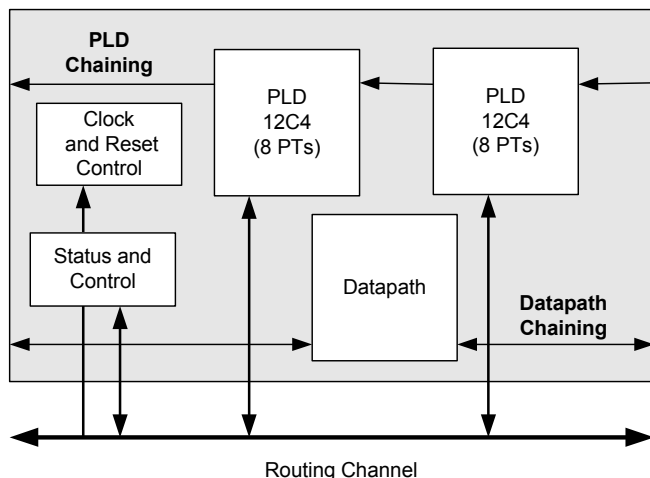

The main component blocks of the UDB are:

- PLD blocks – There are two small PLDs per UDB. These blocks take inputs from the routing array and form registered or combinational sum-of-products logic. PLDs are used to implement state machines, state bits, and combinational logic equations. PLD configuration is automatically generated from graphical primitives.

- Datapath module – This 8-bit wide datapath contains structured logic to implement a dynamically configurable ALU, a variety of compare configurations and condition generation. This block also contains input/output FIFOs, which are the primary parallel data interface between the CPU/DMA system and the UDB.

- Status and control module – The primary role of this block is to provide a way for CPU firmware to interact and synchronize with UDB operation.

- Clock and reset module – This block provides the UDB clocks and reset selection and control.

7.2.1 PLD Module

The primary purpose of the PLD blocks is to implement logic expressions, state machines, sequencers, lookup tables, and decoders. In the simplest use model, consider the PLD blocks as a standalone resource onto which general purpose RTL is synthesized and mapped. The more common and efficient use model is to create digital functions from a combination of PLD and datapath blocks, where the PLD implements only the random logic and state portion of the function while the datapath (ALU) implements the more structured elements.

Figure 7-7. PLD 12C4 Structure
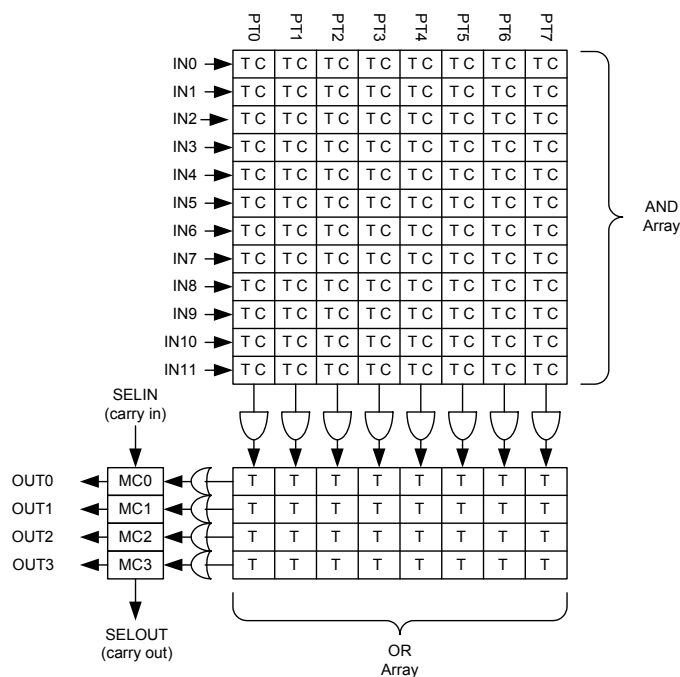
One 12C4 PLD block is shown in Figure 7-7. This PLD has 12 inputs, which feed across eight product terms. Each product term (AND function) can be from 1 to 12 inputs wide, and in a given product term, the true (T) or complement (C) of each input can be selected. The product terms are summed (OR function) to create the PLD outputs. A sum can be from 1 to 8 product terms wide. The 'C' in 12C4 indicates that the width of the OR gate (in this case 8) is constant across all outputs (rather than variable as in a 22V10 device). This PLA like structure gives maximum flexibility and insures that all inputs and outputs are permutable for ease of allocation by the software tools. There are two 12C4 PLDs in each UDB.
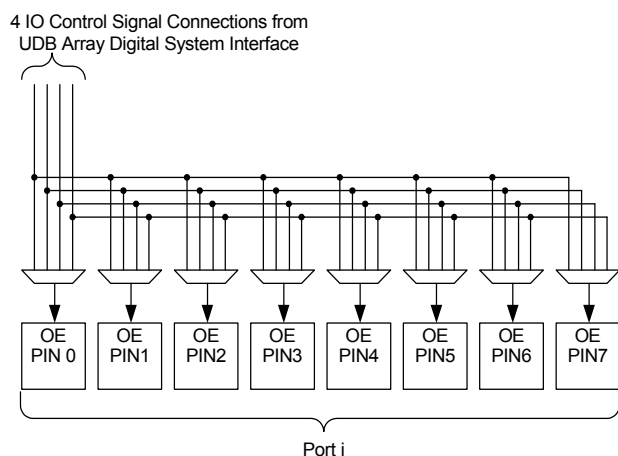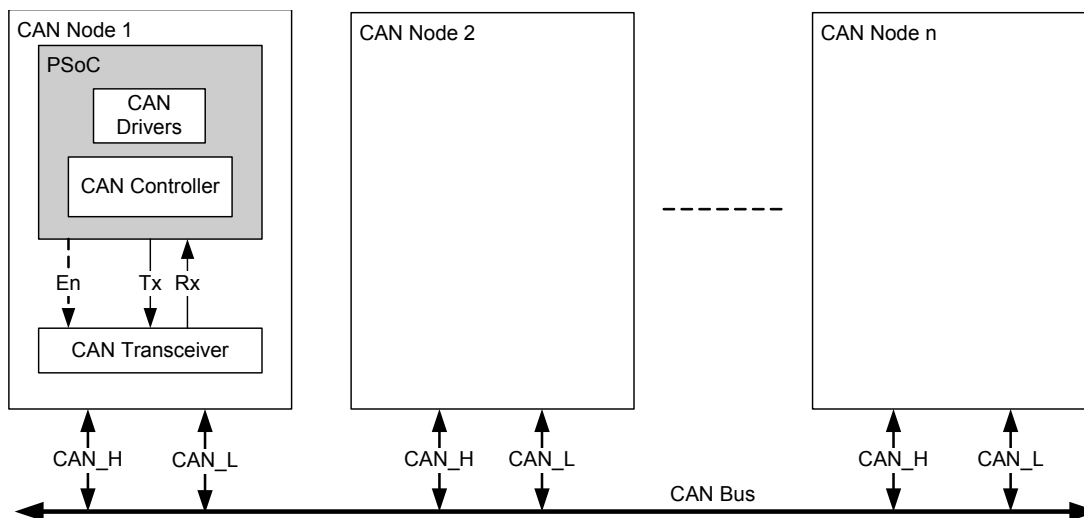
[+] Feedback

Figure 7-17. I/O Pin Output Enable Connectivity

7.5 CAN

The CAN peripheral is a fully functional CAN supporting communication baud rates up to 1 Mbps. The CAN controller implements the CAN2.0A and CAN2.0B specifications as defined in the Bosch specification and conforms to the ISO-11898-1 standard. The CAN protocol was originally designed for automotive applications with a focus on a high level of fault detection. This ensures high communication reliability at a low cost. Because of its success in automotive applications, CAN is used as a standard communication protocol for motion oriented machine control networks (CANOpen) and factory automation applications (DeviceNet). The CAN controller features allow the efficient implementation of higher level protocols without affecting the performance of the microcontroller CPU. Full configuration support is provided in PSoC Creator.

Figure 7-18. CAN Bus System Implementation

7.5.1 CAN Features

- CAN2.0A/B protocol implementation – ISO 11898 compliant
  - Standard and extended frames with up to 8 bytes of data per frame
  - Message filter capabilities
  - Remote Transmission Request (RTR) support
  - Programmable bit rate up to 1 Mbps
- Listen Only mode
- SW readable error counter and indicator
- Sleep mode: Wake the device from sleep with activity on the Rx pin
- Supports two or three wire interface to external transceiver (Tx, Rx, and Enable). The three-wire interface is compatible with the Philips PHY; the PHY is not included on-chip. The three wires can be routed to any I/O
- Enhanced interrupt controller
  - CAN receive and transmit buffers status
  - CAN controller error status including BusOff

- Receive path
  - 16 receive buffers each with its own message filter
  - Enhanced hardware message filter implementation that covers the ID, IDE, and RTR
  - DeviceNet addressing support
  - Multiple receive buffers linkable to build a larger receive message array
  - Automatic transmission request (RTR) response handler
  - Lost received message notification
- Transmit path
  - Eight transmit buffers
  - Programmable transmit priority
    - Round robin
    - Fixed priority
  - Message transmissions abort capability

7.5.2 Software Tools Support

CAN Controller configuration integrated into PSoC Creator:

- CAN Configuration walkthrough with bit timing analyzer
- Receive filter setup

The same opamps and block interfaces are also connectable to an array of resistors which allows the construction of a variety of continuous time functions.

The opamp and resistor array is programmable to perform various analog functions including

■ Naked operational amplifier – Continuous mode

■ Unity-gain buffer – Continuous mode

■ Programmable gain amplifier (PGA) – Continuous mode

■ Transimpedance amplifier (TIA) – Continuous mode

■ Up/down mixer – Continuous mode

■ Sample and hold mixer (NRZ S/H) – Switched cap mode

■ First order analog to digital modulator – Switched cap mode

8.5.1 Naked Opamp

The Naked Opamp presents both inputs and the output for connection to internal or external signals. The opamp has a unity gain bandwidth greater than 6.0 MHz and output drive current up to 650 µA. This is sufficient for buffering internal signals (such as DAC outputs) and driving external loads greater than 7.5 kΩ.

8.5.2 Unity Gain

The Unity Gain buffer is a Naked Opamp with the output directly connected to the inverting input for a gain of 1.00. It has a –3 dB bandwidth greater than 6.0 MHz.

8.5.3 PGA

The PGA amplifies an external or internal signal. The PGA can be configured to operate in inverting mode or noninverting mode. The PGA function may be configured for both positive and negative gains as high as 50 and 49 respectively. The gain is adjusted by changing the values of R1 and R2 as illustrated in Figure 8-9 on page 52. The schematic in Figure 8-9 on page 52 shows the configuration and possible resistor settings for the PGA. The gain is switched from inverting and non inverting by changing the shared select value of the both the input muxes. The bandwidth for each gain case is listed in Table 8-3.

Table 8-3. Bandwidth

Gain	Bandwidth
1	6.0 MHz
24	340 kHz
48	220 kHz
50	215 kHz

Figure 8-9. PGA Resistor Settings
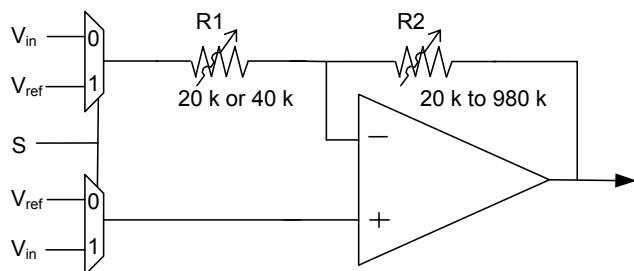
The PGA is used in applications where the input signal may not be large enough to achieve the desired resolution in the ADC, or dynamic range of another SC/CT block such as a mixer. The gain is adjustable at runtime, including changing the gain of the PGA prior to each ADC sample.

8.5.4 TIA

The Transimpedance Amplifier (TIA) converts an internal or external current to an output voltage. The TIA uses an internal feedback resistor in a continuous time configuration to convert input current to output voltage. For an input current Iin, the output voltage is Iin × Rfb +V_{REF}, where V_{REF} is the value placed on the non inverting input. The feedback resistor Rfb is programmable between 20 KΩ and 1 MΩ through a configuration register. Table 8-4 shows the possible values of Rfb and associated configuration settings.

Table 8-4. Feedback Resistor Settings

Configuration Word	Nominal R_{fb} (KΩ)
000b	20
001b	30
010b	40
011b	60
100b	120
101b	250
110b	500
111b	1000

Figure 8-10. Continuous Time TIA Schematic
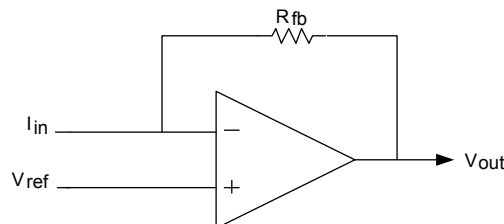
The TIA configuration is used for applications where an external sensor's output is current as a function of some type of stimulus such as temperature, light, magnetic flux etc. In a common application, the voltage DAC output can be connected to the V_{REF} TIA input to allow calibration of the external sensor bias current by adjusting the voltage DAC output voltage.

8.6 LCD Direct Drive

The PSoC Liquid Crystal Display (LCD) driver system is a highly configurable peripheral designed to allow PSoC to directly drive a broad range of LCD glass. All voltages are generated on chip, eliminating the need for external components. With a high multiplex ratio of up to 1/16, the CY8C36 family LCD driver system can drive a maximum of 736 segments. The PSoC LCD driver module was also designed with the conservative power budget of portable devices in mind, enabling different LCD drive modes and power down modes to conserve power.

11.4.2 SIO

Table 11-11. SIO DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Vinmax	Maximum input voltage	All allowed values of Vddio and Vddd, see *Section 11.2.1*	–	–	5.5	V
Vinref	Input voltage reference (Differential input mode)		0.5	–	$0.52 \times V_{DDIO}$	V
Voutref	Output voltage reference (Regulated output mode)					
		$V_{DDIO} > 3.7$	1	–	$V_{DDIO} - 1$	V
		$V_{DDIO} < 3.7$	1	–	$V_{DDIO} - 0.5$	V
V_{IH}	Input voltage high threshold					
	GPIO mode	CMOS input	$0.7 \times V_{DDIO}$	–	–	V
	Differential input mode[34]	Hysteresis disabled	SIO_ref + 0.2	–	–	V
V_{IL}	Input voltage low threshold					
	GPIO mode	CMOS input	–	–	$0.3 \times V_{DDIO}$	V
	Differential input mode[34]	Hysteresis disabled	–	–	SIO_ref – 0.2	V
V_{OH}	Output voltage high					
	Unregulated mode	I_{OH} = 4 mA, V_{DDIO} = 3.3 V	$V_{DDIO} - 0.4$	–	–	V
	Regulated mode[34]	I_{OH} = 1 mA	SIO_ref – 0.65	–	SIO_ref + 0.2	V
	Regulated mode[34]	I_{OH} = 0.1 mA	SIO_ref – 0.3	–	SIO_ref + 0.2	V
V_{OL}	Output voltage low					
		V_{DDIO} = 3.30 V, I_{OL} = 25 mA	–	–	0.8	V
		V_{DDIO} = 1.80 V, I_{OL} = 4 mA	–	–	0.4	V
Rpullup	Pull-up resistor		3.5	5.6	8.5	kΩ
Rpulldown	Pull-down resistor		3.5	5.6	8.5	kΩ
I_{IL}	Input leakage current (absolute value)[35]		–	–	–	–
	$V_{IH} \leq$ Vddsio	25 °C, Vddsio = 3.0 V, V_{IH} = 3.0 V	–	–	14	nA
	$V_{IH} >$ Vddsio	25 °C, Vddsio = 0 V, V_{IH} = 3.0 V	–	–	10	µA
C_{IN}	Input Capacitance[35]		–	–	7	pF
V_H	Input voltage hysteresis (Schmitt-Trigger)[35]	Single ended mode (GPIO mode)	–	40	–	mV
		Differential mode	–	35	–	mV
Idiode	Current through protection diode to V_{SSIO}		–	–	100	µA

Table 11-12. SIO AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
TriseF	Rise time in Fast Strong Mode (90/10%)[35]	Cload = 25 pF, V_{DDIO} = 3.3 V	–	–	12	ns
TfallF	Fall time in Fast Strong Mode (90/10%)[35]	Cload = 25 pF, V_{DDIO} = 3.3 V	–	–	12	ns
TriseS	Rise time in Slow Strong Mode (90/10%)[35]	Cload = 25 pF, V_{DDIO} = 3.0 V	–	–	75	ns
TfallS	Fall time in Slow Strong Mode (90/10%)[35]	Cload = 25 pF, V_{DDIO} = 3.0 V	–	–	60	ns

Notes
34. See Figure 6-9 on page 30 and Figure 6-12 on page 33 for more information on SIO reference.
35. Based on device characterization (Not production tested).

[+] Feedback

Table 11-19. Opamp AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
GBW	Gain-bandwidth product	Power mode = minimum, 200 pF load	1	–	–	MHz
		Power mode = low, 200 pF load	2	–	–	MHz
		Power mode = medium, 200 pF load	1	–	–	MHz
		Power mode = high, 200 pF load	3	–	–	MHz
SR	Slew rate, 20% - 80%	Power mode = low, 200 pF load	1.1	–	–	V/µs
		Power mode = medium, 200 pF load	0.9	–	–	V/µs
		Power mode = high, 200 pF load	3	–	–	V/µs
e_n	Input noise density	Power mode = high, Vdda = 5 V, at 100 kHz	–	45	–	nV/sqrtHz

Figure 11-17. Open Loop Gain and Phase vs Frequency and Temperature, Power Mode = High, Cl = 15 Pf, Vdda = 5V
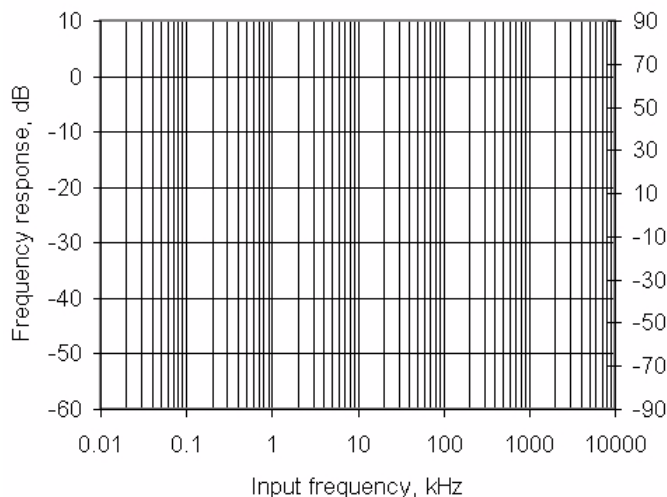
Figure 11-18. Opamp Closed Loop Frequency Response, Gain = 1, Vdda = 5V
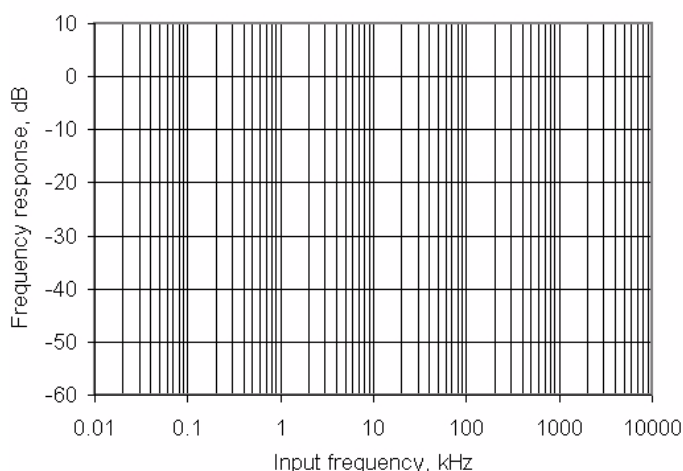
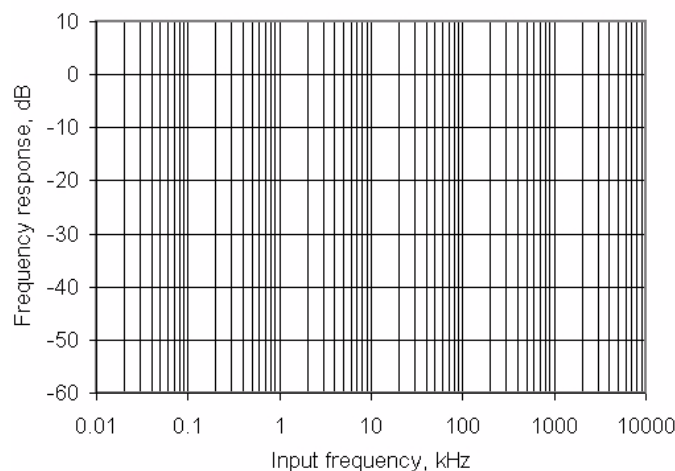**Figure 11-19. Opamp Closed Loop Frequency Response, Gain = 10, Vdda = 5V**

Figure 11-20. Opamp test Circuit for Gain = 10

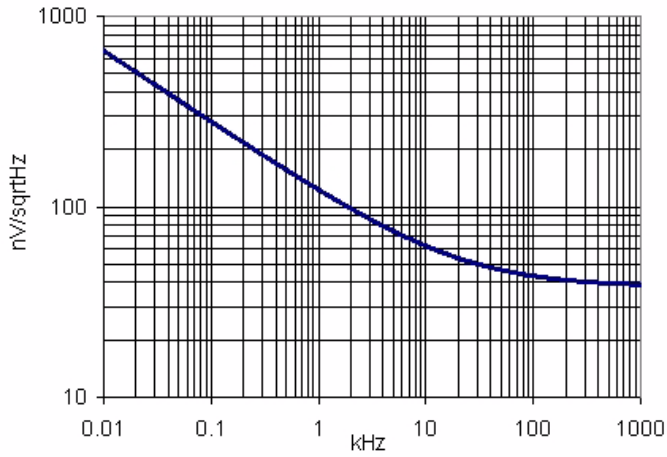**Figure 11-21. Opamp Noise vs Frequency, Power Mode = High, Vdda = 5V**
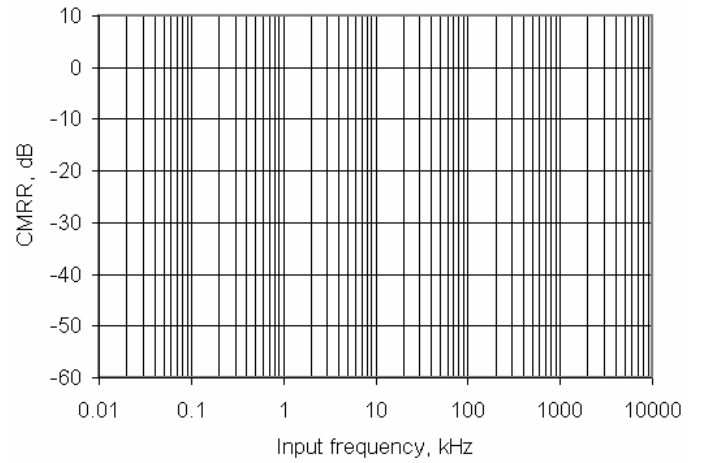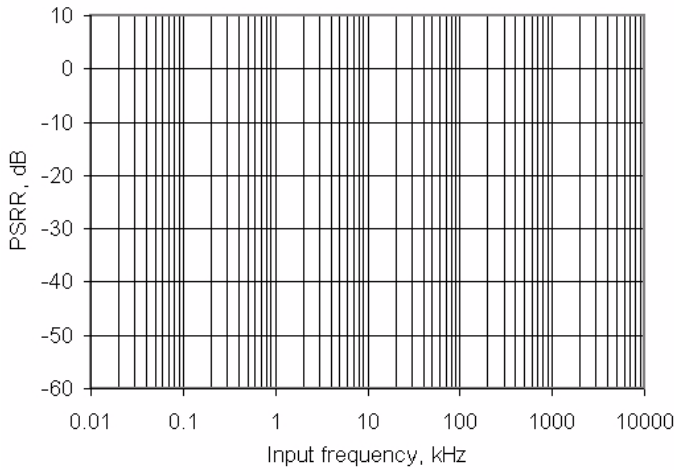

Figure 11-22. Opamp CMRR vs Frequency

Figure 11-23. Opamp PSRR vs Frequency

Note
37. Based on device characterization (Not production tested).

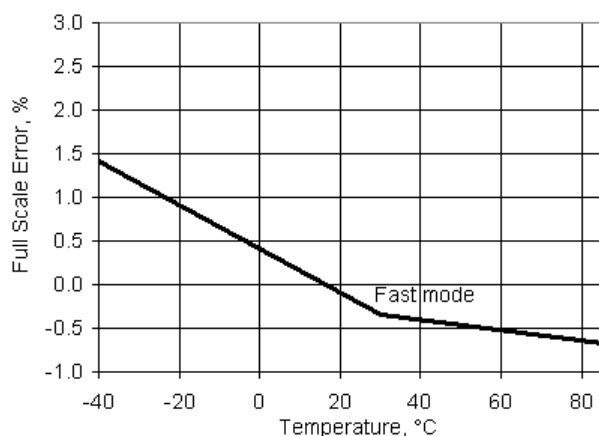**Figure 11-33. IDAC Full Scale Error vs Temperature, Range = 255 µA, Source Mode**

Figure 11-34. IDAC Full Scale Error vs Temperature, Range = 255 µA, Sink Mode
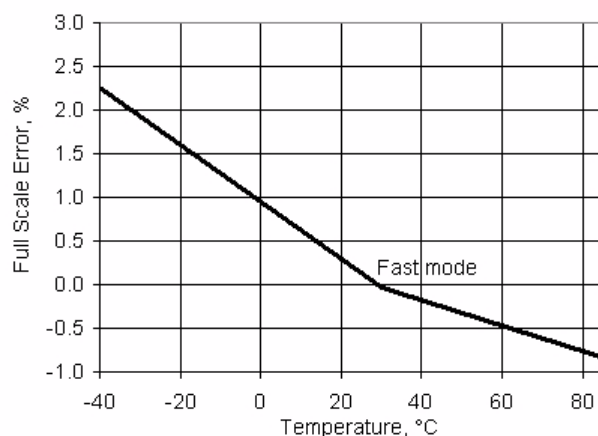

Figure 11-35. IDAC Operating Current vs Temperature, Range = 255 µA, Code = 0, Source Mode
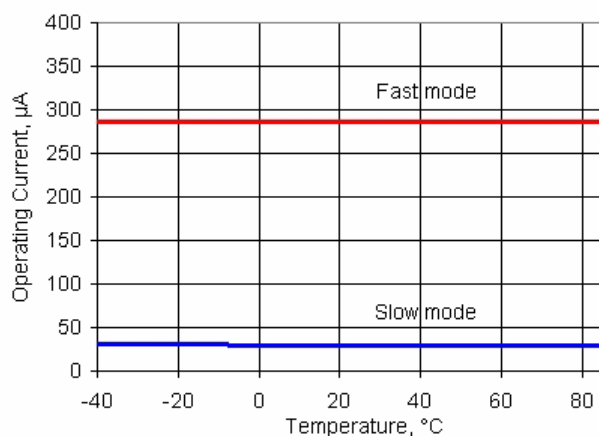

Figure 11-36. IDAC Operating Current vs Temperature, Range = 255 µA, Code = 0, Sink Mode
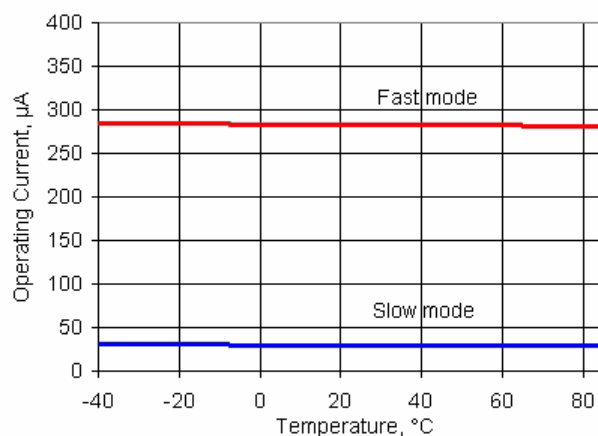

Table 11-28. IDAC AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F_{DAC}	Update rate		–	–	8	Msps
T_{SETTLE}	Settling time to 0.5 LSB	Range = 31.875 µA or 255 µA, full scale transition, fast mode, 600 Ω 15-pF load	–	–	125	ns

11.5.12 LCD Direct Drive

Table 11-38. LCD Direct Drive DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
I_{CC}	LCD system operating current	Device sleep mode with wakeup at 400-Hz rate to refresh LCDs, bus clock = 3 Mhz, Vddio = Vdda = 3 V, 4 commons, 16 segments, 1/4 duty cycle, 50 Hz frame rate, no glass connected	–	38	–	µA
I_{CC_SEG}	Current per segment driver	Strong drive mode	–	260	–	µA
V_{BIAS}	LCD bias range (V_{BIAS} refers to the main output voltage(V0) of LCD DAC)	$V_{DDA} \geq 3$ V and $V_{DDA} \geq V_{BIAS}$	2	–	5	V
	LCD bias step size	$V_{DDA} \geq 3$ V and $V_{DDA} \geq V_{BIAS}$	–	$9.1 \times V_{DDA}$	–	mV
	LCD capacitance per segment/common driver	Drivers may be combined	–	500	5000	pF
	Long term segment offset		–	–	20	mV
I_{OUT}	Output drive current per segment driver)	Vddio = 5.5V, strong drive mode	355	–	710	µA

Table 11-39. LCD Direct Drive AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
f_{LCD}	LCD frame rate		10	50	150	Hz

11.6.6 Digital Filter Block

Table 11-49. DFB DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	DFB operating current	64-tap FIR at F_{DFB}				
		100 kHz (1.3 ksps)	–	0.03	0.05	mA
		500 kHz (6.7 ksps)	–	0.16	0.27	mA
		1 MHz (13.4 ksps)	–	0.33	0.53	mA
		10 MHz (134 ksps)	–	3.3	5.3	mA
		48 MHz (644 ksps)	–	15.7	25.5	mA
		67 MHz (900 ksps)	–	21.8	35.6	mA

Table 11-50. DFB AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F_{DFB}	DFB operating frequency		DC	–	67	MHz

11.6.7 USB

Table 11-51. USB DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{USB_5}	Device supply for USB operation	USB configured, USB regulator enabled	4.35	–	5.25	V
$V_{USB\_3.3}$		USB configured, USB regulator bypassed	3.15	–	3.6	V
V_{USB_3}		USB configured, USB regulator bypassed[47]	2.85	–	3.6	V

Note
47. Rise/fall time matching (TR) not guaranteed, see USB Driver AC Specifications on page 67.

[+] Feedback

Table 11-54. Flash AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
T_{WRITE}	Row write time (erase + program)		–	–	15	ms
T_{ERASE}	Row erase time		–	–	10	ms
	Row program time		–	–	5	ms
T_{BULK}	Bulk erase time (16 KB to 64 KB)		–	–	35	ms
	Sector erase time (8 KB to 16 KB)		–	–	15	ms
	Total device program time (including JTAG, and so on)		–	–	5	seconds
	Flash endurance		100k	–	–	program/ erase cycles
	Flash data retention time, retention period measured from last erase cycle	Average ambient temp. $T_A \leq 55$ °C, 100 K erase/program cycles	20	–	–	years

11.7.2 EEPROM

Table 11-55. EEPROM DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Erase and program voltage		1.71	–	5.5	V

Table 11-56. EEPROM AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
T_{WRITE}	Single row erase/write cycle time		–	2	15	ms
	EEPROM data retention time, retention period measured from last erase cycle (up to 100 K cycles)	Average ambient temp, $T_A \leq 25$ °C, 1M erase/program cycles	20	–	–	years
		Average ambient temp, $T_A \leq 55$ °C, 100 K erase/program cycles	20	–	–	

11.7.3 Nonvolatile Latches (NVL))

Table 11-57. NVL DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Erase and program voltage	V_{DDD} pin	1.71	–	5.5	V

Table 11-58. NVL AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	NVL endurance	Programmed at 25 °C	1K	–	–	program/ erase cycles
		Programmed at 0 °C to 70 °C	100	–	–	program/ erase cycles
	NVL data retention time	Programmed at 25 °C	20	–	–	years
		Programmed at 0 °C to 70 °C	20	–	–	years

11.7.4 SRAM

Table 11-59. SRAM DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{SRAM}	SRAM retention voltage		1.2	–	–	V

Table 11-60. SRAM AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F_{SRAM}	SRAM operating frequency		DC	–	67	MHz

Table 12-1. CY8C36 Family with Single Cycle 8051 *(continued)*

Part Number	MCU Core				Analog									Digital				I/O[66]				Package	JTAG ID[67]
	CPU Speed (MHz)	Flash (KB)	SRAM (KB)	EEPROM (KB)	LCD Segment Drive	ADC	DAC	Comparator	SC/CT Analog Blocks[64]	Opamps	DFB	CapSense	UDBs[65]	16-bit Timer/PWM	FS USB	CAN 2.0b	Total I/O	GPIO	SIO	USBIO		
CY8C3666LTI-012	67	64	8	2	✔	12-bit Del-Sig	4	4	4	2	✔	✔	24	4	–	–	29	25	4	0	48-pin QFN	0×0E00C069
CY8C3666PVI-026	67	64	8	2	✔	12-bit Del-Sig	4	4	4	2	✔	✔	24	4	–	–	29	25	4	0	48-pin SSOP	0×0E01A069
CY8C3666AXI-036	67	64	8	2	✔	12-bit Del-Sig	4	4	4	4	✔	✔	24	4	✔	–	72	62	8	2	100-pin TQFP	0×0E024069
CY8C3666LTI-027	67	64	8	2	✔	12-bit Del-Sig	4	4	4	4	✔	✔	24	4	✔	–	48	38	8	2	68-pin QFN	0×0E01B069
CY8C3666LTI-050	67	64	8	2	✔	12-bit Del-Sig	4	4	4	2	✔	✔	24	4	✔	–	31	25	4	2	48-pin QFN	0×0E032069
CY8C3666PVI-057	67	64	8	2	✔	12-bit Del-Sig	4	4	4	2	✔	✔	24	4	✔	–	31	25	4	2	48-pin SSOP	0×0E039069
CY8C3666AXI-037	67	64	8	2	✔	12-bit Del-Sig	4	4	4	4	✔	✔	24	4	–	✔	70	62	8	0	100-pin TQFP	0×0E025069

Notes
64. Analog blocks support a wide variety of functionality including TIA, PGA, and mixers. See the Example Peripherals on page 35 for more information on how analog blocks can be used.
65. UDBs support a wide variety of functionality including SPI, LIN, UART, timer, counter, PWM, PRS, and others. Individual functions may use a fraction of a UDB or multiple UDBs. Multiple functions can share a single UDB. See the Example Peripherals on page 35 for more information on how UDBs can be used.
66. The I/O Count includes all types of digital I/O: GPIO, SIO, and the two USB I/O. See the I/O System and Routing on page 28 for details on the functionality of each of these types of I/O.
67. The JTAG ID has three major fields. The most significant nibble (left digit) is the version, followed by a 2 byte part number and a 3 nibble manufacturer ID.

[+] Feedback

14. Acronyms

Table 14-1. Acronyms Used in this Document

Acronym	Description
abus	analog local bus
ADC	analog-to-digital converter
AG	analog global
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an ARM data transfer bus
ALU	arithmetic logic unit
AMUXBUS	analog multiplexer bus
API	application programming interface
APSR	application program status register
ARM®	advanced RISC machine, a CPU architecture
ATM	automatic thump mode
BW	bandwidth
CAN	Controller Area Network, a communications protocol
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
DAC	digital-to-analog converter, see also IDAC, VDAC
DFB	digital filter block
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DMA	direct memory access, see also TD
DNL	differential nonlinearity, see also INL
DNU	do not use
DR	port write data registers
DRES	digital logic reset
DSI	digital system interconnect
DWT	data watchpoint and trace
ECC	error correcting code
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
EMIF	external memory interface
EOC	end of conversion
EOF	end of frame
EPSR	execution program status register
ESD	electrostatic discharge

Table 14-1. Acronyms Used in this Document *(continued)*

Acronym	Description
ETM	embedded trace macrocell
FIR	finite impulse response, see also IIR
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output, applies to a PSoC pin
HVI	high-voltage interrupt, see also LVI, LVD
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
I²C, or IIC	Inter-Integrated Circuit, a communications protocol
IIR	infinite impulse response, see also FIR
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
I/O	input/output, see also GPIO, DIO, SIO, USBIO
IPOR	initial power-on reset
IPSR	interrupt program status register
IRQ	interrupt request
ITM	instrumentation trace macrocell
LCD	liquid crystal display
LIN	Local Interconnect Network, a communications protocol.
LR	link register
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVI	low-voltage interrupt, see also HVI
LVTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit
MISO	master-in slave-out
NC	no connect
NMI	nonmaskable interrupt
NRZ	non-return-to-zero
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL
opamp	operational amplifier
PAL	programmable array logic, see also PLD
PC	program counter
PCB	printed circuit board

18. Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturers' representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products		PSoC Solutions
Automotive	cypress.com/go/automotive	psoc.cypress.com/solutions
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Interface	cypress.com/go/interface	
Lighting & Power Control	cypress.com/go/powerpsoc	
	cypress.com/go/plc	
Memory	cypress.com/go/memory	
Optical & Image Sensing	cypress.com/go/image	
PSoC	cypress.com/go/psoc	
Touch Sensing	cypress.com/go/touch	
USB Controllers	cypress.com/go/USB	
Wireless/RF	cypress.com/go/wireless	

[+] Feedback