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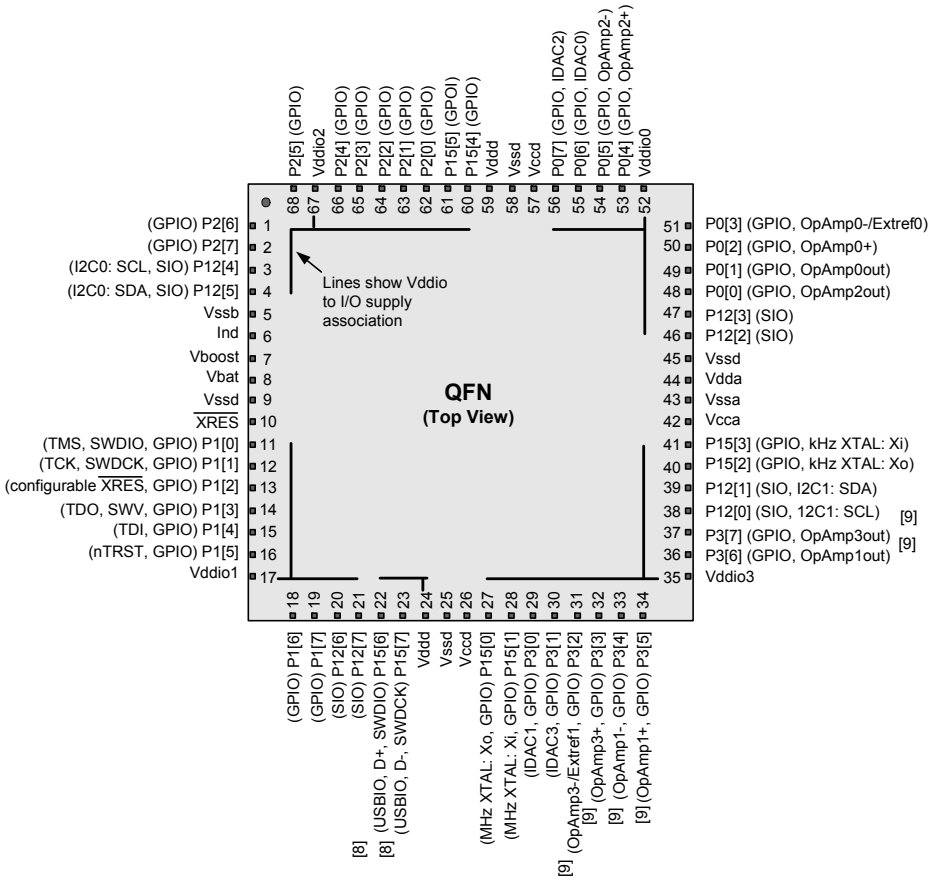
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	67MHz
Connectivity	EBI/EMI, I²C, LINbus, SPI, UART/USART, USB
Peripherals	CapSense, DMA, POR, PWM, WDT
Number of I/O	62
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x12b; D/A 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3665axi-016t

Figure 2-3. 68-pin QFN Part Pinout[10]



Notes
8. Pins are Do Not Use (DNU) on devices without USB. The pin must be left floating.
9. This feature on select devices only. See Ordering Information on page 99 for details.
10. The center pad on the QFN package should be connected to digital ground (Vssd) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floated and not connected to any other signal.

Table 4-2. Logical Instructions *(continued)*

Mnemonic	Description	Bytes	Cycles
ORL A,#data	OR immediate data to accumulator	2	2
ORL Direct, A	OR accumulator to direct byte	2	3
ORL Direct, #data	OR immediate data to direct byte	3	3
XRL A,Rn	XOR register to accumulator	1	1
XRL A,Direct	XOR direct byte to accumulator	2	2
XRL A,@Ri	XOR indirect RAM to accumulator	1	2
XRL A,#data	XOR immediate data to accumulator	2	2
XRL Direct, A	XOR accumulator to direct byte	2	3
XRL Direct, #data	XOR immediate data to direct byte	3	3
CLR A	Clear accumulator	1	1
CPL A	Complement accumulator	1	1
RL A	Rotate accumulator left	1	1
RLC A	Rotate accumulator left through carry	1	1
RR A	Rotate accumulator right	1	1
RRC A	Rotate accumulator right though carry	1	1
SWAP A	Swap nibbles within accumulator	1	1

4.3.1.3 Data Transfer Instructions

The data transfer instructions are of three types: the core RAM, xdata RAM, and the lookup tables. The core RAM transfer includes transfer between any two core RAM locations or SFRs. These instructions can use direct, indirect, register, and immediate addressing. The xdata RAM transfer includes only the transfer between the accumulator and the xdata RAM location. It can use only indirect addressing. The lookup tables involve nothing but the read of program memory using the Indexed addressing mode. Table 4-3 lists the various data transfer instructions available.

4.3.1.4 Boolean Instructions

The 8051 core has a separate bit-addressable memory location. It has 128 bits of bit addressable RAM and a set of SFRs that are bit addressable. The instruction set includes the whole menu of bit operations such as move, set, clear, toggle, OR, and AND instructions and the conditional jump instructions. Table 4-4 on page 14 lists the available Boolean instructions.

Table 4-3. Data Transfer Instructions

Mnemonic	Description	Bytes	Cycles
MOV A,Rn	Move register to accumulator	1	1
MOV A,Direct	Move direct byte to accumulator	2	2
MOV A,@Ri	Move indirect RAM to accumulator	1	2
MOV A,#data	Move immediate data to accumulator	2	2
MOV Rn,A	Move accumulator to register	1	1
MOV Rn,Direct	Move direct byte to register	2	3
MOV Rn, #data	Move immediate data to register	2	2
MOV Direct, A	Move accumulator to direct byte	2	2
MOV Direct, Rn	Move register to direct byte	2	2
MOV Direct, Direct	Move direct byte to direct byte	3	3
MOV Direct, @Ri	Move indirect RAM to direct byte	2	3
MOV Direct, #data	Move immediate data to direct byte	3	3
MOV @Ri, A	Move accumulator to indirect RAM	1	2

6.2.1 Power Modes

PSoC 3 devices have four different power modes, as shown in Table 6-1 and Table 6-2. The power modes allow a design to easily provide required functionality and processing power while simultaneously minimizing power consumption and maximizing battery life in low-power and portable devices.

PSoC 3 power modes, in order of decreasing power consumption are:

- Active
- Alternate Active
- Sleep
- Hibernate

Active is the main processing mode. Its functionality is configurable. Each power controllable subsystem is enabled or disabled by using separate power configuration template registers. In alternate active mode, fewer subsystems are enabled, reducing power. In sleep mode most resources are disabled regardless of the template settings. Sleep mode is optimized to provide timed sleep intervals and RTC functionality. The lowest power mode is hibernate, which retains register and SRAM state, but no clocks, and allows wakeup only from I/O pins. Figure 6-5 illustrates the allowable transitions between power modes.

.

Table 6-1. Power Modes

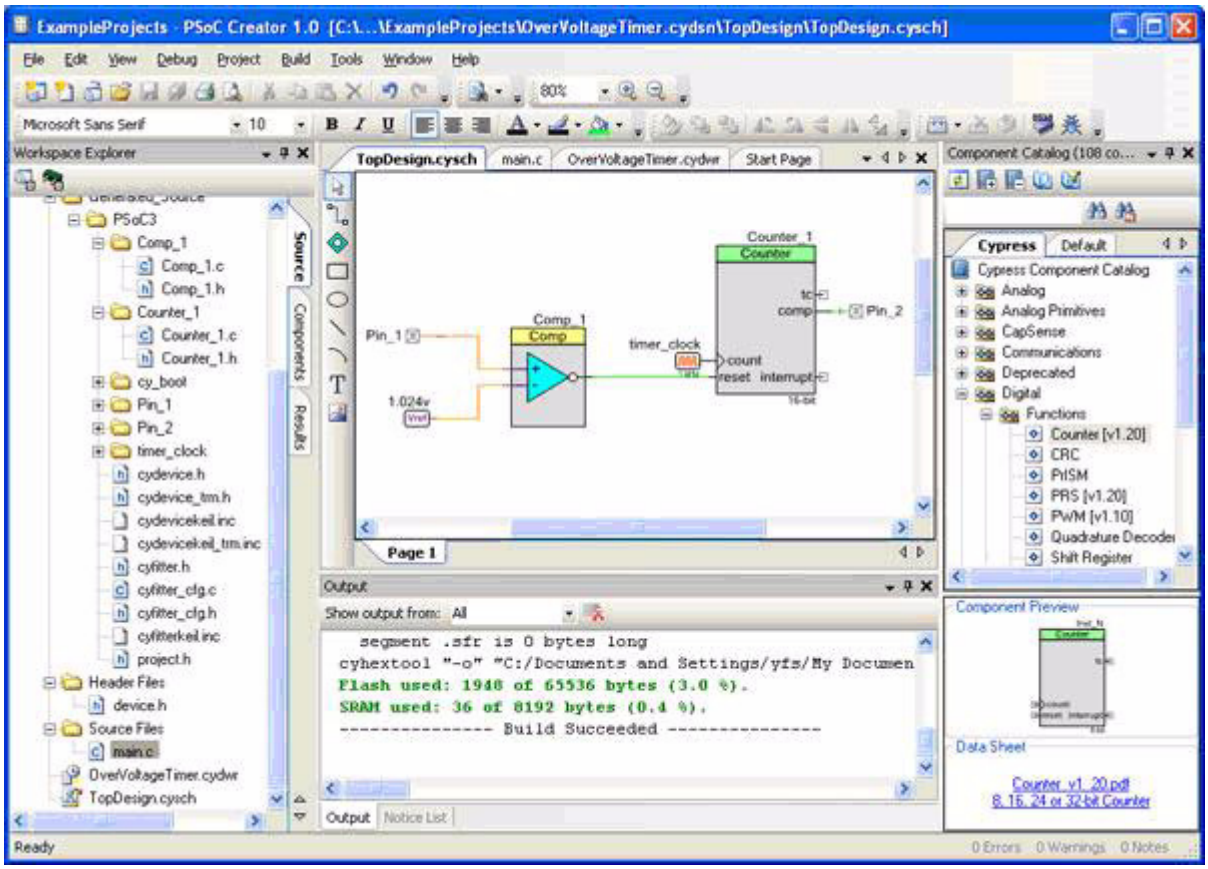
Power Modes	Description	Entry Condition	Wakeup Source	Active Clocks	Regulator
Active	Primary mode of operation, all peripherals available (programmable)	Wakeup, reset, manual register entry	Any interrupt	Any (programmable)	All regulators available. Digital and analog regulators can be disabled if external regulation used.
Alternate Active	Similar to Active mode, and is typically configured to have fewer peripherals active to reduce power. One possible configuration is to use the UDBs for processing, with the CPU turned off	Manual register entry	Any interrupt	Any (programmable)	All regulators available. Digital and analog regulators can be disabled if external regulation used.
Sleep	All subsystems automatically disabled	Manual register entry	Comparator, PICU, I^2C, RTC, CTW, LVD	ILO/kHzECO	Both digital and analog regulators buzzed. Digital and analog regulators can be disabled if external regulation used.
Hibernate	All subsystems automatically disabled Lowest power consuming mode with all peripherals and internal regulators disabled, except hibernate regulator is enabled Configuration and memory contents retained	Manual register entry	PICU	–	Only hibernate regulator active.

Table 6-2. Power Modes Wakeup Time and Power Consumption

Sleep Modes	Wakeup Time	Current (Typ)	Code Execution	Digital Resources	Analog Resources	Clock Sources Available	Wakeup Sources	Reset Sources
Active	–	1.2 mA[16]	Yes	All	All	All	–	All
Alternate Active	–	–	User defined	All	All	All	–	All
Sleep	<15 µs	1 µA	No	I^2C	Comparator	ILO/kHzECO	Comparator, PICU, I^2C, RTC, CTW, LVD	XRES, LVD, WDR
Hibernate	<100 µs	200 nA	No	None	None	None	PICU	XRES

Note
16. Bus clock off. Execute from CPU instruction buffer at 6 MHz. See Table 11-2 on page 59.

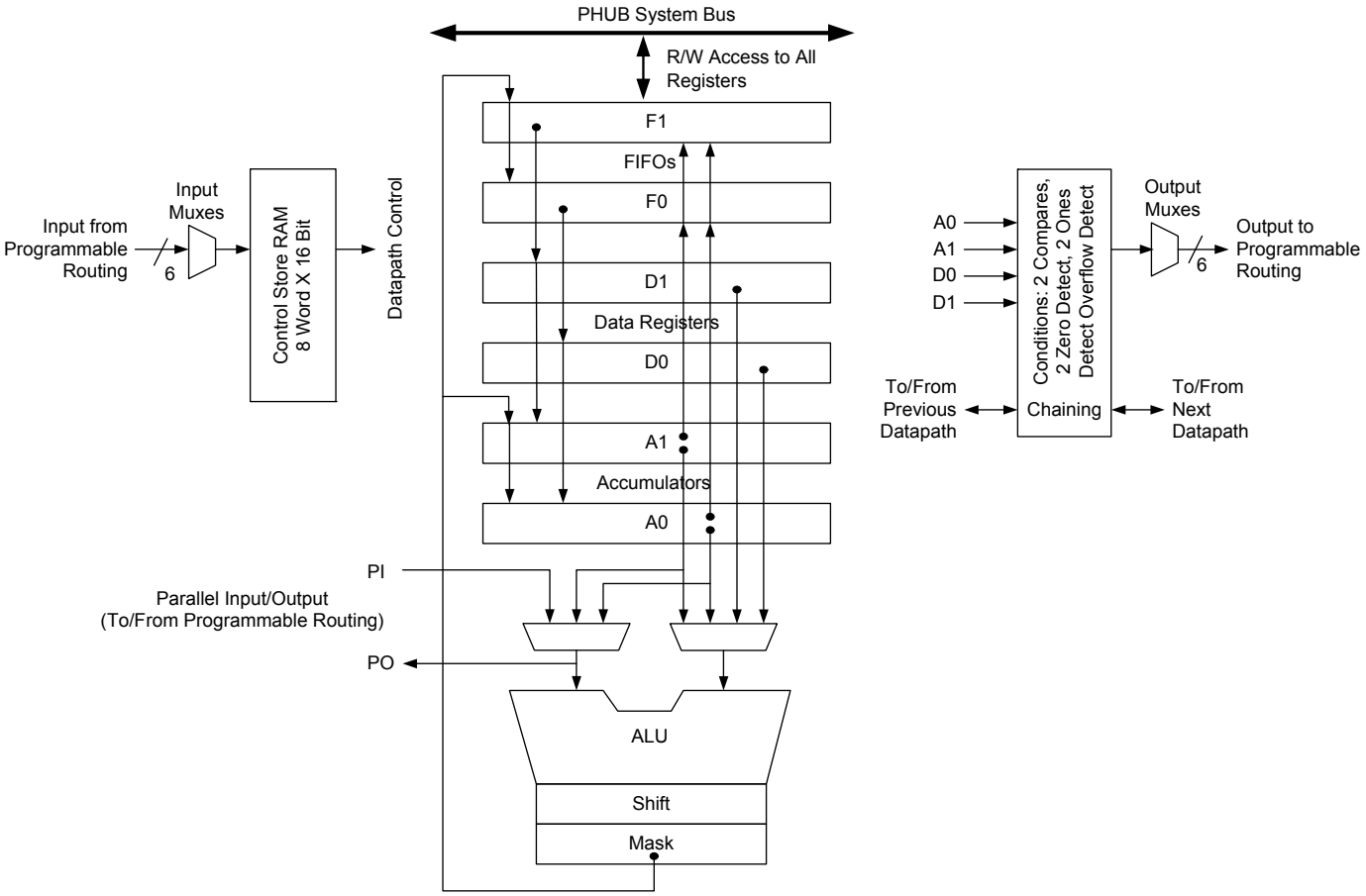
Figure 7-2. PSoC Creator Framework



7.2.2 Datapath Module

The datapath contains an 8-bit single cycle ALU, with associated compare and condition generation logic. This datapath block is optimized to implement embedded functions, such as timers, counters, integrators, PWMs, PRS, CRC, shifters and dead band generators and many others.

Figure 7-8. Datapath Top Level



7.2.2.1 Working Registers

The datapath contains six primary working registers, which are accessed by CPU firmware or DMA during normal operation.

Table 7-1. Working Datapath Registers

Name	Function	Description
A0 and A1	Accumulators	These are sources and sinks for the ALU and also sources for the compares.
D0 and D1	Data Registers	These are sources for the ALU and sources for the compares.
F0 and F1	FIFOs	These are the primary interface to the system bus. They can be a data source for the data registers and accumulators or they can capture data from the accumulators or ALU. Each FIFO is four bytes deep.

7.2.2.2 Dynamic Datapath Configuration RAM

Dynamic configuration is the ability to change the datapath function and internal configuration on a cycle-by-cycle basis, under sequencer control. This is implemented using the 8-word × 16-bit configuration RAM, which stores eight unique 16-bit wide configurations. The address input to this RAM controls the sequence, and can be routed from any block connected to the UDB routing matrix, most typically PLD logic, I/O pins, or from the outputs of this or other datapath blocks.

ALU

The ALU performs eight general purpose functions. They are:

- Increment
- Decrement
- Add
- Subtract
- Logical AND
- Logical OR
- Logical XOR
- Pass, used to pass a value through the ALU to the shift register, mask, or another UDB register

Table 11-2. DC Specifications *(continued)*

Parameter	Description	Conditions		Min	Typ	Max	Units
	Sleep Mode[26]						
	CPU = OFF RTC = ON (= ECO32K ON, in low-power mode) Sleep timer = ON (= ILO ON at 1 kHz)[27] WDT = OFF I^2C Wake = OFF Comparator = OFF POR = ON Boost = OFF SIO pins in single ended input, unregulated output mode	$V_{DD} = V_{DDIO}$ = 4.5–5.5 V	T = –40 °C	–	–	–	µA
			T = 25 °C	–	–	–	µA
			T = 85 °C	–	–	–	µA
		$V_{DD} = V_{DDIO}$ = 2.7–3.6 V	T = –40 °C	–	–	–	µA
			T = 25 °C	–	1	–	µA
			T = 85 °C	–	–	–	µA
		$V_{DD} = V_{DDIO}$ = 1.71–1.95 V	T = –40 °C	–	–	–	µA
			T = 25 °C	–	–	–	µA
			T = 85 °C	–	–	–	µA
	Comparator = ON CPU = OFF RTC = OFF Sleep timer = OFF WDT = OFF I2C Wake = OFF POR = ON Boost = OFF SIO pins in single ended input, unregulated output mode	$V_{DD} = V_{DDIO}$ = 2.7–3.6 V	T = 25 °C	–	–	–	µA
	I2C Wake = ON CPU = OFF RTC = OFF Sleep timer = OFF WDT = OFF Comparator = OFF POR = ON Boost = OFF SIO pins in single ended input, unregulated output mode	$V_{DD} = V_{DDIO}$ = 2.7–3.6 V	T = 25 °C	–	–	–	µA
	Hibernate Mode[26]						
	Hibernate mode current All regulators and oscillators off. SRAM retention GPIO interrupts are active Boost = OFF SIO pins in single ended input, unregulated output mode	$V_{DD} = V_{DDIO}$ = 4.5–5.5 V	T = –40 °C	–	–	–	nA
			T = 25 °C	–	–	–	nA
			T = 85 °C	–	–	–	nA
		$V_{DD} = V_{DDIO}$ = 2.7–3.6 V	T = –40 °C	–	–	–	nA
			T = 25 °C	–	200	–	nA
			T = 85 °C	–	–	–	nA
		$V_{DD} = V_{DDIO}$ = 1.71–1.95 V	T = –40 °C	–	–	–	nA
			T = 25 °C	–	–	–	nA
			T = 85 °C	–	–	–	nA

Notes
25. The current consumption of additional peripherals that are implemented only in programmed logic blocks can be found in their respective datasheets, available in PSoC Creator, the integrated design environment. To compute total current, find CPU current at frequency of interest and add peripheral currents for your particular system from the device datasheet and component datasheets.
26. If V_{CCD} and V_{CCA} are externally regulated, the voltage difference between V_{CCD} and V_{CCA} must be less than 50 mV.
27. Sleep timer generates periodic interrupts to wake up the CPU. This specification applies only to those times that the CPU is off.

11.3 Power Regulators

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.3.1 Digital Core Regulator

Table 11-4. Digital Core Regulator DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{DDD}	Input voltage		1.8	–	5.5	V
V_{CCD}	Output voltage		–	1.80	–	V
	Regulator output capacitor	± 10%, ×5R ceramic or better. The two V_{CCD} pins must be shorted together, with as short a trace as possible, see Power System on page 24	–	1	–	µF

11.3.2 Analog Core Regulator

Table 11-5. Analog Core Regulator DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{DDA}	Input voltage		1.8	–	5.5	V
V_{CCA}	Output voltage		–	1.80	–	V
	Regulator output capacitor	±10%, ×5R ceramic or better	–	1	–	µF

11.3.3 Inductive Boost Regulator.

Table 11-6. Inductive Boost Regulator DC Specifications

Unless otherwise specified, operating conditions are: V_{BAT} = 2.4 V, V_{OUT} = 2.7 V, I_{OUT} = 40 mA, F_{SW} = 400 kHz, L_{BOOST} = 22 µH, C_{BOOST} = 22 µF || 0.1 µF

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{BAT}	Input voltage Includes startup	T=-35 °C to +65 °C	0.5	–	5.5	V
		Over entire temperature range	0.68	–	5.5	V
I_{OUT}	Load current[29, 30]	V_{BAT} = 1.6 – 3.6 V, V_{OUT} = 3.6 – 5.0 V, external diode	–	–	50	mA
		V_{BAT} = 1.6 – 3.6 V, V_{OUT} = 1.6 – 3.6 V, internal diode	–	–	75	mA
		V_{BAT} = 0.8 – 1.6 V, V_{OUT} = 1.6 – 3.6 V, internal diode	–	–	30	mA
		V_{BAT} = 0.8 – 1.6 V, V_{OUT} = 3.6 – 5.0 V, external diode	–	–	20	mA
		V_{BAT} = 0.5 – 0.8 V, V_{OUT} = 1.6 – 3.6 V, internal diode	–	–	15	mA
I_{LPK}	Inductor peak current		–	–	700	mA
I_Q	Quiescent current	Boost active mode	–	200	–	µA
		Boost standby mode, 32 khz external crystal oscillator, I_{OUT} < 1 µA	–	12	–	µA

Notes
29. For output voltages above 3.6 V, an external diode is required.
30. Maximum output current applies for output voltages ≤ 4x input voltage.

Table 11-6. Inductive Boost Regulator DC Specifications *(continued)*

Unless otherwise specified, operating conditions are: V_{BAT} = 2.4 V, V_{OUT} = 2.7 V, I_{OUT} = 40 mA, F_{SW} = 400 kHz, L_{BOOST} = 22 µH, C_{BOOST} = 22 µF || 0.1 µF

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{OUT}	Boost voltage range[31, 32]					
	1.8 V		1.71	1.80	1.89	V
	1.9 V		1.81	1.90	2.00	V
	2.0 V		1.90	2.00	2.10	V
	2.4 V		2.28	2.40	2.52	V
	2.7 V		2.57	2.70	2.84	V
	3.0 V		2.85	3.00	3.15	V
	3.3 V		3.14	3.30	3.47	V
	3.6 V		3.42	3.60	3.78	V
	5.0 V	External diode required	4.75	5.00	5.25	V
Reg_{LOAD}	Load regulation		–	–	3.8	%
Reg_{LINE}	Line regulation		–	–	4.1	%
η_{OUT}	Efficiency	L_{BOOST} = 10 µH	70	85	–	%
		L_{BOOST} = 22 µH	82	90	–	%

Table 11-7. Inductive Boost Regulator AC Specifications

Unless otherwise specified, operating conditions are: V_{BAT} = 2.4 V, V_{OUT} = 2.7 V, I_{OUT} = 40 mA, F_{SW} = 400 kHz, L_{BOOST} = 22 µH, C_{BOOST} = 22 µF || 0.1 µF.

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{RIPPLE}	Ripple voltage (peak-to-peak)	V_{OUT} = 1.8 V, F_{SW} = 400 kHz, I_{OUT} = 10 mA	–	–	100	mV
F_{SW}	Switching frequency		–	0.1, 0.4, or 2	–	MHz

Table 11-8. Recommended External Components for Boost Circuit

Parameter	Description	Conditions	Min	Typ	Max	Units
L_{BOOST}	Boost inductor		4.7	10	47	µH
C_{BOOST}	Filter capacitor[31]		10	22	47	µF
I_F	External Schottky diode average forward current	External Schottky diode is required for V_{OUT} > 3.6 V	1	–	–	A
V_R			20	–	–	V

Notes
31. Based on device characterization (Not production tested).
32. At boost frequency of 2 MHz, Vboost is limited to 2 x Vbat. At 400 kHz, Vboost is limited to 4 x Vbat.

Table 11-12. SIO AC Specifications *(continued)*

Parameter	Description	Conditions	Min	Typ	Max	Units
Fsioout	SIO output operating frequency					
	3.3 V < V_{DDIO} < 5.5 V, Unregulated output (GPIO) mode, fast strong drive mode	90/10% V_{DDIO} into 25 pF	–	–	33	MHz
	1.71 V < V_{DDIO} < 3.3 V, Unregulated output (GPIO) mode, fast strong drive mode	90/10% V_{DDIO} into 25 pF	–	–	16	MHz
	3.3 V < V_{DDIO} < 5.5 V, Unregulated output (GPIO) mode, slow strong drive mode	90/10% V_{DDIO} into 25 pF	–	–	5	MHz
	1.71 V < V_{DDIO} < 3.3 V, Unregulated output (GPIO) mode, slow strong drive mode	90/10% V_{DDIO} into 25 pF	–	–	4	MHz
	3.3 V < V_{DDIO} < 5.5 V, Regulated output mode, fast strong drive mode	Output continuously switching into 25 pF	–	–	20	MHz
	1.71 V < V_{DDIO} < 3.3 V, Regulated output mode, fast strong drive mode	Output continuously switching into 25 pF	–	–	10	MHz
	1.71 V < V_{DDIO} < 5.5 V, Regulated output mode, slow strong drive mode	Output continuously switching into 25 pF	–	–	2.5	MHz
Fsioin	SIO input operating frequency					
	1.71 V ≤ V_{DDIO} ≤ 5.5 V	90/10% V_{DDIO}	–	–	66	MHz

11.4.3 USBIO

For operation in GPIO mode, the standard range for V_{DDD} applies, see Device Level Specifications on page 59.

Table 11-13. USBIO DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Rusbi	USB D+ pull-up resistance	With idle bus	0.900	–	1.575	kΩ
Rusba	USB D+ pull-up resistance	While receiving traffic	1.425	–	3.090	kΩ
Vohusb	Static output high	15 kΩ ±5% to Vss, internal pull-up enabled	2.8	–	3.6	V
Volusb	Static output low	15 kΩ ±5% to Vss, internal pull-up enabled	–	–	0.3	V
Vohgpio	Output voltage high, GPIO mode	I_{OH} = 4 mA, V_{DDD} ≥ 3 V	2.4	–	–	V
Volgpio	Output voltage low, GPIO mode	I_{OL} = 4 mA, V_{DDD} ≥ 3 V	–	–	0.3	V
Vdi	Differential input sensitivity	|(D+)–(D–)|	–	–	0.2	V
Vcm	Differential input common mode range	–	0.8	–	2.5	V
Vse	Single ended receiver threshold	–	0.8	–	2	V
Rps2	PS/2 pull-up resistance	In PS/2 mode, with PS/2 pull-up enabled	3	–	7	kΩ
Rext	External USB series resistor	In series with each USB pin	21.78 (–1%)	22	22.22 (+1%)	Ω
Zo	USB driver output impedance	Including Rext	28	–	44	Ω
C_{IN}	USB transceiver input capacitance		–	–	20	pF
I_{IL}	Input leakage current (absolute value)	25 °C, V_{DDD} = 3.0 V	–	–	2	nA

Figure 11-27. IDAC INL vs Input Code, Range = 255 µA, Source Mode

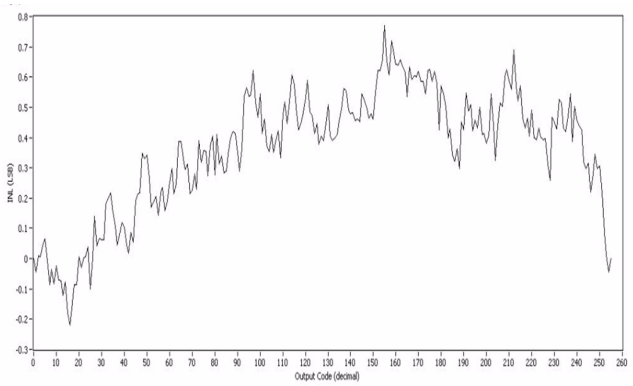


Figure 11-28. IDAC INL vs Input Code, Range = 255 µA, Sink Mode

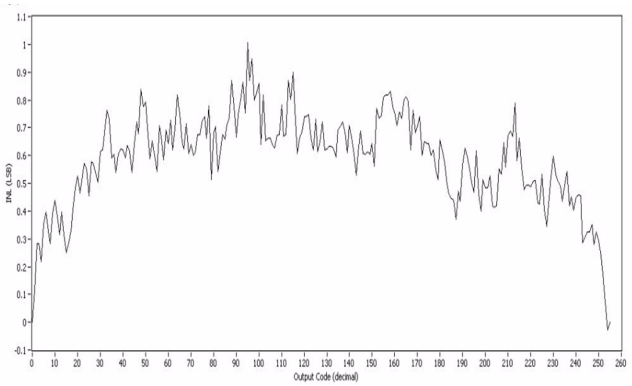


Figure 11-29. IDAC DNL vs Input Code, Range = 255 µA, Source Mode

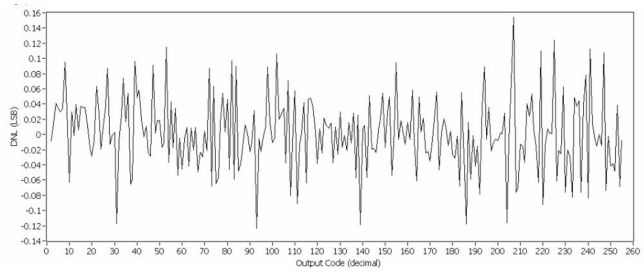


Figure 11-30. IDAC DNL vs Input Code, Range = 255 µA, Sink Mode

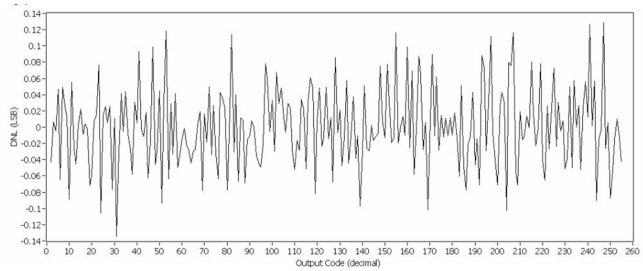


Figure 11-31. IDAC INL vs Temperature, Range = 255 µA, Fast Mode

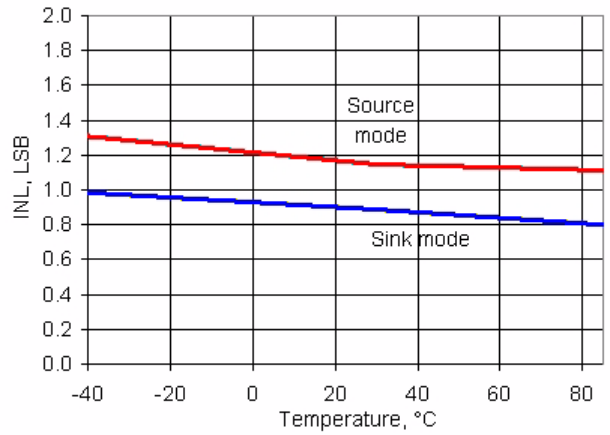


Figure 11-32. IDAC DNL vs Temperature, Range = 255 µA, Fast Mode

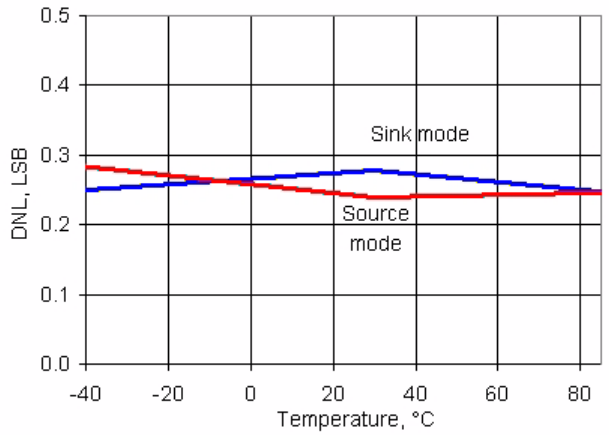


Figure 11-33. IDAC Full Scale Error vs Temperature, Range = 255 µA, Source Mode

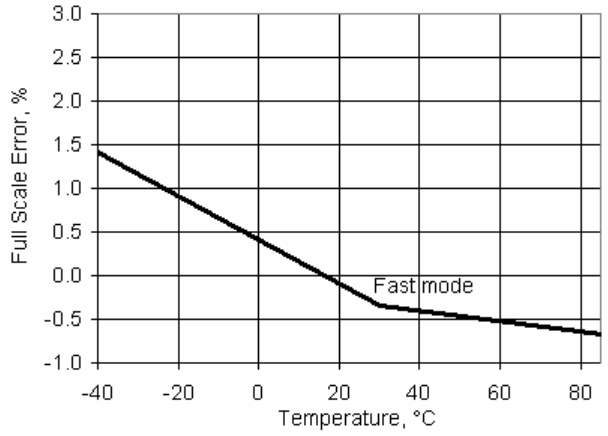


Figure 11-34. IDAC Full Scale Error vs Temperature, Range = 255 µA, Sink Mode

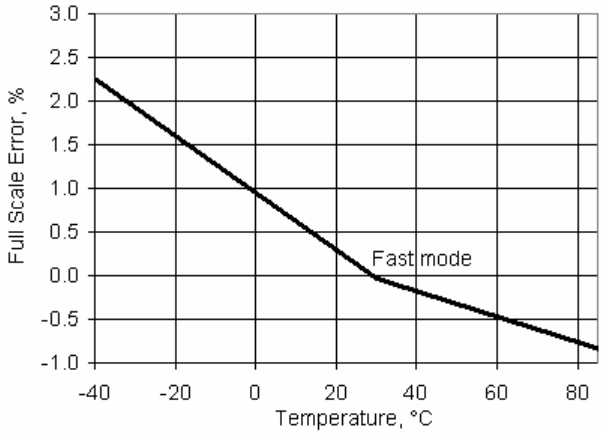


Figure 11-35. IDAC Operating Current vs Temperature, Range = 255 µA, Code = 0, Source Mode

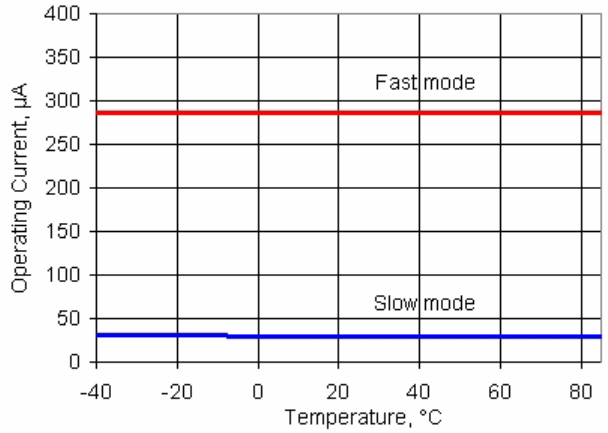


Figure 11-36. IDAC Operating Current vs Temperature, Range = 255 µA, Code = 0, Sink Mode

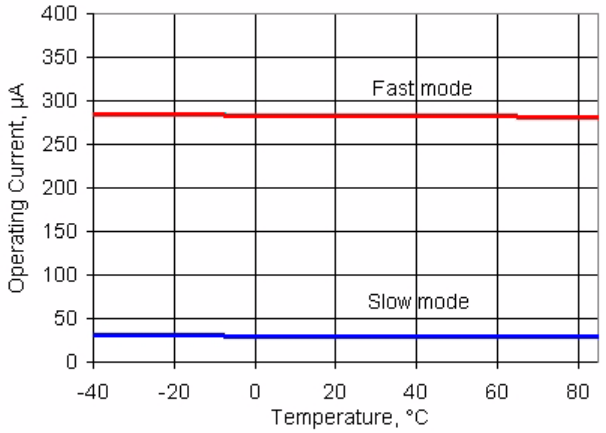


Table 11-28. IDAC AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F_{DAC}	Update rate		–	–	8	Msps
T_{SETTLE}	Settling time to 0.5 LSB	Range = 31.875 µA or 255 µA, full scale transition, fast mode, 600 Ω 15-pF load	–	–	125	ns

11.5.7 Voltage Digital to Analog Converter (VDAC)

See the VDAC component datasheet in PSoC Creator for full electrical specifications and APIs.

Unless otherwise specified, all charts and graphs show typical values.

Table 11-29. VDAC DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Resolution		–	8	–	bits
INL1	Integral nonlinearity	1 V scale	–	±2.1	±2.5	LSB
DNL1	Differential nonlinearity	1 V scale	–	±0.3	±1	LSB
Rout	Output resistance	1 V scale	–	4	–	kΩ
		4 V scale	–	16	–	kΩ
V_{OUT}	Output voltage range, code = 255	1 V scale	–	1	–	V
		4 V scale, Vdda = 5 V	–	4	–	V
	Monotonicity		–	–	Yes	–
V_{OS}	Zero scale error		–	0	±0.9	LSB
Eg	Gain error	1 V scale, 25 °C	–	–	±2.5	%
		4 V scale, 25 °C	–	–	±2.5	%
TC_Eg	Temperature coefficient, gain error	1 V scale, 25 °C	–	–	0.03	%FSR / °C
		4 V scale, 25 °C	–	–	0.03	%FSR / °C
I_{DD}	Operating current	Slow mode	–	–	100	µA
		Fast mode	–	–	500	µA

Figure 11-37. VDAC INL vs Input Code, 1 V Mode

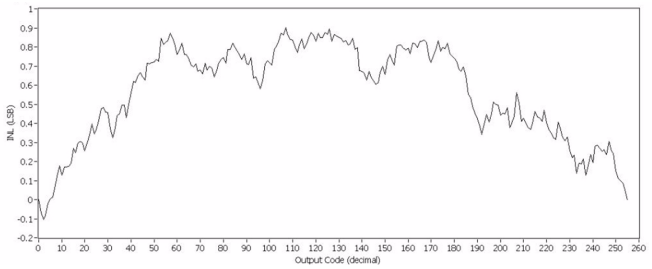


Figure 11-38. VDAC DNL vs Input Code, 1 V Mode

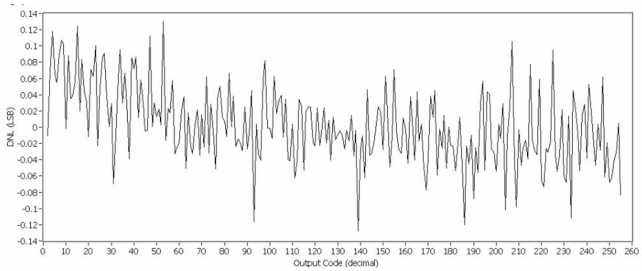


Figure 11-39. VDAC INL vs Temperature, 1 V Mode

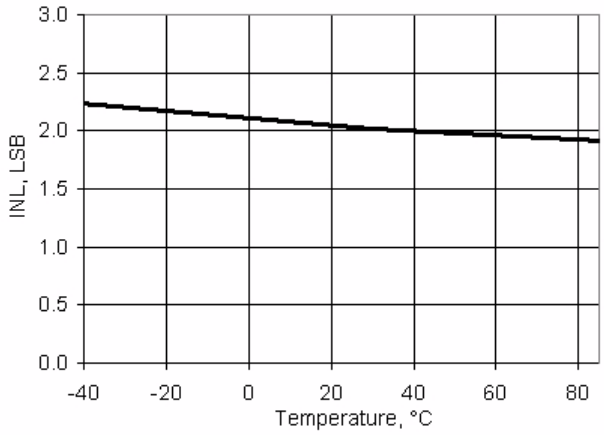
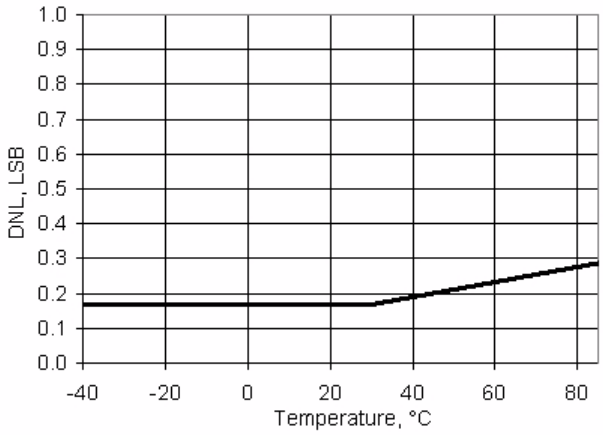


Figure 11-40. VDAC DNL vs Temperature, 1 V Mode



11.6 Digital Peripherals

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.6.1 Timer

The following specifications apply to the Timer/Counter/PWM peripheral in timer mode. Timers can also be implemented in UDBs; for more information, see the Timer component datasheet in PSoC Creator.

Table 11-40. Timer DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Block current consumption	16-bit timer, at listed input clock frequency	–	–	–	µA
	3 MHz		–	15	–	µA
	12 MHz		–	60	–	µA
	48 MHz		–	260	–	µA
	67 MHz		–	350	–	µA

Table 11-41. Timer AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Operating frequency		DC	–	67	MHz
	Capture pulse width (Internal)		15	–	–	ns
	Capture pulse width (external)		30	–	–	ns
	Timer resolution		15	–	–	ns
	Enable pulse width		15	–	–	ns
	Enable pulse width (external)		30	–	–	ns
	Reset pulse width		15	–	–	ns
	Reset pulse width (external)		30	–	–	ns

11.6.2 Counter

The following specifications apply to the Timer/Counter/PWM peripheral, in counter mode. Counters can also be implemented in UDBs; for more information, see the Counter component datasheet in PSoC Creator.

Table 11-42. Counter DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Block current consumption	16–bit counter, at listed input clock frequency	–	–	–	µA
	3 MHz		–	15	–	µA
	12 MHz		–	60	–	µA
	48 MHz		–	260	–	µA
	67 MHz		–	350	–	µA

Table 11-43. Counter AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Operating frequency		DC	–	67	MHz
	Capture pulse		15	–	–	ns
	Resolution		15	–	–	ns
	Pulse width		15	–	–	ns
	Pulse width (external)		30	–	–	ns
	Enable pulse width		15	–	–	ns
	Enable pulse width (external)		30	–	–	ns
	Reset pulse width		15	–	–	ns
	Reset pulse width (external)		30	–	–	ns

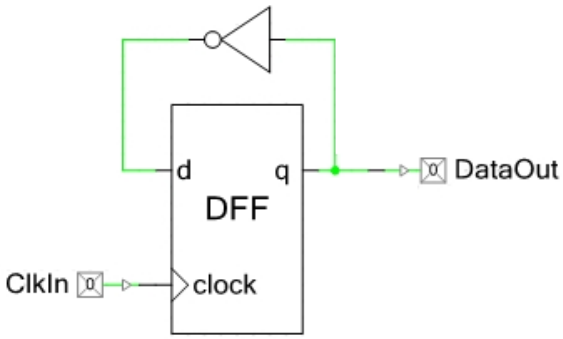
11.6.8 Universal Digital Blocks (UDBs)

PSoC Creator provides a library of prebuilt and tested standard digital peripherals (UART, SPI, LIN, PRS, CRC, timer, counter, PWM, AND, OR, and so on) that are mapped to the UDB array. See the component datasheets in PSoC Creator for full AC/DC specifications, APIs, and example code.

Table 11-52. UDB AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Datapath Performance						
F_{MAX_TIMER}	Maximum frequency of 16-bit timer in a UDB pair		–	–	67	MHz
F_{MAX_ADDER}	Maximum frequency of 16-bit adder in a UDB pair		–	–	67	MHz
F_{MAX_CRC}	Maximum frequency of 16-bit CRC/PRS in a UDB pair		–	–	67	MHz
PLD Performance						
F_{MAX_PLD}	Maximum frequency of a two-pass PLD function in a UDB pair		–	–	67	MHz
Clock to Output Performance						
t_{CLK_OUT}	Propagation delay for clock in to data out, see Figure 11-49.	25 °C, Vddd ≥ 2.7 V	–	20	25	ns
t_{CLK_OUT}	Propagation delay for clock in to data out, see Figure 11-49.	Worst-case placement, routing, and pin selection	–	–	55	ns

Figure 11-49. Clock to Output Performance



11.7 Memory

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.7.1 Flash

Table 11-53. Flash DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Erase and program voltage	V_{DDD} pin	1.71	–	5.5	V

Figure 11-52. Synchronous Read Cycle Timing

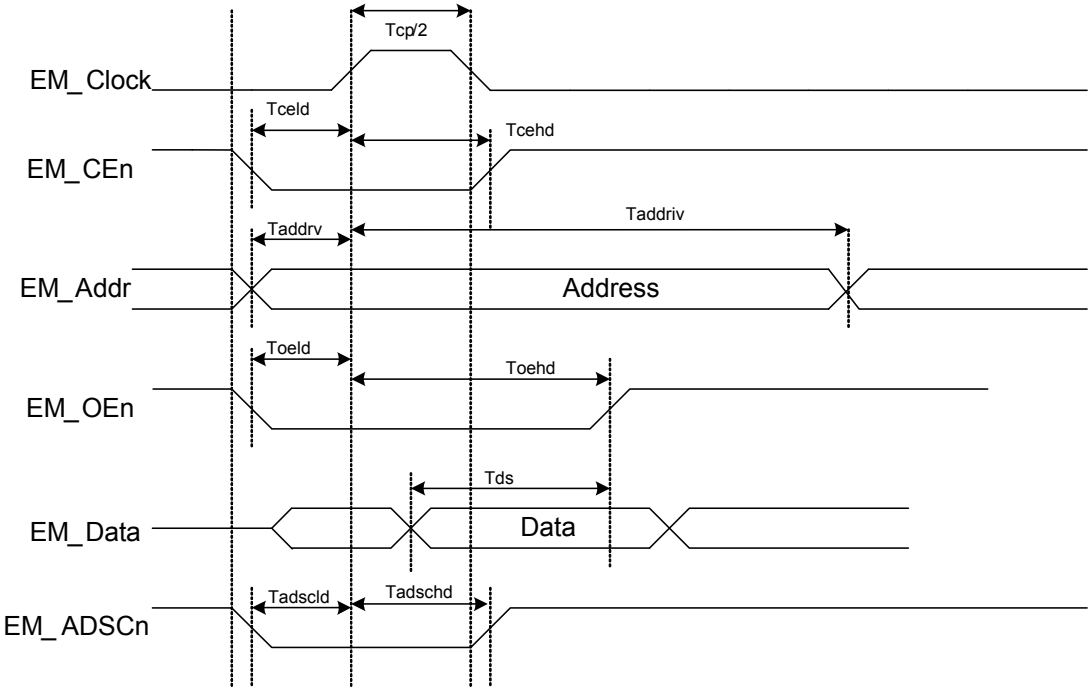


Table 11-63. Synchronous Read Cycle Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
T	EMIF clock period[50]	Vdda ≥ 3.3 V	30.3	–	–	nS
Tcp/2	EM_Clock pulse high		T/2	–	–	nS
Tceld	EM_CEn low to EM_Clock high		5	–	–	nS
Tcehd	EM_Clock high to EM_CEn high		T/2 – 5	–	–	nS
Taddrv	EM_Addr valid to EM_Clock high		5	–	–	nS
Taddriv	EM_Clock high to EM_Addr invalid		T/2 – 5	–	–	nS
Toeld	EM_OEn low to EM_Clock high		5	–	–	nS
Toehd	EM_Clock high to EM_OEn high		T	–	–	nS
Tds	Data valid before EM_OEn high		T + 15	–	–	nS
Tadscld	EM_ADSCn low to EM_Clock high		5	–	–	nS
Tadschd	EM_Clock high to EM_ADSCn high		T/2 – 5	–	–	nS

Note
50. Limited by GPIO output frequency, see Table 11-10 on page 64.

Figure 11-53. Synchronous Write Cycle Timing

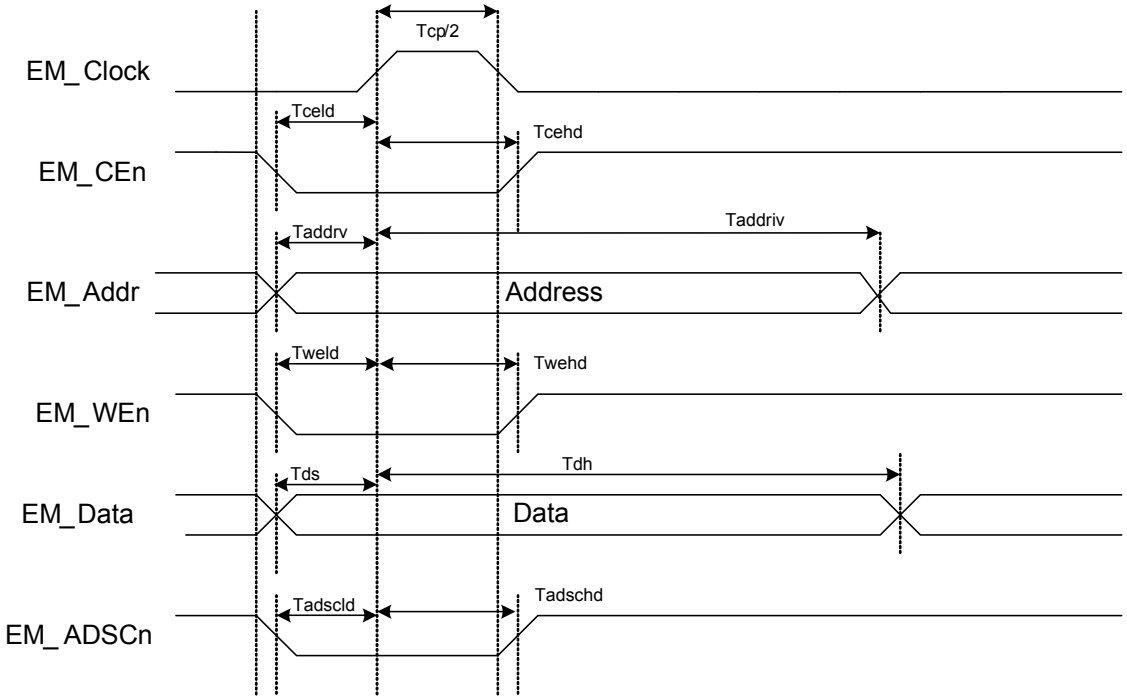


Table 11-64. Synchronous Write Cycle Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
T	EMIF clock Period[51]	Vdda ≥ 3.3 V	30.3	–	–	nS
Tcp/2	EM_Clock pulse high		T/2	–	–	nS
Tceld	EM_CEn low to EM_Clock high		5	–	–	nS
Tcehd	EM_Clock high to EM_CEn high		T/2 – 5	–	–	nS
Taddrv	EM_Addr valid to EM_Clock high		5	–	–	nS
Taddriv	EM_Clock high to EM_Addr invalid		T/2 – 5	–	–	nS
Tweld	EM_WEn low to EM_Clock high		5	–	–	nS
Twehd	EM_Clock high to EM_WEn high		T/2 – 5	–	–	nS
Tds	Data valid before EM_Clock high		5	–	–	nS
Tdh	Data invalid after EM_Clock high		T	–	–	nS
Tadscld	EM_ADSCn low to EM_Clock high		5	–	–	nS
Tadschd	EM_Clock high to EM_ADSCn high		T/2 – 5	–	–	nS

Note
51. Limited by GPIO output frequency, see Table 11-10 on page 64.

11.8.3 Interrupt Controller

Table 11-69. Interrupt Controller AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Delay from interrupt signal input to ISR code execution from ISR code	Includes worse case completion of longest instruction DIV with 6 cycles	–	–	25	Tcy CPU

11.8.4 JTAG Interface

Table 11-70. JTAG Interface AC Specifications[52]

Parameter	Description	Conditions	Min	Typ	Max	Units
f_TCK	TCK frequency	3.3 V ≤ V_{DDD} ≤ 5 V	–	–	14[53]	MHz
		1.71 V ≤ V_{DDD} < 3.3 V	–	–	7[53]	MHz
T_TDI_setup	TDI setup before TCK high		(T/10) – 5	–	–	ns
T_TMS_setup	TMS setup before TCK high		T/4	–	–	
T_TDI_hold	TDI, TMS hold after TCK high	T = 1/f_TCK	T/4	–	–	
T_TDO_valid	TCK low to TDO valid	T = 1/f_TCK	2T/5	–	–	
T_TDO_hold	TDO hold after TCK high	T = 1/f_TCK	T/4	–	–	
	TCK to device outputs valid		–	–	2T/5	

11.8.5 SWD Interface

Table 11-71. SWD Interface AC Specifications[52]

Parameter	Description	Conditions	Min	Typ	Max	Units
f_SWDCK	SWDCLK frequency	3.3 V ≤ V_{DDD} ≤ 5 V	–	–	14[54]	MHz
		1.71 V ≤ V_{DDD} < 3.3 V	–	–	7[54]	MHz
		1.71 V ≤ V_{DDD} < 3.3 V, SWD over USBIO pins	–	–	5.5[54]	MHz
T_SWDI_setup	SWDIO input setup before SWDCK high	T = 1/f_SWDCK	T/4	–	–	–
T_SWDI_hold	SWDIO input hold after SWDCK high	T = 1/f_SWDCK	T/4	–	–	–
T_SWDO_valid	SWDCK low to SWDIO output valid	T = 1/f_SWDCK	2T/5	–	–	–
T_SWDO_hold	SWDIO output hold after SWDCK high	T = 1/f_SWDCK	T/4	–	–	–

11.8.6 SWV Interface

Table 11-72. SWV Interface AC Specifications[52]

Parameter	Description	Conditions	Min	Typ	Max	Units
	SWV mode SWV bit rate		–	–	33	Mbit

Notes
52. Based on device characterization (Not production tested).
53. f_TCK must also be no more than 1/3 CPU clock frequency.
54. f_SWDCK must also be no more than 1/3 CPU clock frequency.

14. Acronyms

Table 14-1. Acronyms Used in this Document

Acronym	Description
abus	analog local bus
ADC	analog-to-digital converter
AG	analog global
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an ARM data transfer bus
ALU	arithmetic logic unit
AMUXBUS	analog multiplexer bus
API	application programming interface
APSR	application program status register
ARM®	advanced RISC machine, a CPU architecture
ATM	automatic thump mode
BW	bandwidth
CAN	Controller Area Network, a communications protocol
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
DAC	digital-to-analog converter, see also IDAC, VDAC
DFB	digital filter block
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DMA	direct memory access, see also TD
DNL	differential nonlinearity, see also INL
DNU	do not use
DR	port write data registers
DRES	digital logic reset
DSI	digital system interconnect
DWT	data watchpoint and trace
ECC	error correcting code
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
EMIF	external memory interface
EOC	end of conversion
EOF	end of frame
EPSR	execution program status register
ESD	electrostatic discharge

Table 14-1. Acronyms Used in this Document *(continued)*

Acronym	Description
ETM	embedded trace macrocell
FIR	finite impulse response, see also IIR
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output, applies to a PSoC pin
HVI	high-voltage interrupt, see also LVI, LVD
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
IIR	infinite impulse response, see also FIR
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
I/O	input/output, see also GPIO, DIO, SIO, USBIO
IPOR	initial power-on reset
IPSR	interrupt program status register
IRQ	interrupt request
ITM	instrumentation trace macrocell
LCD	liquid crystal display
LIN	Local Interconnect Network, a communications protocol.
LR	link register
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVI	low-voltage interrupt, see also HVI
LVTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit
MISO	master-in slave-out
NC	no connect
NMI	nonmaskable interrupt
NRZ	non-return-to-zero
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL
opamp	operational amplifier
PAL	programmable array logic, see also PLD
PC	program counter
PCB	printed circuit board

Table 14-1. Acronyms Used in this Document *(continued)*

Acronym	Description
PGA	programmable gain amplifier
PHUB	peripheral hub
PHY	physical layer
PICU	port interrupt control unit
PLA	programmable logic array
PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration datasheet
POR	power-on reset
PRES	precise power-on reset
PRS	pseudo random sequence
PS	port read data register
PSoC®	Programmable System-on-Chip™
PSRR	power supply rejection ratio
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I^2C serial clock
SDA	I^2C serial data
S/H	sample and hold
SINAD	signal to noise and distortion ratio
SIO	special input/output, GPIO with advanced features. See GPIO.

Table 14-1. Acronyms Used in this Document *(continued)*

Acronym	Description
SOC	start of conversion
SOF	start of frame
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory
SRES	software reset
SWD	serial wire debug, a test protocol
SWV	single-wire viewer
TD	transaction descriptor, see also DMA
THD	total harmonic distortion
TIA	transimpedance amplifier
TRM	technical reference manual
TTL	transistor-transistor logic
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UDB	universal digital block
USB	Universal Serial Bus
USBIO	USB input/output, PSoC pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset I/O pin
XTAL	crystal

15. Reference Documents

PSoC® 3, PSoC® 5 Architecture TRM

PSoC® 3 Registers TRM

Description Title: PSoC® 3: CY8C36 Family Datasheet Programmable System-on-Chip (PSoC®) Document Number: 001-53413				
*D	2903576	04/01/10	MKEA	Updated Vb pin in PCB Schematic Updated Tstartup parameter in AC Specifications table Added Load regulation and Line regulation parameters to Inductive Boost Regulator DC Specifications table Updated I_{CC} parameter in LCD Direct Drive DC Specs table Updated I_{OUT} parameter in LCD Direct Drive DC Specs table Updated Table 6-2 and Table 6-3 Added bullets on CapSense in page 1; added CapSense column in Section 12 Removed some references to footnote [1] Changed INC_Rn cycles from 3 to 2 (Table 4-1) Added footnote in PLL AC Specification table Added PLL intermediate frequency row with footnote in PLL AC Specs table Added UDBs subsection under 11.6 Digital Peripherals Updated Figure 2-6 (PCB Layout) Updated Pin Descriptions section and modified Figures 6-6, 6-8, 6-9 Updated LVD in Tables 6-2 and 6-3; modified Low-power modes bullet in page 1 Added note to Figures 2-5 and 6-2; Updated Figure 6-2 to add capacitors for V_{DDA} and V_{DDD} pins. Changed V_{REF} from 0.9 to 0.1% Updated boost converter section (6.2.2) Updated Tstartup values in Table 11-3. Removed IPOR rows from Table 11-68. Updated 6.3.1.1, Power Voltage Level Monitors. Updated section 5.2 and Table 11-2 to correct suggestion of execution from flash. Updated V_{REF} specs in Table 11-21. Updated IDAC uncompensated gain error in Table 11-25. Updated Delay from Interrupt signal input to ISR code execution from ISR code in Table11- 72. Removed other line in table. Added sentence to last paragraph of section 6.1.1.3. Updated T_{RESP}, high and low-power modes, in Table 11-24. Updated f_TCK values in Table 11-73 and f_SWDCK values in Table 11-74. Updated SNR condition in Table 11-20. Corrected unit of measurement in Table 11-21. Updated sleep wakeup time in Table 6-3 and Tsleep in Table 11-3. Added 1.71 V <= V_{DDD} < 3.3 V, SWD over USBIO pins value to Table 11-74. Removed mention of hibernate reset (HRES) from page 1 features, Table 6-3, Section 6.2.1.4, Section 6.3, and Section 6.3.1.1. Change PPOR/PRES to TBDs in Section 6.3.1.1, Section 6.4.1.6 (changed PPOR to reset), Table 11-3 (changed PPOR to PRES), Table 11-68 (changed title, values TBD), and Table 11-69 (changed PPOR_TR to PRES_TR). Added sentence saying that LVD circuits can generate a reset to Section 6.3.1.1. Changed I_{DD} values on page 1, page 5, and Table 11-2. Changed resume time value in Section 6.2.1.3. Changed ESD HBM value in Table 11-1. Changed sample rate row in Table 11-20. Removed V_{DDA} = 1.65 V rows and changed BWag value in Table 11-22. Changed V_{IOFF} values and changed CMRR value in Table 11-23. Changed INL max value in Table 11-27. Added max value to the Quiescent current specs in Tables 11-29 and 11-31. Changed occurrences of “Block” to “Row” and deleted the “ECC not included” footnote in Table 11-57. Changed max response time value in Tables 11-69 and 11-71. Changed the Startup time in Table 11-79. Added condition to intermediate frequency row in Table 11-85. Added row to Table 11-69. Added brown out note to Section 11.8.1.