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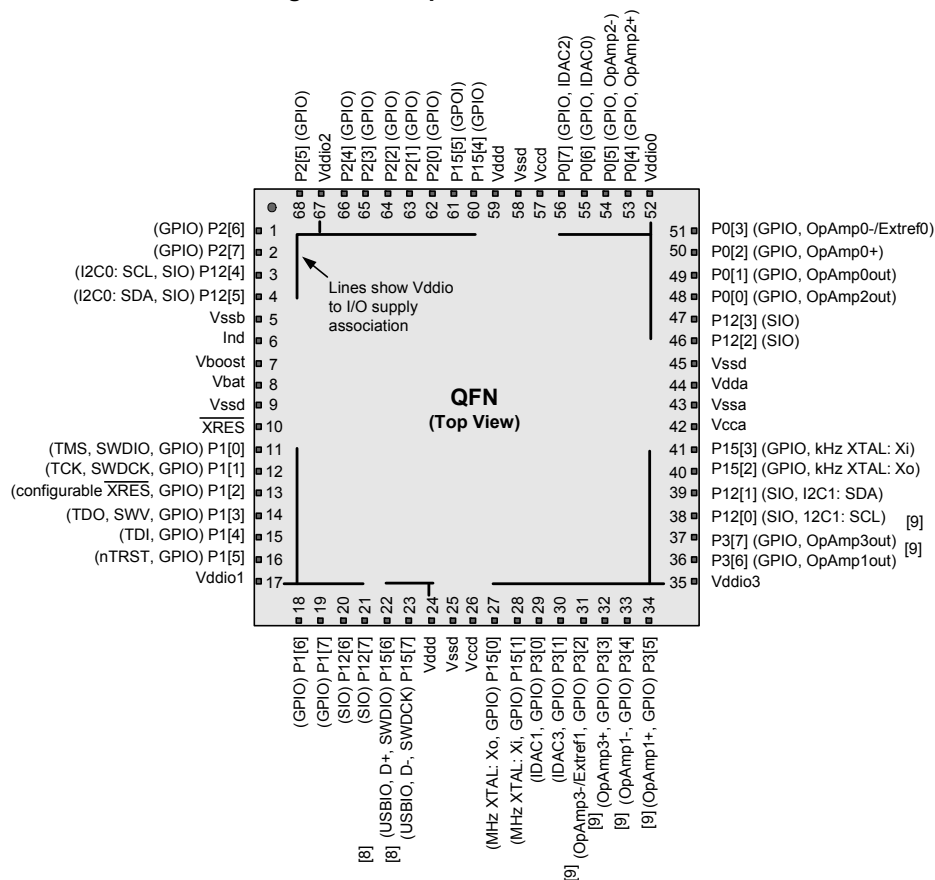
"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	67MHz
Connectivity	EBI/EMI, I ² C, LINbus, SPI, UART/USART, USB
Peripherals	CapSense, DMA, LCD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x12b; D/A 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-BSSOP (0.295", 7.50mm Width)
Supplier Device Package	48-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3666pvi-057

Figure 2-3. 68-pin QFN Part Pinout^[10]



Notes

8. Pins are Do Not Use (DNU) on devices without USB. The pin must be left floating.
9. This feature on select devices only. See [Ordering Information](#) on page 99 for details.
10. The center pad on the QFN package should be connected to digital ground (Vssd) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floated and not connected to any other signal.

Table 4-1. Arithmetic Instructions

Mnemonic	Description	Bytes	Cycles
ADD A,Rn	Add register to accumulator	1	1
ADD A,Direct	Add direct byte to accumulator	2	2
ADD A,@Ri	Add indirect RAM to accumulator	1	2
ADD A,#data	Add immediate data to accumulator	2	2
ADDC A,Rn	Add register to accumulator with carry	1	1
ADDC A,Direct	Add direct byte to accumulator with carry	2	2
ADDC A,@Ri	Add indirect RAM to accumulator with carry	1	2
ADDC A,#data	Add immediate data to accumulator with carry	2	2
SUBB A,Rn	Subtract register from accumulator with borrow	1	1
SUBB A,Direct	Subtract direct byte from accumulator with borrow	2	2
SUBB A,@Ri	Subtract indirect RAM from accumulator with borrow	1	2
SUBB A,#data	Subtract immediate data from accumulator with borrow	2	2
INC A	Increment accumulator	1	1
INC Rn	Increment register	1	2
INC Direct	Increment direct byte	2	3
INC @Ri	Increment indirect RAM	1	3
DEC A	Decrement accumulator	1	1
DEC Rn	Decrement register	1	2
DEC Direct	Decrement direct byte	2	3
DEC @Ri	Decrement indirect RAM	1	3
INC DPTR	Increment data pointer	1	1
MUL	Multiply accumulator and B	1	2
DIV	Divide accumulator by B	1	6
DAA	Decimal adjust accumulator	1	3

4.3.1.2 Logical Instructions

The logical instructions perform Boolean operations such as AND, OR, XOR on bytes, rotate of accumulator contents, and swap of nibbles in an accumulator. The Boolean operations on the bytes are performed on the bit-by-bit basis. [Table 4-2](#) on page 12 shows the list of logical instructions and their description.

Table 4-2. Logical Instructions

Mnemonic	Description	Bytes	Cycles
ANL A,Rn	AND register to accumulator	1	1
ANL A,Direct	AND direct byte to accumulator	2	2
ANL A,@Ri	AND indirect RAM to accumulator	1	2
ANL A,#data	AND immediate data to accumulator	2	2
ANL Direct, A	AND accumulator to direct byte	2	3
ANL Direct, #data	AND immediate data to direct byte	3	3
ORL A,Rn	OR register to accumulator	1	1
ORL A,Direct	OR direct byte to accumulator	2	2
ORL A,@Ri	OR indirect RAM to accumulator	1	2

5. Memory

5.1 Static RAM

CY8C36 Static RAM (SRAM) is used for temporary data storage. Up to 8 KB of SRAM is provided and can be accessed by the 8051 or the DMA controller. See [Memory Map](#) on page 19. Simultaneous access of SRAM by the 8051 and the DMA controller is possible if different 4-KB blocks are accessed.

5.2 Flash Program Memory

Flash memory in PSoC devices provides nonvolatile storage for user firmware, user configuration data, bulk data storage, and optional ECC data. The main flash memory area contains up to 64 KB of user program space.

Up to an additional 8 KB of flash space is available for ECC. If ECC is not used this space can store device configuration data and bulk user data. User code may not be run out of the ECC flash memory section. ECC can correct one bit error and detect two bit errors per 8 bytes of firmware memory; an interrupt can be generated when an error is detected.

Flash is read in units of rows; each row is 9 bytes wide with 8 bytes of data and 1 byte of ECC data. When a row is read, the data bytes are copied into an 8-byte instruction buffer. The CPU fetches its instructions from this buffer, for improved CPU performance.

Flash programming is performed through a special interface and preempts code execution out of flash. The flash programming interface performs flash erasing, programming and setting code protection levels. Flash in-system serial programming (ISSP), typically used for production programming, is possible through both the SWD and JTAG interfaces. In-system programming, typically used for bootloaders, is also possible using serial interfaces such as I²C, USB, UART, and SPI, or any communications protocol.

5.3 Flash Security

All PSoC devices include a flexible flash-protection model that prevents access and visibility to on-chip flash memory. This prevents duplication or reverse engineering of proprietary code. Flash memory is organized in blocks, where each block contains 256 bytes of program or data and 32 bytes of ECC or configuration data. A total of up to 256 blocks is provided on 64-KB flash devices.

The device offers the ability to assign one of four protection levels to each row of flash. [Table 5-1](#) lists the protection modes available. Flash protection levels can only be changed by performing a complete flash erase. The Full Protection and Field Upgrade settings disable external access (through a debugging tool such as PSoC Creator, for example). If your application requires code update through a boot loader, then use the Field Upgrade setting. Use the Unprotected setting only when no security is needed in your application. The PSoC device also offers an advanced security feature called Device Security which permanently disables all test, programming, and debug ports, protecting your application from external access (see [Device Security](#) on page 56). For more information about how to take full advantage of the security features in PSoC, see the [PSoC 3 TRM](#).

Table 5-1. Flash Protection

Protection Setting	Allowed	Not Allowed
Unprotected	External read and write + internal read and write	–
Factory Upgrade	External write + internal read and write	External read
Field Upgrade	Internal read and write	External read and write
Full Protection	Internal read	External read and write + internal write

Disclaimer

Note the following details of the flash code protection features on Cypress devices.

Cypress products meet the specifications contained in their particular Cypress datasheets. Cypress believes that its family of products is one of the most secure families of its kind on the market today, regardless of how they are used. There may be methods, unknown to Cypress, that can breach the code protection features. Any of these methods, to our knowledge, would be dishonest and possibly illegal. Neither Cypress nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

Cypress is willing to work with the customer who is concerned about the integrity of their code. Code protection is constantly evolving. We at Cypress are committed to continuously improving the code protection features of our products.

5.4 EEPROM

PSoC EEPROM memory is a byte-addressable nonvolatile memory. The CY8C36 has up to 2 KB of EEPROM memory to store user data. Reads from EEPROM are random access at the byte level. Reads are done directly; writes are done by sending write commands to an EEPROM programming interface. CPU code execution can continue from flash during EEPROM writes. EEPROM is erasable and writable at the row level. The EEPROM is divided into 128 rows of 16 bytes each.

The CPU can not execute out of EEPROM. There is no ECC hardware associated with EEPROM. If ECC is required it must be handled in firmware.

5.5 External Memory Interface

CY8C36 provides an external memory interface (EMIF) for connecting to external memory devices. The connection allows read and write accesses to external memories. The EMIF operates in conjunction with UDBs, I/O ports, and other hardware to generate external memory address and control signals. At 33 MHz, each memory access cycle takes four bus clock cycles.

[Figure 5-1](#) is the EMIF block diagram. The EMIF supports synchronous and asynchronous memories. The CY8C36 supports only one type of external memory device at a time.

External memory can be accessed through the 8051 xdata space; up to 24 address bits can be used. See [xdata Space](#) on page 21. The memory can be 8 or 16 bits wide.

5.6.3 SFRs

The special function register (SFR) space provides access to frequently accessed registers. The memory map for the SFR memory space is shown in [Table 5-2](#).

Table 5-2. SFR Map

Address	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F
0xF8	SFRPRT15DR	SFRPRT15PS	SFRPRT15SEL	–	–	–	–	–
0xF0	B	–	SFRPRT12SEL	–	–	–	–	–
0xE8	SFRPRT12DR	SFRPRT12PS	MXAX	–	–	–	–	–
0xE0	ACC	–	–	–	–	–	–	–
0xD8	SFRPRT6DR	SFRPRT6PS	SFRPRT6SEL	–	–	–	–	–
0xD0	PSW	–	–	–	–	–	–	–
0xC8	SFRPRT5DR	SFRPRT5PS	SFRPRT5SEL	–	–	–	–	–
0xC0	SFRPRT4DR	SFRPRT4PS	SFRPRT4SEL	–	–	–	–	–
0xB8	–	–	–	–	–	–	–	–
0xB0	SFRPRT3DR	SFRPRT3PS	SFRPRT3SEL	–	–	–	–	–
0xA8	IE	–	–	–	–	–	–	–
0xA0	P2AX	–	SFRPRT1SEL	–	–	–	–	–
0x98	SFRPRT2DR	SFRPRT2PS	SFRPRT2SEL	–	–	–	–	–
0x90	SFRPRT1DR	SFRPRT1PS	–	DPX0	–	DPX1	–	–
0x88	–	SFRPRT0PS	SFRPRT0SEL	–	–	–	–	–
0x80	SFRPRT0DR	SP	DPL0	DPH0	DPL1	DPH1	DPS	–

The CY8C36 family provides the standard set of registers found on industry standard 8051 devices. In addition, the CY8C36 devices add SFRs to provide direct access to the I/O ports on the device. The following sections describe the SFRs added to the CY8C36 family.

XData Space Access SFRs

The 8051 core features dual DPTR registers for faster data transfer operations. The data pointer select SFR, DPS, selects which data pointer register, DPTR0 or DPTR1, is used for the following instructions:

- MOVX @DPTR, A
- MOVX A, @DPTR
- MOVC A, @A+DPTR
- JMP @A+DPTR
- INC DPTR
- MOV DPTR, #data16

The extended data pointer SFRs, DPX0, DPX1, MXAX, and P2AX, hold the most significant parts of memory addresses during access to the xdata space. These SFRs are used only with the MOVX instructions.

During a MOVX instruction using the DPTR0/DPTR1 register, the most significant byte of the address is always equal to the contents of DPX0/DPX1.

During a MOVX instruction using the R0 or R1 register, the most significant byte of the address is always equal to the contents of MXAX, and the next most significant byte is always equal to the contents of P2AX.

I/O Port SFRs

The I/O ports provide digital input sensing, output drive, pin interrupts, connectivity for analog inputs and outputs, LCD, and access to peripherals through the DSI. Full information on I/O ports is found in [I/O System and Routing](#) on page 28.

I/O ports are linked to the CPU through the PHUB and are also available in the SFRs. Using the SFRs allows faster access to a limited set of I/O port registers, while using the PHUB allows boot configuration and access to all I/O port registers.

Each SFR supported I/O port provides three SFRs:

- SFRPRTxDR sets the output data state of the port (where x is port number and includes ports 0–6, 12 and 15).
- The SFRPRTxSEL selects whether the PHUB PRTxDR register or the SFRPRTxDR controls each pin's output buffer within the port. If a SFRPRTxSEL[y] bit is high, the corresponding SFRPRTxDR[y] bit sets the output state for that pin. If a SFRPRTxSEL[y] bit is low, the corresponding PRTxDR[y] bit sets the output state of the pin (where y varies from 0 to 7).
- The SFRPRTxPS is a read only register that contains pin state values of the port pins.

6.2.1 Power Modes

PSoC 3 devices have four different power modes, as shown in [Table 6-1](#) and [Table 6-2](#). The power modes allow a design to easily provide required functionality and processing power while simultaneously minimizing power consumption and maximizing battery life in low-power and portable devices.

PSoC 3 power modes, in order of decreasing power consumption are:

- Active
- Alternate Active
- Sleep
- Hibernate

Active is the main processing mode. Its functionality is configurable. Each power controllable subsystem is enabled or disabled by using separate power configuration template registers. In alternate active mode, fewer subsystems are enabled, reducing power. In sleep mode most resources are disabled regardless of the template settings. Sleep mode is optimized to provide timed sleep intervals and RTC functionality. The lowest power mode is hibernate, which retains register and SRAM state, but no clocks, and allows wakeup only from I/O pins. [Figure 6-5](#) illustrates the allowable transitions between power modes.

Table 6-1. Power Modes

Power Modes	Description	Entry Condition	Wakeup Source	Active Clocks	Regulator
Active	Primary mode of operation, all peripherals available (programmable)	Wakeup, reset, manual register entry	Any interrupt	Any (programmable)	All regulators available. Digital and analog regulators can be disabled if external regulation used.
Alternate Active	Similar to Active mode, and is typically configured to have fewer peripherals active to reduce power. One possible configuration is to use the UDBs for processing, with the CPU turned off	Manual register entry	Any interrupt	Any (programmable)	All regulators available. Digital and analog regulators can be disabled if external regulation used.
Sleep	All subsystems automatically disabled	Manual register entry	Comparator, PICU, I ² C, RTC, CTW, LVD	ILO/kHzECO	Both digital and analog regulators buzzed. Digital and analog regulators can be disabled if external regulation used.
Hibernate	All subsystems automatically disabled Lowest power consuming mode with all peripherals and internal regulators disabled, except hibernate regulator is enabled Configuration and memory contents retained	Manual register entry	PICU	–	Only hibernate regulator active.

Table 6-2. Power Modes Wakeup Time and Power Consumption

Sleep Modes	Wakeup Time	Current (Typ)	Code Execution	Digital Resources	Analog Resources	Clock Sources Available	Wakeup Sources	Reset Sources
Active	–	1.2 mA ^[16]	Yes	All	All	All	–	All
Alternate Active	–	–	User defined	All	All	All	–	All
Sleep	<15 µs	1 µA	No	I ² C	Comparator	ILO/kHzECO	Comparator, PICU, I ² C, RTC, CTW, LVD	XRES, LVD, WDR
Hibernate	<100 µs	200 nA	No	None	None	None	PICU	XRES

Note

¹⁶. Bus clock off. Execute from CPU instruction buffer at 6 MHz. See [Table 11-2](#) on page 59.

■ **ALVI, DLVI, AHVI – Analog/Digital Low Voltage Interrupt, Analog High Voltage Interrupt**

Interrupt circuits are available to detect when V_{dda} and V_{ddd} go outside a voltage range. For AHVI, V_{dda} is compared to a fixed trip level. For ALVI and DLVI, V_{dda} and V_{ddd} are compared to trip levels that are programmable, as listed in Table 6-2. ALVI and DLVI can also be configured to generate a device reset instead of an interrupt.

Table 6-2. Analog/Digital Low Voltage Interrupt, Analog High Voltage Interrupt

Interrupt	Supply	Normal Voltage Range	Available Trip Settings	Accuracy
DLVI	V _{ddd}	1.71 V–5.5 V	1.70 V–5.45 V in 250 mV increments	±2%
ALVI	V _{dda}	1.71 V–5.5 V	1.70 V–5.45 V in 250 mV increments	±2%
AHVI	V _{dda}	1.71 V–5.5 V	5.75 V	±2%

The monitors are disabled until after IPOR. During sleep mode these circuits are periodically activated (buzzed). If an interrupt occurs during buzzing then the system first enters its wake up sequence. The interrupt is then recognized and may be serviced.

6.3.1.2 Other Reset Sources

■ **XRES – External Reset**

PSoC 3 has either a single GPIO pin that is configured as an external reset or a dedicated XRES pin. Either the dedicated XRES pin or the GPIO pin, if configured, holds the part in reset while held active (low). The response to an XRES is the same as to an IPOR reset.

The external reset is active low. It includes an internal pull-up resistor. XRES is active during sleep and hibernate modes.

■ **SRES – Software Reset**

A reset can be commanded under program control by setting a bit in the software reset register. This is done either directly by the program or indirectly by DMA access. The response to a SRES is the same as after an IPOR reset.

Another register bit exists to disable this function.

■ **DRES – Digital Logic Reset**

A logic signal can be routed from the UDBs or other digital peripheral source through the DSI to the Configurable XRES pin, P1[2], to generate a hardware-controlled reset. The pin must be placed in XRES mode. The response to a DRES is the same as after an IPOR reset.

■ **WRES – Watchdog Timer Reset**

The watchdog reset detects when the software program is no longer being executed correctly. To indicate to the watchdog timer that it is running correctly, the program must periodically reset the timer. If the timer is not reset before a user-specified amount of time, then a reset is generated.

Note IPOR disables the watchdog function. The program must enable the watchdog function at an appropriate point in the code by setting a register bit. When this bit is set, it cannot be cleared again except by an IPOR power on reset event.

Note

17. GPIOs with opamp outputs are not recommended for use with CapSense

6.4 I/O System and Routing

PSoC I/Os are extremely flexible. Every GPIO has analog and digital I/O capability. All I/Os have a large number of drive modes, which are set at POR. PSoC also provides up to four individual I/O voltage domains through the V_{ddio} pins.

There are two types of I/O pins on every device; those with USB provide a third type. Both General Purpose I/O (GPIO) and Special I/O (SIO) provide similar digital functionality. The primary differences are their analog capability and drive strength. Devices that include USB also provide two USBIO pins that support specific USB functionality as well as limited GPIO capability.

All I/O pins are available for use as digital inputs and outputs for both the CPU and digital peripherals. In addition, all I/O pins can generate an interrupt. The flexible and advanced capabilities of the PSoC I/O, combined with any signal to any pin routability, greatly simplify circuit design and board layout. All GPIO pins can be used for analog input, CapSense^[17], and LCD segment drive, while SIO pins are used for voltages in excess of V_{DDA} and for programmable output voltages.

■ **Features supported by both GPIO and SIO:**

- User programmable port reset state
- Separate I/O supplies and voltages for up to four groups of I/O
- Digital peripherals use DSI to connect the pins
- Input or output or both for CPU and DMA
- Eight drive modes
- Every pin can be an interrupt source configured as rising edge, falling edge or both edges. If required, level sensitive interrupts are supported through the DSI
- Dedicated port interrupt vector for each port
- Slew rate controlled digital output drive mode
- Access port control and configuration registers on either port basis or pin basis
- Separate port read (PS) and write (DR) data registers to avoid read modify write errors
- Special functionality on a pin by pin basis

■ **Additional features only provided on the GPIO pins:**

- LCD segment drive on LCD equipped devices
- CapSense^[17]
- Analog input and output capability
- Continuous 100 µA clamp current capability
- Standard drive strength down to 1.7 V

■ **Additional features only provided on SIO pins:**

- Higher drive strength than GPIO
- Hot swap capability (5 V tolerance at any operating V_{DD})
- Programmable and regulated high input and output drive levels down to 1.2 V
- No analog input, CapSense, or LCD capability
- Over voltage tolerance up to 5.5 V
- SIO can act as a general purpose analog comparator

■ **USBIO features:**

- Full speed USB 2.0 compliant I/O
- Highest drive strength for general purpose use
- Input, output, or both for CPU and DMA
- Input, output, or both for digital peripherals
- Digital output (CMOS) drive mode
- Each pin can be an interrupt source configured as rising edge, falling edge, or both edges

7.1 Example Peripherals

The flexibility of the CY8C36 family's Universal Digital Blocks (UDBs) and Analog Blocks allow the user to create a wide range of components (peripherals). The most common peripherals were built and characterized by Cypress and are shown in the PSoC Creator component catalog, however, users may also create their own custom components using PSoC Creator. Using PSoC Creator, users may also create their own components for reuse within their organization, for example sensor interfaces, proprietary algorithms, and display interfaces.

The number of components available through PSoC Creator is too numerous to list in the datasheet, and the list is always growing. An example of a component available for use in CY8C36 family, but, not explicitly called out in this datasheet is the UART component.

7.1.1 Example Digital Components

The following is a sample of the digital components available in PSoC Creator for the CY8C36 family. The exact amount of hardware resources (UDBs, routing, RAM, flash) used by a component varies with the features selected in PSoC Creator for the component.

- Communications
 - I²C
 - UART
 - SPI
- Functions
 - EMIF
 - PWMs
 - Timers
 - Counters
- Logic
 - NOT
 - OR
 - XOR
 - AND

7.1.2 Example Analog Components

The following is a sample of the analog components available in PSoC Creator for the CY8C36 family. The exact amount of hardware resources (SC/CT blocks, routing, RAM, flash) used by a component varies with the features selected in PSoC Creator for the component.

- Amplifiers
 - TIA
 - PGA
 - opamp
- ADC
 - Delta-Sigma
- DACs
 - Current

- Voltage
- PWM
- Comparators
- Mixers

7.1.3 Example System Function Components

The following is a sample of the system function components available in PSoC Creator for the CY8C36 family. The exact amount of hardware resources (UDBs, DFB taps, SC/CT blocks, routing, RAM, flash) used by a component varies with the features selected in PSoC Creator for the component.

- CapSense
- LCD Drive
- LCD Control
- Filters

7.1.4 Designing with PSoC Creator

7.1.4.1 More Than a Typical IDE

A successful design tool allows for the rapid development and deployment of both simple and complex designs. It reduces or eliminates any learning curve. It makes the integration of a new design into the production stream straightforward.

PSoC Creator is that design tool.

PSoC Creator is a full featured Integrated Development Environment (IDE) for hardware and software design. It is optimized specifically for PSoC devices and combines a modern, powerful software development platform with a sophisticated graphical design tool. This unique combination of tools makes PSoC Creator the most flexible embedded design platform available.

Graphical design entry simplifies the task of configuring a particular part. You can select the required functionality from an extensive catalog of components and place it in your design. All components are parameterized and have an editor dialog that allows you to tailor functionality to your needs.

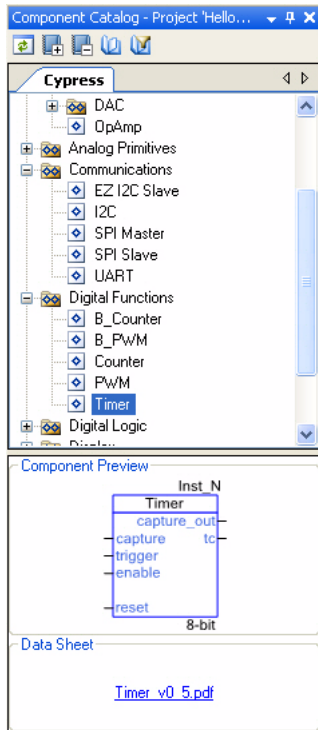
PSoC Creator automatically configures clocks and routes the I/O to the selected pins and then generates APIs to give the application complete control over the hardware. Changing the PSoC device configuration is as simple as adding a new component, setting its parameters, and rebuilding the project.

At any stage of development you are free to change the hardware configuration and even the target processor. To retarget your application (hardware and software) to new devices, even from 8- to 32-bit families, just select the new device and rebuild.

You also have the ability to change the C compiler and evaluate an alternative. Components are designed for portability and are validated against all devices, from all families, and against all supported tool chains. Switching compilers is as easy as editing the from the project options and rebuilding the application with no errors from the generated APIs or boot code.

7.1.4.2 Component Catalog

Figure 7-3. Component Catalog



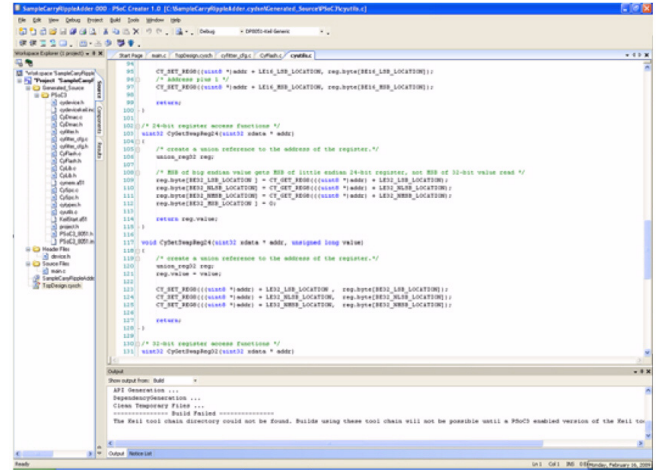
The component catalog is a repository of reusable design elements that select device functionality and customize your PSoC device. It is populated with an impressive selection of content; from simple primitives such as logic gates and device registers, through the digital timers, counters and PWMs, plus analog components such as ADC, DACs, and filters, and communication protocols, such as I²C, USB, and CAN. See [Example Peripherals](#) on page 35 for more details about available peripherals. All content is fully characterized and carefully documented in datasheets with code examples, AC/DC specifications, and user code ready APIs.

7.1.4.3 Design Reuse

The symbol editor gives you the ability to develop reusable components that can significantly reduce future design time. Just draw a symbol and associate that symbol with your proven design. PSoC Creator allows for the placement of the new symbol anywhere in the component catalog along with the content provided by Cypress. You can then reuse your content as many times as you want, and in any number of projects, without ever having to revisit the details of the implementation.

7.1.4.4 Software Development

Figure 7-4. Code Editor

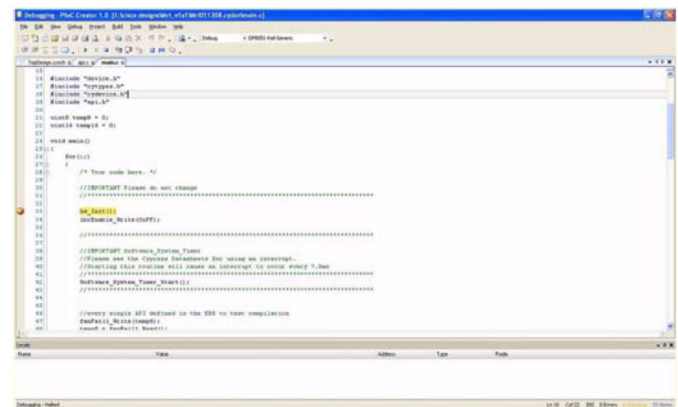


Anchoring the tool is a modern, highly customizable user interface. It includes project management and integrated editors for C and assembler source code, as well the design entry tools.

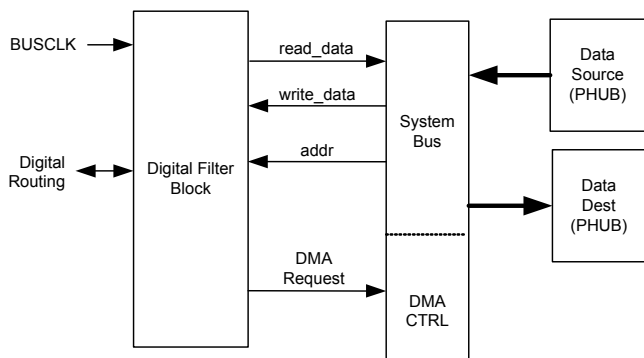
Project build control leverages compiler technology from top commercial vendors such as ARM® Limited, Keil™, and CodeSourcery (GNU). Free versions of Keil C51 and GNU C Compiler (GCC) for ARM, with no restrictions on code size or end product distribution, are included with the tool distribution. Upgrading to more optimizing compilers is a snap with support for the professional Keil C51 product and ARM RealView™ compiler.

7.1.4.5 Nonintrusive Debugging

Figure 7-5. PSoC Creator Debugger



With JTAG (4-wire) and SWD (2-wire) debug connectivity available on all devices, the PSoC Creator debugger offers full control over the target device with minimum intrusion. Breakpoints and code execution commands are all readily available from toolbar buttons and an impressive lineup of windows—register, locals, watch, call stack, memory and peripherals—make for an unparalleled level of visibility into the system.

Figure 7-22. DFB Application Diagram (pwr/gnd not shown)


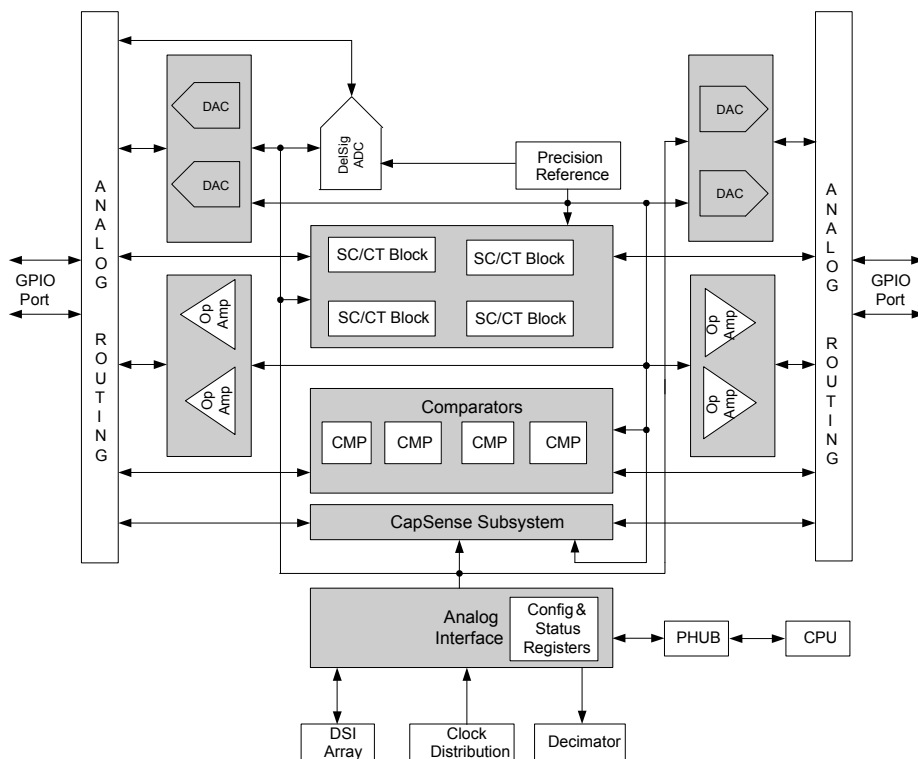
The typical use model is for data to be supplied to the DFB over the system bus from another on-chip system data source such as an ADC. The data typically passes through main memory or is directly transferred from another chip resource through DMA. The DFB processes this data and passes the result to another on-chip resource such as a DAC or main memory through DMA on the system bus.

Data movement in or out of the DFB is typically controlled by the system DMA controller but can be moved directly by the MCU.

8. Analog Subsystem

The analog programmable system creates application specific combinations of both standard and advanced analog signal processing blocks. These blocks are then interconnected to each other and also to any pin on the device, providing a high level of design flexibility and IP security. The features of the analog subsystem are outlined here to provide an overview of capabilities and architecture.

- Flexible, configurable analog routing architecture provided by analog globals, analog mux bus, and analog local buses.
- High resolution Delta-Sigma ADC.
- Up to four 8-bit DACs that provide either voltage or current output.
- Four comparators with optional connection to configurable LUT outputs.
- Up to four configurable switched capacitor/continuous time (SC/CT) blocks for functions that include opamp, unity gain buffer, programmable gain amplifier, transimpedance amplifier, and mixer.
- Up to four opamps for internal use and connection to GPIO that can be used as high current output buffers.
- CapSense subsystem to enable capacitive touch sensing.
- Precision reference for generating an accurate analog voltage for internal analog blocks.

Figure 8-1. Analog Subsystem Block Diagram


The PSoC Creator software program provides a user friendly interface to configure the analog connections between the GPIO and various analog resources and connections from one analog resource to another. PSoC Creator also provides component libraries that allow you to configure the various analog blocks to perform application specific functions (PGA, transimpedance amplifier, voltage DAC, current DAC, and so on). The tool also generates API interface libraries that allow you to write firmware that allows the communication between the analog peripheral and CPU/Memory.

8.1 Analog Routing

The CY8C36 family of devices has a flexible analog routing architecture that provides the capability to connect GPIOs and different analog blocks, and also route signals between different analog blocks. One of the strong points of this flexible routing architecture is that it allows dynamic routing of input and output connections to the different analog blocks.

8.1.1 Features

- Flexible, configurable analog routing architecture
- 16 analog globals (AG) and two analog mux buses (AMUXBUS) to connect GPIOs and the analog blocks
- Each GPIO is connected to one analog global and one analog mux bus
- Eight analog local buses (abus) to route signals between the different analog blocks
- Multiplexers and switches for input and output selection of the analog blocks

8.1.2 Functional Description

Analog globals (AGs) and analog mux buses (AMUXBUS) provide analog connectivity between GPIOs and the various analog blocks. There are 16 AGs in the CY8C36 family. The analog routing architecture is divided into four quadrants as shown in [Figure 8-2](#). Each quadrant has four analog globals (AGL[0..3], AGL[4..7], AGR[0..3], AGR[4..7]). Each GPIO is connected to the corresponding AG through an analog switch. The analog mux bus is a shared routing resource that connects to every GPIO through an analog switch. There are two AMUXBUS routes in CY8C36, one in the left half (AMUXBUSL) and one in the right half (AMUXBUSR), as shown in [Figure 8-2](#).

- One memory access breakpoint—break on reading or writing any memory address and data value
- Break on a sequence of breakpoints (non recursive)
- Debugging at the full speed of the CPU
- Debug operations are possible while the device is reset, or in low-power modes
- Compatible with PSoC Creator and MiniProg3 programmer and debugger
- Standard JTAG programming and debugging interfaces make CY8C36 compatible with other popular third-party tools (for example, ARM / Keil)

9.4 Trace Features

The CY8C36 supports the following trace features when using JTAG or SWD:

- Trace the 8051 program counter (PC), accumulator register (ACC), and one SFR / 8051 core RAM register
- Trace depth up to 1000 instructions if all registers are traced, or 2000 instructions if only the PC is traced (on devices that include trace memory)
- Program address trigger to start tracing
- Trace windowing, that is, only trace when the PC is within a given range
- Two modes for handling trace buffer full: continuous (overwriting the oldest trace data) or break when trace buffer is full

9.5 Single Wire Viewer Interface

The SWV interface is closely associated with SWD but can also be used independently. SWV data is output on the JTAG interface's TDO pin. If using SWV, you must configure the device for SWD, not JTAG. SWV is not supported with the JTAG interface.

SWV is ideal for application debug where it is helpful for the firmware to output data similar to 'printf' debugging on PCs. The SWV is ideal for data monitoring, because it requires only a single pin and can output data in standard UART format or Manchester encoded format. For example, it can be used to tune a PID control loop in which the output and graphing of the three error terms greatly simplifies coefficient tuning.

The following features are supported in SWV:

- 32 virtual channels, each 32 bits long
- Simple, efficient packing and serializing protocol
- Supports standard UART format (N81)

9.6 Programming Features

The JTAG and SWD interfaces provide full programming support. The entire device can be erased, programmed, and verified. You can increase flash protection levels to protect firmware IP. Flash protection can only be reset after a full device erase. Individual flash blocks can be erased, programmed, and verified, if block security settings permit.

9.7 Device Security

PSoC 3 offers an advanced security feature called device security, which permanently disables all test, programming, and debug ports, protecting your application from external access. The device security is activated by programming a 32-bit key (0x50536F43) to a Write Once Latch (WOL).

The Write Once Latch is a type of nonvolatile latch (NVL). The cell itself is an NVL with additional logic wrapped around it. Each WOL device contains four bytes (32 bits) of data. The wrapper outputs a '1' if a super-majority (28 of 32) of its bits match a pre-determined pattern (0x50536F43); it outputs a '0' if this majority is not reached. When the output is 1, the Write Once NV latch locks the part out of Debug and Test modes; it also permanently gates off the ability to erase or alter the contents of the latch. Matching all bits is intentionally not required, so that single (or few) bit failures do not deassert the WOL output. The state of the NVL bits after wafer processing is truly random with no tendency toward 1 or 0.

The WOL only locks the part after the correct 32-bit key (0x50536F43) is loaded into the NVL's volatile memory, programmed into the NVL's nonvolatile cells, and the part is reset. The output of the WOL is only sampled on reset and used to disable the access. This precaution prevents anyone from reading, erasing, or altering the contents of the internal memory.

The user can write the key into the WOL to lock out external access only if no flash protection is set (see ["Flash Security"](#) on page 18). However, after setting the values in the WOL, a user still has access to the part until it is reset. Therefore, a user can write the key into the WOL, program the flash protection data, and then reset the part to lock it.

If the device is protected with a WOL setting, Cypress cannot perform failure analysis and, therefore, cannot accept RMAs from customers. The WOL can be read out through the SWD port to electrically identify protected parts. The user can write the key in WOL to lock out external access only if no flash protection is set. For more information on how to take full advantage of the security features in PSoC see the PSoC 3 TRM.

Disclaimer

Note the following details of the flash code protection features on Cypress devices.

Cypress products meet the specifications contained in their particular Cypress datasheets. Cypress believes that its family of products is one of the most secure families of its kind on the market today, regardless of how they are used. There may be methods, unknown to Cypress, that can breach the code protection features. Any of these methods, to our knowledge, would be dishonest and possibly illegal. Neither Cypress nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Cypress is willing to work with the customer who is concerned about the integrity of their code. Code protection is constantly evolving. We at Cypress are committed to continuously improving the code protection features of our products.

11.2 Device Level Specifications

Specifications are valid for $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ and $T_J \leq 100\text{ }^{\circ}\text{C}$, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.2.1 Device Level Specifications

Table 11-2. DC Specifications

Parameter	Description	Conditions		Min	Typ	Max	Units	
V _{DDA}	Analog supply voltage and input to analog core regulator	Analog core regulator enabled		1.8	–	5.5	V	
V _{DDA}	Analog supply voltage, analog regulator bypassed	Analog core regulator disabled		1.71	1.8	1.89	V	
V _{DDD}	Digital supply voltage relative to V _{SSD}	Digital core regulator enabled		1.8	–	V _{DDA} ^[22]	V	
V _{DDD}	Digital supply voltage, digital regulator bypassed	Digital core regulator disabled		1.71	1.8	1.89	V	
V _{DDIO} ^[23]	I/O supply voltage relative to V _{SSIO}			1.71	–	V _{DDA} ^[22]	V	
V _{CCA}	Direct analog core voltage input (Analog regulator bypass)	Analog core regulator disabled		1.71	1.8	1.89	V	
V _{CCD}	Direct digital core voltage input (Digital regulator bypass)	Digital core regulator disabled		1.71	1.8	1.89	V	
V _{BAT}	Voltage supplied to boost converter			0.5	–	5.5	V	
I _{DD} ^[24]	Active Mode, V _{DD} = 1.71 V–5.5 V							
	Bus clock off. Execute from CPU instruction buffer. See “Flash Program Memory” on page 18.	CPU at 3 MHz	T = –40 °C	–	–	–	mA	
			T = 25 °C	–	0.8	–	mA	
			T = 85 °C	–	–	–	mA	
			CPU at 6 MHz	T = –40 °C	–	–	–	mA
				T = 25 °C	–	1.2	–	mA
				T = 85 °C	–	–	–	mA
			CPU at 12 MHz	T = –40 °C	–	–	–	mA
				T = 25 °C	–	2.0	–	mA
				T = 85 °C	–	–	–	mA
		CPU at 24 MHz	T = –40 °C	–	–	–	mA	
			T = 25 °C	–	3.5	–	mA	
			T = 85 °C	–	–	–	mA	
		CPU at 48 MHz	T = –40 °C	–	–	–	mA	
			T = 25 °C	–	6.6	–	mA	
			T = 85 °C	–	–	–	mA	
		CPU at 62.6 MHz	T = –40 °C	–	–	–	mA	
			T = 25 °C	–	9.0	–	mA	
			T = 85 °C	–	–	–	mA	
	V _{DD} = 3.3 V, T = 25 °C, IMO and bus clock enabled, ILO = 1 kHz, CPU executing from flash and accessing SRAM, all other blocks off, all I/Os tied low.	CPU at 3 MHz		–	1.2	–	mA	
		CPU at 6 MHz		–	1.8	–	mA	
		CPU at 12 MHz		–	3.2	–	mA	
		CPU at 24 MHz		–	5.8	–	mA	
		CPU at 48 MHz		–	12.1	–	mA	
CPU at 62.6 MHz		–	15.6	–	mA			

Notes

22. The power supplies can be brought up in any sequence however once stable V_{DDA} must be greater than or equal to all other supplies.

23. The V_{DDIO} supply voltage must be greater than the maximum analog voltage on the associated GPIO pins. Maximum analog voltage on GPIO pin $\leq V_{DDIO} \leq V_{DDA}$.

24. The current consumption of additional peripherals that are implemented only in programmed logic blocks can be found in their respective datasheets, available in PSoC Creator, the integrated design environment. To estimate total current, find CPU current at frequency of interest and add peripheral currents for your particular system from the device datasheet and component datasheets.

Table 11-2. DC Specifications (continued)

Parameter	Description	Conditions		Min	Typ	Max	Units
	Sleep Mode ^[26]						
	CPU = OFF RTC = ON (= ECO32K ON, in low-power mode) Sleep timer = ON (= ILO ON at 1 kHz) ^[27] WDT = OFF I ² C Wake = OFF Comparator = OFF POR = ON Boost = OFF SIO pins in single ended input, unregulated output mode	V _{DD} = V _{DDIO} = 4.5–5.5 V	T = –40 °C	–	–	–	μA
			T = 25 °C	–	–	–	μA
			T = 85 °C	–	–	–	μA
		V _{DD} = V _{DDIO} = 2.7–3.6 V	T = –40 °C	–	–	–	μA
			T = 25 °C	–	1	–	μA
			T = 85 °C	–	–	–	μA
		V _{DD} = V _{DDIO} = 1.71–1.95 V	T = –40 °C	–	–	–	μA
			T = 25 °C	–	–	–	μA
			T = 85 °C	–	–	–	μA
	Comparator = ON CPU = OFF RTC = OFF Sleep timer = OFF WDT = OFF I2C Wake = OFF POR = ON Boost = OFF SIO pins in single ended input, unregulated output mode	V _{DD} = V _{DDIO} = 2.7–3.6 V	T = 25 °C	–	–	–	μA
	I2C Wake = ON CPU = OFF RTC = OFF Sleep timer = OFF WDT = OFF Comparator = OFF POR = ON Boost = OFF SIO pins in single ended input, unregulated output mode	V _{DD} = V _{DDIO} = 2.7–3.6 V	T = 25 °C	–	–	–	μA
	Hibernate Mode ^[26]						
	Hibernate mode current All regulators and oscillators off. SRAM retention GPIO interrupts are active Boost = OFF SIO pins in single ended input, unregulated output mode	V _{DD} = V _{DDIO} = 4.5–5.5 V	T = –40 °C	–	–	–	nA
			T = 25 °C	–	–	–	nA
T = 85 °C			–	–	–	nA	
V _{DD} = V _{DDIO} = 2.7–3.6 V		T = –40 °C	–	–	–	nA	
		T = 25 °C	–	200	–	nA	
		T = 85 °C	–	–	–	nA	
V _{DD} = V _{DDIO} = 1.71–1.95 V		T = –40 °C	–	–	–	nA	
		T = 25 °C	–	–	–	nA	
		T = 85 °C	–	–	–	nA	

Notes

25. The current consumption of additional peripherals that are implemented only in programmed logic blocks can be found in their respective datasheets, available in PSoC Creator, the integrated design environment. To compute total current, find CPU current at frequency of interest and add peripheral currents for your particular system from the device datasheet and component datasheets.

26. If V_{CCD} and V_{CCA} are externally regulated, the voltage difference between V_{CCD} and V_{CCA} must be less than 50 mV.

27. Sleep timer generates periodic interrupts to wake up the CPU. This specification applies only to those times that the CPU is off.

Table 11-14. USBIO AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Tdrate	Full-speed data rate average bit rate		12 – 0.25%	12	12 + 0.25%	MHz
Tjr1	Receiver data jitter tolerance to next transition		–8	–	8	ns
Tjr2	Receiver data jitter tolerance to pair transition		–5	–	5	ns
Tdj1	Driver differential jitter to next transition		–3.5	–	3.5	ns
Tdj2	Driver differential jitter to pair transition		–4	–	4	ns
Tfdeop	Source jitter for differential transition to SE0 transition		–2	–	5	ns
Tfeopt	Source SE0 interval of EOP		160	–	175	ns
Tfeopr	Receiver SE0 interval of EOP		82	–	–	ns
Tfst	Width of SE0 interval during differential transition		–	–	14	ns
Fgpio_out	GPIO mode output operating frequency	$3\text{ V} \leq V_{\text{DDD}} \leq 5.5\text{ V}$	–	–	20	MHz
		$V_{\text{DDD}} = 1.71\text{ V}$	–	–	6	MHz
Tr_gpio	Rise time, GPIO mode, 10%/90% V_{DDD}	$V_{\text{DDD}} > 3\text{ V}$, 25 pF load	–	–	12	ns
		$V_{\text{DDD}} = 1.71\text{ V}$, 25 pF load	–	–	40	ns
Tf_gpio	Fall time, GPIO mode, 90%/10% V_{DDD}	$V_{\text{DDD}} > 3\text{ V}$, 25 pF load	–	–	12	ns
		$V_{\text{DDD}} = 1.71\text{ V}$, 25 pF load	–	–	40	ns

Table 11-15. USB Driver AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Tr	Transition rise time		–	–	20	ns
Tf	Transition fall time		–	–	20	ns
TR	Rise/fall time matching	V_{USB_5} , $V_{\text{USB}_3,3}$, see USB DC Specifications on page 87	90%	–	111%	
Vcrs	Output signal crossover voltage		1.3	–	2	V

11.4.4 XRES

Table 11-16. XRES DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{IH}	Input voltage high threshold		$0.7 \times V_{\text{DDIO}}$	–	–	V
V_{IL}	Input voltage low threshold		–	–	$0.3 \times V_{\text{DDIO}}$	V
Rpullup	Pull-up resistor		3.5	5.6	8.5	k Ω
C_{IN}	Input capacitance ^[36]		–	3	–	pF
V_{H}	Input voltage hysteresis (Schmitt–Trigger) ^[36]		–	100	–	mV
Idiode	Current through protection diode to V_{DDIO} and V_{SSIO}		–	–	100	μA

Table 11-17. XRES AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
T_{RESET}	Reset pulse width		1	–	–	μs

Note

36. Based on device characterization (Not production tested).

Table 11-27. IDAC DC Specifications (continued)

Parameter	Description	Conditions	Min	Typ	Max	Units
Eg	Gain error	Range = 2.048 mA, 25 °C	–	–	±2.5	%
		Range = 255 µA, 25 °C	–	–	±2.5	%
		Range = 31.875 µA, 25 °C	–	–	±3.5	%
TC_Eg	Temperature coefficient of gain error	Range = 2.048 mA	–	–	0.04	% / °C
		Range = 255 µA	–	–	0.04	% / °C
		Range = 31.875 µA	–	–	0.05	% / °C
INL	Integral nonlinearity	Sink mode, range = 255 µA, Codes 8 – 255, Rload = 2.4 kΩ, Cload = 15 pF	–	±0.9	±1	LSB
		Source mode, range = 255 µA, Codes 8 – 255, Rload = 2.4 kΩ, Cload = 15 pF	–	±1.2	±1.5	LSB
DNL	Differential nonlinearity	Sink mode, range = 255 µA, Rload = 2.4 kΩ, Cload = 15 pF	–	±0.3	±1	LSB
		Source mode, range = 255 µA, Rload = 2.4 kΩ, Cload = 15 pF	–	±0.3	±1	LSB
Vcompliance	Dropout voltage, source or sink mode	Voltage headroom at max current, Rload to Vdda or Rload to Vssa, Vdiff from Vdda	1	–	–	V
IDD	Operating current, code = 0	Slow mode, source mode, range = 31.875 µA	–	–	44	µA
		Slow mode, source mode, range = 255 µA,	–	–	33	µA
		Slow mode, source mode, range = 2.04 mA	–	–	33	µA
		Slow mode, sink mode, range = 31.875 µA	–	–	36	µA
		Slow mode, sink mode, range = 255 µA	–	–	33	µA
		Slow mode, sink mode, range = 2.04 mA	–	–	33	µA
		Fast mode, source mode, range = 31.875 µA	–	–	310	µA
		Fast mode, source mode, range = 255 µA	–	–	305	µA
		Fast mode, source mode, range = 2.04 mA	–	–	305	µA
		Fast mode, sink mode, range = 31.875 µA	–	–	310	µA
		Fast mode, sink mode, range = 255 µA	–	–	300	µA
		Fast mode, sink mode, range = 2.04 mA	–	–	300	µA

11.5.8 Mixer

The mixer is created using a SC/CT analog block; see the Mixer component datasheet in PSoC Creator for full electrical specifications and APIs.

Table 11-31. Mixer DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V _{OS}	Input offset voltage		–	–	10	mV
	Quiescent current		–	0.9	2	mA
G	Gain		–	0	–	dB

Table 11-32. Mixer AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
f _{LO}	Local oscillator frequency	Down mixer mode	–	–	4	MHz
f _{in}	Input signal frequency	Down mixer mode	–	–	14	MHz
f _{LO}	Local oscillator frequency	Up mixer mode	–	–	1	MHz
f _{in}	Input signal frequency	Up mixer mode	–	–	1	MHz
SR	Slew rate		3	–	–	V/μs

11.5.9 Transimpedance Amplifier

The TIA is created using a SC/CT analog block; see the TIA component datasheet in PSoC Creator for full electrical specifications and APIs.

Table 11-33. Transimpedance Amplifier (TIA) DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V _{I_{OFF}}	Input offset voltage		–	–	10	mV
R _{conv}	Conversion resistance ^[45]	R = 20K; 40 pF load	–25	–	+35	%
		R = 30K; 40 pF load	–25	–	+35	%
		R = 40K; 40 pF load	–25	–	+35	%
		R = 80K; 40 pF load	–25	–	+35	%
		R = 120K; 40 pF load	–25	–	+35	%
		R = 250K; 40 pF load	–25	–	+35	%
		R = 500K; 40 pF load	–25	–	+35	%
		R = 1M; 40 pF load	–25	–	+35	%
	Quiescent current		–	1.1	2	mA

Table 11-34. Transimpedance Amplifier (TIA) AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
BW	Input bandwidth (–3 dB)	R = 20K; –40 pF load	1500	–	–	kHz
		R = 120K; –40 pF load	240	–	–	kHz
		R = 1M; –40 pF load	25	–	–	kHz

Notes

44. Based on device characterization (Not production tested).

45. Conversion resistance values are not calibrated. Calibrated values and details about calibration are provided in PSoC Creator component datasheets. External precision resistors can also be used.

11.5.10 Programmable Gain Amplifier

The PGA is created using a SC/CT analog block; see the PGA component datasheet in PSoC Creator for full electrical specifications and APIs.

Unless otherwise specified, operating conditions are:

- Operating temperature = 25 °C for typical values
- Unless otherwise specified, all charts and graphs show typical values

Table 11-35. PGA DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V _{in}	Input voltage range	Power mode = minimum	V _{ssa}	–	V _{dda}	V
V _{os}	Input offset voltage	Power mode = high, gain = 1	–	–	10	mV
TCV _{os}	Input offset voltage drift with temperature	Power mode = high, gain = 1	–	–	±30	µV/°C
Ge ₁	Gain error, gain = 1		–	–	±0.15	%
Ge ₁₆	Gain error, gain = 16		–	–	±2.5	%
Ge ₅₀	Gain error, gain = 50		–	–	±5	%
V _{onl}	DC output nonlinearity	Gain = 1	–	–	±0.01	% of FSR
C _{in}	Input capacitance		–	–	7	pF
V _{oh}	Output voltage swing	Power mode = high, gain = 1, R _{load} = 100 kΩ to V _{DDA} / 2	V _{DDA} – 0.15	–	–	V
V _{ol}	Output voltage swing	Power mode = high, gain = 1, R _{load} = 100 kΩ to V _{DDA} / 2	–	–	V _{SSA} + 0.15	V
V _{src}	Output voltage under load	I _{load} = 250 µA, V _{dda} ≥ 2.7V, power mode = high	–	–	300	mV
I _{dd}	Operating current	Power mode = high	–	1.5	1.65	mA
PSRR	Power supply rejection ratio		48	–	–	dB

Figure 11-45. V_{offset} Histogram, 1000 Samples, V_{dda} = 5 V

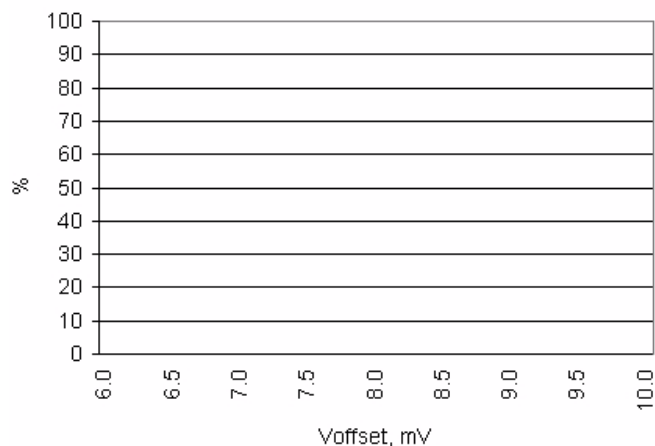


Figure 11-52. Synchronous Read Cycle Timing

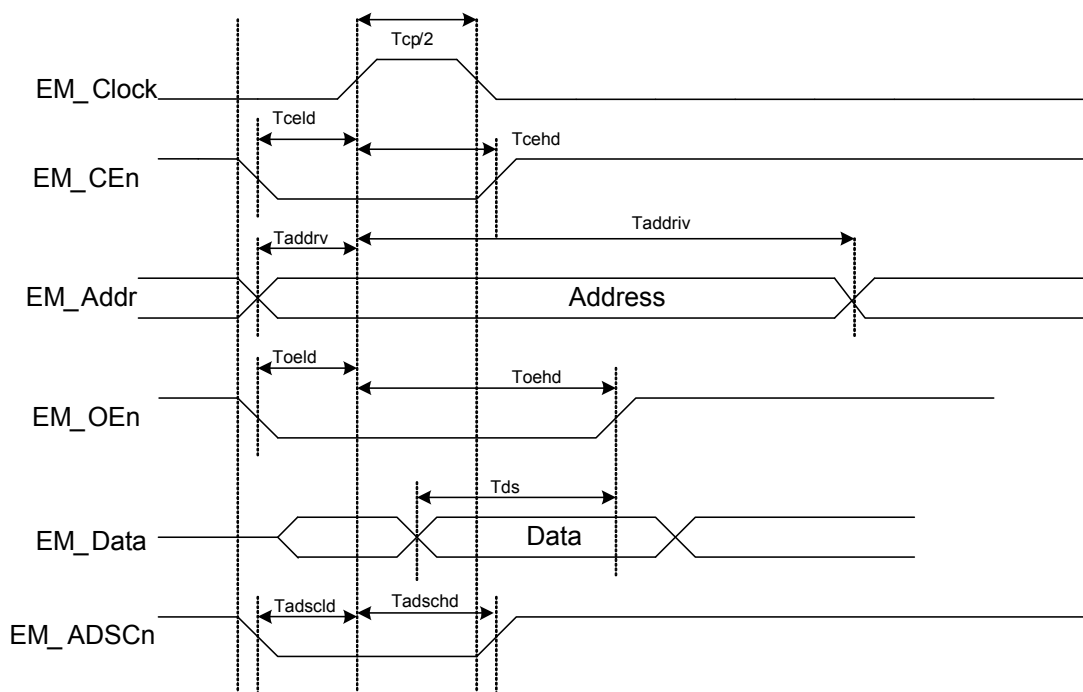


Table 11-63. Synchronous Read Cycle Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
T	EMIF clock period ^[50]	Vdda ≥ 3.3 V	30.3	–	–	nS
Tcp/2	EM_Clock pulse high		T/2	–	–	nS
Tceld	EM_CEn low to EM_Clock high		5	–	–	nS
Tcehd	EM_Clock high to EM_CEn high		T/2 – 5	–	–	nS
Taddrv	EM_Addr valid to EM_Clock high		5	–	–	nS
Taddriv	EM_Clock high to EM_Addr invalid		T/2 – 5	–	–	nS
Toeld	EM_OEn low to EM_Clock high		5	–	–	nS
Toehd	EM_Clock high to EM_OEn high		T	–	–	nS
Tds	Data valid before EM_OEn high		T + 15	–	–	nS
Tadscl	EM_ADSCn low to EM_Clock high		5	–	–	nS
Tadschd	EM_Clock high to EM_ADSCn high		T/2 – 5	–	–	nS

Note

50. Limited by GPIO output frequency, see [Table 11-10](#) on page 64.

Figure 11-53. Synchronous Write Cycle Timing

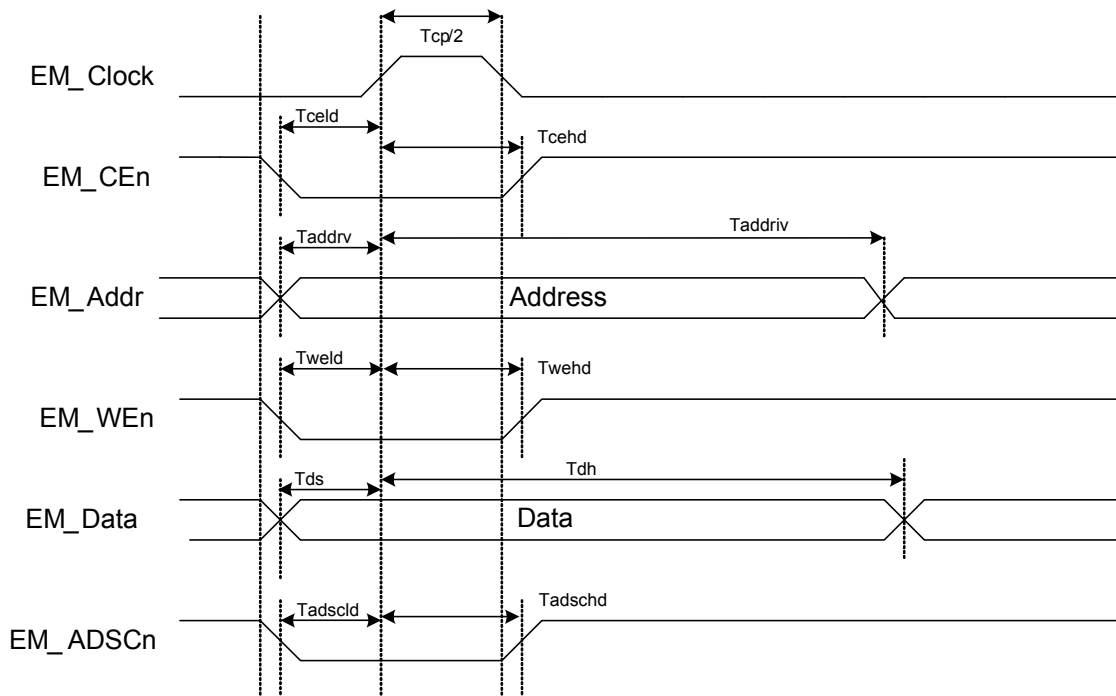


Table 11-64. Synchronous Write Cycle Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
T	EMIF clock Period ^[51]	Vdda ≥ 3.3 V	30.3	–	–	nS
Tcp/2	EM_Clock pulse high		T/2	–	–	nS
Tceld	EM_CEn low to EM_Clock high		5	–	–	nS
Tcehd	EM_Clock high to EM_CEn high		T/2 – 5	–	–	nS
Taddrv	EM_Addr valid to EM_Clock high		5	–	–	nS
Taddriv	EM_Clock high to EM_Addr invalid		T/2 – 5	–	–	nS
Tweld	EM_WEn low to EM_Clock high		5	–	–	nS
Twehd	EM_Clock high to EM_WEn high		T/2 – 5	–	–	nS
Tds	Data valid before EM_Clock high		5	–	–	nS
Tdh	Data invalid after EM_Clock high		T	–	–	nS
Tadscl	EM_ADSCn low to EM_Clock high		5	–	–	nS
Tadschd	EM_Clock high to EM_ADSCn high		T/2 – 5	–	–	nS

Note

51. Limited by GPIO output frequency, see [Table 11-10](#) on page 64.

Figure 13-4. 100-pin TQFP (14 × 14 × 1.4 mm) Package Outline

