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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	23
Program Memory Size	16KB (8K × 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	768 × 8
Voltage - Supply (Vcc/Vdd)	4.2V ~ 5.5V
Data Converters	A/D 5x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f242-e-so

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

TABLE 1-2: PIC18F2X2 PINOUT I/O DESCRIPTIONS (CONTINUED)

Din Norro	Pin N	umber	Pin Buffer		Description		
Pin Name	DIP	SOIC	Туре	Туре	Description		
					PORTC is a bi-directional I/O port.		
RC0/T1OSO/T1CKI RC0 T1OSO T1CKI	11	11	I/O O I	ST — ST	Digital I/O. Timer1 oscillator output. Timer1/Timer3 external clock input.		
RC1/T1OSI/CCP2 RC1 T1OSI CCP2	12	12	I/O I I/O	ST CMOS ST	Digital I/O. Timer1 oscillator input. Capture2 input, Compare2 output, PWM2 output.		
RC2/CCP1 RC2 CCP1	13	13	I/O I/O	ST ST	Digital I/O. Capture1 input/Compare1 output/PWM1 output.		
RC3/SCK/SCL RC3 SCK SCL	14	14	I/O I/O I/O	ST ST ST	Digital I/O. Synchronous serial clock input/output for SPI mode. Synchronous serial clock input/output for I ² C mode		
RC4/SDI/SDA RC4 SDI SDA	15	15	I/O I I/O	ST ST ST	Digital I/O. SPI Data In. I ² C Data I/O.		
RC5/SDO RC5 SDO	16	16	I/O O	ST —	Digital I/O. SPI Data Out.		
RC6/TX/CK RC6 TX CK	17	17	I/O O I/O	ST — ST	Digital I/O. USART Asynchronous Transmit. USART Synchronous Clock (see related RX/DT).		
RC7/RX/DT RC7 RX DT	18	18	I/O I I/O	ST ST ST	Digital I/O. USART Asynchronous Receive. USART Synchronous Data (see related TX/CK).		
Vss	8, 19	8, 19	Р	_	Ground reference for logic and I/O pins.		
Vdd	20	20	Р	_	Positive supply for logic and I/O pins.		
Legend: TTL = TTL o	compati	ble inpu	ıt		CMOS = CMOS compatible input or output		

ST = Schmitt Trigger input with CMOS levels

I = Input P = Power

O = Output OD = Open Drain (no P diode to VDD)

2.4 External Clock Input

The EC and ECIO Oscillator modes require an external clock source to be connected to the OSC1 pin. The feedback device between OSC1 and OSC2 is turned off in these modes to save current. There is no oscillator start-up time required after a Power-on Reset or after a recovery from SLEEP mode.

In the EC Oscillator mode, the oscillator frequency divided by 4 is available on the OSC2 pin. This signal may be used for test purposes or to synchronize other logic. Figure 2-4 shows the pin connections for the EC Oscillator mode.

FIGURE 2-4: EXTERNAL CLOCK INPUT OPERATION



The ECIO Oscillator mode functions like the EC mode, except that the OSC2 pin becomes an additional general purpose I/O pin. The I/O pin becomes bit 6 of PORTA (RA6). Figure 2-5 shows the pin connections for the ECIO Oscillator mode.

FIGURE 2-5:

OPERATION (ECIO CONFIGURATION)

EXTERNAL CLOCK INPUT



2.5 HS/PLL

A Phase Locked Loop circuit is provided as a programmable option for users that want to multiply the frequency of the incoming crystal oscillator signal by 4. For an input clock frequency of 10 MHz, the internal clock frequency will be multiplied to 40 MHz. This is useful for customers who are concerned with EMI due to high frequency crystals.

The PLL can only be enabled when the oscillator configuration bits are programmed for HS mode. If they are programmed for any other mode, the PLL is not enabled and the system clock will come directly from OSC1.

The PLL is one of the modes of the FOSC<2:0> configuration bits. The Oscillator mode is specified during device programming.

A PLL lock timer is used to ensure that the PLL has locked before device execution starts. The PLL lock timer has a time-out that is called TPLL.





FIGURE 3-4: TIME-OUT SEQUENCE ON POWER-UP (MCLR NOT TIED TO VDD): CASE 1



FIGURE 3-5: TIME-OUT SEQUENCE ON POWER-UP (MCLR NOT TIED TO VDD): CASE 2









8.5 RCON Register

The RCON register contains the bit which is used to enable prioritized interrupts (IPEN).

REGISTER 8-10: RCON REGISTER

	R/W-0	U-0	U-0	R/W-1	R-1	R-1	R/W-0	R/W-0
	IPEN	_	_	RI	TO	PD	POR	BOR
	bit 7							bit 0
bit 7	IPEN: Inte 1 = Enable 0 = Disabl	rrupt Priority e priority leve le priority leve	Enable bit Is on interrup els on interru	ots pts (16CXXX	Compatibil	ity mode)		
bit 6-5	Unimplem	nented: Read	as '0'					
bit 4	RI: RESET	Instruction F	lag bit					
	For details	of bit operati	on, see Regi	ister 4-3				
bit 3	TO: Watch	dog Time-ou	t Flag bit					
	For details	of bit operati	on, see Regi	ister 4-3				
bit 2	PD: Power	r-down Detec	tion Flag bit					
	For details	of bit operati	on, see Regi	ister 4-3				
bit 1	POR: Pow	ver-on Reset	Status bit					
	For details	of bit operati	on, see Regi	ister 4-3				
bit 0	BOR: Brow	wn-out Reset	Status bit					
	For details of bit operation, see Register 4-3							
	Legend:							
	R = Reada	able bit	W = Wr	itable bit	U = Unimp	lemented	bit, read as	'0'
	- n = Value	e at POR	'1' = Bit	is set	'0' = Bit is	cleared	x = Bit is ι	Inknown

10.1 Timer0 Operation

Timer0 can operate as a timer or as a counter.

Timer mode is selected by clearing the T0CS bit. In Timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If the TMR0L register is written, the increment is inhibited for the following two instruction cycles. The user can work around this by writing an adjusted value to the TMR0L register.

Counter mode is selected by setting the T0CS bit. In Counter mode, Timer0 will increment, either on every rising or falling edge of pin RA4/T0CKI. The incrementing edge is determined by the Timer0 Source Edge Select bit (T0SE). Clearing the T0SE bit selects the rising edge. Restrictions on the external clock input are discussed below.

When an external clock input is used for Timer0, it must meet certain requirements. The requirements ensure the external clock can be synchronized with the internal phase clock (Tosc). Also, there is a delay in the actual incrementing of Timer0 after synchronization.

10.2 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module. The prescaler is not readable or writable.

The PSA and T0PS2:T0PS0 bits determine the prescaler assignment and prescale ratio.

Clearing bit PSA will assign the prescaler to the Timer0 module. When the prescaler is assigned to the Timer0 module, prescale values of 1:2, 1:4,..., 1:256 are selectable.

When assigned to the Timer0 module, all instructions writing to the TMR0L register (e.g., CLRF TMR0, MOVWF TMR0, BSF TMR0, x....etc.) will clear the prescaler count.

Note:	Writing to TMR0L when the prescaler is
	assigned to Timer0 will clear the prescaler
	count, but will not change the prescaler
	assignment.

10.2.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control, (i.e., it can be changed "on-the-fly" during program execution).

10.3 Timer0 Interrupt

The TMR0 interrupt is generated when the TMR0 register overflows from FFh to 00h in 8-bit mode, or FFFFh to 0000h in 16-bit mode. This overflow sets the TMR0IF bit. The interrupt can be masked by clearing the TMR0IE bit. The TMR0IE bit must be cleared in software by the Timer0 module Interrupt Service Routine before re-enabling this interrupt. The TMR0 interrupt cannot awaken the processor from SLEEP, since the timer is shut-off during SLEEP.

10.4 16-Bit Mode Timer Reads and Writes

TMR0H is not the high byte of the timer/counter in 16-bit mode, but is actually a buffered version of the high byte of Timer0 (refer to Figure 10-2). The high byte of the Timer0 counter/timer is not directly readable nor writable. TMR0H is updated with the contents of the high byte of Timer0 during a read of TMR0L. This provides the ability to read all 16-bits of Timer0 without having to verify that the read of the high and low byte were valid due to a rollover between successive reads of the high and low byte.

A write to the high byte of Timer0 must also take place through the TMR0H buffer register. Timer0 high byte is updated with the contents of TMR0H when a write occurs to TMR0L. This allows all 16-bits of Timer0 to be updated at once.

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on All Other RESETS
TMR0L	Timer0 Modu	ule Low Byte F	Register						xxxx xxxx	uuuu uuuu
TMR0H	Timer0 Modu	ule High Byte	Register						0000 0000	0000 0000
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	x000 0000	0000 000u
T0CON	TMR0ON	ON T08BIT TOCS TOSE PSA TOPS2 TOPS1 TOPS0							1111 1111	1111 1111
TRISA	_	- PORTA Data Direction Register						-111 1111	-111 1111	

TABLE 10-1: REGISTERS ASSOCIATED WITH TIMER0

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by Timer0.

11.2 Timer1 Oscillator

A crystal oscillator circuit is built-in between pins T1OSI (input) and T1OSO (amplifier output). It is enabled by setting control bit T1OSCEN (T1CON<3>). The oscillator is a low power oscillator rated up to 200 kHz. It will continue to run during SLEEP. It is primarily intended for a 32 kHz crystal. Table 11-1 shows the capacitor selection for the Timer1 oscillator.

The user must provide a software time delay to ensure proper start-up of the Timer1 oscillator.

TABLE 11-1: CAPACITOR SELECTION FOR THE ALTERNATE OSCILLATOR

Osc Type	Freq	C1	C2			
LP	32 kHz	TBD ⁽¹⁾	TBD ⁽¹⁾			
	Crystal to be Tested:					
32.768 kHz	Epson C-001R32.768K-A ± 20 PPM					

- **Note 1:** Microchip suggests 33 pF as a starting point in validating the oscillator circuit.
 - 2: Higher capacitance increases the stability of the oscillator, but also increases the start-up time.
 - **3:** Since each resonator/crystal has its own characteristics, the user should consult the resonator/crystal manufacturer for appropriate values of external components.
 - 4: Capacitor values are for design guidance only.

11.3 Timer1 Interrupt

The TMR1 Register pair (TMR1H:TMR1L) increments from 0000h to FFFFh and rolls over to 0000h. The TMR1 Interrupt, if enabled, is generated on overflow, which is latched in interrupt flag bit TMR1IF (PIR1<0>). This interrupt can be enabled/disabled by setting/ clearing TMR1 interrupt enable bit, TMR1IE (PIE1<0>).

11.4 Resetting Timer1 using a CCP Trigger Output

If the CCP module is configured in Compare mode to generate a "special event trigger" (CCP1M3:CCP1M0 = 1011), this signal will reset Timer1 and start an A/D conversion (if the A/D module is enabled).

Note:	The spe	cial e	vent	trigg	ers from tl	ne CC	P1
	module	will	not	set	interrupt	flag	bit
	TMR1IF	(PIR	1<0>).			

Timer1 must be configured for either Timer or Synchronized Counter mode to take advantage of this feature. If Timer1 is running in Asynchronous Counter mode, this RESET operation may not work.

In the event that a write to Timer1 coincides with a special event trigger from CCP1, the write will take precedence.

In this mode of operation, the CCPR1H:CCPR1L registers pair effectively becomes the period register for Timer1.

11.5 Timer1 16-Bit Read/Write Mode

Timer1 can be configured for 16-bit reads and writes (see Figure 11-2). When the RD16 control bit (T1CON<7>) is set, the address for TMR1H is mapped to a buffer register for the high byte of Timer1. A read from TMR1L will load the contents of the high byte of Timer1 into the Timer1 high byte buffer. This provides the user with the ability to accurately read all 16-bits of Timer1 without having to determine whether a read of the high byte followed by a read of the low byte is valid, due to a rollover between reads.

A write to the high byte of Timer1 must also take place through the TMR1H buffer register. Timer1 high byte is updated with the contents of TMR1H when a write occurs to TMR1L. This allows a user to write all 16 bits to both the high and low bytes of Timer1 at once.

The high byte of Timer1 is not directly readable or writable in this mode. All reads and writes must take place through the Timer1 high byte buffer register. Writes to TMR1H do not clear the Timer1 prescaler. The prescaler is only cleared on writes to TMR1L.

13.0 TIMER3 MODULE

The Timer3 module timer/counter has the following features:

- 16-bit timer/counter (two 8-bit registers; TMR3H and TMR3L)
- Readable and writable (both registers)
- Internal or external clock select
- Interrupt-on-overflow from FFFFh to 0000h
- RESET from CCP module trigger

Figure 13-1 is a simplified block diagram of the Timer3 module.

Register 13-1 shows the Timer3 control register. This register controls the Operating mode of the Timer3 module and sets the CCP clock source.

Register 11-1 shows the Timer1 control register. This register controls the Operating mode of the Timer1 module, as well as contains the Timer1 oscillator enable bit (T1OSCEN), which can be a clock source for Timer3.

REGISTER 13-1: T3CON: TIMER3 CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RD16	T3CCP2	T3CKPS1	T3CKPS0	T3CCP1	T3SYNC	TMR3CS	TMR3ON
bit 7							bit 0

bit 7	RD16: 16-bit Read/Write I 1 = Enables register Read 0 = Enables register Read	Mode Enable bit I/Write of Timer3 in on I/Write of Timer3 in two	e 16-bit operation o 8-bit operations	
bit 6-3	T3CCP2:T3CCP1: Timer3 1x = Timer3 is the clock so 01 = Timer3 is the clock so Timer1 is the clock so 00 = Timer1 is the clock so	3 and Timer1 to CCPx ource for compare/cap ource for compare/cap ource for compare/cap ource for compare/cap	Enable bits oture CCP modules oture of CCP2, oture of CCP1 oture CCP modules	
bit 5-4	T3CKPS1:T3CKPS0 : Tim 11 = 1:8 Prescale value 10 = 1:4 Prescale value 01 = 1:2 Prescale value 00 = 1:1 Prescale value	er3 Input Clock Presc	ale Select bits	
bit 2	T3SYNC: Timer3 External (Not usable if the system of <u>When TMR3CS = 1:</u> 1 = Do not synchronize external0 = Synchronize externalWhen TMR3CS = 0:This bit is ignored. Timer3	I Clock Input Synchror clock comes from Time kternal clock input clock input	hization Control bit er1/Timer3) k when TMR3CS = 0.	
bit 1	TMR3CS: Timer3 Clock S 1 = External clock input fr (on the rising edge af 0 = Internal clock (Fosc/4	ource Select bit om Timer1 oscillator c ter the first falling edge	ər T1CKI ə)	
bit 0	TMR3ON: Timer3 On bit 1 = Enables Timer3 0 = Stops Timer3			
	Legend:			
	R = Readable bit - n = Value at POR	W = Writable bit '1' = Bit is set	U = Unimplemented '0' = Bit is cleared	bit, read as '0' x = Bit is unknown

15.3.1 REGISTERS

The MSSP module has four registers for SPI mode operation. These are:

- MSSP Control Register1 (SSPCON1)
- MSSP Status Register (SSPSTAT)
- Serial Receive/Transmit Buffer (SSPBUF)
- MSSP Shift Register (SSPSR) Not directly accessible

SSPCON1 and SSPSTAT are the control and status registers in SPI mode operation. The SSPCON1 register is readable and writable. The lower 6 bits of the SSPSTAT are read only. The upper two bits of the SSPSTAT are read/write. SSPSR is the shift register used for shifting data in or out. SSPBUF is the buffer register to which data bytes are written to or read from.

In receive operations, SSPSR and SSPBUF together create a double buffered receiver. When SSPSR receives a complete byte, it is transferred to SSPBUF and the SSPIF interrupt is set.

During transmission, the SSPBUF is not double buffered. A write to SSPBUF will write to both SSPBUF and SSPSR.

REGISTER 15-1: SSPSTAT: MSSP STATUS REGISTER (SPI MODE)

	R/W-0	R/W-0	R-0	R-0	R-0	R-0	R-0	R-0			
	SMP	CKE	D/A	Р	S	R/W	UA	BF			
	bit 7							bit 0			
bit 7	SMP: Sam	ple bit									
	SPI Master	mode:									
	1 = Input da	ata sampled	at end of da	ata output tir	ne						
		ata sampieu	at middle o	data outpu	time						
	SMP must	<u>node:</u> be cleared v	when SPI is	used in Slav	e mode						
hit 6		Clock Edge	Select		e mode						
	When CKP		001001								
	1 = Data tra	<u> </u>	n rising edge	of SCK							
	0 = Data tra	ansmitted or	n falling edge	e of SCK							
	When CKP	= 1:									
	1 = Data tra	ansmitted or	n falling edge	e of SCK							
	0 = Data tra	ansmitted or	n rising edge	of SCK							
bit 5	D/A: Data/	Address bit									
	Used in I ² C	c mode only									
bit 4	P: STOP bi	it									
	Used in I ² (cleared.	C mode only	y. This bit is	cleared wh	nen the MS	SP module	is disabled,	SSPEN is			
bit 3	S: START b	oit									
	Used in I ² C	mode only									
bit 2	R/W: Read	/Write bit inf	ormation								
	Used in I ² C	mode only									
bit 1	UA: Update	UA: Update Address									
	Used in I ² C	mode only									
bit 0	BF: Buffer	Full Status b	it (Receive i	mode only)							
	1 = Receive complete, SSPBUF is full										
	0 = Receive	e not comple	ete, SSPBUI	is empty							
	Legend:										
		bla hit	\// _ \//ritab	lo hit		lomontod bi	t road as 'O	,			
								alvaavra			
	-n = value	al POR	I = BIT IS S	sei	v = Bit IS	ciearea	x = BIT IS U	IKNOWN			



FIGURE 15-6: SPI MODE WAVEFORM (SLAVE MODE WITH CKE = 1)



REGISTER 15-4: SSPCON1: MSSP CONTROL REGISTER1 (I²C MODE)

| R/W-0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| WCOL | SSPOV | SSPEN | CKP | SSPM3 | SSPM2 | SSPM1 | SSPM0 |
| bit 7 | | | | | | | bit 0 |

bit 7 WCOL: Write Collision Detect bit

In Master Transmit mode:

- 1 = A write to the SSPBUF register was attempted while the I^2C conditions were not valid for a transmission to be started (must be cleared in software)
- 0 = No collision
- In Slave Transmit mode:
- 1 = The SSPBUF register is written while it is still transmitting the previous word (must be cleared in software)
- $0 = No \ collision$
- In Receive mode (Master or Slave modes):

This is a "don't care" bit

bit 6 SSPOV: Receive Overflow Indicator bit

- In Receive mode:
 - 1 = A byte is received while the SSPBUF register is still holding the previous byte (must be cleared in software)
 - 0 = No overflow
 - In Transmit mode:

This is a "don't care" bit in Transmit mode

bit 5 SSPEN: Synchronous Serial Port Enable bit

- 1 = Enables the serial port and configures the SDA and SCL pins as the serial port pins
- 0 = Disables serial port and configures these pins as I/O port pins

When enabled, the SDA and SCL pins must be properly configured as input or output. Note:

bit 4 CKP: SCK Belease Control bit

- In Slave mode:
- 1 = Release clock
- 0 = Holds clock low (clock stretch), used to ensure data setup time
- In Master mode:

Unused in this mode

bit 3-0 SSPM3:SSPM0: Synchronous Serial Port Mode Select bits

- 1111 = I^2C Slave mode, 10-bit address with START and STOP bit interrupts enabled
- $1110 = I^2C$ Slave mode, 7-bit address with START and STOP bit interrupts enabled
- $1011 = I^2C$ Firmware Controlled Master mode (Slave IDLE)
- 1000 = I²C Master mode, clock = Fosc / (4 * (SSPADD+1))
- $0111 = I^2C$ Slave mode, 10-bit address
- $0110 = I^2C$ Slave mode, 7-bit address
 - Note: Bit combinations not specifically listed here are either reserved, or implemented in SPI mode only.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	t, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

15.4.4 CLOCK STRETCHING

Both 7- and 10-bit Slave modes implement automatic clock stretching during a transmit sequence.

The SEN bit (SSPCON2<0>) allows clock stretching to be enabled during receives. Setting SEN will cause the SCL pin to be held low at the end of each data receive sequence.

15.4.4.1 Clock Stretching for 7-bit Slave Receive Mode (SEN = 1)

In 7-bit Slave Receive mode, on the falling edge of the ninth clock at the end of the ACK sequence, if the BF bit is set, the CKP bit in the SSPCON1 register is automatically cleared, forcing the SCL output to be held low. The CKP being cleared to '0' will assert the SCL line low. The CKP bit must be set in the user's ISR before reception is allowed to continue. By holding the SCL line low, the user has time to service the ISR and read the contents of the SSPBUF before the master device can initiate another receive sequence. This will prevent buffer overruns from occurring (see Figure 15-13).

- Note 1: If the user reads the contents of the SSPBUF before the falling edge of the ninth clock, thus clearing the BF bit, the CKP bit will not be cleared and clock stretching will not occur.
 - 2: The CKP bit can be set in software, regardless of the state of the BF bit. The user should be careful to clear the BF bit in the ISR before the next receive sequence, in order to prevent an overflow condition.

15.4.4.2 Clock Stretching for 10-bit Slave Receive Mode (SEN = 1)

In 10-bit Slave Receive mode, during the address sequence, clock stretching automatically takes place but CKP is not cleared. During this time, if the UA bit is set after the ninth clock, clock stretching is initiated. The UA bit is set after receiving the upper byte of the 10-bit address, and following the receive of the second byte of the 10-bit address with the R/W bit cleared to '0'. The release of the clock line occurs upon updating SSPADD. Clock stretching will occur on each data receive sequence as described in 7-bit mode.

Note: If the user polls the UA bit and clears it by updating the SSPADD register before the falling edge of the ninth clock occurs, and if the user hasn't cleared the BF bit by reading the SSPBUF register before that time, then the CKP bit will still NOT be asserted low. Clock stretching on the basis of the state of the BF bit only occurs during a data sequence, not an address sequence.

15.4.4.3 Clock Stretching for 7-bit Slave Transmit Mode

7-bit Slave Transmit mode implements clock stretching by clearing the CKP bit after the falling edge of the ninth clock, if the BF bit is clear. This occurs, regardless of the state of the SEN bit.

The user's ISR must set the CKP bit before transmission is allowed to continue. By holding the SCL line low, the user has time to service the ISR and load the contents of the SSPBUF before the master device can initiate another transmit sequence (see Figure 15-9).

Note 1: If the user loads the contents of SSPBUF, setting the BF bit before the falling edge of the ninth clock, the CKP bit will not be cleared and clock stretching will not occur.
2: The CKP bit can be set in software, regardless of the state of the BF bit.

15.4.4.4 Clock Stretching for 10-bit Slave Transmit Mode

In 10-bit Slave Transmit mode, clock stretching is controlled during the first two address sequences by the state of the UA bit, just as it is in 10-bit Slave Receive mode. The first two addresses are followed by a third address sequence, which contains the high order bits of the 10-bit address and the R/W bit set to '1'. After the third address sequence is performed, the UA bit is not set, the module is now configured in Transmit mode, and clock stretching is controlled by the BF flag, as in 7-bit Slave Transmit mode (see Figure 15-11).

NOTES:

TABLE 20-2:	PIC18FXXX INSTRUCTION SET	(CONTINUED)
-------------	---------------------------	-------------

Mnemonic,		Description	Cycles	16-Bit Instruction Word				Status	Notoo
Opera	nds	Description	Cycles	MSb			LSb	Affected	Notes
CONTROL	OPERA	TIONS							
BC	n	Branch if Carry	1 (2)	1110	0010	nnnn	nnnn	None	
BN	n	Branch if Negative	1 (2)	1110	0110	nnnn	nnnn	None	
BNC	n	Branch if Not Carry	1 (2)	1110	0011	nnnn	nnnn	None	
BNN	n	Branch if Not Negative	1 (2)	1110	0111	nnnn	nnnn	None	
BNOV	n	Branch if Not Overflow	1 (2)	1110	0101	nnnn	nnnn	None	
BNZ	n	Branch if Not Zero	2	1110	0001	nnnn	nnnn	None	
BOV	n	Branch if Overflow	1 (2)	1110	0100	nnnn	nnnn	None	
BRA	n	Branch Unconditionally	1 (2)	1101	0nnn	nnnn	nnnn	None	
BZ	n	Branch if Zero	1 (2)	1110	0000	nnnn	nnnn	None	
CALL	n, s	Call subroutine1st word	2	1110	110s	kkkk	kkkk	None	
		2nd word		1111	kkkk	kkkk	kkkk		
CLRWDT	—	Clear Watchdog Timer	1	0000	0000	0000	0100	TO, PD	
DAW	—	Decimal Adjust WREG	1	0000	0000	0000	0111	С	
GOTO	n	Go to address1st word	2	1110	1111	kkkk	kkkk	None	
		2nd word		1111	kkkk	kkkk	kkkk		
NOP	—	No Operation	1	0000	0000	0000	0000	None	
NOP	—	No Operation	1	1111	xxxx	XXXX	xxxx	None	4
POP	—	Pop top of return stack (TOS)	1	0000	0000	0000	0110	None	
PUSH	_	Push top of return stack (TOS)	1	0000	0000	0000	0101	None	
RCALL	n	Relative Call	2	1101	1nnn	nnnn	nnnn	None	
RESET		Software device RESET	1	0000	0000	1111	1111	All	
RETFIE	S	Return from interrupt enable	2	0000	0000	0001	000s	GIE/GIEH,	
								PEIE/GIEL	
RETLW	k	Return with literal in WREG	2	0000	1100	kkkk	kkkk	None	
RETURN	S	Return from Subroutine	2	0000	0000	0001	001s	None	
SLEEP	—	Go into Standby mode	1	0000	0000	0000	0011	TO, PD	

Note 1: When a PORT register is modified as a function of itself (e.g., MOVF PORTB, 1, 0), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

2: If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned.

3: If Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

4: Some instructions are 2-word instructions. The second word of these instructions will be executed as a NOP, unless the first word of the instruction retrieves the information embedded in these 16-bits. This ensures that all program memory locations have a valid instruction.

5: If the Table Write starts the write cycle to internal memory, the write will continue until terminated.

AND	DWF	AND W w	ith f		BC		Branch if	Carry			
Syn	tax:	[label] A	NDWF f[,d [,a]	Syn	tax:	[<i>label</i>] B	[<i>label</i>] BC n			
Ope	rands:	$0 \le f \le 25$	5		Ope	erands:	-128 ≤ n ≤	127			
		d ∈ [0,1] a ∈ [0,1]			Ope	eration:	if carry bit (PC) + 2	if carry bit is '1' (PC) + 2 + 2n \rightarrow PC			
Ope	ration:	(W) .AND	. (f) $ ightarrow$ dest		Stat	us Affected:	None				
Stat	us Affected:	N,Z			Enc	odina:	1110	0010 nr	nnn nnnn		
Enc	oding:	0001	01da ff	ff ffff		crintion.	If the Carr	v bit is '1' t	hen the		
Des	escription: The contents of W are AND'ed with register 'f'. If 'd' is 0, the result is stored in W. If 'd' is 1, the result is stored back in register 'f' (default). If 'a' is 0, the Access Bank will be selected. If 'a' is 1, the BSR will not be overridden (default).				program v The 2's cc added to t have incre instructior PC+2+2n a two-cycl	vill branch. omplement r he PC. Sin emented to f n, the new a . This instru- le instruction	number '2n' is ce the PC will fetch the next ddress will be iction is then n.				
Wor	ds:	1			Wor	rds:	1				
Сус	les:	1			Сус	les:	1(2)				
QC	Cycle Activity:				QQ	Cycle Activity	/:				
	Q1	Q2	Q3	Q4	If J	ump:					
	Decode	Read	Process	Write to		Q1	Q2	Q3	Q4		
		register 'f'	Data	destination	J	Decode	Read literal 'n'	Process Data	Write to PC		
<u>Exa</u>	<u>mple</u> :	ANDWF	REG, 0, 0			No	No	No	No		
	Before Instru	iction				operation	operation	operation	operation		
	W	= 0x17			lf N	lo Jump:					
	REG	= 0xC2				Q1	Q2	Q3	Q4		
	After Instruct	tion				Decode	Read literal	Process	No		
	W	= 0x02					11	Dala	operation		
	REG	= 0xC2			<u>Exa</u>	mple:	HERE	BC 5			
						Before Instr	ruction				
						PC		droce (UEDI	7)		

Before Instruction	n		
PC	=	address	(HERE)
After Instruction			
If Carry	=	1;	
PC	=	address	(HERE+12)
If Carry	=	0;	
PC	=	address	(HERE+2)

BNC	;	Branch if	Not Carry		BNN	Branch if	Not Negati	ve
Synt	ax:	[<i>label</i>] B	NC n		Syntax:	[label] B	NN n	
Ope	rands:	-128 ≤ n ≤ 127		Operands:	-128 ≤ n ≤	127		
Ope	ration:	if carry bit (PC) + 2 +	is '0' · 2n → PC		Operation:	if negative (PC) + 2 +	bit is '0' $2n \rightarrow PC$	
Statu	us Affected:	None			Status Affected:	None		
Enco	oding:	1110	0011 nn:	nn nnnn	Encoding:	1110	0111 nn	nn nnnn
Des	cription:	If the Carry bit is '0', then the program will branch. The 2's complement number '2n' is added to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC+2+2n. This instruction is then a two-cycle instruction.		Description:	If the Neg program w The 2's cc added to t have incre instruction PC+2+2n. a two-cycl	ative bit is '0 vill branch. mplement n he PC. Since mented to fu , the new ac This instru e instruction	', then the umber '2n' is se the PC will etch the next ldress will be ction is then	
Wor	ds:	1			Words:	1		
Cycl	es:	1(2)		Cycles:	1(2)	1(2)		
Q C If Ju	cycle Activity: ump:				Q Cycle Activity: If Jump:			
	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4
	Decode	Read literal 'n'	Process Data	Write to PC	Decode	Read literal 'n'	Process Data	Write to PC
	No	No	No	No	No	No	No	No
14 8 1	operation	operation	operation	operation	operation	operation	operation	operation
IT IN	o Jump: Q1	02	03	Q4	IT INO JUMP: Q1	02	03	Q4
	Decode	Read literal 'n'	Process Data	No operation	Decode	Read literal 'n'	Process Data	No operation
<u>Exa</u>	<u>mple</u> :	HERE	BNC Jump		Example:	HERE	BNN Jump)
Before Instruction			Before Instru	uction				
PC = address (HERE) After Instruction If Carry = 0; PC = address (Jump) If Carry = 1;					PC After Instruct If Negativ PC If Negativ	= ad tion /e = 0; /e = 1;	dress (HERE dress (Jump)





TABLE 22-15:	I ² C BUS START/STOP	BITS REQUIREMENTS	(SLAVE MODE)
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Param. No.	Symbol	Characteristic		Min	Max	Units	Conditions
90	TSU:STA	START condition	100 kHz mode	4700	—	ns	Only relevant for Repeated
		Setup time	400 kHz mode	600	_		START condition
91	THD:STA	START condition	100 kHz mode	4000	_	ns	After this period, the first
		Hold time	400 kHz mode	600	_		clock pulse is generated
92	Tsu:sto	STOP condition	100 kHz mode	4700	_	ns	
		Setup time	400 kHz mode	600	_		
93	THD:STO	STOP condition	100 kHz mode	4000	_	ns	
		Hold time	400 kHz mode	600			





24.2 Package Details

The following sections give the technical details of the packages.

28-Lead Skinny Plastic Dual In-line (SP) – 300 mil Body (PDIP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	INCHES*			MILLIMETERS		
Dimension L	imits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		28			28	
Pitch	р		.100			2.54	
Top to Seating Plane	А	.140	.150	.160	3.56	3.81	4.06
Molded Package Thickness	A2	.125	.130	.135	3.18	3.30	3.43
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	Е	.300	.310	.325	7.62	7.87	8.26
Molded Package Width	E1	.275	.285	.295	6.99	7.24	7.49
Overall Length	D	1.345	1.365	1.385	34.16	34.67	35.18
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	С	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.040	.053	.065	1.02	1.33	1.65
Lower Lead Width	В	.016	.019	.022	0.41	0.48	0.56
Overall Row Spacing §	eB	.320	.350	.430	8.13	8.89	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter § Significant Characteristic

Notes:

Dimension D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side. JEDEC Equivalent: MO-095

Drawing No. C04-070

40-Lead Plastic Dual In-line (P) – 600 mil Body (PDIP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



wolded Package Thickness	AZ	.140	.150	.160	3.50	3.01	4.00
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.595	.600	.625	15.11	15.24	15.88
Molded Package Width	E1	.530	.545	.560	13.46	13.84	14.22
Overall Length	D	2.045	2.058	2.065	51.94	52.26	52.45
Tip to Seating Plane	L	.120	.130	.135	3.05	3.30	3.43
Lead Thickness	С	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.030	.050	.070	0.76	1.27	1.78
Lower Lead Width	В	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.620	.650	.680	15.75	16.51	17.27
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter § Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side. JEDEC Equivalent: MO-011

Drawing No. C04-016

44-Lead Plastic Thin Quad Flatpack (PT) 10x10x1 mm Body, 1.0/0.10 mm Lead Form (TQFP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units INCHES			MILLIMETERS*			
Dimension Limi	MIN	NOM	MAX	MIN	NOM	MAX	
Number of Pins	n		44			4	4
Pitch	р		.031			0.	80
Pins per Side	n1		11			1	1
Overall Height	Α	.039	.043	.047	1.00	1.10	1.20
Molded Package Thickness	A2	.037	.039	.041	0.95	1.00	1.05
Standoff	A1	.002	.004	.006	0.05	0.10	0.15
Foot Length	L	.018	.024	.030	0.45	0.60	0.75
Footprint (Reference)	F		.039 REF.		1.00 REF.		
Foot Angle	φ	0	3.5	7	0	3.5	7
Overall Width	E	.463	.472	.482	11.75	12.00	12.25
Overall Length	D	.463	.472	.482	11.75	12.00	12.25
Molded Package Width	E1	.390	.394	.398	9.90	10.00	10.10
Molded Package Length	D1	.390	.394	.398	9.90	10.00	10.10
Lead Thickness	с	.004	.006	.008	0.09	0.15	0.20
Lead Width	В	.012	.015	.017	0.30	0.38	0.44
Pin 1 Corner Chamfer	СН	.025	.035	.045	0.64	0.89	1.14
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side. REF: Reference Dimension, usually without tolerance, for information purposes only.

See ASME Y14.5M

JEDEC Equivalent: MS-026 Drawing No. C04-076

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