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Applications of "<u>Embedded - Microcontrollers</u>"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	23
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	4.2V ~ 5.5V
Data Converters	A/D 5x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f242t-i-so

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

1.0 DEVICE OVERVIEW

This document contains device specific information for the following devices:

PIC18F242PIC18F442PIC18F252PIC18F452

These devices come in 28-pin and 40/44-pin packages. The 28-pin devices do not have a Parallel Slave Port (PSP) implemented and the number of Analog-to-Digital (A/D) converter input channels is reduced to 5. An overview of features is shown in Table 1-1.

The following two figures are device block diagrams sorted by pin count: 28-pin for Figure 1-1 and 40/44-pin for Figure 1-2. The 28-pin and 40/44-pin pinouts are listed in Table 1-2 and Table 1-3, respectively.

TABLE 1-1: DEVICE FEATURES

Features	PIC18F242	PIC18F252	PIC18F442	PIC18F452
Operating Frequency	DC - 40 MHz			
Program Memory (Bytes)	16K	32K	16K	32K
Program Memory (Instructions)	8192	16384	8192	16384
Data Memory (Bytes)	768	1536	768	1536
Data EEPROM Memory (Bytes)	256	256	256	256
Interrupt Sources	17	17	18	18
I/O Ports	Ports A, B, C	Ports A, B, C	Ports A, B, C, D, E	Ports A, B, C, D, E
Timers	4	4	4	4
Capture/Compare/PWM Modules	2	2	2	2
Serial Communications	MSSP, Addressable USART	MSSP, Addressable USART	MSSP, Addressable USART	MSSP, Addressable USART
Parallel Communications	_	_	PSP	PSP
10-bit Analog-to-Digital Module	5 input channels	5 input channels	8 input channels	8 input channels
RESETS (and Delays)	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST)			
Programmable Low Voltage Detect	Yes	Yes	Yes	Yes
Programmable Brown-out Reset	Yes	Yes	Yes	Yes
Instruction Set	75 Instructions	75 Instructions	75 Instructions	75 Instructions
Packages	28-pin DIP 28-pin SOIC	28-pin DIP 28-pin SOIC	40-pin DIP 44-pin PLCC 44-pin TQFP	40-pin DIP 44-pin PLCC 44-pin TQFP

FIGURE 4-1: PROGRAM MEMORY MAP AND STACK FOR PIC18F442/242

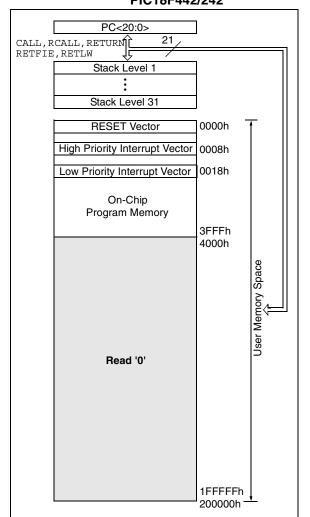
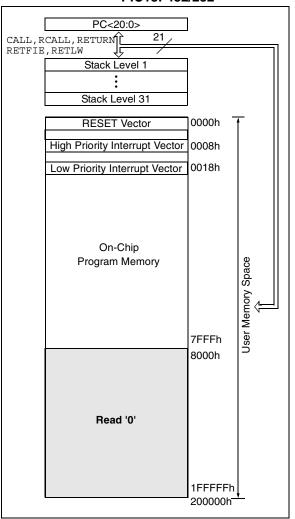


FIGURE 4-2: PROGRAM MEMORY MAP AND STACK FOR PIC18F452/252



REGISTER 4-1: STKPTR REGISTER

R/C-0	R/C-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STKOVF	STKUNF	_	SP4	SP3	SP2	SP1	SP0
bit 7							bit 0

bit 7(1) STKOVF: Stack Full Flag bit

1 = Stack became full or overflowed

0 = Stack has not become full or overflowed

bit 6(1) STKUNF: Stack Underflow Flag bit

1 =Stack underflow occurred

0 = Stack underflow did not occur

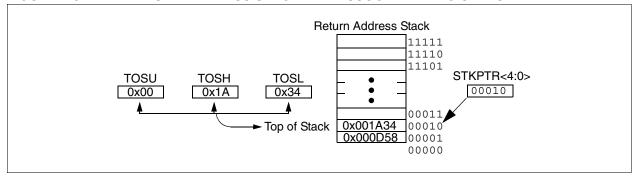
bit 5 **Unimplemented:** Read as '0'

bit 4-0 **SP4:SP0:** Stack Pointer Location bits

Note 1: Bit 7 and bit 6 can only be cleared in user software or by a POR.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented	bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

FIGURE 4-3: RETURN ADDRESS STACK AND ASSOCIATED REGISTERS



4.2.3 PUSH AND POP INSTRUCTIONS

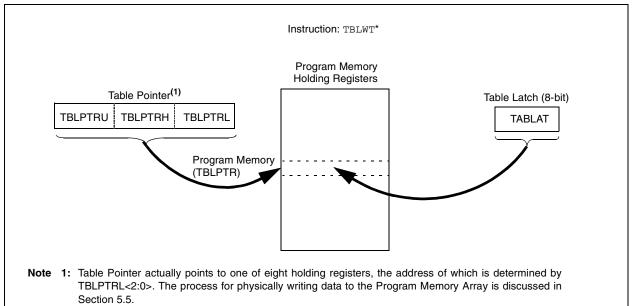
Since the Top-of-Stack (TOS) is readable and writable, the ability to push values onto the stack and pull values off the stack without disturbing normal program execution is a desirable option. To push the current PC value onto the stack, a PUSH instruction can be executed. This will increment the stack pointer and load the current PC value onto the stack. TOSU, TOSH and TOSL can then be modified to place a return address on the stack.

The ability to pull the TOS value off of the stack and replace it with the value that was previously pushed onto the stack, without disturbing normal execution, is achieved by using the POP instruction. The POP instruction discards the current TOS by decrementing the stack pointer. The previous value pushed onto the stack then becomes the TOS value.

4.2.4 STACK FULL/UNDERFLOW RESETS

These resets are enabled by programming the STVREN configuration bit. When the STVREN bit is disabled, a full or underflow condition will set the appropriate STKFUL or STKUNF bit, but not cause a device RESET. When the STVREN bit is enabled, a full or underflow will set the appropriate STKFUL or STKUNF bit and then cause a device RESET. The STKFUL or STKUNF bits are only cleared by the user software or a POR Reset.

FIGURE 5-2: TABLE WRITE OPERATION



5.2 Control Registers

Several control registers are used in conjunction with the TBLRD and TBLWT instructions. These include the:

- EECON1 register
- EECON2 register
- TABLAT register
- · TBLPTR registers

5.2.1 EECON1 AND EECON2 REGISTERS

EECON1 is the control register for memory accesses.

EECON2 is not a physical register. Reading EECON2 will read all '0's. The EECON2 register is used exclusively in the memory write and erase sequences.

Control bit EEPGD determines if the access will be a program or data EEPROM memory access. When clear, any subsequent operations will operate on the data EEPROM memory. When set, any subsequent operations will operate on the program memory.

Control bit CFGS determines if the access will be to the configuration registers or to program memory/data EEPROM memory. When set, subsequent operations will operate on configuration registers, regardless of EEPGD (see "Special Features of the CPU", Section 19.0). When clear, memory selection access is determined by EEPGD.

The FREE bit, when set, will allow a program memory erase operation. When the FREE bit is set, the erase operation is initiated on the next WR command. When FREE is clear, only writes are enabled.

The WREN bit, when set, will allow a write operation. On power-up, the WREN bit is clear. The WRERR bit is set when a write operation is interrupted by a MCLR Reset or a WDT Time-out Reset during normal operation. In these situations, the user can check the WRERR bit and rewrite the location. It is necessary to reload the data and address registers (EEDATA and EEADR), due to RESET values of zero.

Control bit WR initiates write operations. This bit cannot be cleared, only set, in software. It is cleared in hardware at the completion of the write operation. The inability to clear the WR bit in software prevents the accidental or premature termination of a write operation.

Note: Interrupt flag bit EEIF, in the PIR2 register, is set when the write is complete. It must be cleared in software.

REGISTER 8-7: PIE2: PERIPHERAL INTERRUPT ENABLE REGISTER 2

U-0	U-0	U-0	R/W-0	R/W-0 BCLIE	R/W-0 LVDIE	R/W-0 TMR3IE	R/W-0 CCP2IE
			LLIL	DOLIL	LVDIL	TIVITIOIL	OOI ZIL

bit 7

bit 7-5 Unimplemented: Read as '0'

bit 4 **EEIE**: Data EEPROM/FLASH Write Operation Interrupt Enable bit

1 = Enabled

0 = Disabled

bit 3 BCLIE: Bus Collision Interrupt Enable bit

1 = Enabled

0 = Disabled

bit 2 LVDIE: Low Voltage Detect Interrupt Enable bit

1 = Enabled 0 = Disabled

bit 1 TMR3IE: TMR3 Overflow Interrupt Enable bit

1 = Enables the TMR3 overflow interrupt

0 = Disables the TMR3 overflow interrupt

bit 0 CCP2IE: CCP2 Interrupt Enable bit

1 = Enables the CCP2 interrupt 0 = Disables the CCP2 interrupt

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

- n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

9.4 PORTD, TRISD and LATD Registers

This section is applicable only to the PIC18F4X2 devices.

PORTD is an 8-bit wide, bi-directional port. The corresponding Data Direction register is TRISD. Setting a TRISD bit (= 1) will make the corresponding PORTD pin an input (i.e., put the corresponding output driver in a Hi-Impedance mode). Clearing a TRISD bit (= 0) will make the corresponding PORTD pin an output (i.e., put the contents of the output latch on the selected pin).

The Data Latch register (LATD) is also memory mapped. Read-modify-write operations on the LATD register reads and writes the latched output value for PORTD.

PORTD is an 8-bit port with Schmitt Trigger input buffers. Each pin is individually configurable as an input or output.

Note: On a Power-on Reset, these pins are configured as digital inputs.

PORTD can be configured as an 8-bit wide microprocessor port (parallel slave port) by setting control bit PSPMODE (TRISE<4>). In this mode, the input buffers are TTL. See Section 9.6 for additional information on the Parallel Slave Port (PSP).

EXAMPLE 9-4: INITIALIZING PORTD

CLRF	PORTD	; Initialize PORTD by ; clearing output
CLRF	LATD	<pre>; data latches ; Alternate method ; to clear output ; data latches</pre>
MOVLW	0xCF	<pre>; Value used to ; initialize data : direction</pre>
MOVWF	TRISD	; Set RD<3:0> as inputs ; RD<5:4> as outputs ; RD<7:6> as inputs
	CLRF	

FIGURE 9-8: PORTD BLOCK DIAGRAM IN I/O PORT MODE

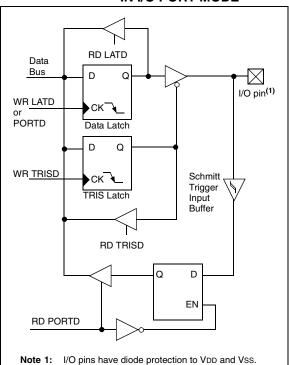


TABLE 9-9: PORTE FUNCTIONS

Name	Bit#	Buffer Type	Function
RE0/RD/AN5	bit0	ST/TTL ⁽¹⁾	Input/output port pin or read control input in Parallel Slave Port mode or analog input: RD
			1 = Not a read operation0 = Read operation. Reads PORTD register (if chip selected).
RE1/WR/AN6	bit1	ST/TTL ⁽¹⁾	Input/output port pin or write control input in Parallel Slave Port mode or analog input: WR 1 = Not a write operation 0 = Write operation. Writes PORTD register (if chip selected).
RE2/CS/AN7	bit2	ST/TTL ⁽¹⁾	Input/output port pin or chip select control input in Parallel Slave Port mode or analog input: CS 1 = Device is not selected 0 = Device is selected

Legend: ST = Schmitt Trigger input, TTL = TTL input

Note 1: Input buffers are Schmitt Triggers when in I/O mode and TTL buffers when in Parallel Slave Port mode.

TABLE 9-10: SUMMARY OF REGISTERS ASSOCIATED WITH PORTE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on All Other RESETS
PORTE	_	_		_	_	RE2	RE1	RE0	000	000
LATE	_	_	_	_	_	LATE Data Output Register			xxx	uuu
TRISE	IBF	OBF	IBOV	PSPMODE	_	PORTE Data Direction bits			0000 -111	0000 -111
ADCON1	ADFM	ADCS2	_	_	PCFG3	PCFG2	PCFG1	PCFG0	00 0000	00 0000

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by PORTE.

15.4.9 I²C MASTER MODE REPEATED START CONDITION TIMING

A Repeated START condition occurs when the RSEN bit (SSPCON2<1>) is programmed high and the I²C logic module is in the IDLE state. When the RSEN bit is set, the SCL pin is asserted low. When the SCL pin is sampled low, the baud rate generator is loaded with the contents of SSPADD<5:0> and begins counting. The SDA pin is released (brought high) for one baud rate generator count (TBRG). When the baud rate generator times out, if SDA is sampled high, the SCL pin will be de-asserted (brought high). When SCL is sampled high, the baud rate generator is reloaded with the contents of SSPADD<6:0> and begins counting. SDA and SCL must be sampled high for one TBRG. This action is then followed by assertion of the SDA pin (SDA = 0) for one TBRG while SCL is high. Following this, the RSEN bit (SSPCON2<1>) will be automatically cleared and the baud rate generator will not be reloaded, leaving the SDA pin held low. As soon as a START condition is detected on the SDA and SCL pins, the S bit (SSPSTAT<3>) will be set. The SSPIF bit will not be set until the baud rate generator has timed out.

Note 1: If RSEN is programmed while any other event is in progress, it will not take effect.

- **2:** A bus collision during the Repeated START condition occurs if:
 - SDA is sampled low when SCL goes from low to high.
 - SCL goes low before SDA is asserted low. This may indicate that another master is attempting to transmit a data "1".

Immediately following the SSPIF bit getting set, the user may write the SSPBUF with the 7-bit address in 7-bit mode, or the default first address in 10-bit mode. After the first eight bits are transmitted and an ACK is received, the user may then transmit an additional eight bits of address (10-bit mode) or eight bits of data (7-bit mode).

15.4.9.1 WCOL Status Flag

Note:

If the user writes the SSPBUF when a Repeated START sequence is in progress, the WCOL is set and the contents of the buffer are unchanged (the write doesn't occur).

Because queueing of events is not allowed, writing of the lower 5 bits of SSPCON2 is disabled until the Repeated START condition is complete.

FIGURE 15-20: REPEAT START CONDITION WAVEFORM

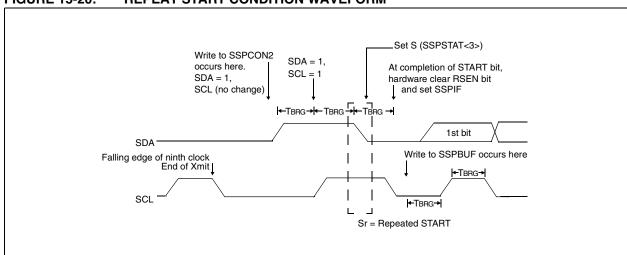


TABLE 19-1: CONFIGURATION BITS AND DEVICE IDS

File	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default/ Unprogrammed Value
300001h	CONFIG1H	_	_	OSCSEN	_	_	FOSC2	FOSC1	FOSC0	1111
300002h	CONFIG2L	_	_	_	_	BORV1	BORV0	BOREN	PWRTEN	1111
300003h	CONFIG2H	_	_	_	_	WDTPS2	WDTPS1	WDTPS0	WDTEN	1111
300005h	CONFIG3H	_	_	_	_	_	_	_	CCP2MX	1
300006h	CONFIG4L	DEBUG	_	_	_	_	LVP	_	STVREN	11-1
300008h	CONFIG5L	_	_	_	_	CP3	CP2	CP1	CP0	1111
300009h	CONFIG5H	CPD	CPB	_	_	_	_	_	_	11
30000Ah	CONFIG6L	_	_	_	_	WRT3	WRT2	WRT1	WRT0	1111
30000Bh	CONFIG6H	WRTD	WRTB	WRTC	_	_	_	ı	_	111
30000Ch	CONFIG7L	_	_	_	_	EBTR3	EBTR2	EBTR1	EBTR0	1111
30000Dh	CONFIG7H	_	EBTRB	_	_	_	_	_	_	-1
3FFFFEh	DEVID1	DEV2	DEV1	DEV0	REV4	REV3	REV2	REV1	REV0	(1)
3FFFFFh	DEVID2	DEV10	DEV9	DEV8	DEV7	DEV6	DEV5	DEV4	DEV3	0000 0100

 $\label{eq:local_equation} \textbf{Legend:} \quad x = \textbf{unknown}, \, u = \textbf{unchanged}, \, \textbf{-} = \textbf{unimplemented}, \, q = \textbf{value depends on condition}.$

Shaded cells are unimplemented, read as '0'.

Note 1: See Register 19-12 for DEVID1 values.

REGISTER 19-1: CONFIGURATION REGISTER 1 HIGH (CONFIG1H: BYTE ADDRESS 300001h)

U-0	U-0	R/P-1	U-0	U-0	R/P-1	R/P-1	R/P-1
_	_	OSCSEN	_	_	FOSC2	FOSC1	FOSC0
bit 7							bit 0

bit 7-6 Unimplemented: Read as '0'

bit 5 OSCSEN: Oscillator System Clock Switch Enable bit

1 = Oscillator system clock switch option is disabled (main oscillator is source)

0 = Oscillator system clock switch option is enabled (oscillator switching is enabled)

bit 4-3 Unimplemented: Read as '0'

bit 2-0 FOSC2:FOSC0: Oscillator Selection bits

111 = RC oscillator w/ OSC2 configured as RA6

110 = HS oscillator with PLL enabled/Clock frequency = (4 x Fosc)

101 = EC oscillator w/ OSC2 configured as RA6

100 = EC oscillator w/ OSC2 configured as divide-by-4 clock output

011 = RC oscillator

010 = HS oscillator

001 = XT oscillator

000 = LP oscillator

Legend:

R = Readable bit P = Programmable bit U = Unimplemented bit, read as '0'

- n = Value when device is unprogrammed u = Unchanged from programmed state

BTF	sc	Bit Test Fi	le, Skip if Cl	ear	BTF	SS	Bit Test Fi	le, Skip if Se	t
Synt	ax:	[label] B1	TFSC f,b[,a]		Synt	ax:	[label] B1	FSS f,b[,a]	
Ope	rands:	$0 \le f \le 255$ $0 \le b \le 7$ $a \in [0,1]$			Ope	rands:	$0 \le f \le 255$ $0 \le b \le 7$ $a \in [0,1]$		
Ope	ration:	skip if (f <b:< td=""><td>>) = 0</td><td></td><td>Ope</td><td>ration:</td><td colspan="3">skip if $(f < b >) = 1$</td></b:<>	>) = 0		Ope	ration:	skip if $(f < b >) = 1$		
Statu	tatus Affected: None			Statu	us Affected:	None			
Enco	oding:	1011	bbba ff	ff ffff	Enco	oding:	1010	bbba ffi	ff ffff
Desc	cription:	next instruction of the control of t	egister 'f' is 0 ction is skippe of the the nearing the curre s discarded, anstead, makin action. If 'a' is nk will be selected (default).	ed. ext instruction nt instruction and a NOP is ng this a two- 0, the ected, over- a' = 1, then	Desc	cription:	If bit 'b' in register 'f' is 1, then the next instruction is skipped. If bit 'b' is 1, then the next instruction fetched during the current instruction execution, is discarded and a NOP is executed instead, making this a two-cycle instruction. If 'a' is 0, the Access Bank will be selected, overriding the BSR value. If 'a' = 1, then the bank will be selected as per the BSR value (default).		
Word	ds:	1			Wor	ds:	1		
Cycle	es:		ycles if skip a a 2-word inst		Cycl	es:		cycles if skip a a 2-word inst	
QC	ycle Activity:				QC	cycle Activity:			
	Q1	Q2	Q3	Q4		Q1	Q2	Q3	Q4
	Decode	Read register 'f'	Process Data	No operation		Decode	Read register 'f'	Process Data	No operation
If sk	in:	i ogloto.	1	operane	If sk	cin:	i ogloto.		opo.uo
	Q1	Q2	Q3	Q4	0.	Q1	Q2	Q3	Q4
	No operation	No operation	No operation	No operation		No	No	No	No
If ok		ed by 2-word		operation		operation	operation	operation	operation
11 51	Q1	Q2	Q3	Q4	IT SH	kip and follow Q1	ed by 2-word Q2	Q3	Q4
	No No	No	No	No No		No	No	No No	No
	operation	operation	operation	operation		operation	operation	operation	operation
	No operation	No operation	No operation	No operation		No operation	No operation	No operation	No operation
	mple: Before Instru PC After Instruct If FLAG< PC If FLAG< PC PC	FALSE : TRUE : ction = add ion 1> = 0; = add 1> = 1;		s, 1, 0		mple: Before Instru PC After Instruct If FLAG< PC If FLAG<	FALSE : TRUE : ction = add ion 1> = 0; = add 1> = 1;	ress (HERE) ress (FALSE)	, 1, 0

PIC18FXX2

MULLW	Multiply	Literal v	vith W	
Syntax:	[label]	MULLW	' k	
Operands:	$0 \le k \le 2$	55		
Operation:	(W) x k –	→ PRODI	H:PRODL	=
Status Affected:	None			
Encoding:	0000	1101	kkkk	kkkk
Description:	W and the 16-bit research PRODH: PRODH W is uncluded None of taffected.	petween to e 8-bit litte sult is plate PRODL in contains the status of t	the conte eral 'k'. T ced in register p the high l s flags are overflow in this ope	nts of he air. byte. e nor
Words:	1			
Cycles:	1			
Q Cycle Activity:				
Q1	Q2	Q3	3	Q4

Q1	Q2	Q3	Q4
Decode	Read	Process	Write
	literal 'k'	Data	registers
			PRODH:
			PRODL

Example: MULLW 0xC4

Before Instruction

 $\begin{array}{lll} W & = & 0xE2 \\ PRODH & = & ? \\ PRODL & = & ? \end{array}$

After Instruction

 $\begin{array}{lll} W & = & 0xE2 \\ PRODH & = & 0xAD \\ PRODL & = & 0x08 \end{array}$

MULWF	Multiply	W with	f					
Syntax:	[label]	MULWI	f [,a]					
Operands:	$0 \le f \le 255$ $a \in [0,1]$							
Operation:	(W) x (f) \rightarrow PRODH:PRODL							
Status Affected:	None							
Encoding:	0000	001a	ffff	ffff				
Description:	An unsig ried out to W and the The 16-b PRODH: PRODH Both W a Mone of 1 affected. Note that carry is p tion. A zero to detect Access E overriding 'a' = 1, the selected (default).	petween e registe it result PRODL contains and 'f' are the statu a neither cossible ero resul sted. If 'a Bank will g the BS een the b as per the	the conterfile localis stored register particle localis stored register particle localis stored register particle localis stored register particle localis stored localis s	ents of tion 'f'. in the pair. byte. ged. re nor era-ple but eted, If				
	•							
,	1							
Words: Cycles:	tion. A ze not detect Access E overriding 'a' = 1, th selected (default).	ero resulted. If 'as ank will generate BS ank will generate BS as per tless as per	t is possil d' is 0, the be selec d'R value. Dank will b	ole but e ted, If oe				

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read	Process	Write
	register 'f'	Data	registers
			PRODH:
			PRODL

Example: MULWF REG, 1

Before Instruction

W = 0xC4 REG = 0xB5 PRODH = ? PRODL = ?

After Instruction

W = 0xC4 REG = 0xB5 PRODH = 0x8A PRODL = 0x94

RETURN	Return from Subroutine					
Syntax:	[label] RETURN [s]					
Operands:	$s \in [0,1]$					
Operation:	$ \begin{split} &(TOS) \to PC,\\ &if \; s = 1\\ &(WS) \to W,\\ &(STATUSS) \to STATUS,\\ &(BSRS) \to BSR,\\ &PCLATU, \; PCLATH \; are \; unchanged \end{split} $					
Status Affected:	None					
Encoding:	0000 0000 0001 001s					
Description:	Return from subroutine. The stack is popped and the top of the stack (TOS) is loaded into the program counter. If 's'= 1, the contents of the shadow registers WS, STATUSS and BSRS are loaded into their corresponding registers, W, STATUS					

Words: 1 Cycles: 2

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	No	Process	pop PC from
	operation	Data	stack
No	No	No	No
operation	operation	operation	operation

and BSR. If 's' = 0, no update of these registers occurs (default).

Example: RETURN

> After Interrupt PC = TOS

RLC	F	Rotate L	eft f thro	ugh Cai	rry			
Synt	ax:	[label]	RLCF	f [,d [,a]				
Ope	rands:	$0 \le f \le 25$ $d \in [0,1]$ $a \in [0,1]$	55					
Ope	ration:	(f<7>) →	(f <n>) → dest<n+1>, (f<7>) → C, (C) → dest<0></n+1></n>					
Statu	us Affected:	C, N, Z	C, N, Z					
Enco	oding:	0011	01da	ffff	ffff			
Desc	cription:	rotated or the Carry is placed is stored (default). Bank will the BSR bank will	The contents of register 'f' are rotated one bit to the left through the Carry Flag. If 'd' is 0, the result is placed in W. If 'd' is 1, the result is stored back in register 'f' (default). If 'a' is 0, the Access Bank will be selected, overriding the BSR value. If 'a' = 1, then the bank will be selected as per the BSR value (default).					
Wor	ds:	1						
Cycl	es:	1						
QC	cycle Activity:							
	Q1	Q2	Q3		Q4			
	Decode	Read register 'f'	Proces Data	-	rite to tination			

Example: RLCF REG, 0, 0

Before Instruction

REG C 1110 0110 **0**

After Instruction

REG 1110 0110 1100 1100

SUBLW	Subtract	W from literal	SUBWF	Subtract W from f
Syntax:	[label] S	SUBLW k	Syntax:	[label] SUBWF f [,d [,a]
Operands:	$0 \le k \le 25$	55	Operands:	$0 \le f \le 255$
Operation:	k – (W) –	\rightarrow W		$d \in [0,1]$
Status Affected:	N, OV, C,	, DC, Z	On and the man	$a \in [0,1]$
Encoding:	0000	1000 kkkk kkkk	Operation:	$(f) - (W) \rightarrow dest$
Description:	W is subt	racted from the eight-bit	Status Affected:	N, OV, C, DC, Z
	literal 'k'. in W.	The result is placed	Encoding: Description:	0101 11da ffff ffff Subtract W from register 'f' (2's
Words:	1		·	complement method). If 'd' is 0,
Cycles:	1			the result is stored in W. If 'd' is 1, the result is stored back in regis-
Q Cycle Activity:				ter 'f' (default). If 'a' is 0, the
Q1	Q2	Q3 Q4		Access Bank will be selected,
Decode	Read literal 'k'	Process Write to W Data		overriding the BSR value. If 'a' is 1, then the bank will be selected as per the BSR value (default).
Example 1:	SUBLW 0)x02	Words:	1
Before Instru	ction		Cycles:	1
W C	= 1 = ?		Q Cycle Activity:	
After Instruct			Q1	Q2 Q3 Q4
W	= 1		Decode	Read Process Write to
C Z	= 1 ; re = 0	esult is positive		register 'f' Data destination
N	= 0		Example 1:	SUBWF REG, 1, 0
Example 2:	SUBLW 0)x02	Before Instru	
Before Instru	ction		REG W	= 3 = 2
W C	= 2 = ?		С	= ?
After Instruct	•		After Instruc	tion = 1
W	= 0		W	= 2
C Z	= 1 ; re = 1	esult is zero	C Z	= 1 ; result is positive = 0
N	= 0		N	= 0
Example 3:	SUBLW 0)x02	Example 2:	SUBWF REG, 0, 0
Before Instru	ction		Before Instru	
W C	= 3 = ?		REG W	= 2 = 2
After Instruct			С	= ?
W		's complement)	After Instruc	tion = 2
С	= 0 ; res	sult is negative	W REG	= 2 = 0
Z N	= 0 = 1		С	= 1 ; result is zero
			Z N	= 1 = 0
			Example 3:	SUBWF REG, 1, 0
			Before Instru	uction
			REG	= 1
			W C	= 2 = ?
			After Instruc	
			REG	= FFh ;(2's complement)
			W C	= 2 = 0 ; result is negative
			Z	= 0
			N	= 1

FIGURE 22-3: LOW VOLTAGE DETECT CHARACTERISTICS

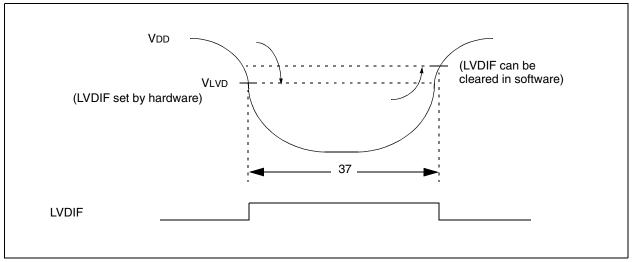


TABLE 22-1: LOW VOLTAGE DETECT CHARACTERISTICS

					-	erature ·	-40°C ≤ T	a (unless otherwise stated) TA ≤ +85°C for industrial TA ≤ +125°C for extended
Param No.	Symbol	Character	ristic	Min	Тур	Max	Units	Conditions
D420	D420 VLVD LVD Voltage on VDD transition high to low	LVV = 0001	1.98	2.06	2.14	V	T ≥ 25°C	
		LVV = 0010	2.18	2.27	2.36	V	T ≥ 25°C	
		LVV = 0011	2.37	2.47	2.57	V	T ≥ 25°C	
			LVV = 0100	2.48	2.58	2.68	V	
			LVV = 0101	2.67	2.78	2.89	V	
		LVV = 0110	2.77	2.89	3.01	V		
		LVV = 0111	2.98	3.1	3.22	V		
			LVV = 1000	3.27	3.41	3.55	V	
			LVV = 1001	3.47	3.61	3.75	V	
		LVV = 1010	3.57	3.72	3.87	V		
		LVV = 1011	3.76	3.92	4.08	V		
			LVV = 1100	3.96	4.13	4.3	V	
			LVV = 1101	4.16	4.33	4.5	V	
			LVV = 1110	4.45	4.64	4.83	V	

22.3.2 TIMING CONDITIONS

The temperature and voltages specified in Table 22-3 apply to all timing specifications unless otherwise noted. Figure 22-4 specifies the load conditions for the timing specifications.

TABLE 22-3: TEMPERATURE AND VOLTAGE SPECIFICATIONS - AC

Standard Operating Conditions (unless otherwise stated)

Operating temperature -40°C ≤ TA ≤ +85°C for industrial

-40°C ≤ TA ≤ +125°C for extended

Operating voltage VDD range as described in DC spec Section 22.1 and Section 22.2.

LC parts operate for industrial temperatures only.

FIGURE 22-4: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

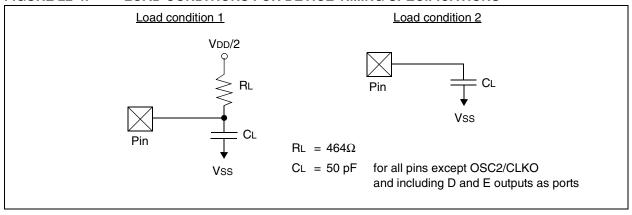


TABLE 22-5: PLL CLOCK TIMING SPECIFICATIONS (VDD = 4.2 TO 5.5V)

Param No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
_	Fosc	Oscillator Frequency Range	4	_	10	MHz	HS mode only
_	Fsys	On-chip VCO System Frequency	16	_	40	MHz	HS mode only
_	t _{rc}	PLL Start-up Time (Lock Time)	_	_	2	ms	
_	Δ CLK	CLKO Stability (Jitter)	-2		+2	%	

[†] Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.



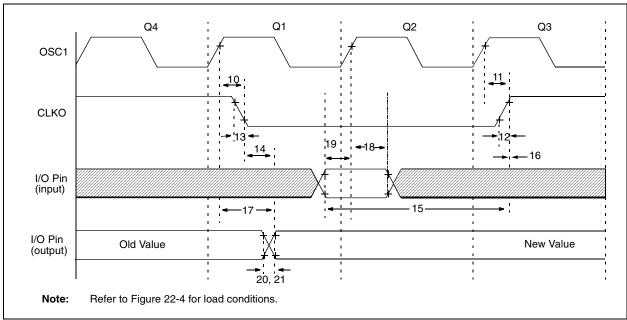
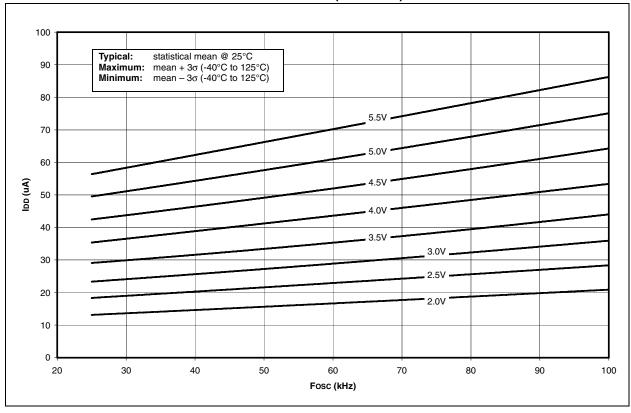


FIGURE 23-7: TYPICAL IDD vs. FOSC OVER VDD (LP MODE)





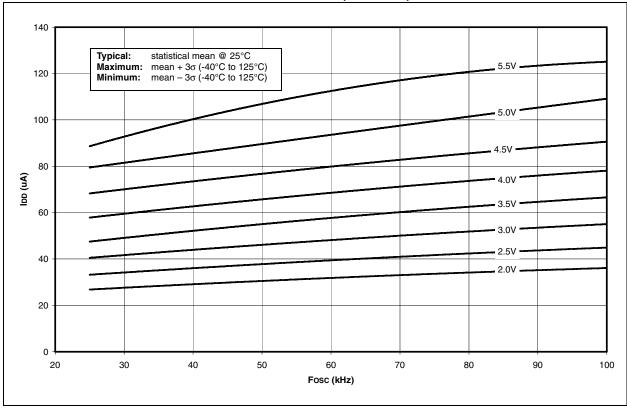


FIGURE 23-25: MINIMUM AND MAXIMUM VIN vs. VDD (ST INPUT, -40°C TO +125°C)

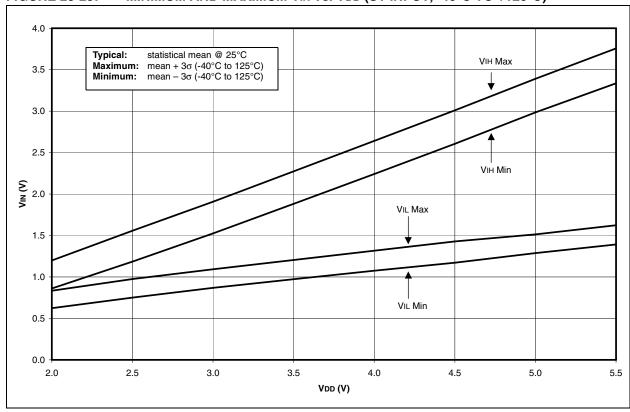
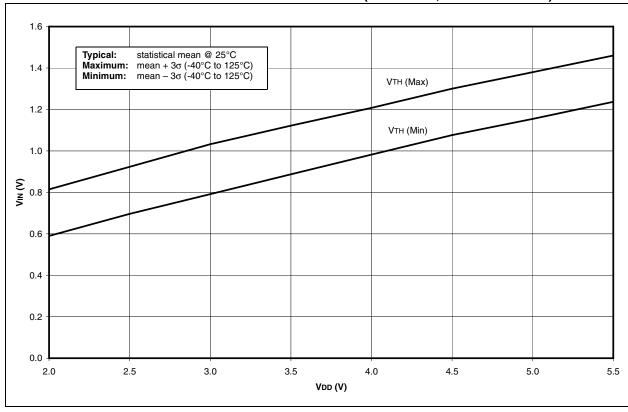


FIGURE 23-26: MINIMUM AND MAXIMUM VIN vs. VDD (TTL INPUT, -40°C TO +125°C)



P		RC7/RX/DT	_
Packaging	305	RD0/PSP0	16
Details		RD1/PSP1	16
Marking Information		RD2/PSP2	16
Parallel Slave Port		RD3/PSP3	16
PORTD	100	RD4/PSP4	16
Parallel Slave Port (PSP)		RD5/PSP5	16
		RD6/PSP6	16
Associated Registers		RD7/PSP7	16
REO/RD/AN5 Pin		RE0/RD/AN5	16
RE1/WR/AN6 Pin		RE1/WR/AN6	16
RE2/CS/AN7 Pin		RE2/CS/AN7	
Select (PSPMODE Bit)	95, 100	VDD	
PIC18F2X2 Pin Functions		Vss	
MCLR/VPP		PIC18FXX2 Voltage-Frequency Graph	10
OSC1/CLKI		(Industrial)	260
OSC2/CLKO/RA6	10	PIC18LFXX2 Voltage-Frequency Graph	200
RA0/AN0	10		000
RA1/AN1	10	(Industrial)	200
RA2/AN2/VREF	10	PICDEM 1 Low Cost PICmicro	055
RA3/AN3/VREF+	10	Demonstration Board	
RA4/T0CKI	10	PICDEM 17 Demonstration Board	256
RA5/AN4/SS/LVDIN	10	PICDEM 2 Low Cost PIC16CXX	
RB0/INT0		Demonstration Board	255
RB1/INT1		PICDEM 3 Low Cost PIC16CXXX	
RB2/INT2		Demonstration Board	256
RB3/CCP2		PICSTART Plus Entry Level Development	
RB4		Programmer	255
		PIE Registers	
RB5/PGM		Pinout I/O Descriptions	
RB6/PGC		PIC18F2X2	10
RB7/PGD		PIR Registers	
RC0/T1OSO/T1CKI		PLL Lock Time-out	
RC1/T1OSI/CCP2		Pointer, FSR	
RC2/CCP1			
RC3/SCK/SCL	12	POP Book as Book	240
RC4/SDI/SDA	12	POR. See Power-on Reset	
RC5/SDO	12	PORTA	
RC6/TX/CK	12	Associated Registers	
RC7/RX/DT	12	LATA Register	
VDD	12	PORTA Register	
Vss	12	TRISA Register	87
PIC18F4X2 Pin Functions		PORTB	
MCLR/VPP	13	Associated Registers	
OSC1/CLKI		LATB Register	
OSC2/CLKO	• • • • • • • • • • • • • • • • • • • •	PORTB Register	90
BAO/ANO		RB0/INT Pin, External	85
	• • • • • • • • • • • • • • • • • • • •	RB7:RB4 Interrupt-on-Change Flag (RBIF Bit)	90
RA1/AN1		TRISB Register	
RA2/AN2/VREF		PORTC	
RA3/AN3/VREF+		Associated Registers	94
RA4/T0CKI		LATC Register	
RA5/AN4/SS/LVDIN		PORTC Register	
RB0/INT	14	RC3/SCK/SCL Pin	
RB1	14	RC7/RX/DT Pin	
RB2	14		
RB3	14	TRISC Register	.93, 165
RB4	14	PORTD	
RB5/PGM	14	Associated Registers	
RB6/PGC		LATD Register	
RB7/PGD		Parallel Slave Port (PSP) Function	
RC0/T1OSO/T1CKI		PORTD Register	95
RC1/T1OSI/CCP2		TRISD Register	95
RC2/CCP1			
RC3/SCK/SCL			
RC4/SDI/SDA			
RC5/SDO			
RC6/TX/CK	15		

PIC18FXX2

PORTE	Regis	sters	
Analog Port Pins99, 1	00	ADCON0 (A/D Control 0)	18
Associated Registers	99	ADCON1 (A/D Control 1)	182
LATE Register		CCP1CON and CCP2CON	
PORTE Register		(Capture/Compare/PWM Control)	117
PSP Mode Select (PSPMODE Bit)95, 1		CONFIG1H (Configuration 1 High)	
RE0/RD/AN5 Pin		CONFIG2H (Configuration 2 High)	
RE1/WR/AN6 Pin		CONFIG2L (Configuration 2 Low)	
RE2/CS/AN7 Pin		CONFIG3H (Configuration 3 High)	
TRISE Register		CONFIG4L (Configuration 4 Low)	
Postscaler, WDT		CONFIG5H (Configuration 5 High)	
Assignment (PSA Bit)1		CONFIG5L (Configuration 5 Low)	
Rate Select (T0PS2:T0PS0 Bits)		CONFIG6H (Configuration 6 High)	
Switching Between Timer0 and WDT			
•		CONFIG6L (Configuration 6 Low)	
Power-down Mode. See SLEEP		CONFIG7H (Configuration 7 High)	
Power-on Reset (POR)		CONFIG7L (Configuration 7 Low)	
Oscillator Start-up Timer (OST)		DEVID1 (Device ID Register 1)	
Power-up Timer (PWRT)		DEVID2 (Device ID Register 2)	
Prescaler, Capture		EECON1 (Data EEPROM Control 1)	
Prescaler, Timer0		File Summary	
Assignment (PSA Bit)		INTCON (Interrupt Control)	
Rate Select (T0PS2:T0PS0 Bits)1		INTCON2 (Interrupt Control 2)	
Switching Between Timer0 and WDT1		INTCON3 (Interrupt Control 3)	
Prescaler, Timer21		IPR1 (Peripheral Interrupt Priority 1)	
PRO MATE II Universal Device Programmer		IPR2 (Peripheral Interrupt Priority 2)	83
Product Identification System3		LVDCON (LVD Control)	
Program Counter	(OSCCON (Oscillator Control)	2 ⁻
PCL Register	39 I	PIE1 (Peripheral Interrupt Enable 1)	80
PCLATH Register	39 I	PIE2 (Peripheral Interrupt Enable 2)	8 ⁻
PCLATU Register	39 I	PIR1 (Peripheral Interrupt Request 1)	78
Program Memory	I	PIR2 (Peripheral Interrupt Request 2)	79
Interrupt Vector		RCON (Register Control)	
Map and Stack for PIC18F442/242		RCON (RESET Control)	
Map and Stack for PIC18F452/252		RCSTA (Receive Status and Control)	
RESET Vector		SSPCON1 (MSSP Control 1)	
Program Verification and Code Protection		I ² C Mode	136
Associated Registers2		SPI Mode	
Programming, Device Instructions		SSPCON2 (MSSP Control 2)	
PSP. See Parallel Slave Port.		I ² C Mode	13
Pulse Width Modulation. See PWM (CCP Module).	9	SSPSTAT (MSSP Status)	
PUSH		I ² C Mode	139
PWM (CCP Module)		SPI Mode	
Associated Registers1		STATUS	
CCPR1H:CCPR1L Registers		STKPTR (Stack Pointer)	
Duty Cycle1		TOCON (Timer0 Control)	
Example Frequencies/Resolutions1		T1CON (Timer 1 Control)	10
Period		T2CON (Timer 2 Control)	
Setup for PWM Operation1	22	T3CON (Timer 2 Control)	!!
TMR2 to PR2 Match111.1		TRISE	
TMR2 to PR2 Match 111, 1			
Q		TXSTA (Transmit Status and Control)	
Q Clock1		WDTCON (Watchdog Timer Control)	
Q Clock		ET25, 19	
R		Brown-out Reset (BOR)	
DAM Can Data Mamony		MCLR Reset (During SLEEP)	
RAM. See Data Memory RC Oscillator		MCLR Reset (Normal Operation)	
	`	Oscillator Start-up Timer (OST)	
RCALL		Power-on Reset (POR)2	
RCSTA Register		Power-up Timer (PWRT)	
SPEN Bit		Programmable Brown-out Reset (BOR)	
Register File		RESET Instruction	
		Stack Full Reset	
	;	Stack Underflow Reset	2
	,	Watchdog Timer (WDT) Reset	2