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#### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

#### Applications of "[Embedded - Microcontrollers](#)"

##### Details

|                            |   |
|----------------------------|---|
| Product Status             | Active  |
| Core Processor             | PIC   |
| Core Size                  | 8-Bit   |
| Speed                      | 40MHz   |
| Connectivity               | I <sup>2</sup> C, SPI, UART/USART   |
| Peripherals                | Brown-out Detect/Reset, LVD, POR, PWM, WDT  |
| Number of I/O              | 34  |
| Program Memory Size        | 16KB (8K x 16)  |
| Program Memory Type        | FLASH   |
| EEPROM Size                | 256 x 8   |
| RAM Size                   | 768 x 8   |
| Voltage - Supply (Vcc/Vdd) | 4.2V ~ 5.5V   |
| Data Converters            | A/D 8x10b   |
| Oscillator Type            | External  |
| Operating Temperature      | -40°C ~ 85°C (TA)   |
| Mounting Type              | Surface Mount   |
| Package / Case             | 44-LCC (J-Lead)   |
| Supplier Device Package    | 44-PLCC (16.59x16.59)   |
| Purchase URL               | <a href="https://www.e-xfl.com/product-detail/microchip-technology/pic18f442-i-l">https://www.e-xfl.com/product-detail/microchip-technology/pic18f442-i-l</a> |

# PIC18FXX2

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**TABLE 1-2: PIC18F2X2 PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name                                 | Pin Number |       | Pin Type          | Buffer Type      | Description  |
|--|------------|-------|-------------------|------------------|--|
|  | DIP        | SOIC  |                   |                  |  |
| RC0/T1OSO/T1CKI<br>RC0<br>T1OSO<br>T1CKI | 11         | 11    | I/O<br>O<br>I     | ST<br>—<br>ST    | PORTC is a bi-directional I/O port.<br><br>Digital I/O.<br>Timer1 oscillator output.<br>Timer1/Timer3 external clock input.            |
| RC1/T1OSI/CCP2<br>RC1<br>T1OSI<br>CCP2   | 12         | 12    | I/O<br>I<br>I/O   | ST<br>CMOS<br>ST | Digital I/O.<br>Timer1 oscillator input.<br>Capture2 input, Compare2 output, PWM2 output.  |
| RC2/CCP1<br>RC2<br>CCP1                  | 13         | 13    | I/O<br>I/O        | ST<br>ST         | Digital I/O.<br>Capture1 input/Compare1 output/PWM1 output.  |
| RC3/SCK/SCL<br>RC3<br>SCK<br>SCL         | 14         | 14    | I/O<br>I/O<br>I/O | ST<br>ST<br>ST   | Digital I/O.<br>Synchronous serial clock input/output for SPI mode.<br>Synchronous serial clock input/output for I <sup>2</sup> C mode |
| RC4/SDI/SDA<br>RC4<br>SDI<br>SDA         | 15         | 15    | I/O<br>I<br>I/O   | ST<br>ST<br>ST   | Digital I/O.<br>SPI Data In.<br>I <sup>2</sup> C Data I/O.   |
| RC5/SDO<br>RC5<br>SDO                    | 16         | 16    | I/O<br>O          | ST<br>—          | Digital I/O.<br>SPI Data Out.  |
| RC6/TX/CK<br>RC6<br>TX<br>CK             | 17         | 17    | I/O<br>O<br>I/O   | ST<br>—<br>ST    | Digital I/O.<br>USART Asynchronous Transmit.<br>USART Synchronous Clock (see related RX/DT).   |
| RC7/RX/DT<br>RC7<br>RX<br>DT             | 18         | 18    | I/O<br>I<br>I/O   | ST<br>ST<br>ST   | Digital I/O.<br>USART Asynchronous Receive.<br>USART Synchronous Data (see related TX/CK).   |
| Vss                                      | 8, 19      | 8, 19 | P                 | —                | Ground reference for logic and I/O pins.   |
| VDD                                      | 20         | 20    | P                 | —                | Positive supply for logic and I/O pins.  |

Legend: TTL = TTL compatible input

ST = Schmitt Trigger input with CMOS levels

O = Output

OD = Open Drain (no P diode to VDD)

CMOS = CMOS compatible input or output

I = Input

P = Power

## 5.2.2 TABLAT - TABLE LATCH REGISTER

The Table Latch (TABLAT) is an 8-bit register mapped into the SFR space. The Table Latch is used to hold 8-bit data during data transfers between program memory and data RAM.

## 5.2.3 TBLPTR - TABLE POINTER REGISTER

The Table Pointer (TBLPTR) addresses a byte within the program memory. The TBLPTR is comprised of three SFR registers: Table Pointer Upper Byte, Table Pointer High Byte and Table Pointer Low Byte (TBLPTRU:TBLPTRH:TBLPTRL). These three registers join to form a 22-bit wide pointer. The low order 21 bits allow the device to address up to 2 Mbytes of program memory space. The 22nd bit allows access to the Device ID, the User ID and the Configuration bits.

The table pointer, TBLPTR, is used by the TBLRD and TBLWT instructions. These instructions can update the TBLPTR in one of four ways based on the table operation. These operations are shown in Table 5-1. These operations on the TBLPTR only affect the low order 21 bits.

## 5.2.4 TABLE POINTER BOUNDARIES

TBLPTR is used in reads, writes, and erases of the FLASH program memory.

When a TBLRD is executed, all 22 bits of the Table Pointer determine which byte is read from program memory into TABLAT.

When a TBLWT is executed, the three LSbs of the Table Pointer (TBLPTR<2:0>) determine which of the eight program memory holding registers is written to. When the timed write to program memory (long write) begins, the 19 MSbs of the Table Pointer, TBLPTR (TBLPTR<21:3>), will determine which program memory block of 8 bytes is written to. For more detail, see Section 5.5 ("Writing to FLASH Program Memory").

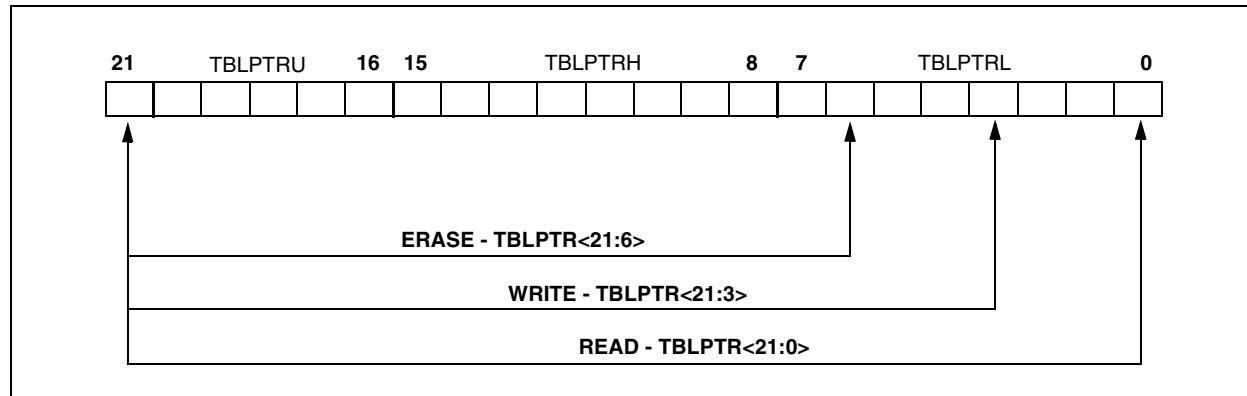
When an erase of program memory is executed, the 16 MSbs of the Table Pointer (TBLPTR<21:6>) point to the 64-byte block that will be erased. The Least Significant bits (TBLPTR<5:0>) are ignored.

Figure 5-3 describes the relevant boundaries of TBLPTR based on FLASH program memory operations.

**TABLE 5-1: TABLE POINTER OPERATIONS WITH TBLRD AND TBLWT INSTRUCTIONS**

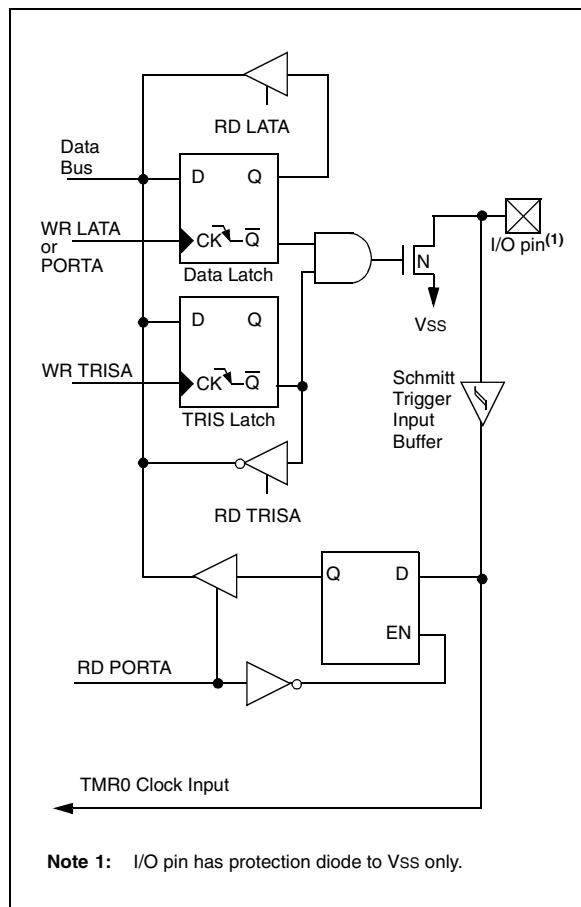
| Example | Operation on Table Pointer                  |
|---------|---|
| TBLRD*  | TBLPTR is not modified                      |
| TBLWT*  |   |
| TBLRD*+ | TBLPTR is incremented after the read/write  |
| TBLWT*+ |   |
| TBLRD*- | TBLPTR is decremented after the read/write  |
| TBLWT*- |   |
| TBLRD+* | TBLPTR is incremented before the read/write |
| TBLWT+* |   |

**FIGURE 5-3: TABLE POINTER BOUNDARIES BASED ON OPERATION**

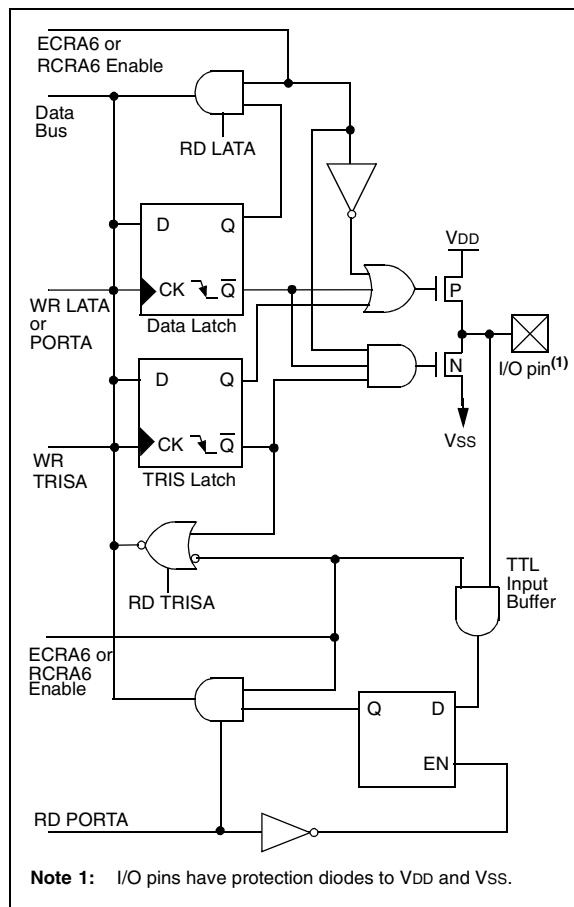


# PIC18FXX2

**FIGURE 9-2: BLOCK DIAGRAM OF RA4/T0CKI PIN**



**FIGURE 9-3: BLOCK DIAGRAM OF RA6 PIN**



## 14.4 Compare Mode

In Compare mode, the 16-bit CCPR1 (CCPR2) register value is constantly compared against either the TMR1 register pair value, or the TMR3 register pair value. When a match occurs, the RC2/CCP1 (RC1/CCP2) pin is:

- driven High
- driven Low
- toggle output (High to Low or Low to High)
- remains unchanged

The action on the pin is based on the value of control bits CCP1M3:CCP1M0 (CCP2M3:CCP2M0). At the same time, interrupt flag bit CCP1IF (CCP2IF) is set.

### 14.4.1 CCP PIN CONFIGURATION

The user must configure the CCPx pin as an output by clearing the appropriate TRISC bit.

**Note:** Clearing the CCP1CON register will force the RC2/CCP1 compare output latch to the default low level. This is not the PORTC I/O data latch.

### 14.4.2 TIMER1/TIMER3 MODE SELECTION

Timer1 and/or Timer3 must be running in Timer mode or Synchronized Counter mode if the CCP module is using the compare feature. In Asynchronous Counter mode, the compare operation may not work.

### 14.4.3 SOFTWARE INTERRUPT MODE

When generate software interrupt is chosen, the CCP1 pin is not affected. Only a CCP interrupt is generated (if enabled).

### 14.4.4 SPECIAL EVENT TRIGGER

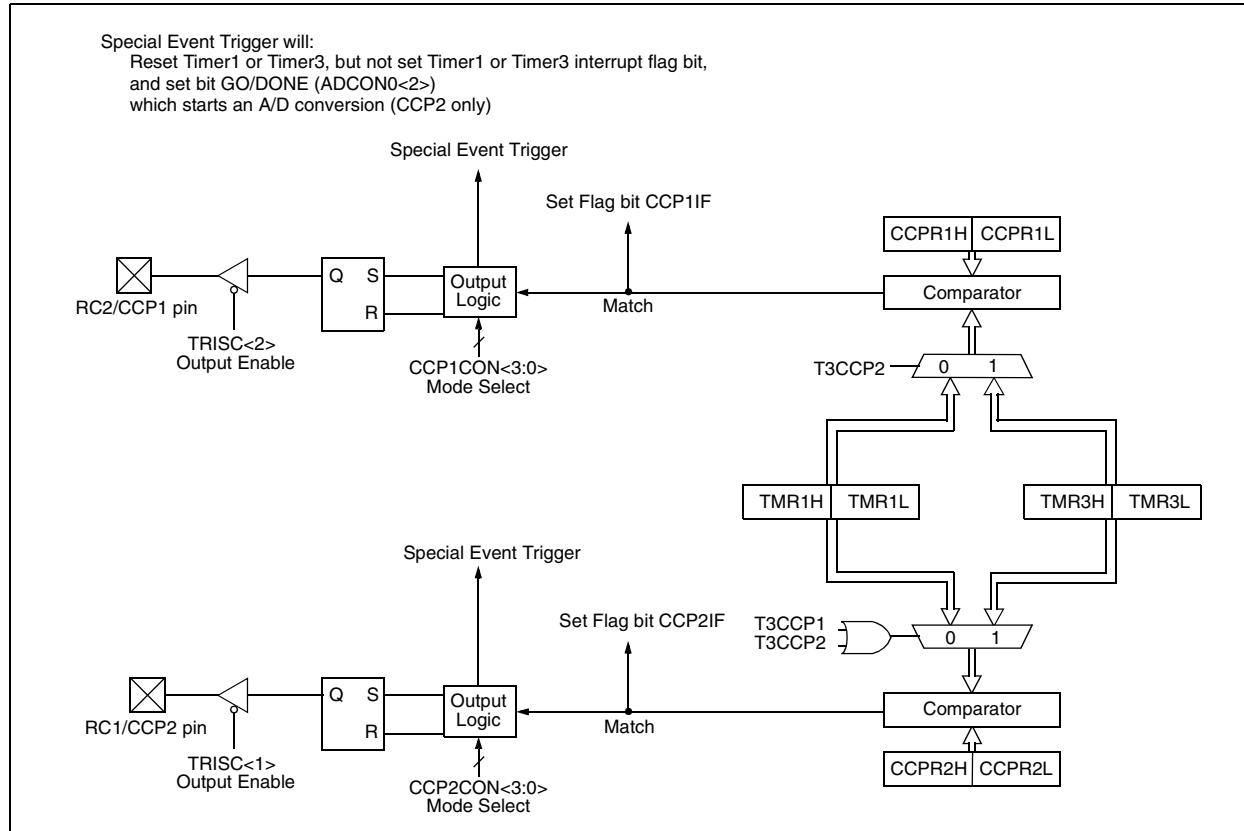
In this mode, an internal hardware trigger is generated, which may be used to initiate an action.

The special event trigger output of CCP1 resets the TMR1 register pair. This allows the CCPR1 register to effectively be a 16-bit programmable period register for Timer1.

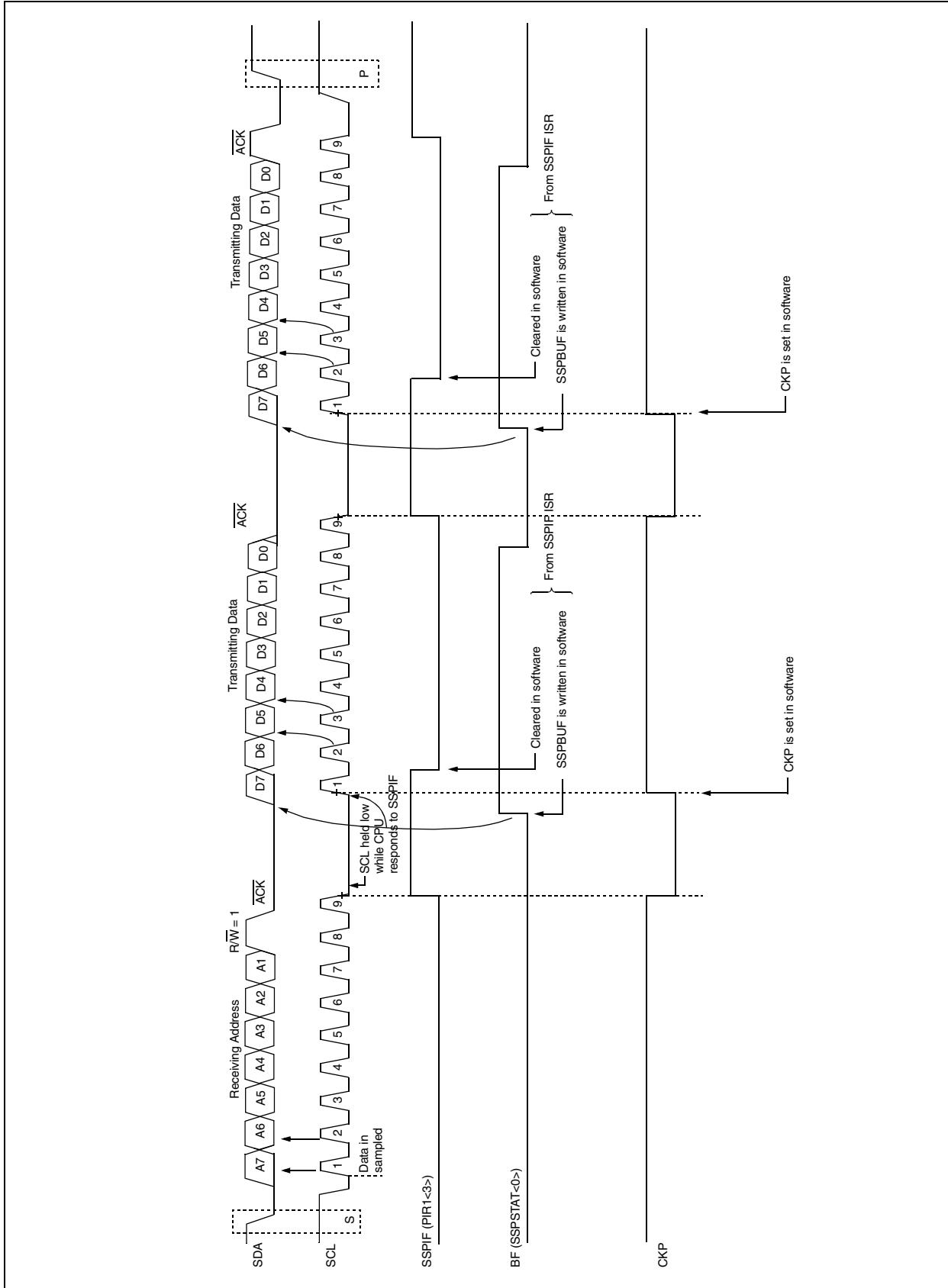
The special trigger output of CCPx resets either the TMR1 or TMR3 register pair. Additionally, the CCP2 Special Event Trigger will start an A/D conversion if the A/D module is enabled.

**Note:** The special event trigger from the CCP2 module will not set the Timer1 or Timer3 interrupt flag bits.

**FIGURE 14-2: COMPARE MODE OPERATION BLOCK DIAGRAM**

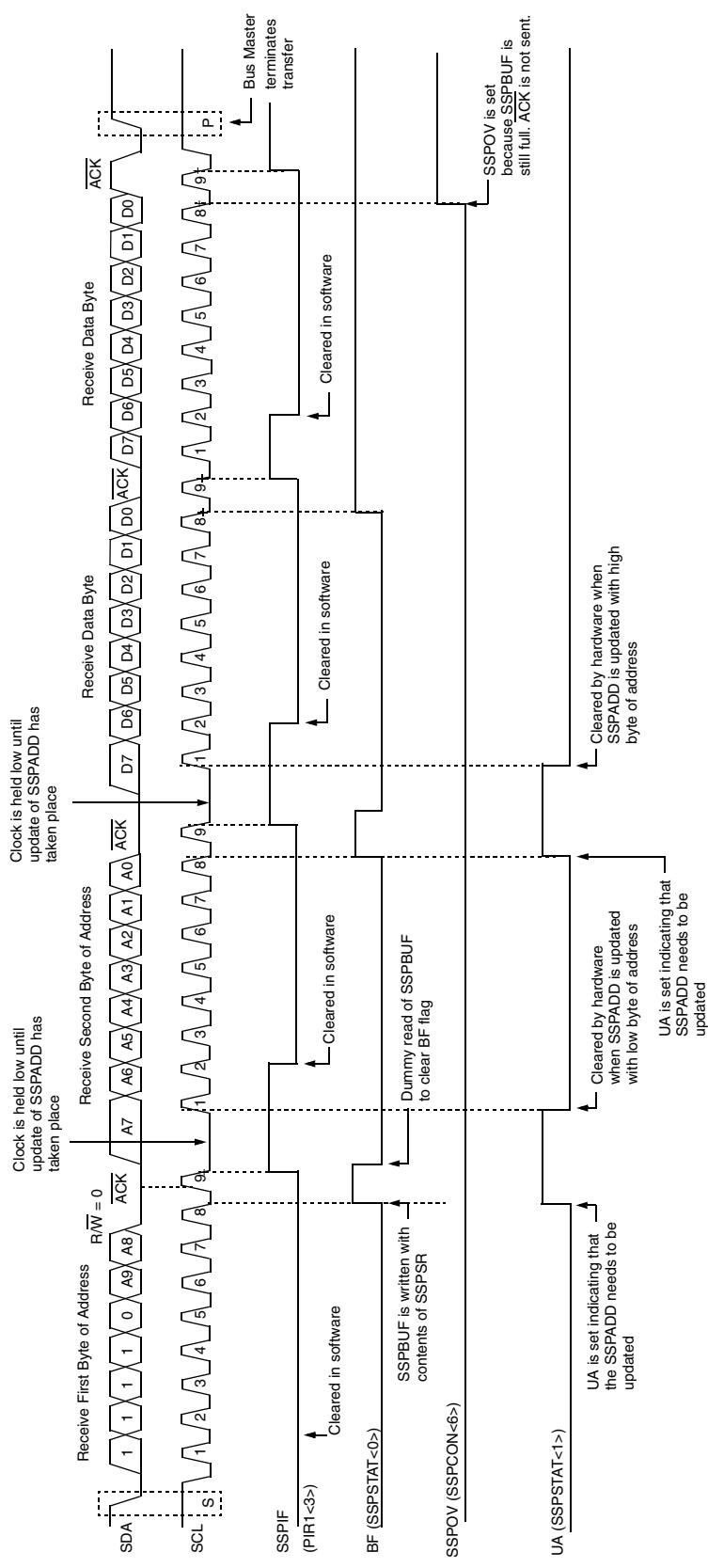


**FIGURE 15-9: I<sup>2</sup>C SLAVE MODE TIMING (TRANSMISSION, 7-BIT ADDRESS)**



# **PIC18FXX2**

**FIGURE 15-10:** I<sup>2</sup>C SLAVE MODE TIMING WITH SEN = 0 (RECEPTION, 10-BIT ADDRESS)



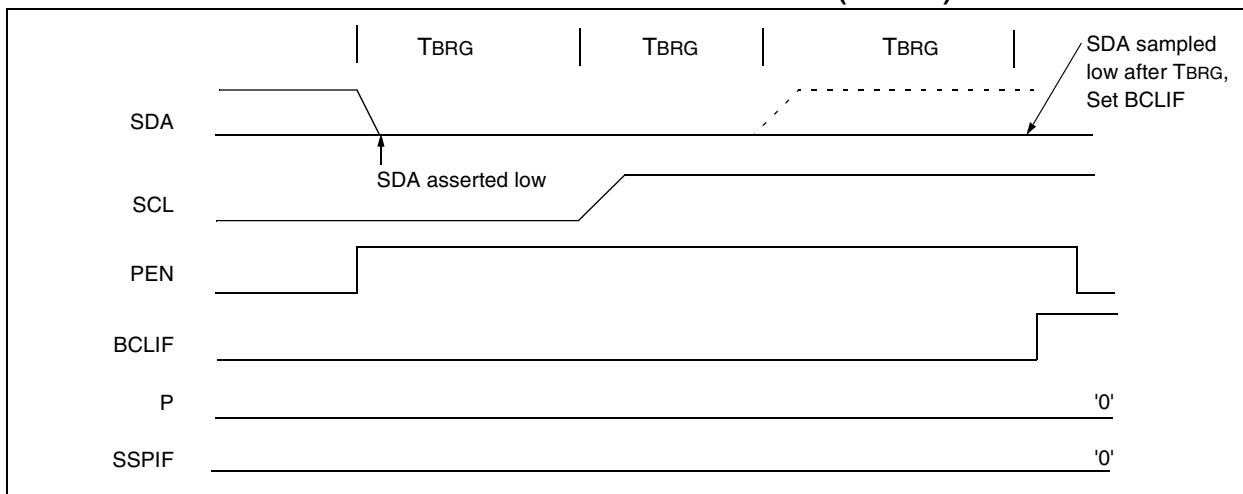
### 15.4.17.3 Bus Collision During a STOP Condition

Bus collision occurs during a STOP condition if:

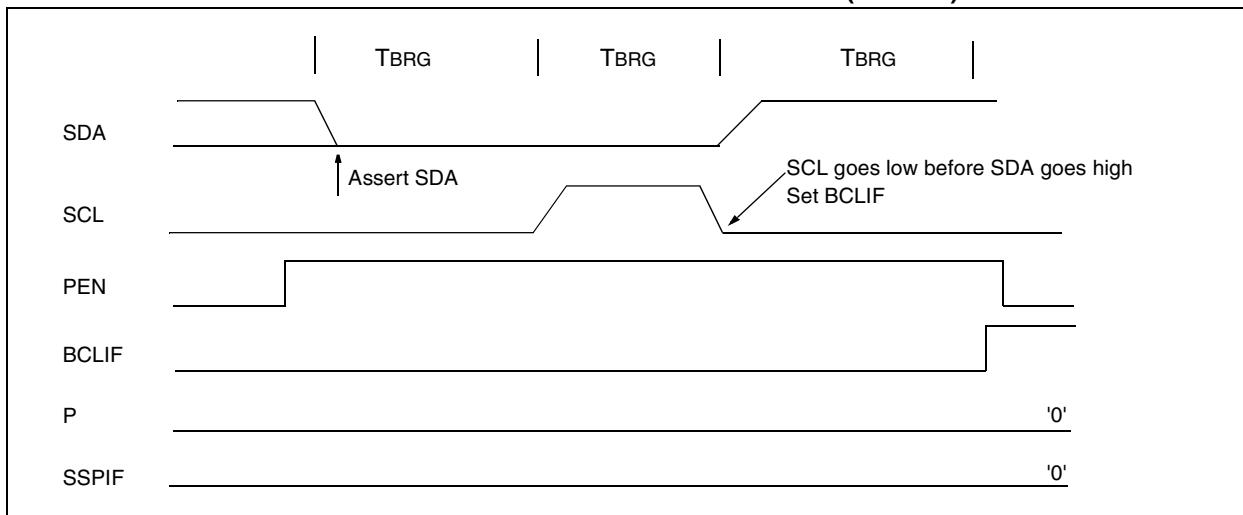
- After the SDA pin has been de-asserted and allowed to float high, SDA is sampled low after the BRG has timed out.
- After the SCL pin is de-asserted, SCL is sampled low before SDA goes high.

The STOP condition begins with SDA asserted low. When SDA is sampled low, the SCL pin is allowed to float. When the pin is sampled high (clock arbitration), the baud rate generator is loaded with SSPADD<6:0> and counts down to 0. After the BRG times out, SDA is sampled. If SDA is sampled low, a bus collision has occurred. This is due to another master attempting to drive a data '0' (Figure 15-31). If the SCL pin is sampled low before SDA is allowed to float high, a bus collision occurs. This is another case of another master attempting to drive a data '0' (Figure 15-32).

**FIGURE 15-31: BUS COLLISION DURING A STOP CONDITION (CASE 1)**



**FIGURE 15-32: BUS COLLISION DURING A STOP CONDITION (CASE 2)**



The analog reference voltage is software selectable to either the device's positive and negative supply voltage (VDD and Vss), or the voltage level on the RA3/AN3/VREF+ pin and RA2/AN2/VREF- pin.

The A/D converter has a unique feature of being able to operate while the device is in SLEEP mode. To operate in SLEEP, the A/D conversion clock must be derived from the A/D's internal RC oscillator.

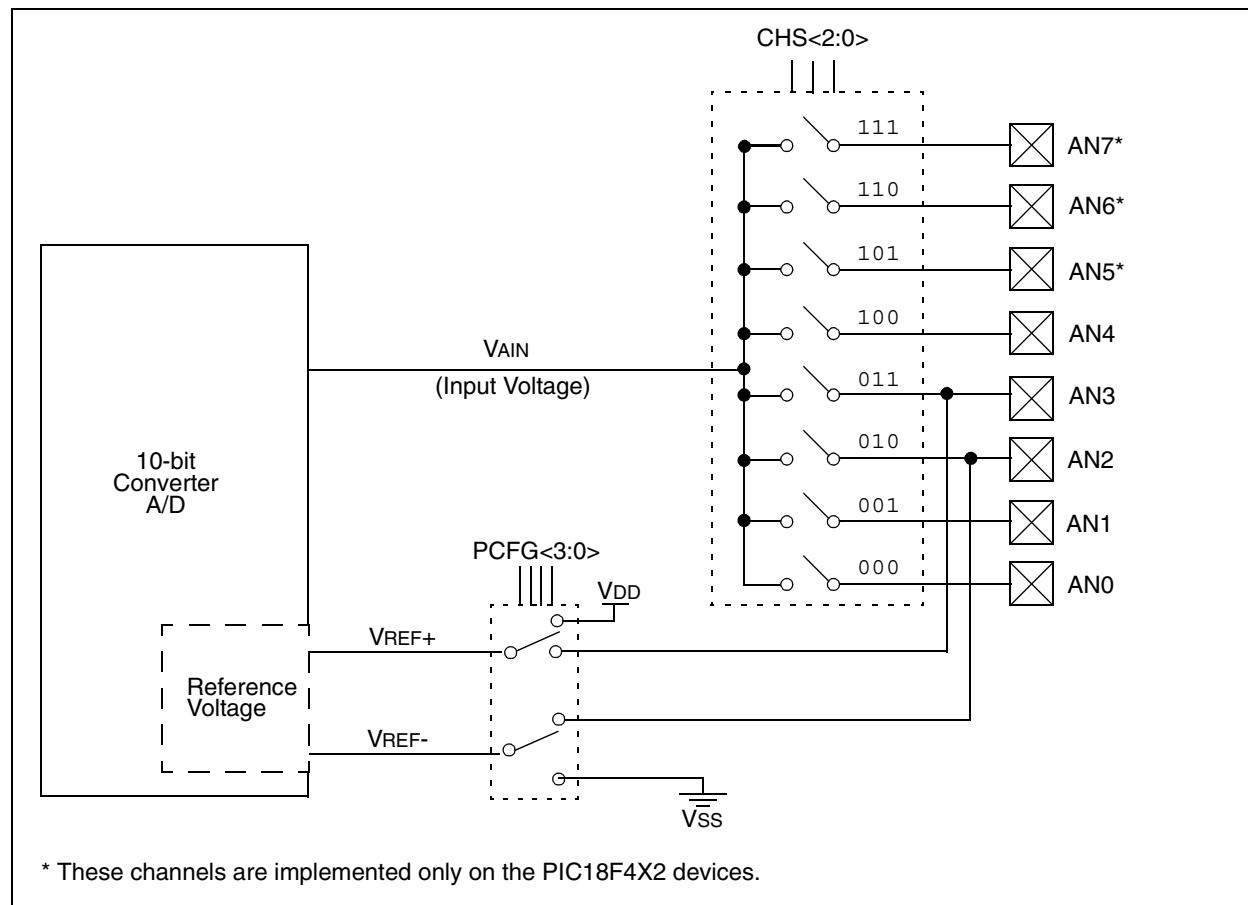
The output of the sample and hold is the input into the converter, which generates the result via successive approximation.

A device RESET forces all registers to their RESET state. This forces the A/D module to be turned off and any conversion is aborted.

Each port pin associated with the A/D converter can be configured as an analog input (RA3 can also be a voltage reference) or as a digital I/O.

The ADRESH and ADRESL registers contain the result of the A/D conversion. When the A/D conversion is complete, the result is loaded into the ADRESH/ADRESL registers, the GO/DONE bit (ADCON0<2>) is cleared, and A/D interrupt flag bit, ADIF is set. The block diagram of the A/D module is shown in Figure 17-1.

**FIGURE 17-1: A/D BLOCK DIAGRAM**



# **PIC18FXX2**

**REGISTER 19-4: CONFIGURATION REGISTER 3 HIGH (CONFIG3H: BYTE ADDRESS 300005h)**

bit 7-1      **Unimplemented:** Read as '0'

bit 0      **CCP2MX**: CCP2 Mux bit

1 = CCP2 input/output is multiplexed with RC1  
0 = CCP2 input/output is multiplexed with RB3

---

**Legend:**

R = Readable bit      P = Programmable bit      U = Unimplemented bit, read as '0'  
 - n = Value when device is unprogrammed      u = Unchanged from programmed state

**REGISTER 19-5: CONFIGURATION REGISTER 4 LOW (CONFIG4L: BYTE ADDRESS 300006h)**

| R/P-1 | U-0 | U-0 | U-0 | U-0   | R/P-1 | U-0 | R/P-1  |
|-------|-----|-----|-----|-------|-------|-----|--------|
| BKBUG | —   | —   | —   | —     | LVP   | —   | STVREN |
| bit 7 |     |     |     | bit 0 |       |     |        |

**bit 7      DEBUG:** Background Debugger Enable bit

**1** = Background Debugger disabled. RB6 and RB7 configured as general purpose I/O pins.  
**0** = Background Debugger enabled. RB6 and RB7 are dedicated to In-Circuit Debug.

bit 6-3      **Unimplemented:** Read as '0'

bit 2      **LVP:** Low Voltage ICSP Enable bit

1 = Low Voltage ICSP enabled  
0 = Low Voltage ICSP disabled

bit 1      **Unimplemented:** Read as '0'

**bit 0 STVBEN:** Stack Full/I Underflow Reset Enable bit

1 – Stack Full/Underflow will cause RESET  
 0 – Stack Full/Underflow will not cause RESET

#### Legend:

R = Readable bit      C = Clearable bit      U = Unimplemented bit, read as '0'  
 - n = Value when device is unprogrammed      U = Unchanged from programmed state

**FIGURE 19-5: EXTERNAL BLOCK TABLE READ (EBTRn) DISALLOWED**

| Register Values | Program Memory                | Configuration Bit Settings |
|-----------------|-------------------------------|----------------------------|
| TBLPTR = 000FFF | 000000h<br>0001FFh<br>000200h | WRTB,EBTRB = 11            |
| PC = 002FFE     | 001FFFh<br>002000h<br>TBLRD * | WRT0,EBTR0 = 10            |
|                 | 003FFFh<br>004000h            | WRT1,EBTR1 = 11            |
|                 | 005FFFh<br>006000h            | WRT2,EBTR2 = 11            |
|                 | 007FFFh                       | WRT3,EBTR3 = 11            |

**Results:** All Table Reads from external blocks to Blockn are disabled whenever EBTRn = '0'. TABLAT register returns a value of "0".

**FIGURE 19-6: EXTERNAL BLOCK TABLE READ (EBTRn) ALLOWED**

| Register Values | Program Memory                | Configuration Bit Settings |
|-----------------|-------------------------------|----------------------------|
| TBLPTR = 000FFF | 000000h<br>0001FFh<br>000200h | WRTB,EBTRB = 11            |
| PC = 001FFE     | 001FFFh<br>002000h<br>TBLRD * | WRT0,EBTR0 = 10            |
|                 | 003FFFh<br>004000h            | WRT1,EBTR1 = 11            |
|                 | 005FFFh<br>006000h            | WRT2,EBTR2 = 11            |
|                 | 007FFFh                       | WRT3,EBTR3 = 11            |

**Results:** Table Reads permitted within Blockn, even when EBTRBn = '0'. TABLAT register returns the value of the data at the location TBLPTR.

| <b>BTG</b>        | <b>Bit Toggle f</b>   |              |                    |      |      |        |                   |              |                    |
|-------------------|---|--------------|--------------------|------|------|--------|-------------------|--------------|--------------------|
| Syntax:           | [ <i>label</i> ] BTG f,b[ <i>a</i> ]  |              |                    |      |      |        |                   |              |                    |
| Operands:         | 0 ≤ f ≤ 255<br>0 ≤ b ≤ 7<br>$a \in [0,1]$   |              |                    |      |      |        |                   |              |                    |
| Operation:        | $(f < b) \rightarrow f < b$   |              |                    |      |      |        |                   |              |                    |
| Status Affected:  | None  |              |                    |      |      |        |                   |              |                    |
| Encoding:         | <table border="1" style="display: inline-table; vertical-align: middle;"> <tr><td>0111</td><td>bbba</td><td>ffff</td><td>ffff</td></tr> </table>  | 0111         | bbba               | ffff | ffff |        |                   |              |                    |
| 0111              | bbba  | ffff         | ffff               |      |      |        |                   |              |                    |
| Description:      | Bit 'b' in data memory location 'f' is inverted. If 'a' is 0, the Access Bank will be selected, overriding the BSR value. If 'a' = 1, then the bank will be selected as per the BSR value (default).                            |              |                    |      |      |        |                   |              |                    |
| Words:            | 1   |              |                    |      |      |        |                   |              |                    |
| Cycles:           | 1   |              |                    |      |      |        |                   |              |                    |
| Q Cycle Activity: | <table border="1" style="width: 100%; text-align: center;"> <tr> <th>Q1</th><th>Q2</th><th>Q3</th><th>Q4</th></tr> <tr> <td>Decode</td><td>Read register 'f'</td><td>Process Data</td><td>Write register 'f'</td></tr> </table> | Q1           | Q2                 | Q3   | Q4   | Decode | Read register 'f' | Process Data | Write register 'f' |
| Q1                | Q2  | Q3           | Q4                 |      |      |        |                   |              |                    |
| Decode            | Read register 'f'   | Process Data | Write register 'f' |      |      |        |                   |              |                    |

Example: BTG PORTC, 4, 0

Before Instruction:

PORTC = 0111 0101 [0x75]

After Instruction:

PORTC = 0110 0101 [0x65]

| <b>BOV</b>        | <b>Branch if Overflow</b>  |              |              |      |      |        |                  |              |             |              |              |              |              |
|-------------------|--|--------------|--------------|------|------|--------|------------------|--------------|-------------|--------------|--------------|--------------|--------------|
| Syntax:           | [ <i>label</i> ] BOV n   |              |              |      |      |        |                  |              |             |              |              |              |              |
| Operands:         | -128 ≤ n ≤ 127   |              |              |      |      |        |                  |              |             |              |              |              |              |
| Operation:        | if overflow bit is '1'<br>$(PC) + 2 + 2n \rightarrow PC$   |              |              |      |      |        |                  |              |             |              |              |              |              |
| Status Affected:  | None   |              |              |      |      |        |                  |              |             |              |              |              |              |
| Encoding:         | <table border="1" style="display: inline-table; vertical-align: middle;"> <tr><td>1110</td><td>0100</td><td>nnnn</td><td>nnnn</td></tr> </table>   | 1110         | 0100         | nnnn | nnnn |        |                  |              |             |              |              |              |              |
| 1110              | 0100   | nnnn         | nnnn         |      |      |        |                  |              |             |              |              |              |              |
| Description:      | If the Overflow bit is '1', then the program will branch.<br>The 2's complement number '2n' is added to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be $PC+2+2n$ . This instruction is then a two-cycle instruction.  |              |              |      |      |        |                  |              |             |              |              |              |              |
| Words:            | 1  |              |              |      |      |        |                  |              |             |              |              |              |              |
| Cycles:           | 1(2)   |              |              |      |      |        |                  |              |             |              |              |              |              |
| Q Cycle Activity: | <table border="1" style="width: 100%; text-align: center;"> <tr> <th>Q1</th><th>Q2</th><th>Q3</th><th>Q4</th></tr> <tr> <td>Decode</td><td>Read literal 'n'</td><td>Process Data</td><td>Write to PC</td></tr> <tr> <td>No operation</td><td>No operation</td><td>No operation</td><td>No operation</td></tr> </table> | Q1           | Q2           | Q3   | Q4   | Decode | Read literal 'n' | Process Data | Write to PC | No operation | No operation | No operation | No operation |
| Q1                | Q2   | Q3           | Q4           |      |      |        |                  |              |             |              |              |              |              |
| Decode            | Read literal 'n'   | Process Data | Write to PC  |      |      |        |                  |              |             |              |              |              |              |
| No operation      | No operation   | No operation | No operation |      |      |        |                  |              |             |              |              |              |              |

If No Jump:

| Q1     | Q2               | Q3           | Q4           |
|--------|------------------|--------------|--------------|
| Decode | Read literal 'n' | Process Data | No operation |

Example: HERE BOV Jump

Before Instruction

PC = address (HERE)

After Instruction

If Overflow = 1;  
 PC = address (Jump)  
 If Overflow = 0;  
 PC = address (HERE+2)

## 21.0 DEVELOPMENT SUPPORT

The PICmicro® microcontrollers are supported with a full range of hardware and software development tools:

- Integrated Development Environment
  - MPLAB® IDE Software
- Assemblers/Compilers/Linkers
  - MPASM™ Assembler
  - MPLAB C17 and MPLAB C18 C Compilers
  - MPLINK™ Object Linker/  
MPLIB™ Object Librarian
- Simulators
  - MPLAB SIM Software Simulator
- Emulators
  - MPLAB ICE 2000 In-Circuit Emulator
  - ICEPIC™ In-Circuit Emulator
- In-Circuit Debugger
  - MPLAB ICD
- Device Programmers
  - PRO MATE® II Universal Device Programmer
  - PICSTART® Plus Entry-Level Development  
Programmer
- Low Cost Demonstration Boards
  - PICDEM™ 1 Demonstration Board
  - PICDEM 2 Demonstration Board
  - PICDEM 3 Demonstration Board
  - PICDEM 17 Demonstration Board
  - KEELoQ® Demonstration Board

### 21.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8-bit microcontroller market. The MPLAB IDE is a Windows® based application that contains:

- An interface to debugging tools
  - simulator
  - programmer (sold separately)
  - emulator (sold separately)
  - in-circuit debugger (sold separately)
- A full-featured editor
- A project manager
- Customizable toolbar and key mapping
- A status bar
- On-line help

The MPLAB IDE allows you to:

- Edit your source files (either assembly or 'C')
- One touch assemble (or compile) and download to PICmicro emulator and simulator tools (automatically updates all project information)
- Debug using:
  - source files
  - absolute listing file
  - machine code

The ability to use MPLAB IDE with multiple debugging tools allows users to easily switch from the cost-effective simulator to a full-featured emulator with minimal retraining.

### 21.2 MPASM Assembler

The MPASM assembler is a full-featured universal macro assembler for all PICmicro MCU's.

The MPASM assembler has a command line interface and a Windows shell. It can be used as a stand-alone application on a Windows 3.x or greater system, or it can be used through MPLAB IDE. The MPASM assembler generates relocatable object files for the MPLINK object linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, an absolute LST file that contains source lines and generated machine code, and a COD file for debugging.

The MPASM assembler features include:

- Integration into MPLAB IDE projects.
- User-defined macros to streamline assembly code.
- Conditional assembly for multi-purpose source files.
- Directives that allow complete control over the assembly process.

### 21.3 MPLAB C17 and MPLAB C18 C Compilers

The MPLAB C17 and MPLAB C18 Code Development Systems are complete ANSI 'C' compilers for Microchip's PIC17CXXX and PIC18CXXX family of microcontrollers, respectively. These compilers provide powerful integration capabilities and ease of use not found with other compilers.

For easier source level debugging, the compilers provide symbol information that is compatible with the MPLAB IDE memory display.

# PIC18FXX2

FIGURE 22-1: PIC18FXX2 VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)

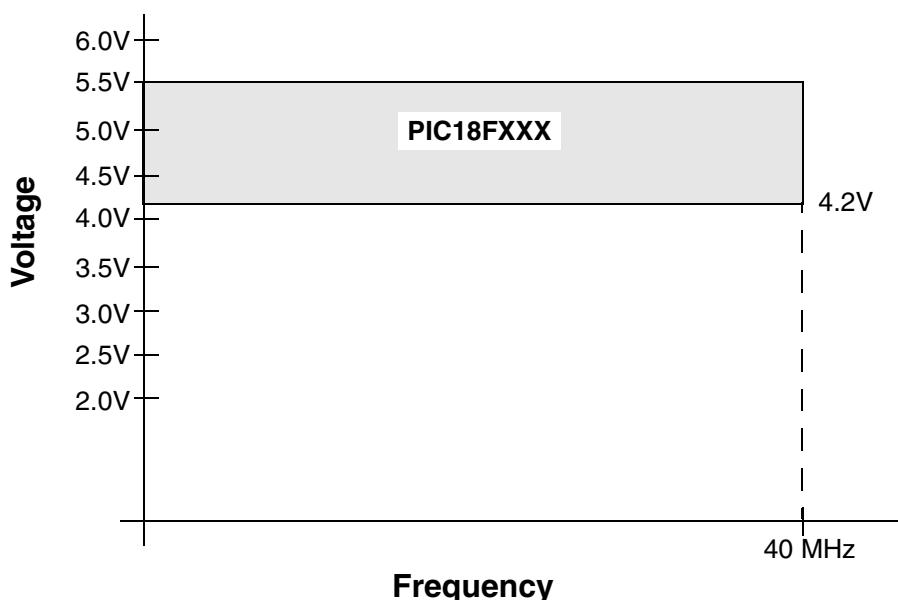
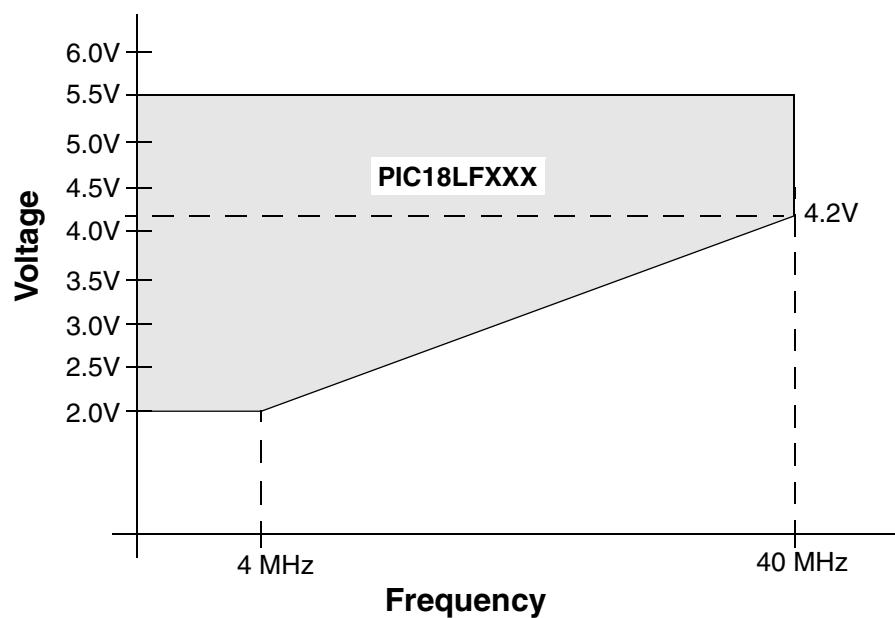
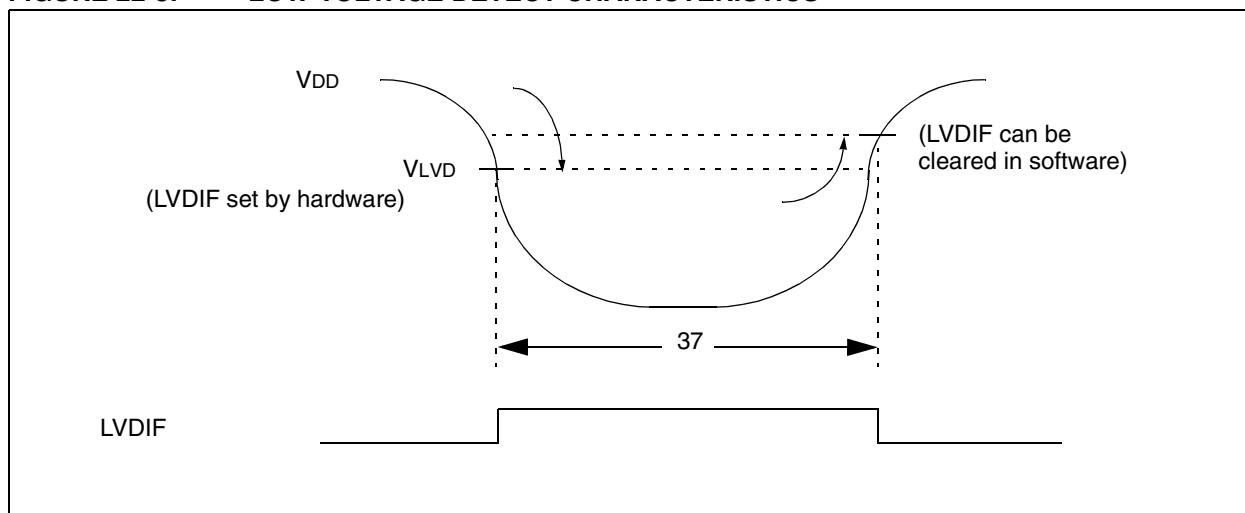


FIGURE 22-2: PIC18LFXX2 VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)



$$F_{MAX} = (16.36 \text{ MHz/V}) (V_{DDAPPMIN} - 2.0V) + 4 \text{ MHz}$$

**Note:**  $V_{DDAPPMIN}$  is the minimum voltage of the PICmicro® device in the application.

**FIGURE 22-3: LOW VOLTAGE DETECT CHARACTERISTICS****TABLE 22-1: LOW VOLTAGE DETECT CHARACTERISTICS**

|           |        |   | Standard Operating Conditions (unless otherwise stated)<br>Operating temperature $-40^{\circ}\text{C} \leq \text{TA} \leq +85^{\circ}\text{C}$ for industrial<br>$-40^{\circ}\text{C} \leq \text{TA} \leq +125^{\circ}\text{C}$ for extended |      |      |       |            |                                    |
|-----------|--------|---|--|------|------|-------|------------|------------------------------------|
| Param No. | Symbol | Characteristic                            | Min  | Typ  | Max  | Units | Conditions |                                    |
| D420      | VLVD   | LVD Voltage on VDD transition high to low | LVV = 0001   | 1.98 | 2.06 | 2.14  | V          | $\text{T} \geq 25^{\circ}\text{C}$ |
|           |        |   | LVV = 0010   | 2.18 | 2.27 | 2.36  | V          | $\text{T} \geq 25^{\circ}\text{C}$ |
|           |        |   | LVV = 0011   | 2.37 | 2.47 | 2.57  | V          | $\text{T} \geq 25^{\circ}\text{C}$ |
|           |        |   | LVV = 0100   | 2.48 | 2.58 | 2.68  | V          |                                    |
|           |        |   | LVV = 0101   | 2.67 | 2.78 | 2.89  | V          |                                    |
|           |        |   | LVV = 0110   | 2.77 | 2.89 | 3.01  | V          |                                    |
|           |        |   | LVV = 0111   | 2.98 | 3.1  | 3.22  | V          |                                    |
|           |        |   | LVV = 1000   | 3.27 | 3.41 | 3.55  | V          |                                    |
|           |        |   | LVV = 1001   | 3.47 | 3.61 | 3.75  | V          |                                    |
|           |        |   | LVV = 1010   | 3.57 | 3.72 | 3.87  | V          |                                    |
|           |        |   | LVV = 1011   | 3.76 | 3.92 | 4.08  | V          |                                    |
|           |        |   | LVV = 1100   | 3.96 | 4.13 | 4.3   | V          |                                    |
|           |        |   | LVV = 1101   | 4.16 | 4.33 | 4.5   | V          |                                    |
|           |        |   | LVV = 1110   | 4.45 | 4.64 | 4.83  | V          |                                    |

# PIC18FXX2

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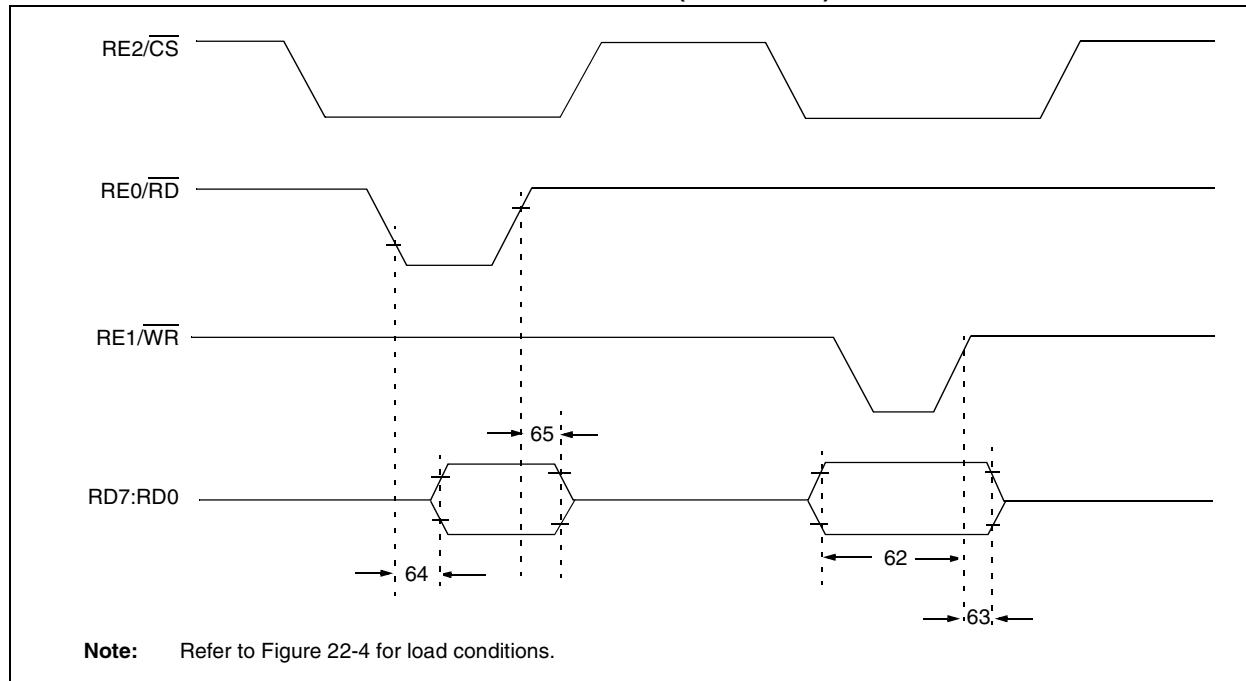
**TABLE 22-2: MEMORY PROGRAMMING REQUIREMENTS**

| DC Characteristics |       |  | Standard Operating Conditions (unless otherwise stated) |      |       |       |   |
|--------------------|-------|--|---|------|-------|-------|---|
| Param No.          | Sym   | Characteristic   | Min   | Typ† | Max   | Units | Conditions  |
| D110               | VPP   | <b>Internal Program Memory Programming Specifications</b>        | 9.00  | —    | 13.25 | V     |   |
| D113               | IDDP  | Voltage on MCLR/VPP pin  | —   | —    | 10    | mA    |   |
|                    |       | Supply Current during Programming                                |   |      |       |       |   |
| D120               | ED    | <b>Data EEPROM Memory</b>  | 100K  | 1M   | —     | E/W   | -40°C to +85°C  |
| D121               | VDRW  | Cell Endurance<br>VDD for Read/Write                             | VMIN  | —    | 5.5   | V     | Using EECON to read/write<br>VMIN = Minimum operating voltage |
| D122               | TDEW  | Erase/Write Cycle Time   | —   | 4    | —     | ms    |   |
| D123               | TRETD | Characteristic Retention   | 40  | —    | —     | Year  | Provided no other specifications are violated                 |
| D124               | TREF  | Number of Total Erase/Write Cycles before Refresh <sup>(1)</sup> | 1M  | 10M  | —     | E/W   | -40°C to +85°C  |
| D130               | EP    | <b>Program FLASH Memory</b>                                      | 10K   | 100K | —     | E/W   | -40°C to +85°C  |
| D131               | VPR   | Cell Endurance<br>VDD for Read                                   | VMIN  | —    | 5.5   | V     | VMIN = Minimum operating voltage                              |
| D132               | VIE   | VDD for Block Erase  | 4.5   | —    | 5.5   | V     | Using ICSP port   |
| D132A              | VIW   | VDD for Externally Timed Erase or Write                          | 4.5   | —    | 5.5   | V     | Using ICSP port   |
| D132B              | VPEW  | VDD for Self-timed Write   | VMIN  | —    | 5.5   | V     | VMIN = Minimum operating voltage                              |
| D133               | TIE   | ICSP Block Erase Cycle Time                                      | —   | 4    | —     | ms    | VDD ≥ 4.5V  |
| D133A              | TIW   | ICSP Erase or Write Cycle Time (externally timed)                | 1   | —    | —     | ms    | VDD ≥ 4.5V  |
| D133A              | TIW   | Self-timed Write Cycle Time                                      | —   | 2    | —     | ms    |   |
| D134               | TRETD | Characteristic Retention   | 40  | —    | —     | Year  | Provided no other specifications are violated                 |

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** Refer to Section 6.8 for a more detailed discussion on data EEPROM endurance.

**FIGURE 22-11: PARALLEL SLAVE PORT TIMING (PIC18F4X2)**

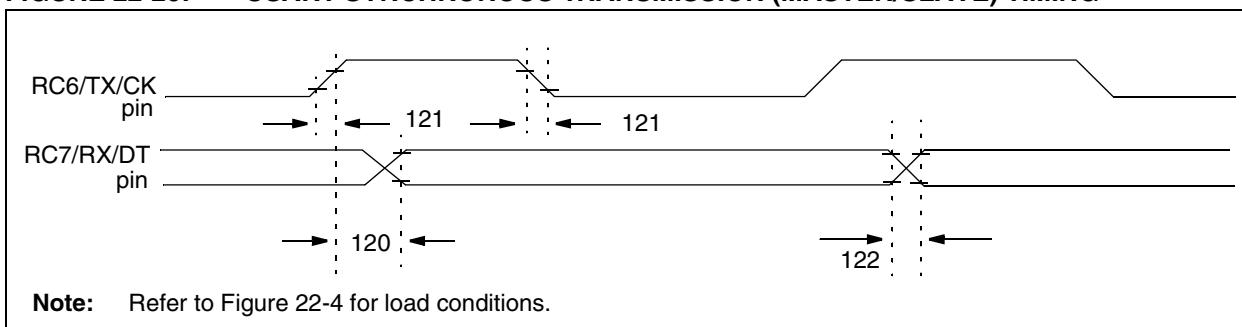


**TABLE 22-10: PARALLEL SLAVE PORT REQUIREMENTS (PIC18F4X2)**

| Param. No. | Symbol   | Characteristic  | Min        | Max      | Units    | Conditions           |
|------------|----------|---|------------|----------|----------|----------------------|
| 62         | TdtV2wrH | Data in valid before $\overline{WR} \uparrow$ or $\overline{CS} \uparrow$ (setup time)              | 20<br>25   | —        | ns<br>ns | Extended Temp. Range |
| 63         | TwrH2dtl | $\overline{WR} \uparrow$ or $\overline{CS} \uparrow$ to data-in invalid (hold time)                 | PIC18FXXX  | 20       | —        | ns                   |
|            |          |   | PIC18LFXXX | 35       | —        | ns<br>$VDD = 2V$     |
| 64         | TrdL2dtV | $\overline{RD} \downarrow$ and $\overline{CS} \downarrow$ to data-out valid                         | —<br>—     | 80<br>90 | ns<br>ns | Extended Temp. Range |
| 65         | TrdH2dtl | $\overline{RD} \uparrow$ or $\overline{CS} \downarrow$ to data-out invalid                          | 10         | 30       | ns       |                      |
| 66         | TibflNH  | Inhibit of the IBF flag bit being cleared from $\overline{WR} \uparrow$ or $\overline{CS} \uparrow$ | —          | 3 TCY    |          |                      |

# PIC18FXX2

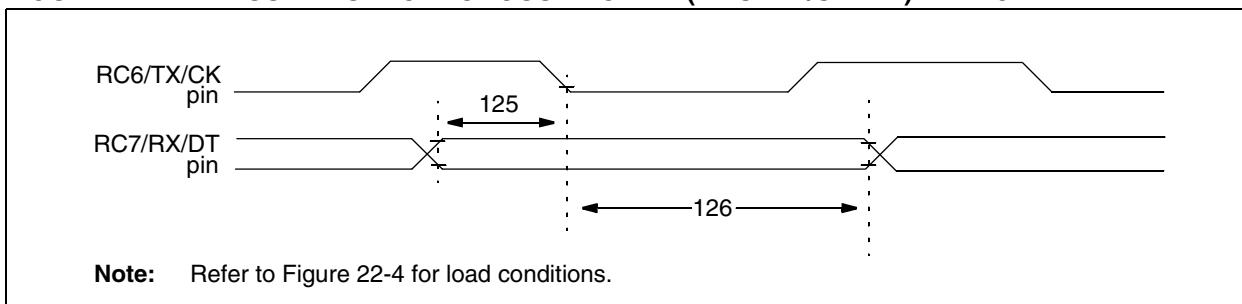
**FIGURE 22-20: USART SYNCHRONOUS TRANSMISSION (MASTER/SLAVE) TIMING**



**TABLE 22-19: USART SYNCHRONOUS TRANSMISSION REQUIREMENTS**

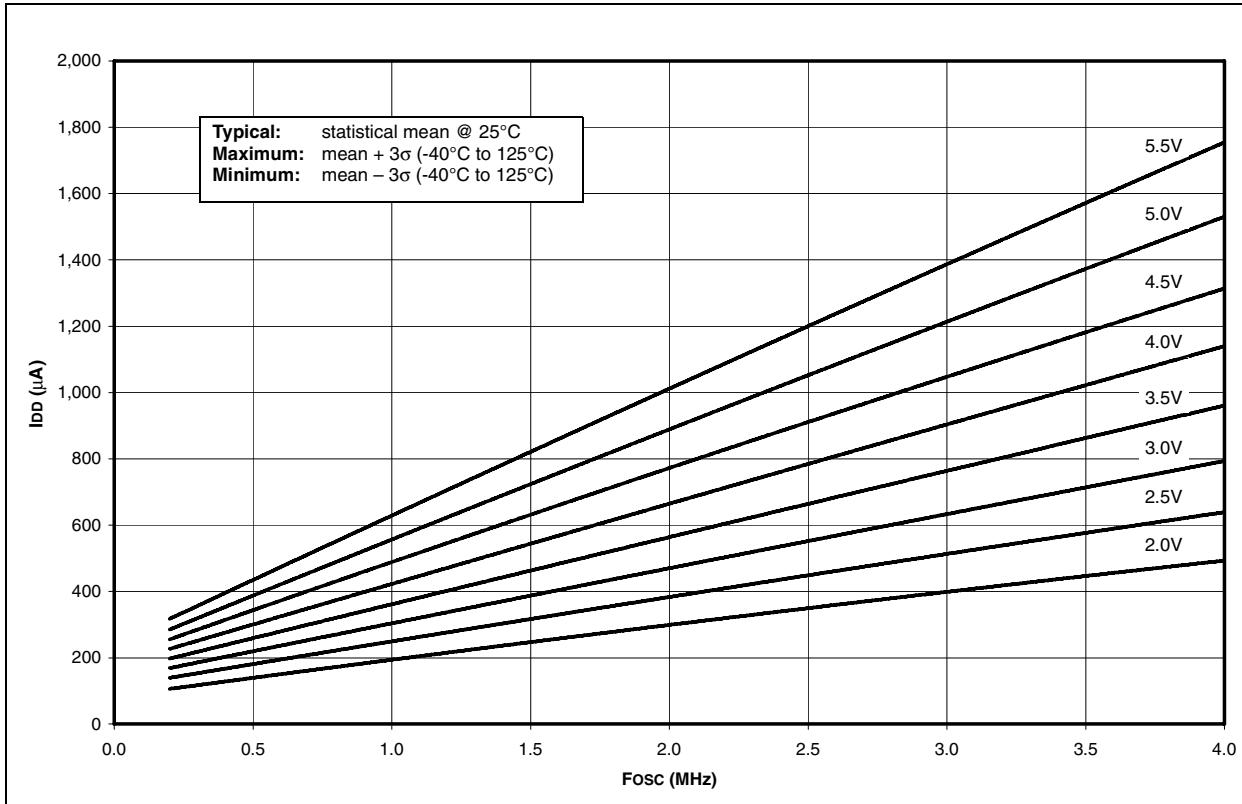
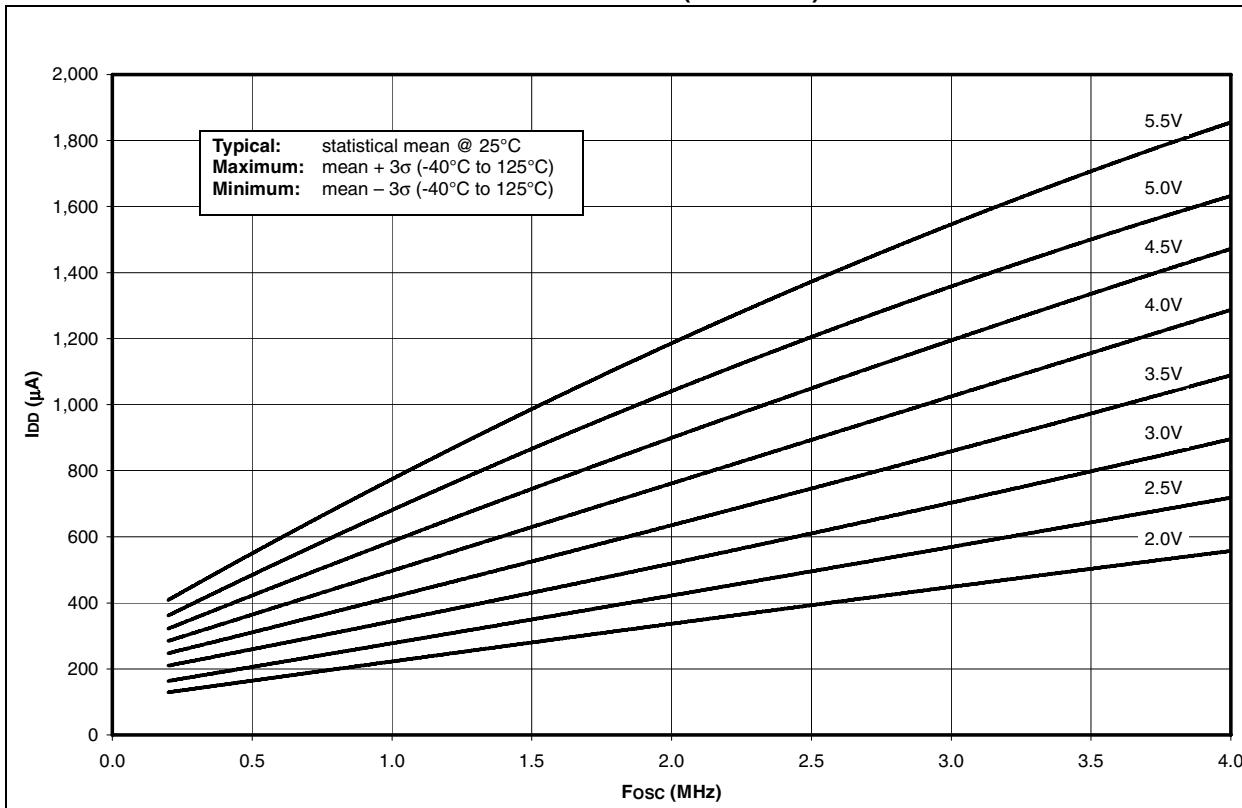
| Param. No. | Symbol   | Characteristic  | Min        | Max | Units | Conditions     |
|------------|----------|---|------------|-----|-------|----------------|
| 120        | TckH2dtV | <b>SYNC XMIT (MASTER &amp; SLAVE)</b><br>Clock high to data out valid | PIC18FXXX  | —   | 50    | ns             |
|            |          |   | PIC18LFXXX | —   | 150   | ns<br>VDD = 2V |
| 121        | Tckr     | Clock out rise time and fall time (Master mode)                       | PIC18FXXX  | —   | 25    | ns             |
|            |          |   | PIC18LFXXX | —   | 60    | ns<br>VDD = 2V |
| 122        | Tdtr     | Data out rise time and fall time                                      | PIC18FXXX  | —   | 25    | ns             |
|            |          |   | PIC18LFXXX | —   | 60    | ns<br>VDD = 2V |

**FIGURE 22-21: USART SYNCHRONOUS RECEIVE (MASTER/SLAVE) TIMING**



**TABLE 22-20: USART SYNCHRONOUS RECEIVE REQUIREMENTS**

| Param. No. | Symbol   | Characteristic   | Min        | Max | Units | Conditions     |
|------------|----------|--|------------|-----|-------|----------------|
| 125        | TdtV2clk | <b>SYNC RCV (MASTER &amp; SLAVE)</b><br>Data hold before CK ↓ (DT hold time) | 10         | —   | ns    |                |
| 126        | TckL2dtl | Data hold after CK ↓ (DT hold time)  | PIC18FXXX  | 15  | —     | ns             |
|            |          |  | PIC18LFXXX | 20  | —     | ns<br>VDD = 2V |

**FIGURE 23-5: TYPICAL IDD vs. Fosc OVER VDD (XT MODE)****FIGURE 23-6: MAXIMUM IDD vs. Fosc OVER VDD (XT MODE)**

## P

|   |         |
|---|---------|
| Packaging .....                                   | 305     |
| Details .....                                     | 307     |
| Marking Information .....                         | 305     |
| Parallel Slave Port                               |         |
| PORTD .....                                       | 100     |
| Parallel Slave Port (PSP)                         | 95, 100 |
| Associated Registers .....                        | 101     |
| RE0/RD/AN5 Pin .....                              | 99, 100 |
| RE1/WR/AN6 Pin .....                              | 99, 100 |
| RE2/CS/AN7 Pin .....                              | 99, 100 |
| Select (PSPMODE Bit) .....                        | 95, 100 |
| PIC18F2X2 Pin Functions                           |         |
| MCLR/VPP .....                                    | 10      |
| OSC1/CLKI .....                                   | 10      |
| OSC2/CLKO/RA6 .....                               | 10      |
| RA0/AN0 .....                                     | 10      |
| RA1/AN1 .....                                     | 10      |
| RA2/AN2/VREF- .....                               | 10      |
| RA3/AN3/VREF+ .....                               | 10      |
| RA4/T0CKI .....                                   | 10      |
| RA5/AN4/SS/LVDIN .....                            | 10      |
| RB0/INT0 .....                                    | 11      |
| RB1/INT1 .....                                    | 11      |
| RB2/INT2 .....                                    | 11      |
| RB3/CCP2 .....                                    | 11      |
| RB4 .....   | 11      |
| RB5/PGM .....                                     | 11      |
| RB6/PGC .....                                     | 11      |
| RB7/PGD .....                                     | 11      |
| RC0/T1OSO/T1CKI .....                             | 12      |
| RC1/T1OSI/CCP2 .....                              | 12      |
| RC2/CCP1 .....                                    | 12      |
| RC3/SCK/SCL .....                                 | 12      |
| RC4/SDI/SDA .....                                 | 12      |
| RC5/SDO .....                                     | 12      |
| RC6/TX/CK .....                                   | 12      |
| RC7/RX/DT .....                                   | 12      |
| VDD .....   | 12      |
| VSS .....   | 12      |
| PIC18F4X2 Pin Functions                           |         |
| MCLR/VPP .....                                    | 13      |
| OSC1/CLKI .....                                   | 13      |
| OSC2/CLKO .....                                   | 13      |
| RA0/AN0 .....                                     | 13      |
| RA1/AN1 .....                                     | 13      |
| RA2/AN2/VREF- .....                               | 13      |
| RA3/AN3/VREF+ .....                               | 13      |
| RA4/T0CKI .....                                   | 13      |
| RA5/AN4/SS/LVDIN .....                            | 13      |
| RB0/INT .....                                     | 14      |
| RB1 .....   | 14      |
| RB2 .....   | 14      |
| RB3 .....   | 14      |
| RB4 .....   | 14      |
| RB5/PGM .....                                     | 14      |
| RB6/PGC .....                                     | 14      |
| RB7/PGD .....                                     | 14      |
| RC0/T1OSO/T1CKI .....                             | 15      |
| RC1/T1OSI/CCP2 .....                              | 15      |
| RC2/CCP1 .....                                    | 15      |
| RC3/SCK/SCL .....                                 | 15      |
| RC4/SDI/SDA .....                                 | 15      |
| RC5/SDO .....                                     | 15      |
| RC6/TX/CK .....                                   | 15      |
| RC7/RX/DT .....                                   | 15      |
| RD7/RX/DT .....                                   | 15      |
| RD0/PSP0 .....                                    | 16      |
| RD1/PSP1 .....                                    | 16      |
| RD2/PSP2 .....                                    | 16      |
| RD3/PSP3 .....                                    | 16      |
| RD4/PSP4 .....                                    | 16      |
| RD5/PSP5 .....                                    | 16      |
| RD6/PSP6 .....                                    | 16      |
| RD7/PSP7 .....                                    | 16      |
| RE0/RD/AN5 .....                                  | 16      |
| RE1/WR/AN6 .....                                  | 16      |
| RE2/CS/AN7 .....                                  | 16      |
| VDD .....   | 16      |
| VSS .....   | 16      |
| <b>PIC18FXX2 Voltage-Frequency Graph</b>          |         |
| (Industrial) .....                                | 260     |
| <b>PIC18LFXX2 Voltage-Frequency Graph</b>         |         |
| (Industrial) .....                                | 260     |
| <b>PICDEM 1 Low Cost PICmicro</b>                 |         |
| Demonstration Board .....                         | 255     |
| <b>PICDEM 17 Demonstration Board</b>              | 256     |
| <b>PICDEM 2 Low Cost PIC16CXX</b>                 |         |
| Demonstration Board .....                         | 255     |
| <b>PICDEM 3 Low Cost PIC16CXXX</b>                |         |
| Demonstration Board .....                         | 256     |
| <b>PICSTART Plus Entry Level Development</b>      |         |
| Programmer .....                                  | 255     |
| <b>PIE Registers</b>                              | 80-81   |
| <b>Pinout I/O Descriptions</b>                    |         |
| PIC18F2X2 .....                                   | 10      |
| <b>PIR Registers</b>                              | 78-79   |
| <b>PLL Lock Time-out</b>                          | 26      |
| <b>Pointer, FSR</b>                               | 50      |
| <b>POP</b>  | 240     |
| <b>POR. See Power-on Reset</b>                    |         |
| <b>PORTA</b>                                      |         |
| Associated Registers .....                        | 89      |
| LATA Register .....                               | 87      |
| PORTA Register .....                              | 87      |
| TRISA Register .....                              | 87      |
| <b>PORTB</b>                                      |         |
| Associated Registers .....                        | 92      |
| LATB Register .....                               | 90      |
| PORTB Register .....                              | 90      |
| RB0/INT Pin, External .....                       | 85      |
| RB7:RB4 Interrupt-on-Change Flag (RBIF Bit) ..... | 90      |
| TRISB Register .....                              | 90      |
| <b>PORTC</b>                                      |         |
| Associated Registers .....                        | 94      |
| LATC Register .....                               | 93      |
| PORTC Register .....                              | 93      |
| RC3/SCK/SCL Pin .....                             | 139     |
| RC7/RX/DT Pin .....                               | 168     |
| TRISC Register .....                              | 93, 165 |
| <b>PORTD</b>                                      |         |
| Associated Registers .....                        | 96      |
| LATD Register .....                               | 95      |
| Parallel Slave Port (PSP) Function .....          | 95      |
| PORTD Register .....                              | 95      |
| TRISD Register .....                              | 95      |

|   |          |
|---|----------|
| Example SPI Master Mode (CKE = 0) .....   | 278      |
| Example SPI Master Mode (CKE = 1) .....   | 279      |
| Example SPI Slave Mode (CKE = 0) .....  | 280      |
| Example SPI Slave Mode (CKE = 1) .....  | 281      |
| External Clock (All Modes except PLL) .....   | 271      |
| First START Bit Timing .....  | 153      |
| I <sup>2</sup> C Bus Data .....   | 282      |
| I <sup>2</sup> C Bus START/STOP Bits .....  | 282      |
| I <sup>2</sup> C Master Mode (Reception, 7-bit Address) .....   | 157      |
| I <sup>2</sup> C Master Mode (Transmission,<br>7 or 10-bit Address) .....                                     | 156      |
| I <sup>2</sup> C Slave Mode Timing (10-bit Reception,<br>SEN = 0) .....                                       | 142      |
| I <sup>2</sup> C Slave Mode Timing (10-bit Transmission) .....  | 143      |
| I <sup>2</sup> C Slave Mode Timing (7-bit Reception,<br>SEN = 0) .....  | 140      |
| I <sup>2</sup> C Slave Mode Timing (7-bit Reception,<br>SEN = 1) .....  | 146, 147 |
| I <sup>2</sup> C Slave Mode Timing (7-bit Transmission) .....   | 141      |
| Low Voltage Detect .....  | 192      |
| Master SSP I <sup>2</sup> C Bus Data .....  | 284      |
| Master SSP I <sup>2</sup> C Bus START/STOP Bits .....   | 284      |
| Parallel Slave Port (PIC18F4X2) .....   | 277      |
| Parallel Slave Port (Read) .....  | 101      |
| Parallel Slave Port (Write) .....   | 100      |
| PWM Output .....  | 122      |
| Repeat START Condition .....  | 154      |
| RESET, Watchdog Timer (WDT),<br>Oscillator Start-up Timer (OST) and<br>Power-up Timer (PWRT) .....            | 273      |
| Slave Synchronization .....   | 131      |
| Slaver Mode General Call Address Sequence<br>(7 or 10-bit Address Mode) .....                                 | 148      |
| Slow Rise Time (MCLR Tied to VDD) .....   | 33       |
| SPI Mode (Master Mode) .....  | 130      |
| SPI Mode (Slave Mode with CKE = 0) .....  | 132      |
| SPI Mode (Slave Mode with CKE = 1) .....  | 132      |
| Stop Condition Receive or Transmit Mode .....   | 158      |
| Time-out Sequence on POR w/PLL Enabled<br>(MCLR Tied to VDD) .....  | 33       |
| Time-out Sequence on Power-up<br>(MCLR Not Tied to VDD)<br>Case 1 .....                                       | 32       |
| Time-out Sequence on Power-up<br>(MCLR Tied to VDD) .....   | 32       |
| Timer0 and Timer1 External Clock .....  | 275      |
| Timing for Transition Between Timer1 and<br>OSC1 (HS with PLL) .....  | 23       |
| Transition Between Timer1 and OSC1<br>(HS, XT, LP) .....  | 22       |
| Transition Between Timer1 and OSC1<br>(RC, EC) .....  | 23       |
| Transition from OSC1 to Timer1 Oscillator .....   | 22       |
| USART Asynchronous Master Transmission .....  | 173      |
| USART Asynchronous Master Transmission<br>(Back to Back) .....  | 173      |
| USART Asynchronous Reception .....  | 175      |
| USART Synchronous Receive (Master/Slave) .....  | 286      |
| USART Synchronous Reception<br>(Master Mode, SREN) .....  | 178      |
| USART Synchronous Transmission .....  | 177      |
| USART Synchronous Transmission<br>(Master/Slave) .....  | 286      |
|   |          |
| USART Synchronous Transmission<br>(Through TXEN) .....  | 177      |
| Wake-up from SLEEP via Interrupt .....  | 206      |
|   |          |
| Timing Diagrams Requirements  |          |
| Master SSP I <sup>2</sup> C Bus START/STOP Bits .....   | 284      |
|   |          |
| Timing Requirements   |          |
| A/D Conversion .....  | 288      |
| Capture/Compare/PWM (CCP1 and CCP2) .....   | 276      |
| CLKO and I/O .....  | 273      |
| Example SPI Mode (Master Mode, CKE = 0) .....   | 278      |
| Example SPI Mode (Master Mode, CKE = 1) .....   | 279      |
| Example SPI Mode (Slave Mode, CKE = 0) .....  | 280      |
| Example SPI Slave Mode (CKE = 1) .....  | 281      |
| External Clock .....  | 271      |
| I <sup>2</sup> C Bus Data (Slave Mode) .....  | 283      |
| Master SSP I <sup>2</sup> C Bus Data .....  | 285      |
| Parallel Slave Port (PIC18F4X2) .....   | 277      |
| RESET, Watchdog Timer, Oscillator Start-up<br>Timer, Power-up Timer and<br>Brown-out Reset Requirements ..... | 274      |
| Timer0 and Timer1 External Clock .....  | 275      |
| USART Synchronous Receive .....   | 286      |
| USART Synchronous Transmission .....  | 286      |
|   |          |
| Timing Specifications   |          |
| PLL Clock .....   | 272      |
| TRISE Register  |          |
| PSPMODE Bit .....   | 95, 100  |
| TSTFSZ  |          |
| Two-Word Instructions   |          |
| Example Cases .....   | 41       |
| TXSTA Register  |          |
| BRGH Bit .....  | 168      |
|   |          |
| <b>U</b>  |          |
| Universal Synchronous Asynchronous<br>Receiver Transmitter. See USART   |          |
| USART   |          |
| Asynchronous Mode .....   | 172      |
| Associated Registers, Receive .....   | 175      |
| Associated Registers, Transmit .....  | 173      |
| Receiver .....  | 174      |
| Transmitter .....   | 172      |
| Baud Rate Generator (BRG) .....   | 168      |
| Associated Registers .....  | 168      |
| Baud Rate Error, Calculating .....  | 168      |
| Baud Rate Formula .....   | 168      |
| Baud Rates for Asynchronous Mode<br>(BRGH = 0) .....  | 170      |
| Baud Rates for Asynchronous Mode<br>(BRGH = 1) .....  | 171      |
| Baud Rates for Synchronous Mode .....   | 169      |
| High Baud Rate Select (BRGH Bit) .....  | 168      |
| Sampling .....  | 168      |
| Serial Port Enable (SPEN Bit) .....   | 165      |
| Synchronous Master Mode .....   | 176      |
| Associated Registers, Reception .....   | 178      |
| Associated Registers, Transmit .....  | 176      |
| Reception .....   | 178      |
| Transmission .....  | 176      |
| Synchronous Slave Mode .....  | 179      |
| Associated Registers, Receive .....   | 180      |
| Associated Registers, Transmit .....  | 179      |
| Reception .....   | 180      |
| Transmission .....  | 179      |