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#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	I <sup>2</sup> C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	23
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 5x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18lf252t-i-so

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

# 2.4 External Clock Input

The EC and ECIO Oscillator modes require an external clock source to be connected to the OSC1 pin. The feedback device between OSC1 and OSC2 is turned off in these modes to save current. There is no oscillator start-up time required after a Power-on Reset or after a recovery from SLEEP mode.

In the EC Oscillator mode, the oscillator frequency divided by 4 is available on the OSC2 pin. This signal may be used for test purposes or to synchronize other logic. Figure 2-4 shows the pin connections for the EC Oscillator mode.

# FIGURE 2-4: EXTERNAL CLOCK INPUT OPERATION



The ECIO Oscillator mode functions like the EC mode, except that the OSC2 pin becomes an additional general purpose I/O pin. The I/O pin becomes bit 6 of PORTA (RA6). Figure 2-5 shows the pin connections for the ECIO Oscillator mode.

# FIGURE 2-5:

#### OPERATION (ECIO CONFIGURATION)

**EXTERNAL CLOCK INPUT** 



# 2.5 HS/PLL

A Phase Locked Loop circuit is provided as a programmable option for users that want to multiply the frequency of the incoming crystal oscillator signal by 4. For an input clock frequency of 10 MHz, the internal clock frequency will be multiplied to 40 MHz. This is useful for customers who are concerned with EMI due to high frequency crystals.

The PLL can only be enabled when the oscillator configuration bits are programmed for HS mode. If they are programmed for any other mode, the PLL is not enabled and the system clock will come directly from OSC1.

The PLL is one of the modes of the FOSC<2:0> configuration bits. The Oscillator mode is specified during device programming.

A PLL lock timer is used to ensure that the PLL has locked before device execution starts. The PLL lock timer has a time-out that is called TPLL.



# 2.7 Effects of SLEEP Mode on the On-Chip Oscillator

When the device executes a SLEEP instruction, the on-chip clocks and oscillator are turned off and the device is held at the beginning of an instruction cycle (Q1 state). With the oscillator off, the OSC1 and OSC2 signals will stop oscillating. Since all the transistor switching currents have been removed, SLEEP mode achieves the lowest current consumption of the device (only leakage currents). Enabling any on-chip feature that will operate during SLEEP will increase the current consumed during SLEEP. The user can wake from SLEEP through external RESET, Watchdog Timer Reset, or through an interrupt.

# TABLE 2-3: OSC1 AND OSC2 PIN STATES IN SLEEP MODE

OSC Mode	OSC1 Pin	OSC2 Pin
RC	Floating, external resistor should pull high	At logic low
RCIO	Floating, external resistor should pull high	Configured as PORTA, bit 6
ECIO	Floating	Configured as PORTA, bit 6
EC	Floating	At logic low
LP, XT, and HS	Feedback inverter disabled, at quiescent voltage level	Feedback inverter disabled, at quiescent voltage level

Note: See Table 3-1, in the "Reset" section, for time-outs due to SLEEP and MCLR Reset.

# 2.8 Power-up Delays

Power up delays are controlled by two timers, so that no external RESET circuitry is required for most applications. The delays ensure that the device is kept in RESET, until the device power supply and clock are stable. For additional information on RESET operation, see Section 3.0.

The first timer is the Power-up Timer (PWRT), which optionally provides a fixed delay of 72 ms (nominal) on power-up only (POR and BOR). The second timer is the Oscillator Start-up Timer (OST), intended to keep the chip in RESET until the crystal oscillator is stable.

With the PLL enabled (HS/PLL Oscillator mode), the time-out sequence following a Power-on Reset is different from other Oscillator modes. The time-out sequence is as follows: First, the PWRT time-out is invoked after a POR time delay has expired. Then, the Oscillator Start-up Timer (OST) is invoked. However, this is still not a sufficient amount of time to allow the PLL to lock at high frequencies. The PWRT timer is used to provide an additional fixed 2 ms (nominal) time-out to allow the PLL ample time to lock to the incoming clock frequency.

# 4.0 MEMORY ORGANIZATION

There are three memory blocks in Enhanced MCU devices. These memory blocks are:

- Program Memory
- Data RAM
- Data EEPROM

Data and program memory use separate busses, which allows for concurrent access of these blocks.

Additional detailed information for FLASH program memory and Data EEPROM is provided in Section 5.0 and Section 6.0, respectively.

# 4.1 **Program Memory Organization**

A 21-bit program counter is capable of addressing the 2-Mbyte program memory space. Accessing a location between the physically implemented memory and the 2-Mbyte address will cause a read of all '0's (a NOP instruction).

The PIC18F252 and PIC18F452 each have 32 Kbytes of FLASH memory, while the PIC18F242 and PIC18F442 have 16 Kbytes of FLASH. This means that PIC18FX52 devices can store up to 16K of single word instructions, and PIC18FX42 devices can store up to 8K of single word instructions.

The RESET vector address is at 0000h and the interrupt vector addresses are at 0008h and 0018h.

Figure 4-1 shows the Program Memory Map for PIC18F242/442 devices and Figure 4-2 shows the Program Memory Map for PIC18F252/452 devices.

# 4.12 Indirect Addressing, INDF and FSR Registers

Indirect addressing is a mode of addressing data memory, where the data memory address in the instruction is not fixed. An FSR register is used as a pointer to the data memory location that is to be read or written. Since this pointer is in RAM, the contents can be modified by the program. This can be useful for data tables in the data memory and for software stacks. Figure 4-9 shows the operation of indirect addressing. This shows the moving of the value to the data memory address specified by the value of the FSR register.

Indirect addressing is possible by using one of the INDF registers. Any instruction using the INDF register actually accesses the register pointed to by the File Select Register, FSR. Reading the INDF register itself, indirectly (FSR = 0), will read 00h. Writing to the INDF register indirectly, results in a no operation. The FSR register contains a 12-bit address, which is shown in Figure 4-10.

The INDFn register is not a physical register. Addressing INDFn actually addresses the register whose address is contained in the FSRn register (FSRn is a pointer). This is indirect addressing.

Example 4-4 shows a simple use of indirect addressing to clear the RAM in Bank1 (locations 100h-1FFh) in a minimum number of instructions.

#### EXAMPLE 4-4: HOW TO CLEAR RAM (BANK1) USING INDIRECT ADDRESSING

	LFSR	FSR0 ,0x100	;	
NEXT	CLRF	POSTINC0	;	Clear INDF
			;	register and
			;	inc pointer
	BTFSS	FSROH, 1	;	All done with
			;	Bank1?
	GOTO	NEXT	;	NO, clear next
CONTINU	JΕ		;	YES, continue

There are three indirect addressing registers. To address the entire data memory space (4096 bytes), these registers are 12-bit wide. To store the 12-bits of addressing information, two 8-bit registers are required. These indirect addressing registers are:

- 1. FSR0: composed of FSR0H:FSR0L
- 2. FSR1: composed of FSR1H:FSR1L
- 3. FSR2: composed of FSR2H:FSR2L

In addition, there are registers INDF0, INDF1 and INDF2, which are not physically implemented. Reading or writing to these registers activates indirect addressing, with the value in the corresponding FSR register being the address of the data. If an instruction writes a value to INDF0, the value will be written to the address pointed to by FSR0H:FSR0L. A read from INDF1 reads

the data from the address pointed to by FSR1H:FSR1L. INDFn can be used in code anywhere an operand can be used.

If INDF0, INDF1 or INDF2 are read indirectly via an FSR, all '0's are read (zero bit is set). Similarly, if INDF0, INDF1 or INDF2 are written to indirectly, the operation will be equivalent to a NOP instruction and the STATUS bits are not affected.

#### 4.12.1 INDIRECT ADDRESSING OPERATION

Each FSR register has an INDF register associated with it, plus four additional register addresses. Performing an operation on one of these five registers determines how the FSR will be modified during indirect addressing.

When data access is done to one of the five INDFn locations, the address selected will configure the FSRn register to:

- Do nothing to FSRn after an indirect access (no change) INDFn
- Auto-decrement FSRn after an indirect access (post-decrement) POSTDECn
- Auto-increment FSRn after an indirect access (post-increment) POSTINCn
- Auto-increment FSRn before an indirect access (pre-increment) PREINCn
- Use the value in the WREG register as an offset to FSRn. Do not modify the value of the WREG or the FSRn register after an indirect access (no change) - PLUSWn

When using the auto-increment or auto-decrement features, the effect on the FSR is not reflected in the STATUS register. For example, if the indirect address causes the FSR to equal '0', the Z bit will not be set.

Incrementing or decrementing an FSR affects all 12 bits. That is, when FSRnL overflows from an increment, FSRnH will be incremented automatically.

Adding these features allows the FSRn to be used as a stack pointer, in addition to its uses for table operations in data memory.

Each FSR has an address associated with it that performs an indexed indirect access. When a data access to this INDFn location (PLUSWn) occurs, the FSRn is configured to add the signed value in the WREG register and the value in FSR to form the address before an indirect access. The FSR value is not changed.

If an FSR register contains a value that points to one of the INDFn, an indirect read will read 00h (zero bit is set), while an indirect write will be equivalent to a NOP (STATUS bits are not affected).

If an indirect addressing operation is done where the target address is an FSRnH or FSRnL register, the write operation will dominate over the pre- or post-increment/decrement functions.

# 4.14 RCON Register

The Reset Control (RCON) register contains flag bits that allow differentiation between the sources of a device RESET. These flags include the TO, PD, POR, BOR and RI bits. This register is readable and writable.

- Note 1: If the BOREN configuration bit is set (Brown-out Reset enabled), the BOR bit is '1' on a Power-on Reset. After a Brownout Reset has occurred, the BOR bit will be cleared, and must be set by firmware to indicate the occurrence of the next Brown-out Reset.
  - 2: It is recommended that the POR bit be set after a Power-on Reset has been detected, so that subsequent Power-on Resets may be detected.

# REGISTER 4-3: RCON REGISTER

R/W-0	U-0	U-0	R/W-1	R-1	R-1	R/W-0	R/W-0
IPEN	_	—	RI	TO	PD	POR	BOR
bit 7							bit 0

bit 7	IPEN: Interrupt Priority Enable bit		
	1 = Enable priority levels on inter	rupts	
	0 = Disable priority levels on inter-	rupts (16CXXX	(Compatibility mode)
bit 6-5	Unimplemented: Read as '0'		
bit 4	RI: RESET Instruction Flag bit		
	1 = The RESET instruction was no	ot executed	
	0 = The RESET instruction was e	kecuted causing	g a device RESET
	(must be set in software after	a Brown-out R	eset occurs)
bit 3	<b>TO:</b> Watchdog Time-out Flag bit		
	1 = After power-up, CLRWDT instr	uction, or SLEE	IP instruction
	0 = A WDI time-out occurred		
bit 2	PD: Power-down Detection Flag I	bit	
	1 = After power-up or by the CLR	WDT instruction	
		struction	
bit 1	<b>POR:</b> Power-on Reset Status bit		
	1 = A Power-on Reset has not or	curred	
	0 = A Power-on Reset occurred	a Power-on R	aset occurs)
hit O	(Indici de set in soltware alter	a rower-on ne	
DIL U	BOR: Brown-out Reset Status bit	a autor d	
	$\perp$ = A Brown-out Reset has not o	currea	
	(must be set in software after	a Brown-out R	eset occurs)
	(		
	Legend:		
	R = Readable bit W =	Writable bit	U = Unimplemented bit, read as '0'

'1' = Bit is set

'0' = Bit is cleared

- n = Value at POR

x = Bit is unknown

#### REGISTER 8-3: INTCON3 REGISTER

	R/W-1	R/W-1	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
	INT2IP	INT1IP		INT2IE	INT1IE		INT2IF	INT1IF
	bit 7							bit 0
bit 7	INT2IP: IN	IT2 External I	nterrupt Prio	rity bit				
	1 = High p	riority						
	0 = Low pr	iority						
bit 6	INT1IP: IN	IT1 External I	nterrupt Prio	rity bit				
	1 = High p	riority						
	0 = Low pr	iority						
bit 5	Unimplem	nented: Read	as '0'					
bit 4	INT2IE: IN	IT2 External I	nterrupt Ena	ble bit				
	1 = Enable	es the INT2 ex	ternal interr	upt				
	0 = Disable	es the INT2 e	xternal interr	upt				
bit 3	INT1IE: IN	IT1 External I	nterrupt Ena	ble bit				
	1 = Enable	es the INT1 ex	ternal interr	upt				
	0 = Disable	es the INT1 e	xternal interr	upt				
bit 2	Unimplem	nented: Read	as '0'					
bit 1	INT2IF: IN	T2 External I	nterrupt Flag	bit				
	1 = The IN	T2 external ir	nterrupt occu	rred (must b	e cleared in	software)		
	0 = The IN	T2 external ir	nterrupt did n	ot occur				
bit 0	INT1IF: IN	T1 External I	nterrupt Flag	bit				
	1 = The IN	T1 external ir	nterrupt occu	rred (must b	e cleared in	software)		
	0 = The IN	T1 external ir	nterrupt did n	ot occur				
	Legend:							
	R = Reada	able bit	W = Wr	itable bit	U = Unimp	lemented	bit, read as	'0'
	- n = Value	at POR	'1' = Bit	is set	'0' = Bit is	cleared	x = Bit is u	Inknown

**Note:** Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt. This feature allows for software polling.

## TABLE 11-2: REGISTERS ASSOCIATED WITH TIMER1 AS A TIMER/COUNTER

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value POR,	e on BOR	Valu All C RES	e on )ther ETS
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000	000x	0000	000u
PIR1	PSPIF <sup>(1)</sup>	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000	0000	0000	0000
PIE1	PSPIE <sup>(1)</sup>	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000	0000	0000	0000
IPR1	PSPIP <sup>(1)</sup>	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	0000	0000	0000	0000
TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register xxxx xxxx uuuu uuuu								uuuu			
TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register xxxx xxxx uuuu uuuu											
T1CON	RD16		T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR10N	0-00	0000	u-uu	uuuu

Note 1: The PSPIF, PSPIE and PSPIP bits are reserved on the PIC18F2X2 devices; always maintain these bits clear.

# 13.0 TIMER3 MODULE

The Timer3 module timer/counter has the following features:

- 16-bit timer/counter (two 8-bit registers; TMR3H and TMR3L)
- Readable and writable (both registers)
- Internal or external clock select
- Interrupt-on-overflow from FFFFh to 0000h
- RESET from CCP module trigger

Figure 13-1 is a simplified block diagram of the Timer3 module.

Register 13-1 shows the Timer3 control register. This register controls the Operating mode of the Timer3 module and sets the CCP clock source.

Register 11-1 shows the Timer1 control register. This register controls the Operating mode of the Timer1 module, as well as contains the Timer1 oscillator enable bit (T1OSCEN), which can be a clock source for Timer3.

#### REGISTER 13-1: T3CON: TIMER3 CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RD16	T3CCP2	T3CKPS1	T3CKPS0	T3CCP1	<b>T3SYNC</b>	TMR3CS	TMR3ON
bit 7							bit 0

bit 7	<b>RD16:</b> 16-bit Read/Write I 1 = Enables register Read 0 = Enables register Read	Mode Enable bit I/Write of Timer3 in on I/Write of Timer3 in two	e 16-bit operation o 8-bit operations				
bit 6-3	T3CCP2:T3CCP1: Timer3 and Timer1 to CCPx Enable bits 1x = Timer3 is the clock source for compare/capture CCP modules 01 = Timer3 is the clock source for compare/capture of CCP2, Timer1 is the clock source for compare/capture of CCP1 00 = Timer1 is the clock source for compare/capture CCP modules						
bit 5-4	<b>T3CKPS1:T3CKPS0</b> : Timer3 Input Clock Prescale Select bits 11 = 1:8 Prescale value 10 = 1:4 Prescale value 01 = 1:2 Prescale value 00 = 1:1 Prescale value						
bit 2	T3SYNC: Timer3 External Clock Input Synchronization Control bit         (Not usable if the system clock comes from Timer1/Timer3)         When TMR3CS = 1:         1 = Do not synchronize external clock input         0 = Synchronize external clock input         When TMR3CS = 0:						
bit 1	TMR3CS: Timer3 Clock S 1 = External clock input fr (on the rising edge af 0 = Internal clock (Fosc/4	ource Select bit om Timer1 oscillator c ter the first falling edge	ər T1CKI ə)				
bit 0	<b>TMR3ON:</b> Timer3 On bit 1 = Enables Timer3 0 = Stops Timer3						
	Legend:						
	R = Readable bit - n = Value at POR	W = Writable bit '1' = Bit is set	U = Unimplemented '0' = Bit is cleared	bit, read as '0' x = Bit is unknown			

# 14.1 CCP1 Module

Capture/Compare/PWM Register 1 (CCPR1) is comprised of two 8-bit registers: CCPR1L (low byte) and CCPR1H (high byte). The CCP1CON register controls the operation of CCP1. All are readable and writable.

## TABLE 14-1: CCP MODE - TIMER RESOURCE

CCP Mode	Timer Resource
Capture	Timer1 or Timer3
Compare	Timer1 or Timer3
PWM	Timer2

# 14.2 CCP2 Module

Capture/Compare/PWM Register2 (CCPR2) is comprised of two 8-bit registers: CCPR2L (low byte) and CCPR2H (high byte). The CCP2CON register controls the operation of CCP2. All are readable and writable.

# TABLE 14-2: INTERACTION OF TWO CCP MODULES

CCPx Mode	CCPy Mode	Interaction
Capture	Capture	TMR1 or TMR3 time-base. Time-base can be different for each CCP.
Capture	Compare	The compare could be configured for the special event trigger, which clears either TMR1 or TMR3 depending upon which time-base is used.
Compare	Compare	The compare(s) could be configured for the special event trigger, which clears TMR1 or TMR3 depending upon which time-base is used.
PWM	PWM	The PWMs will have the same frequency and update rate (TMR2 interrupt).
PWM	Capture	None
PWM	Compare	None

# 14.3 Capture Mode

In Capture mode, CCPR1H:CCPR1L captures the 16-bit value of the TMR1 or TMR3 registers when an event occurs on pin RC2/CCP1. An event is defined as one of the following:

- every falling edge
- every rising edge
- every 4th rising edge
- every 16th rising edge

The event is selected by control bits CCP1M3:CCP1M0 (CCP1CON<3:0>). When a capture is made, the interrupt request flag bit CCP1IF (PIR1<2>) is set; it must be cleared in software. If another capture occurs before the value in register CCPR1 is read, the old captured value is overwritten by the new captured value.

#### 14.3.1 CCP PIN CONFIGURATION

In Capture mode, the RC2/CCP1 pin should be configured as an input by setting the TRISC<2> bit.

Note:	If the RC2/CCP1 is configured as an out-
	put, a write to the port can cause a capture
	condition.

#### 14.3.2 TIMER1/TIMER3 MODE SELECTION

The timers that are to be used with the capture feature (either Timer1 and/or Timer3) must be running in Timer mode or Synchronized Counter mode. In Asynchronous Counter mode, the capture operation may not work. The timer to be used with each CCP module is selected in the T3CON register.

#### 14.3.3 SOFTWARE INTERRUPT

When the Capture mode is changed, a false capture interrupt may be generated. The user should keep bit CCP1IE (PIE1<2>) clear to avoid false interrupts and should clear the flag bit, CCP1IF, following any such change in Operating mode.

#### 14.3.4 CCP PRESCALER

There are four prescaler settings, specified by bits CCP1M3:CCP1M0. Whenever the CCP module is turned off or the CCP module is not in Capture mode, the prescaler counter is cleared. This means that any RESET will clear the prescaler counter.

Switching from one capture prescaler to another may generate an interrupt. Also, the prescaler counter will not be cleared, therefore, the first capture may be from a non-zero prescaler. Example 14-1 shows the recommended method for switching between capture prescalers. This example also clears the prescaler counter and will not generate the "false" interrupt.

# EXAMPLE 14-1: CHANGING BETWEEN CAPTURE PRESCALERS

CLRF	CCP1CON, F	;	Turn CCP module off
MOVLW	NEW_CAPT_PS	;	Load WREG with the
		;	new prescaler mode
		;	value and CCP ON
MOVWF	CCP1CON	;	Load CCP1CON with
		;	this value





## 14.5 PWM Mode

In Pulse Width Modulation (PWM) mode, the CCP1 pin produces up to a 10-bit resolution PWM output. Since the CCP1 pin is multiplexed with the PORTC data latch, the TRISC<2> bit must be cleared to make the CCP1 pin an output.

Note:	Clearing the CCP1CON register will force
	the CCP1 PWM output latch to the default
	low level. This is not the PORTC I/O data
	aun.

Figure 14-3 shows a simplified block diagram of the CCP module in PWM mode.

For a step-by-step procedure on how to set up the CCP module for PWM operation, see Section 14.5.3.

#### FIGURE 14-3: SIMPLIFIED PWM BLOCK DIAGRAM



A PWM output (Figure 14-4) has a time-base (period) and a time that the output stays high (duty cycle). The frequency of the PWM is the inverse of the period (1/period).





#### 14.5.1 PWM PERIOD

The PWM period is specified by writing to the PR2 register. The PWM period can be calculated using the following formula:

$$PWM period = (PR2) + 1] \bullet 4 \bullet TOSC \bullet$$
  
(TMR2 prescale value)

PWM frequency is defined as 1 / [PWM period].

When TMR2 is equal to PR2, the following three events occur on the next increment cycle:

- TMR2 is cleared
- The CCP1 pin is set (exception: if PWM duty cycle = 0%, the CCP1 pin will not be set)
- The PWM duty cycle is latched from CCPR1L into CCPR1H

Note:	The Timer2 postscaler (see Section 12.0)
	is not used in the determination of the
	PWM frequency. The postscaler could be
	used to have a servo update rate at a
	different frequency than the PWM output.

#### 14.5.2 PWM DUTY CYCLE

The PWM duty cycle is specified by writing to the CCPR1L register and to the CCP1CON<5:4> bits. Up to 10-bit resolution is available. The CCPR1L contains the eight MSbs and the CCP1CON<5:4> contains the two LSbs. This 10-bit value is represented by CCPR1L:CCP1CON<5:4>. The following equation is used to calculate the PWM duty cycle in time:

CCPR1L and CCP1CON<5:4> can be written to at any time, but the duty cycle value is not latched into CCPR1H until after a match between PR2 and TMR2 occurs (i.e., the period is complete). In PWM mode, CCPR1H is a read only register.

The CCPR1H register and a 2-bit internal latch are used to double buffer the PWM duty cycle. This double buffering is essential for glitchless PWM operation.

When the CCPR1H and 2-bit latch match TMR2 concatenated with an internal 2-bit Q clock or 2 bits of the TMR2 prescaler, the CCP1 pin is cleared.

The maximum PWM resolution (bits) for a given PWM frequency is given by the equation:

PWM Resolution (max) = 
$$\frac{\log(\frac{\text{Fosc}}{\text{FPWM}})}{\log(2)}$$
 bits

Note: If the PWM duty cycle value is longer than the PWM period, the CCP1 pin will not be cleared.

#### 15.4.7 BAUD RATE GENERATOR

In I<sup>2</sup>C Master mode, the baud rate generator (BRG) reload value is placed in the lower 7 bits of the SSPADD register (Figure 15-17). When a write occurs to SSPBUF, the baud rate generator will automatically begin counting. The BRG counts down to 0 and stops until another reload has taken place. The BRG count is decremented twice per instruction cycle (TcY) on the Q2 and Q4 clocks. In I<sup>2</sup>C Master mode, the BRG is reloaded automatically.

Once the given operation is complete (i.e., transmission of the last data bit is followed by  $\overline{ACK}$ ), the internal clock will automatically stop counting and the SCL pin will remain in its last state.

Table 15-3 demonstrates clock rates based on instruction cycles and the BRG value loaded into SSPADD.

#### FIGURE 15-17: BAUD RATE GENERATOR BLOCK DIAGRAM



## TABLE 15-3: I<sup>2</sup>C CLOCK RATE W/BRG

Fcy	Fcy*2	BRG Value	FSCL <sup>(2)</sup> (2 Rollovers of BRG)
10 MHz	20 MHz	19h	400 kHz <sup>(1)</sup>
10 MHz	20 MHz	20h	312.5 kHz
10 MHz	20 MHz	3Fh	100 kHz
4 MHz	8 MHz	0Ah	400 kHz <sup>(1)</sup>
4 MHz	8 MHz	0Dh	308 kHz
4 MHz	8 MHz	28h	100 kHz
1 MHz	2 MHz	03h	333 kHz <sup>(1)</sup>
1 MHz	2 MHz	0Ah	100kHz
1 MHz	2 MHz	00h	1 MHz <sup>(1)</sup>

**Note 1:** The I<sup>2</sup>C interface does not conform to the 400 kHz I<sup>2</sup>C specification (which applies to rates greater than 100 kHz) in all details, but may be used with care where higher rates are required by the application.

2: Actual frequency will depend on bus conditions. Theoretically, bus conditions will add rise time and extend low time of clock period, producing the effective frequency.

#### 15.4.17.1 Bus Collision During a START Condition

During a START condition, a bus collision occurs if:

- a) SDA or SCL are sampled low at the beginning of the START condition (Figure 15-26).
- b) SCL is sampled low before SDA is asserted low (Figure 15-27).

During a START condition, both the SDA and the SCL pins are monitored.

If the SDA pin is already low, or the SCL pin is already low, then all of the following occur:

- the START condition is aborted,
- the BCLIF flag is set, and
- the MSSP module is reset to its IDLE state (Figure 15-26).

The START condition begins with the SDA and SCL pins de-asserted. When the SDA pin is sampled high, the baud rate generator is loaded from SSPADD<6:0> and counts down to 0. If the SCL pin is sampled low while SDA is high, a bus collision occurs, because it is assumed that another master is attempting to drive a data '1' during the START condition.

If the SDA pin is sampled low during this count, the BRG is reset and the SDA line is asserted early (Figure 15-28). If, however, a '1' is sampled on the SDA pin, the SDA pin is asserted low at the end of the BRG count. The baud rate generator is then reloaded and counts down to 0, and during this time, if the SCL pins are sampled as '0', a bus collision does not occur. At the end of the BRG count, the SCL pin is asserted low.

Note: The reason that bus collision is not a factor during a START condition is that no two bus masters can assert a START condition at the exact same time. Therefore, one master will always assert SDA before the other. This condition does not cause a bus collision, because the two masters must be allowed to arbitrate the first address following the START condition. If the address is the same, arbitration must be allowed to continue into the data portion, Repeated START or STOP conditions.



#### FIGURE 15-26: BUS COLLISION DURING START CONDITION (SDA ONLY)

### 16.3 USART Synchronous Master Mode

In Synchronous Master mode, the data is transmitted in a half-duplex manner (i.e., transmission and reception do not occur at the same time). When transmitting data, the reception is inhibited and vice versa. Synchronous mode is entered by setting bit SYNC (TXSTA<4>). In addition, enable bit SPEN (RCSTA<7>) is set in order to configure the RC6/TX/CK and RC7/RX/DT I/O pins to CK (clock) and DT (data) lines, respectively. The Master mode indicates that the processor transmits the master clock on the CK line. The Master mode is entered by setting bit CSRC (TXSTA<7>).

#### 16.3.1 USART SYNCHRONOUS MASTER TRANSMISSION

The USART transmitter block diagram is shown in Figure 16-1. The heart of the transmitter is the Transmit (serial) Shift Register (TSR). The shift register obtains its data from the read/write transmit buffer register TXREG. The TXREG register is loaded with data in software. The TSR register is not loaded until the last bit has been transmitted from the previous load. As soon as the last bit is transmitted, the TSR is loaded with new data from the TXREG (if available). Once the TXREG register transfers the data to the TSR register (occurs in one TCYCLE), the TXREG is empty and interrupt bit TXIF (PIR1<4>) is set. The interrupt can be enabled/disabled by setting/clearing enable bit TXIE

(PIE1<4>). Flag bit TXIF will be set, regardless of the state of enable bit TXIE, and cannot be cleared in software. It will reset only when new data is loaded into the TXREG register. While flag bit TXIF indicates the status of the TXREG register, another bit TRMT (TXSTA<1>) shows the status of the TSR register. TRMT is a read only bit, which is set when the TSR is empty. No interrupt logic is tied to this bit, so the user has to poll this bit in order to determine if the TSR register is empty. The TSR is not mapped in data memory, so it is not available to the user.

To set up a Synchronous Master Transmission:

- 1. Initialize the SPBRG register for the appropriate baud rate (Section 16.1).
- 2. Enable the synchronous master serial port by setting bits SYNC, SPEN, and CSRC.
- 3. If interrupts are desired, set enable bit TXIE.
- 4. If 9-bit transmission is desired, set bit TX9.
- 5. Enable the transmission by setting bit TXEN.
- 6. If 9-bit transmission is selected, the ninth bit should be loaded in bit TX9D.
- 7. Start transmission by loading data to the TXREG register.

Note: TXIF is not cleared immediately upon loading data into the transmit buffer TXREG. The flag bit becomes valid in the second instruction cycle following the load instruction.

# TABLE 16-8: REGISTERS ASSOCIATED WITH SYNCHRONOUS MASTER TRANSMISSION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on All Other RESETS
INTCON	GIE/ GIEH	PEIE/ GIEL	TMR0IE	INTOIE	RBIE	TMR0IF	INTOIF	RBIF	0000 000x	0000 000u
PIR1	PSPIF <sup>(1)</sup>	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
PIE1	PSPIE <sup>(1)</sup>	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
IPR1	PSPIP <sup>(1)</sup>	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	0000 0000	0000 0000
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	x00- 0000	0000 -00x
TXREG	USART T	ransmit F	Register						0000 0000	0000 0000
TXSTA	CSRC	TX9	TXEN	SYNC	_	BRGH	TRMT	TX9D	0000 -010	0000 -010
SPBRG	Baud Rate	e Genera	ator Regist	er					0000 0000	0000 0000

Legend: x = unknown, - = unimplemented, read as '0'.

Shaded cells are not used for Synchronous Master Transmission.

Note 1: The PSPIF, PSPIE and PSPIP bits are reserved on the PIC18F2X2 devices; always maintain these bits clear.

# 16.4.2 USART SYNCHRONOUS SLAVE RECEPTION

The operation of the Synchronous Master and Slave modes is identical, except in the case of the SLEEP mode and bit SREN, which is a "don't care" in Slave mode.

If receive is enabled by setting bit CREN prior to the SLEEP instruction, then a word may be received during SLEEP. On completely receiving the word, the RSR register will transfer the data to the RCREG register, and if enable bit RCIE bit is set, the interrupt generated will wake the chip from SLEEP. If the global interrupt is enabled, the program will branch to the interrupt vector.

To set up a Synchronous Slave Reception:

- Enable the synchronous master serial port by setting bits SYNC and SPEN and clearing bit CSRC.
- 2. If interrupts are desired, set enable bit RCIE.
- 3. If 9-bit reception is desired, set bit RX9.
- 4. To enable reception, set enable bit CREN.
- 5. Flag bit RCIF will be set when reception is complete. An interrupt will be generated if enable bit RCIE was set.
- Read the RCSTA register to get the ninth bit (if enabled) and determine if any error occurred during reception.
- 7. Read the 8-bit received data by reading the RCREG register.
- 8. If any error occurred, clear the error by clearing bit CREN.
- If using interrupts, ensure that the GIE and PEIE bits in the INTCON register (INTCON<7:6>) are set.

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Valu POR,	e on BOR	Valu All C RES	e on )ther ETS
INTCON	GIE/ GIEH	PEIE/ GIEL	TMR0IE	INTOIE	RBIE	TMR0IF	INTOIF	RBIF	0000	000x	0000	000u
PIR1	PSPIF <sup>(1)</sup>	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000	0000	0000	0000
PIE1	PSPIE <sup>(1)</sup>	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000	0000	0000	0000
IPR1	PSPIP <sup>(1)</sup>	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	0000	0000	0000	0000
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000	-00x	0000	-00x
RCREG	USART Receive Register							0000	0000	0000	0000	
TXSTA	CSRC	TX9	TXEN	SYNC	_	BRGH	TRMT	TX9D	0000	-010	0000	-010
SPBRG	Baud Rate	Generat	or Registe	r					0000	0000	0000	0000

#### TABLE 16-11: REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE RECEPTION

Legend: x = unknown, - = unimplemented, read as '0'.

Shaded cells are not used for Synchronous Slave Reception.

Note 1: The PSPIF, PSPIE and PSPIP bits are reserved on the PIC18F2X2 devices; always maintain these bits clear.

# 22.0 ELECTRICAL CHARACTERISTICS

#### Absolute Maximum Ratings (†)

Ambient temperature under bias	55°C to +125°C
Storage temperature	65°C to +150°C
Voltage on any pin with respect to Vss (except VDD, MCLR, and RA4)	-0.3V to (VDD + 0.3V)
Voltage on VDD with respect to Vss	-0.3V to +7.5V
Voltage on MCLR with respect to Vss (Note 2)	0V to +13.25V
Voltage on RA4 with respect to Vss	0V to +8.5V
Total power dissipation (Note 1)	1.0W
Maximum current out of Vss pin	
Maximum current into VDD pin	250 mA
Input clamp current, Iik (VI < 0 or VI > VDD)	±20 mA
Output clamp current, Ioк (Vo < 0 or Vo > VDD)	±20 mA
Maximum output current sunk by any I/O pin	25 mA
Maximum output current sourced by any I/O pin	25 mA
Maximum current sunk by PORTA, PORTB, and PORTE (Note 3) (combined)	200 mA
Maximum current sourced by PORTA, PORTB, and PORTE (Note 3) (combined)	200 mA
Maximum current sunk by PORTC and PORTD (Note 3) (combined)	200 mA
Maximum current sourced by PORTC and PORTD (Note 3) (combined)	200 mA

- Note 1: Power dissipation is calculated as follows: Pdis = VDD x {IDD -  $\sum$  IOH} +  $\sum$  {(VDD-VOH) x IOH} +  $\sum$ (VOI x IOL)
  - **2:** Voltage spikes below Vss at the  $\overline{\text{MCLR}}/\text{VPP}$  pin, inducing currents greater than 80 mA, may cause latchup. Thus, a series resistor of 50-100 $\Omega$  should be used when applying a "low" level to the  $\overline{\text{MCLR}}/\text{VPP}$  pin, rather than pulling this pin directly to Vss.
  - 3: PORTD and PORTE not available on the PIC18F2X2 devices.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

# PIC18FXX2





FIGURE 22-2: PIC18LFXX2 VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)





# FIGURE 22-18: MASTER SSP I<sup>2</sup>C BUS START/STOP BITS TIMING WAVEFORMS

TABLE 22-17:	MASTER SSP I <sup>2</sup> C BL	S START/STOP BITS	<b>REQUIREMENTS</b>
--------------	--------------------------------	-------------------	---------------------

Param. No.	Varam. No. Symbol Characteristic		ristic	stic Min		Units	Conditions
90	TSU:STA	START condition	100 kHz mode	2(Tosc)(BRG + 1)		ns	Only relevant for
		Setup time	400 kHz mode	2(Tosc)(BRG + 1)	_		Repeated START
			1 MHz mode <sup>(1)</sup>	2(Tosc)(BRG + 1)	_		condition
91	THD:STA	START condition	100 kHz mode	2(Tosc)(BRG + 1)	_	ns	After this period, the first clock pulse is generated
		Hold time	400 kHz mode	2(Tosc)(BRG + 1)	_	-	
			1 MHz mode <sup>(1)</sup>	2(Tosc)(BRG + 1)			
92	Tsu:sto	STOP condition	100 kHz mode	2(Tosc)(BRG + 1)		ns	
		Setup time	400 kHz mode	2(Tosc)(BRG + 1)	_		
			1 MHz mode <sup>(1)</sup>	2(Tosc)(BRG + 1)			
93	THD:STO	STOP condition	100 kHz mode	2(Tosc)(BRG + 1)	_	ns	
		Hold time	400 kHz mode	2(Tosc)(BRG + 1)	_		
			1 MHz mode <sup>(1)</sup>	2(Tosc)(BRG + 1)			

**Note 1:** Maximum pin capacitance = 10 pF for all  $I^2C$  pins.

# FIGURE 22-19: MASTER SSP I<sup>2</sup>C BUS DATA TIMING



#### TABLE 22-22: A/D CONVERSION REQUIREMENTS

Param No.	Symbol	Characte	eristic	Min	Max	Units	Conditions
130	Tad	A/D clock period PIC18FXXX		1.6	20 <sup>(4)</sup>	μs	Tosc based
			PIC18FXXX	2.0	6.0	μs	A/D RC mode
131	TCNV	Conversion time (not including acquisitic	11	12	Tad		
132	TACQ	Acquisition time (Note	5	_	μs	VREF = VDD = 5.0V	
			10		μs	VREF = VDD = 2.5V	
135	Tswc	Switching Time from co		(Note 3)			

**Note 1:** ADRES register may be read on the following TCY cycle.

**2:** The time for the holding capacitor to acquire the "New" input voltage, when the new input value has not changed by more than 1 LSB from the last sampled voltage. The source impedance (*Rs*) on the input channels is 50Ω. See Section 17.0 for more information on acquisition time consideration.

3: On the next Q4 cycle of the device clock.

4: The time of the A/D clock period is dependent on the device frequency and the TAD clock divider.

# Package Marking Information (Cont'd)

44-Lead TQFP



44-Lead PLCC



Example



Example

