



Welcome to [E-XFL.COM](https://www.e-xfl.com)

### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	I <sup>2</sup> C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	34
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic18lf442-i-ml">https://www.e-xfl.com/product-detail/microchip-technology/pic18lf442-i-ml</a>

## TO OUR VALUED CUSTOMERS

It is our intention to provide our valued customers with the best documentation possible to ensure successful use of your Microchip products. To this end, we will continue to improve our publications to better suit your needs. Our publications will be refined and enhanced as new volumes and updates are introduced.

If you have any questions or comments regarding this publication, please contact the Marketing Communications Department via E-mail at [docerrors@microchip.com](mailto:docerrors@microchip.com) or fax the **Reader Response Form** in the back of this data sheet to (480) 792-4150. We welcome your feedback.

### Most Current Data Sheet

To obtain the most up-to-date version of this data sheet, please register at our Worldwide Web site at:

<http://www.microchip.com>

You can determine the version of a data sheet by examining its literature number found on the bottom outside corner of any page. The last character of the literature number is the version number, (e.g., DS30000A is version A of document DS30000).

### Errata

An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

To determine if an errata sheet exists for a particular device, please check with one of the following:

- Microchip's Worldwide Web site; <http://www.microchip.com>
- Your local Microchip sales office (see last page)

When contacting a sales office, please specify which device, revision of silicon and data sheet (include literature number) you are using.

### Customer Notification System

Register on our web site at [www.microchip.com](http://www.microchip.com) to receive the most current information on all of our products.

# PIC18FXX2

---

NOTES:

## 4.14 RCON Register

The Reset Control (RCON) register contains flag bits that allow differentiation between the sources of a device RESET. These flags include the  $\overline{TO}$ ,  $\overline{PD}$ ,  $\overline{POR}$ ,  $\overline{BOR}$  and  $\overline{RI}$  bits. This register is readable and writable.

**Note 1:** If the BOREN configuration bit is set (Brown-out Reset enabled), the  $\overline{BOR}$  bit is '1' on a Power-on Reset. After a Brown-out Reset has occurred, the  $\overline{BOR}$  bit will be cleared, and must be set by firmware to indicate the occurrence of the next Brown-out Reset.

**2:** It is recommended that the  $\overline{POR}$  bit be set after a Power-on Reset has been detected, so that subsequent Power-on Resets may be detected.

### REGISTER 4-3: RCON REGISTER

R/W-0	U-0	U-0	R/W-1	R-1	R-1	R/W-0	R/W-0
IPEN	—	—	$\overline{RI}$	$\overline{TO}$	$\overline{PD}$	$\overline{POR}$	$\overline{BOR}$
bit 7							bit 0

- bit 7 **IPEN:** Interrupt Priority Enable bit  
 1 = Enable priority levels on interrupts  
 0 = Disable priority levels on interrupts (16CXXX Compatibility mode)
- bit 6-5 **Unimplemented:** Read as '0'
- bit 4  **$\overline{RI}$ :** RESET Instruction Flag bit  
 1 = The RESET instruction was not executed  
 0 = The RESET instruction was executed causing a device RESET  
 (must be set in software after a Brown-out Reset occurs)
- bit 3  **$\overline{TO}$ :** Watchdog Time-out Flag bit  
 1 = After power-up, CLRWD $\overline{T}$  instruction, or SLEEP instruction  
 0 = A WDT time-out occurred
- bit 2  **$\overline{PD}$ :** Power-down Detection Flag bit  
 1 = After power-up or by the CLRWD $\overline{T}$  instruction  
 0 = By execution of the SLEEP instruction
- bit 1  **$\overline{POR}$ :** Power-on Reset Status bit  
 1 = A Power-on Reset has not occurred  
 0 = A Power-on Reset occurred  
 (must be set in software after a Power-on Reset occurs)
- bit 0  **$\overline{BOR}$ :** Brown-out Reset Status bit  
 1 = A Brown-out Reset has not occurred  
 0 = A Brown-out Reset occurred  
 (must be set in software after a Brown-out Reset occurs)

#### Legend:

R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '0'  
 - n = Value at POR      '1' = Bit is set      '0' = Bit is cleared      x = Bit is unknown

## 10.0 TIMER0 MODULE

The Timer0 module has the following features:

- Software selectable as an 8-bit or 16-bit timer/counter
- Readable and writable
- Dedicated 8-bit software programmable prescaler
- Clock source selectable to be external or internal
- Interrupt-on-overflow from FFh to 00h in 8-bit mode and FFFFh to 0000h in 16-bit mode
- Edge select for external clock

Figure 10-1 shows a simplified block diagram of the Timer0 module in 8-bit mode and Figure 10-2 shows a simplified block diagram of the Timer0 module in 16-bit mode.

The T0CON register (Register 10-1) is a readable and writable register that controls all the aspects of Timer0, including the prescale selection.

### REGISTER 10-1: T0CON: TIMER0 CONTROL REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
TMR0ON	T08BIT	T0CS	T0SE	PSA	T0PS2	T0PS1	T0PS0
bit 7							bit 0

- bit 7 **TMR0ON:** Timer0 On/Off Control bit  
 1 = Enables Timer0  
 0 = Stops Timer0
- bit 6 **T08BIT:** Timer0 8-bit/16-bit Control bit  
 1 = Timer0 is configured as an 8-bit timer/counter  
 0 = Timer0 is configured as a 16-bit timer/counter
- bit 5 **T0CS:** Timer0 Clock Source Select bit  
 1 = Transition on T0CKI pin  
 0 = Internal instruction cycle clock (CLKO)
- bit 4 **T0SE:** Timer0 Source Edge Select bit  
 1 = Increment on high-to-low transition on T0CKI pin  
 0 = Increment on low-to-high transition on T0CKI pin
- bit 3 **PSA:** Timer0 Prescaler Assignment bit  
 1 = Timer0 prescaler is NOT assigned. Timer0 clock input bypasses prescaler.  
 0 = Timer0 prescaler is assigned. Timer0 clock input comes from prescaler output.
- bit 2-0 **T0PS2:T0PS0:** Timer0 Prescaler Select bits  
 111 = 1:256 prescale value  
 110 = 1:128 prescale value  
 101 = 1:64 prescale value  
 100 = 1:32 prescale value  
 011 = 1:16 prescale value  
 010 = 1:8 prescale value  
 001 = 1:4 prescale value  
 000 = 1:2 prescale value

#### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared      x = Bit is unknown

## 14.0 CAPTURE/COMPARE/PWM (CCP) MODULES

Each CCP (Capture/Compare/PWM) module contains a 16-bit register which can operate as a 16-bit Capture register, as a 16-bit Compare register or as a PWM Master/Slave Duty Cycle register. Table 14-1 shows the timer resources of the CCP Module modes.

The operation of CCP1 is identical to that of CCP2, with the exception of the special event trigger. Therefore, operation of a CCP module in the following sections is described with respect to CCP1.

Table 14-2 shows the interaction of the CCP modules.

**REGISTER 14-1: CCP1CON REGISTER/CCP2CON REGISTER**

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	DCxB1	DCxB0	CCPxM3	CCPxM2	CCPxM1	CCPxM0
bit 7		bit 0					

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **DCxB1:DCxB0:** PWM Duty Cycle bit1 and bit0

Capture mode:

Unused

Compare mode:

Unused

PWM mode:

These bits are the two LSbs (bit1 and bit0) of the 10-bit PWM duty cycle. The upper eight bits (DCx9:DCx2) of the duty cycle are found in CCPxL.

bit 3-0 **CCPxM3:CCPxM0:** CCPx Mode Select bits

0000 = Capture/Compare/PWM disabled (resets CCPx module)

0001 = Reserved

0010 = Compare mode, toggle output on match (CCPxIF bit is set)

0011 = Reserved

0100 = Capture mode, every falling edge

0101 = Capture mode, every rising edge

0110 = Capture mode, every 4th rising edge

0111 = Capture mode, every 16th rising edge

1000 = Compare mode,

Initialize CCP pin Low, on compare match force CCP pin High (CCPIF bit is set)

1001 = Compare mode,

Initialize CCP pin High, on compare match force CCP pin Low (CCPIF bit is set)

1010 = Compare mode,

Generate software interrupt on compare match (CCPIF bit is set, CCP pin is unaffected)

1011 = Compare mode,

Trigger special event (CCPIF bit is set)

11xx = PWM mode

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

- n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

# PIC18FXX2

## 14.4 Compare Mode

In Compare mode, the 16-bit CCPR1 (CCPR2) register value is constantly compared against either the TMR1 register pair value, or the TMR3 register pair value. When a match occurs, the RC2/CCP1 (RC1/CCP2) pin is:

- driven High
- driven Low
- toggle output (High to Low or Low to High)
- remains unchanged

The action on the pin is based on the value of control bits CCP1M3:CCP1M0 (CCP2M3:CCP2M0). At the same time, interrupt flag bit CCP1IF (CCP2IF) is set.

### 14.4.1 CCP PIN CONFIGURATION

The user must configure the CCPx pin as an output by clearing the appropriate TRISC bit.

**Note:** Clearing the CCP1CON register will force the RC2/CCP1 compare output latch to the default low level. This is not the PORTC I/O data latch.

### 14.4.2 TIMER1/TIMER3 MODE SELECTION

Timer1 and/or Timer3 must be running in Timer mode or Synchronized Counter mode if the CCP module is using the compare feature. In Asynchronous Counter mode, the compare operation may not work.

### 14.4.3 SOFTWARE INTERRUPT MODE

When generate software interrupt is chosen, the CCP1 pin is not affected. Only a CCP interrupt is generated (if enabled).

### 14.4.4 SPECIAL EVENT TRIGGER

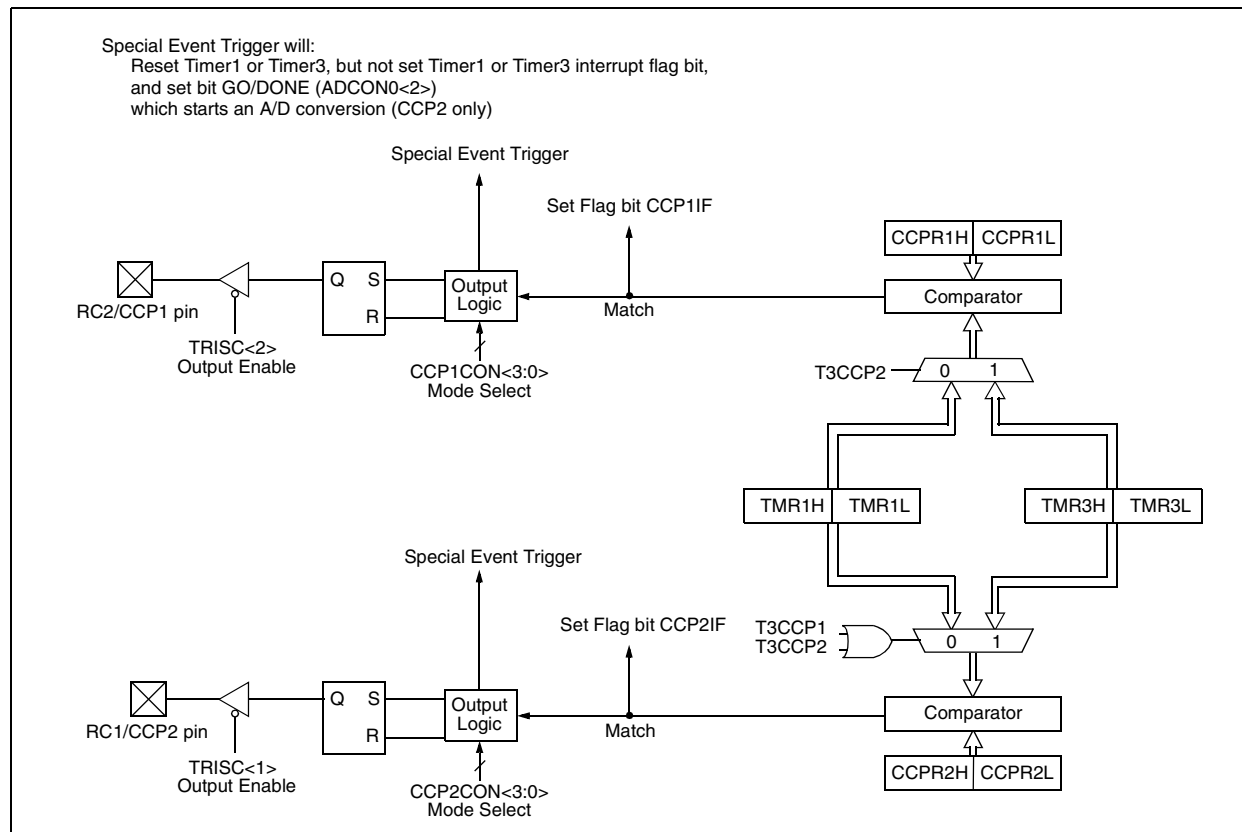
In this mode, an internal hardware trigger is generated, which may be used to initiate an action.

The special event trigger output of CCP1 resets the TMR1 register pair. This allows the CCPR1 register to effectively be a 16-bit programmable period register for Timer1.

The special trigger output of CCPx resets either the TMR1 or TMR3 register pair. Additionally, the CCP2 Special Event Trigger will start an A/D conversion if the A/D module is enabled.

**Note:** The special event trigger from the CCP2 module will not set the Timer1 or Timer3 interrupt flag bits.

**FIGURE 14-2: COMPARE MODE OPERATION BLOCK DIAGRAM**



## 15.3.6 SLAVE MODE

In Slave mode, the data is transmitted and received as the external clock pulses appear on SCK. When the last bit is latched, the SSPIF interrupt flag bit is set.

While in Slave mode, the external clock is supplied by the external clock source on the SCK pin. This external clock must meet the minimum high and low times as specified in the electrical specifications.

While in SLEEP mode, the slave can transmit/receive data. When a byte is received, the device will wake-up from sleep.

## 15.3.7 SLAVE SELECT SYNCHRONIZATION

The  $\overline{SS}$  pin allows a Synchronous Slave mode. The SPI must be in Slave mode with  $\overline{SS}$  pin control enabled ( $SSPCON1<3:0> = 04h$ ). The pin must not be driven low for the  $\overline{SS}$  pin to function as an input. The Data Latch must be high. When the  $\overline{SS}$  pin is low, transmission and reception are enabled and the SDO pin is driven. When the  $\overline{SS}$  pin goes high, the SDO pin is no

longer driven, even if in the middle of a transmitted byte, and becomes a floating output. External pull-up/pull-down resistors may be desirable, depending on the application.

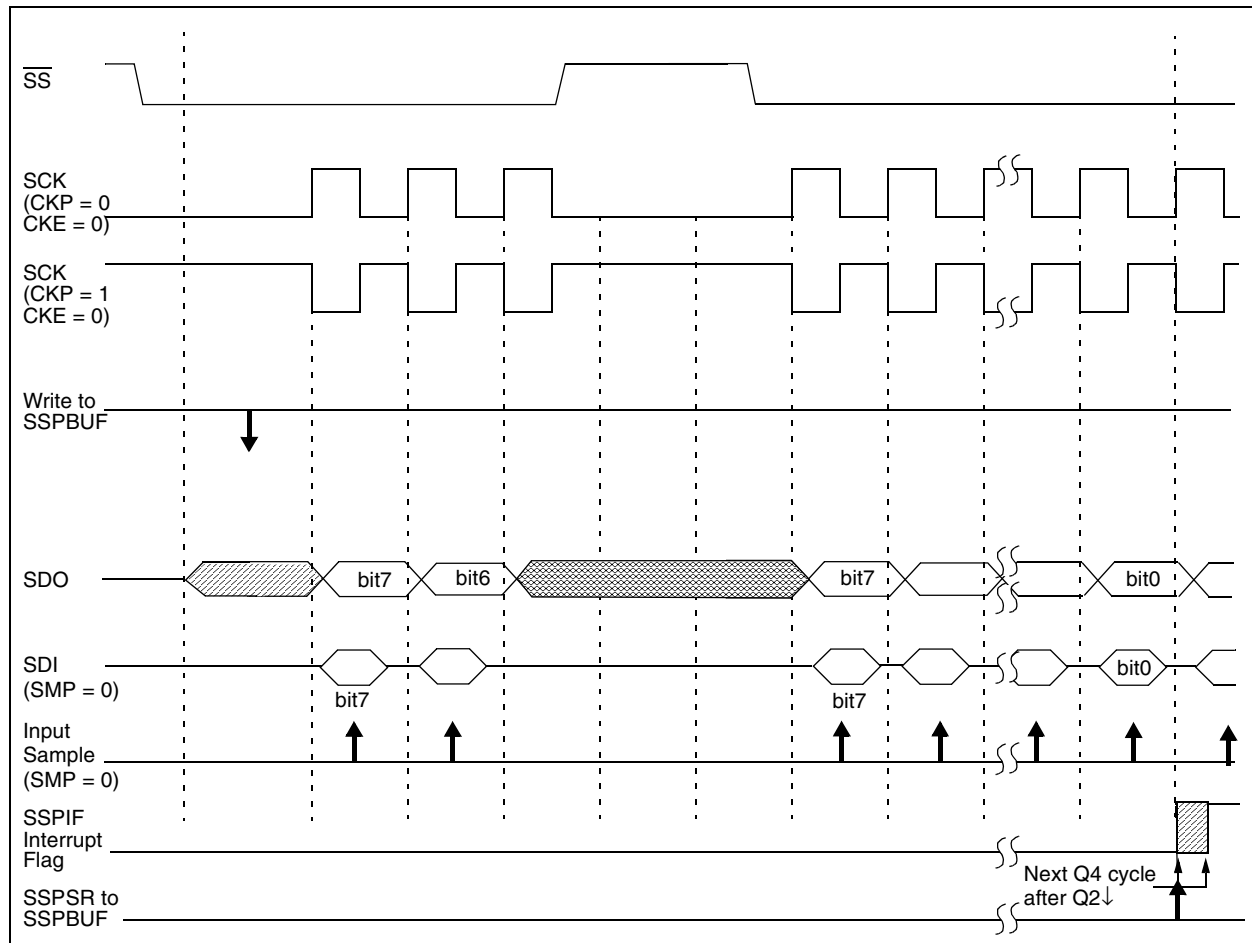
**Note 1:** When the SPI is in Slave mode with  $\overline{SS}$  pin control enabled ( $SSPCON<3:0> = 0100$ ), the SPI module will reset if the  $\overline{SS}$  pin is set to VDD.

**2:** If the SPI is used in Slave mode with CKE set, then the  $\overline{SS}$  pin control must be enabled.

When the SPI module resets, the bit counter is forced to 0. This can be done by either forcing the  $\overline{SS}$  pin to a high level or clearing the SSPEN bit.

To emulate two-wire communication, the SDO pin can be connected to the SDI pin. When the SPI needs to operate as a receiver the SDO pin can be configured as an input. This disables transmissions from the SDO. The SDI can always be left as an input (SDI function), since it cannot create a bus conflict.

**FIGURE 15-4: SLAVE SYNCHRONIZATION WAVEFORM**





# PIC18FXX2

## 15.4.5 GENERAL CALL ADDRESS SUPPORT

The addressing procedure for the I<sup>2</sup>C bus is such that the first byte after the START condition usually determines which device will be the slave addressed by the master. The exception is the general call address, which can address all devices. When this address is used, all devices should, in theory, respond with an Acknowledge.

The general call address is one of eight addresses reserved for specific purposes by the I<sup>2</sup>C protocol. It consists of all 0's with R/W = 0.

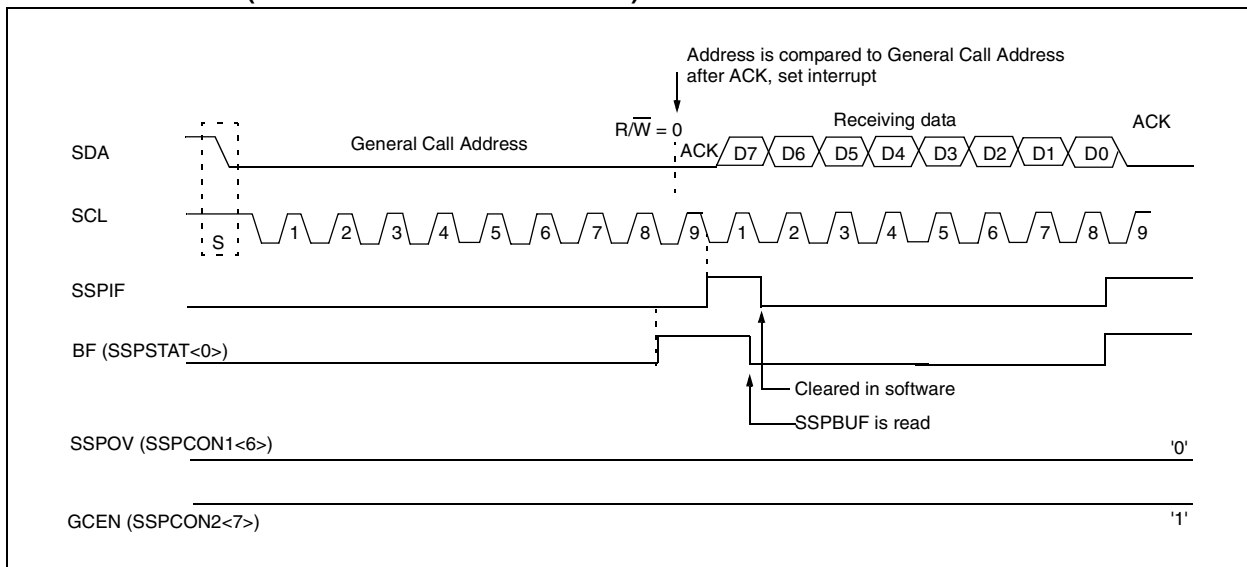
The general call address is recognized when the General Call Enable bit (GCEN) is enabled (SSPCON2<7> set). Following a START bit detect, 8-bits are shifted into the SSPSR and the address is compared against the SSPADD. It is also compared to the general call address and fixed in hardware.

If the general call address matches, the SSPSR is transferred to the SSPBUF, the BF flag bit is set (eighth bit), and on the falling edge of the ninth bit (ACK bit), the SSPIF interrupt flag bit is set.

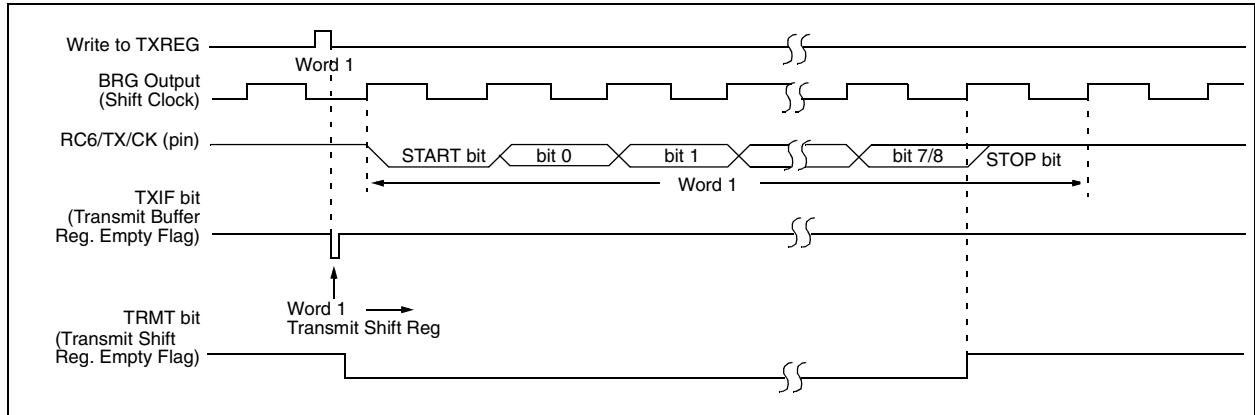
When the interrupt is serviced, the source for the interrupt can be checked by reading the contents of the SSPBUF. The value can be used to determine if the address was device specific or a general call address.

In 10-bit mode, the SSPADD is required to be updated for the second half of the address to match, and the UA bit is set (SSPSTAT<1>). If the general call address is sampled when the GCEN bit is set, while the slave is configured in 10-bit Address mode, then the second half of the address is not necessary, the UA bit will not be set, and the slave will begin receiving data after the Acknowledge (Figure 15-15).

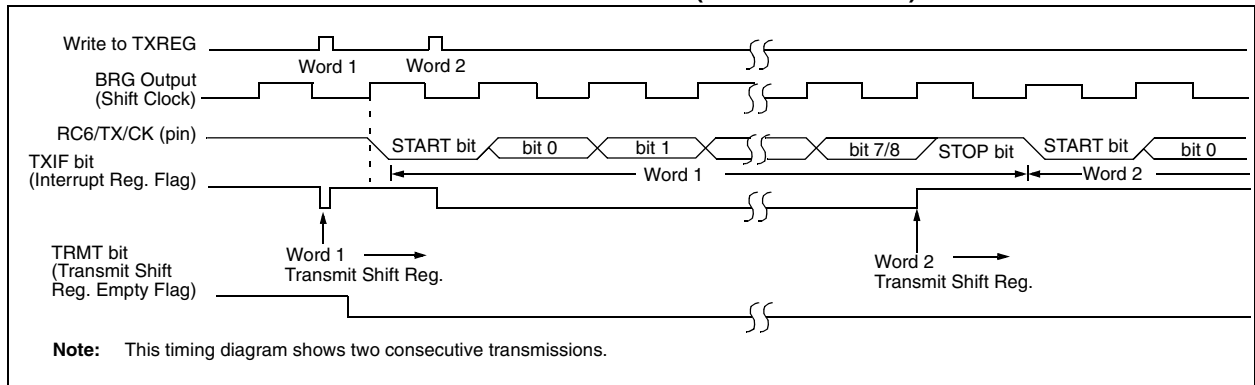
**FIGURE 15-15: SLAVE MODE GENERAL CALL ADDRESS SEQUENCE (7 OR 10-BIT ADDRESS MODE)**



**FIGURE 16-2: ASYNCHRONOUS TRANSMISSION**



**FIGURE 16-3: ASYNCHRONOUS TRANSMISSION (BACK TO BACK)**



**TABLE 16-6: REGISTERS ASSOCIATED WITH ASYNCHRONOUS TRANSMISSION**

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on All Other RESETS
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 000x	0000 000u
PIR1	PSPIF <sup>(1)</sup>	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
PIE1	PSPIE <sup>(1)</sup>	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
IPR1	PSPIP <sup>(1)</sup>	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	0000 0000	0000 0000
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 -00x	0000 -00x
TXREG	USART Transmit Register								0000 0000	0000 0000
TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
SPBRG	Baud Rate Generator Register								0000 0000	0000 0000

Legend: x = unknown, - = unimplemented locations read as '0'.

Shaded cells are not used for Asynchronous Transmission.

**Note 1:** The PSPIF, PSPIE and PSPIP bits are reserved on the PIC18F2X2 devices; always maintain these bits clear.

## 17.0 COMPATIBLE 10-BIT ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE

The Analog-to-Digital (A/D) converter module has five inputs for the PIC18F2X2 devices and eight for the PIC18F4X2 devices. This module has the ADCON0 and ADCON1 register definitions that are compatible with the mid-range A/D module.

The A/D allows conversion of an analog input signal to a corresponding 10-bit digital number.

The A/D module has four registers. These registers are:

- A/D Result High Register (ADRESH)
- A/D Result Low Register (ADRESL)
- A/D Control Register 0 (ADCON0)
- A/D Control Register 1 (ADCON1)

The ADCON0 register, shown in Register 17-1, controls the operation of the A/D module. The ADCON1 register, shown in Register 17-2, configures the functions of the port pins.

### REGISTER 17-1: ADCON0 REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/DONE	—	ADON
bit 7							bit 0

bit 7-6 **ADCS1:ADCS0:** A/D Conversion Clock Select bits (ADCON0 bits in **bold**)

ADCON1 <ADCS2>	ADCON0 <ADCS1:ADCS0>	Clock Conversion
0	<b>00</b>	Fosc/2
0	<b>01</b>	Fosc/8
0	<b>10</b>	Fosc/32
0	<b>11</b>	FRC (clock derived from the internal A/D RC oscillator)
1	<b>00</b>	Fosc/4
1	<b>01</b>	Fosc/16
1	<b>10</b>	Fosc/64
1	<b>11</b>	FRC (clock derived from the internal A/D RC oscillator)

bit 5-3 **CHS2:CHS0:** Analog Channel Select bits

000 = channel 0, (AN0)  
 001 = channel 1, (AN1)  
 010 = channel 2, (AN2)  
 011 = channel 3, (AN3)  
 100 = channel 4, (AN4)  
 101 = channel 5, (AN5)  
 110 = channel 6, (AN6)  
 111 = channel 7, (AN7)

**Note:** The PIC18F2X2 devices do not implement the full 8 A/D channels; the unimplemented selections are reserved. Do not select any unimplemented channel.

bit 2 **GO/DONE:** A/D Conversion Status bit

When ADON = 1:

1 = A/D conversion in progress (setting this bit starts the A/D conversion which is automatically cleared by hardware when the A/D conversion is complete)  
 0 = A/D conversion not in progress

bit 1 **Unimplemented:** Read as '0'

bit 0 **ADON:** A/D On bit

1 = A/D converter module is powered up  
 0 = A/D converter module is shut-off and consumes no operating current

Legend:

R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '0'  
 - n = Value at POR      '1' = Bit is set      '0' = Bit is cleared      x = Bit is unknown

# PIC18FXX2

## 17.2 Selecting the A/D Conversion Clock

The A/D conversion time per bit is defined as TAD. The A/D conversion requires 12 TAD per 10-bit conversion. The source of the A/D conversion clock is software selectable. The seven possible options for TAD are:

- 2 TOSC
- 4 TOSC
- 8 TOSC
- 16 TOSC
- 32 TOSC
- 64 TOSC
- Internal A/D module RC oscillator (2-6  $\mu$ s)

For correct A/D conversions, the A/D conversion clock (TAD) must be selected to ensure a minimum TAD time of 1.6  $\mu$ s.

Table 17-1 shows the resultant TAD times derived from the device operating frequencies and the A/D clock source selected.

## 17.3 Configuring Analog Port Pins

The ADCON1, TRISA and TRISE registers control the operation of the A/D port pins. The port pins that are desired as analog inputs, must have their corresponding TRIS bits set (input). If the TRIS bit is cleared (output), the digital output level (VOH or VOL) will be converted.

The A/D operation is independent of the state of the CHS2:CHS0 bits and the TRIS bits.

**Note 1:** When reading the port register, all pins configured as analog input channels will read as cleared (a low level). Pins configured as digital inputs will convert an analog input. Analog levels on a digitally configured input will not affect the conversion accuracy.

**2:** Analog levels on any pin that is defined as a digital input (including the AN4:AN0 pins) may cause the input buffer to consume current that is out of the device's specification.

**TABLE 17-1: TAD vs. DEVICE OPERATING FREQUENCIES**

AD Clock Source (TAD)		Maximum Device Frequency	
Operation	ADCS2:ADCS0	PIC18FXX2	PIC18LFX2
2 TOSC	000	1.25 MHz	666 kHz
4 TOSC	100	2.50 MHz	1.33 MHz
8 TOSC	001	5.00 MHz	2.67 MHz
16 TOSC	101	10.00 MHz	5.33 MHz
32 TOSC	010	20.00 MHz	10.67 MHz
64 TOSC	110	40.00 MHz	21.33 MHz
RC	011	—	—

CPFSGT		Compare f with W, skip if f > W							
Syntax:	[ label ] CPFSGT f [,a]								
Operands:	0 ≤ f ≤ 255 a ∈ [0,1]								
Operation:	(f) – (W), skip if (f) > (W) (unsigned comparison)								
Status Affected:	None								
Encoding:	<table border="1"><tr><td>0110</td><td>010a</td><td>ffff</td><td>ffff</td></tr></table>					0110	010a	ffff	ffff
0110	010a	ffff	ffff						
Description:	<p>Compares the contents of data memory location 'f' to the contents of the W by performing an unsigned subtraction.</p> <p>If the contents of 'f' are greater than the contents of WREG, then the fetched instruction is discarded and a NOP is executed instead, making this a two-cycle instruction. If 'a' is 0, the Access Bank will be selected, overriding the BSR value. If 'a' = 1, then the bank will be selected as per the BSR value (default).</p>								
Words:	1								
Cycles:	1(2)								
	<b>Note:</b> 3 cycles if skip and followed by a 2-word instruction.								

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	No operation

If skip:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation

If skip and followed by 2-word instruction:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation
No operation	No operation	No operation	No operation

**Example:**

```

HERE      CPFSGT REG, 0
NGREATER  :
GREATER   :
```

Before Instruction

```

PC      = Address (HERE)
W       = ?
```

After Instruction

```

If REG > W;
PC      = Address (GREATER)
If REG ≤ W;
PC      = Address (NGREATER)
```

CPFSLT	Compare f with W, skip if f < W				
Syntax:	[ label ] CPFSLT f [,a]				
Operands:	$0 \leq f \leq 255$ $a \in [0,1]$				
Operation:	(f) – (W), skip if (f) < (W) (unsigned comparison)				
Status Affected:	None				
Encoding:	<table border="1"><tr><td>0110</td><td>000a</td><td>ffff</td><td>ffff</td></tr></table>	0110	000a	ffff	ffff
0110	000a	ffff	ffff		
Description:	<p>Compares the contents of data memory location 'f' to the contents of W by performing an unsigned subtraction.</p> <p>If the contents of 'f' are less than the contents of W, then the fetched instruction is discarded and a NOP is executed instead, making this a two-cycle instruction. If 'a' is 0, the Access Bank will be selected. If 'a' is 1, the BSR will not be overridden (default).</p>				
Words:	1				
Cycles:	1(2) <b>Note:</b> 3 cycles if skip and followed by a 2-word instruction.				

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	No operation

If skip:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation

If skip and followed by 2-word instruction:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation
No operation	No operation	No operation	No operation

**Example:**

```

HERE      CPFSLT REG, 1
NLESS    :
LESS     :
```

Before Instruction

```

PC      = Address (HERE)
W       = ?
```

After Instruction

```

If REG < W;
PC      = Address (LESS)
If REG ≥ W;
PC      = Address (NLESS)
```

LFSR	Load FSR								
Syntax:	[ <i>label</i> ] LFSR f,k								
Operands:	$0 \leq f \leq 2$ $0 \leq k \leq 4095$								
Operation:	$k \rightarrow \text{FSRf}$								
Status Affected:	None								
Encoding:	<table><tr><td>1110</td><td>1110</td><td>00ff</td><td><math>k_{11}kkk</math></td></tr><tr><td>1111</td><td>0000</td><td><math>k_7kkk</math></td><td>kkkk</td></tr></table>	1110	1110	00ff	$k_{11}kkk$	1111	0000	$k_7kkk$	kkkk
1110	1110	00ff	$k_{11}kkk$						
1111	0000	$k_7kkk$	kkkk						
Description:	The 12-bit literal 'k' is loaded into the file select register pointed to by 'f'.								
Words:	2								
Cycles:	2								
Q Cycle Activity:									

Q1	Q2	Q3	Q4
Decode	Read literal 'k' MSB	Process Data	Write literal 'k' MSB to FSRfH
Decode	Read literal 'k' LSB	Process Data	Write literal 'k' to FSRfL

**Example:** LFSR 2, 0x3AB

After Instruction

FSR2H = 0x03  
FSR2L = 0xAB

MOVF		Move f								
Syntax:	[ <i>label</i> ]    MOVF    f [,d [,a]]									
Operands:	$0 \leq f \leq 255$ $d \in [0,1]$ $a \in [0,1]$									
Operation:	$f \rightarrow \text{dest}$									
Status Affected:	N, Z									
Encoding:	<table border="1"><tr><td>0101</td><td>00da</td><td>ffff</td><td>ffff</td></tr></table>						0101	00da	ffff	ffff
0101	00da	ffff	ffff							
Description:	<p>The contents of register 'f' are moved to a destination dependent upon the status of 'd'. If 'd' is 0, the result is placed in W. If 'd' is 1, the result is placed back in register 'f' (default). Location 'f' can be anywhere in the 256 byte bank. If 'a' is 0, the Access Bank will be selected, overriding the BSR value. If 'a' = 1, then the bank will be selected as per the BSR value (default).</p>									
Words:	1									
Cycles:	1									
Q Cycle Activity:										

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write W

**Example:** MOVF REG, 0, 0

Before Instruction

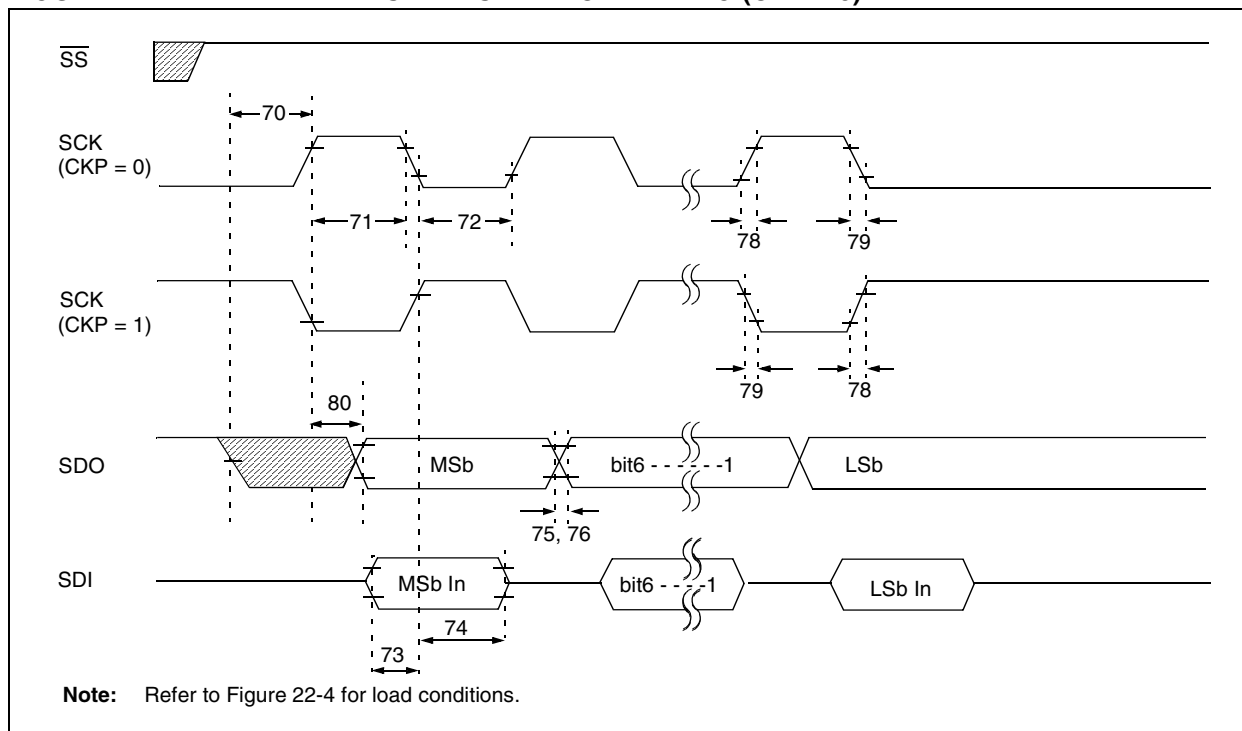
REG = 0x22  
W = 0xFF

After Instruction

REG = 0x22  
W = 0x22

# PIC18FXX2

**FIGURE 22-12: EXAMPLE SPI MASTER MODE TIMING (CKE = 0)**



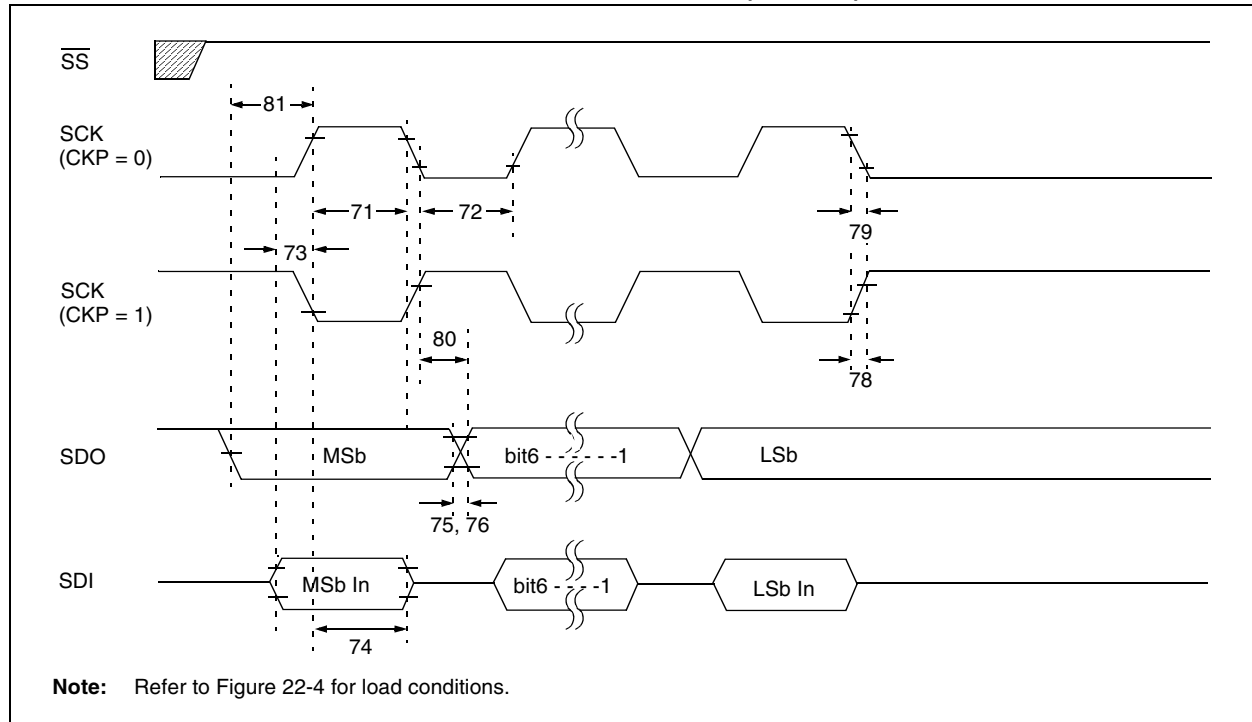
**TABLE 22-11: EXAMPLE SPI MODE REQUIREMENTS (MASTER MODE, CKE = 0)**

Param. No.	Symbol	Characteristic		Min	Max	Units	Conditions
70	TssL2scH, TssL2scL	SS↓ to SCK↓ or SCK↑ input		T <sub>CY</sub>	—	ns	
71	TscH	SCK input high time (Slave mode)	Continuous	1.25 T <sub>CY</sub> + 30	—	ns	
71A			Single Byte	40	—	ns	(Note 1)
72	TscL	SCK input low time (Slave mode)	Continuous	1.25 T <sub>CY</sub> + 30	—	ns	
72A			Single Byte	40	—	ns	(Note 1)
73	TdiV2scH, TdiV2scL	Setup time of SDI data input to SCK edge		100	—	ns	
73A	Tb2B	Last clock edge of Byte1 to the 1st clock edge of Byte2		1.5 T <sub>CY</sub> + 40	—	ns	(Note 2)
74	TscH2diL, TscL2diL	Hold time of SDI data input to SCK edge		100	—	ns	
75	TdoR	SDO data output rise time	PIC18FXXX	—	25	ns	
			PIC18LFXXX	—	60	ns	V <sub>DD</sub> = 2V
76	TdoF	SDO data output fall time	PIC18FXXX	—	25	ns	
			PIC18LFXXX	—	60	ns	V <sub>DD</sub> = 2V
78	TscR	SCK output rise time (Master mode)	PIC18FXXX	—	25	ns	
			PIC18LFXXX	—	60	ns	V <sub>DD</sub> = 2V
79	TscF	SCK output fall time (Master mode)	PIC18FXXX	—	25	ns	
			PIC18LFXXX	—	60	ns	V <sub>DD</sub> = 2V
80	TscH2doV, TscL2doV	SDO data output valid after SCK edge	PIC18FXXX	—	50	ns	
			PIC18LFXXX	—	150	ns	V <sub>DD</sub> = 2V

**Note 1:** Requires the use of Parameter # 73A.

**Note 2:** Only if Parameter # 71A and # 72A are used.

**FIGURE 22-13: EXAMPLE SPI MASTER MODE TIMING (CKE = 1)**



**TABLE 22-12: EXAMPLE SPI MODE REQUIREMENTS (MASTER MODE, CKE = 1)**

Param. No.	Symbol	Characteristic	Min	Max	Units	Conditions
71	TscH	SCK input high time	1.25 Tcy + 30	—	ns	
71A		(Slave mode)				
		Continuous	40	—	ns	(Note 1)
		Single Byte	40	—	ns	(Note 1)
72	TscL	SCK input low time	1.25 Tcy + 30	—	ns	
72A		(Slave mode)				
		Continuous	40	—	ns	(Note 1)
		Single Byte	40	—	ns	(Note 1)
73	TdiV2scH, TdiV2scL	Setup time of SDI data input to SCK edge	100	—	ns	
73A	Tb2B	Last clock edge of Byte1 to the 1st clock edge of Byte2	1.5 Tcy + 40	—	ns	(Note 2)
74	Tsch2diL, TscL2diL	Hold time of SDI data input to SCK edge	100	—	ns	
75	TdoR	SDO data output rise time	—	25	ns	
		PIC18FXXX	—	60	ns	VDD = 2V
		PIC18LFXXX	—	60	ns	VDD = 2V
76	TdoF	SDO data output fall time	—	25	ns	
		PIC18FXXX	—	60	ns	VDD = 2V
		PIC18LFXXX	—	60	ns	VDD = 2V
78	TscR	SCK output rise time (Master mode)	—	25	ns	
		PIC18FXXX	—	60	ns	VDD = 2V
		PIC18LFXXX	—	60	ns	VDD = 2V
79	TscF	SCK output fall time (Master mode)	—	25	ns	
		PIC18FXXX	—	60	ns	VDD = 2V
		PIC18LFXXX	—	60	ns	VDD = 2V
80	Tsch2doV, TscL2doV	SDO data output valid after SCK edge	—	50	ns	
		PIC18FXXX	—	150	ns	VDD = 2V
		PIC18LFXXX	—	150	ns	VDD = 2V
81	TdoV2scH, TdoV2scL	SDO data output setup to SCK edge	Tcy	—	ns	

**Note 1:** Requires the use of Parameter # 73A.

**Note 2:** Only if Parameter # 71A and # 72A are used.



# PIC18FXX2

FIGURE 22-16: I<sup>2</sup>C BUS START/STOP BITS TIMING

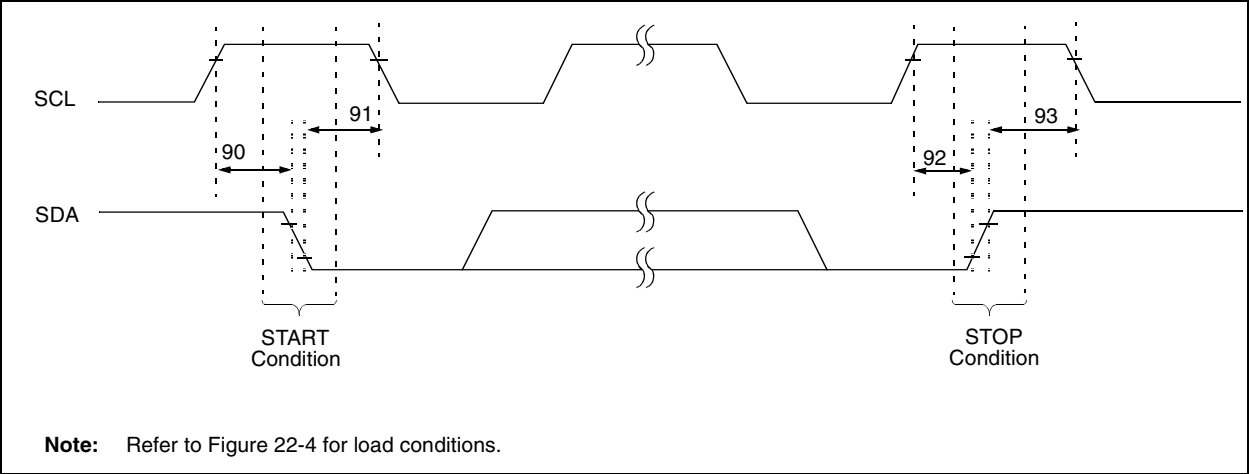
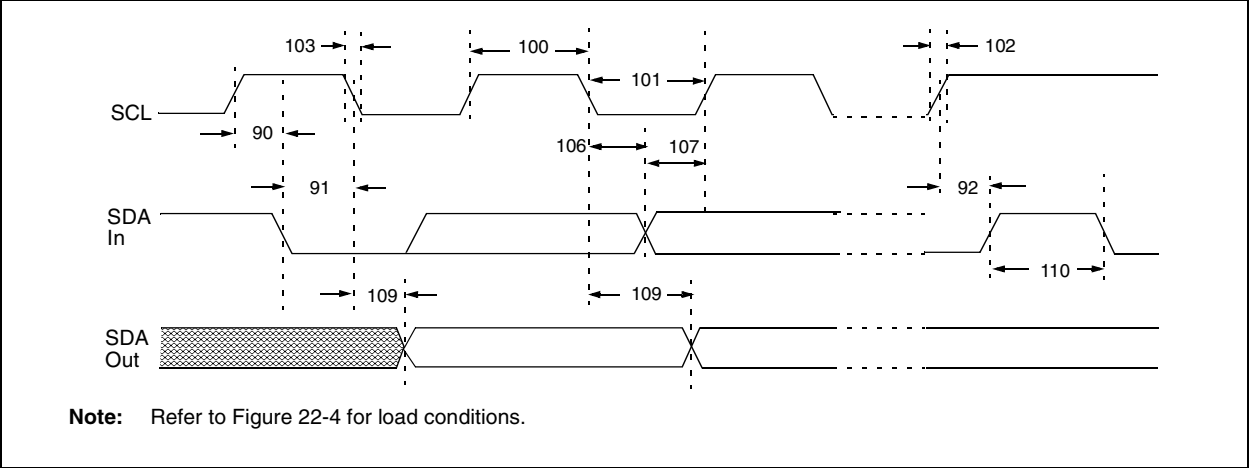


TABLE 22-15: I<sup>2</sup>C BUS START/STOP BITS REQUIREMENTS (SLAVE MODE)

Param. No.	Symbol	Characteristic		Min	Max	Units	Conditions
90	TSU:STA	START condition	100 kHz mode	4700	—	ns	Only relevant for Repeated START condition
		Setup time	400 kHz mode	600	—		
91	THD:STA	START condition	100 kHz mode	4000	—	ns	After this period, the first clock pulse is generated
		Hold time	400 kHz mode	600	—		
92	TSU:STO	STOP condition	100 kHz mode	4700	—	ns	
		Setup time	400 kHz mode	600	—		
93	THD:STO	STOP condition	100 kHz mode	4000	—	ns	
		Hold time	400 kHz mode	600	—		

FIGURE 22-17: I<sup>2</sup>C BUS DATA TIMING



# PIC18FXX2

TBLRD .....	249
TBLWT .....	250
TSTFSZ .....	251
XORLW .....	251
XORWF .....	252
Summary Table .....	214
Instructions in Program Memory .....	40
Two-Word Instructions .....	41
INT Interrupt (RB0/INT). <i>See</i> Interrupt Sources	
INTCON Register	
RBIF Bit .....	90
INTCON Registers .....	75–77
Inter-Integrated Circuit. <i>See</i> I <sup>2</sup> C	
Interrupt Sources .....	195
A/D Conversion Complete .....	184
Capture Complete (CCP) .....	119
Compare Complete (CCP) .....	120
INT0 .....	85
Interrupt-on-Change (RB7:RB4) .....	90
PORTB, Interrupt-on-Change .....	85
RB0/INT Pin, External .....	85
TMR0 .....	85
TMR0 Overflow .....	105
TMR1 Overflow .....	107, 109
TMR2 to PR2 Match .....	112
TMR2 to PR2 Match (PWM) .....	111, 122
TMR3 Overflow .....	113, 115
USART Receive/Transmit Complete .....	165
Interrupts .....	73
Logic .....	74
Interrupts, Enable Bits	
CCP1 Enable (CCP1IE Bit) .....	119
Interrupts, Flag Bits	
A/D Converter Flag (ADIF Bit) .....	183
CCP1 Flag (CCP1IF Bit) .....	119
CCP1IF Flag (CCP1IF Bit) .....	120
Interrupt-on-Change (RB7:RB4) Flag (RBIF Bit) .....	90
IORLW .....	234
IORWF .....	234
IPR Registers .....	82–83
<b>K</b>	
KEELOQ Evaluation and Programming Tools .....	256
<b>L</b>	
LFSR .....	235
Lookup Tables	
Computed GOTO .....	41
Table Reads, Table Writes .....	41
Low Voltage Detect .....	189
Converter Characteristics .....	267
Effects of a RESET .....	193
Operation .....	192
Current Consumption .....	193
During SLEEP .....	193
Reference Voltage Set Point .....	193
Typical Application .....	189
LVD. <i>See</i> Low Voltage Detect. ....	189

## M

Master SSP (MSSP) Module Overview .....	125
Master Synchronous Serial Port (MSSP). <i>See</i> MSSP.	
Master Synchronous Serial Port. <i>See</i> MSSP	
Memory Organization	
Data Memory .....	42
Program Memory .....	35
Memory Programming Requirements .....	268
Migration from Baseline to Enhanced Devices .....	314
Migration from High-End to Enhanced Devices .....	315
Migration from Mid-Range to Enhanced Devices .....	315
MOVF .....	235
MOVFF .....	236
MOVLB .....	236
MOVLW .....	237
MOVWF .....	237
MPLAB C17 and MPLAB C18 C Compilers .....	253
MPLAB ICD In-Circuit Debugger .....	255
MPLAB ICE High Performance Universal In-Circuit Emulator with MPLAB IDE .....	254
MPLAB Integrated Development Environment Software .....	253
MPLINK Object Linker/MPLIB Object Librarian .....	254
MSSP .....	125
Control Registers (general) .....	125
Enabling SPI I/O .....	129
Operation .....	128
Typical Connection .....	129
MSSP Module	
SPI Master Mode .....	130
SPI Master./Slave Connection .....	129
SPI Slave Mode .....	131
MULLW .....	238
MULWF .....	238

## N

NEGF .....	239
NOP .....	239

## O

Opcode Field Descriptions .....	212
OPTION_REG Register	
PSA Bit .....	105
T0CS Bit .....	105
T0PS2:T0PS0 Bits .....	105
T0SE Bit .....	105
Oscillator Configuration .....	17
EC .....	17
ECIO .....	17
HS .....	17
HS + PLL .....	17
LP .....	17
RC .....	17
RCIO .....	17
XT .....	17
Oscillator Selection .....	195
Oscillator, Timer1 .....	107, 109, 115
Oscillator, Timer3 .....	113
Oscillator, WDT .....	203

# PIC18FXX2

## PORTE

Analog Port Pins .....	99, 100
Associated Registers .....	99
LATE Register .....	97
PORTE Register .....	97
PSP Mode Select (PSPMODE Bit) .....	95, 100
RE0/RD/AN5 Pin .....	99, 100
RE1/WR/AN6 Pin .....	99, 100
RE2/CS/AN7 Pin .....	99, 100
TRISE Register .....	97

## Postscaler, WDT

Assignment (PSA Bit) .....	105
Rate Select (T0PS2:T0PS0 Bits) .....	105
Switching Between Timer0 and WDT .....	105

## Power-down Mode. *See* SLEEP

Power-on Reset (POR) .....	26
Oscillator Start-up Timer (OST) .....	26
Power-up Timer (PWRT) .....	26

## Prescaler, Capture ..... 119 |

Prescaler, Timer0 .....	105
Assignment (PSA Bit) .....	105
Rate Select (T0PS2:T0PS0 Bits) .....	105
Switching Between Timer0 and WDT .....	105

## Prescaler, Timer2 ..... 122 |

## PRO MATE II Universal Device Programmer ..... 255 |

## Product Identification System ..... 327 |

## Program Counter

PCL Register .....	39
PCLATH Register .....	39
PCLATU Register .....	39

## Program Memory

Interrupt Vector .....	35
Map and Stack for PIC18F442/242 .....	36
Map and Stack for PIC18F452/252 .....	36
RESET Vector .....	35

## Program Verification and Code Protection ..... 207 |

## Associated Registers ..... 207 |

## Programming, Device Instructions ..... 211 |

## PSP. *See* Parallel Slave Port.

## Pulse Width Modulation. *See* PWM (CCP Module).

## PUSH ..... 240 |

## PWM (CCP Module) ..... 122 |

Associated Registers .....	123
CCPR1H:CCPR1L Registers .....	122
Duty Cycle .....	122
Example Frequencies/Resolutions .....	123
Period .....	122
Setup for PWM Operation .....	123
TMR2 to PR2 Match .....	111, 122

## Q

Q Clock .....	122
---------------	-----

## R

## RAM. *See* Data Memory

## RC Oscillator ..... 18 |

## RCALL ..... 241 |

## RCSTA Register

SPEN Bit .....	165
----------------	-----

## Register File ..... 42 |

## Registers

ADCON0 (A/D Control 0) .....	181
ADCON1 (A/D Control 1) .....	182
CCP1CON and CCP2CON (Capture/Compare/PWM Control) .....	117
CONFIG1H (Configuration 1 High) .....	196
CONFIG2H (Configuration 2 High) .....	197
CONFIG2L (Configuration 2 Low) .....	197
CONFIG3H (Configuration 3 High) .....	198
CONFIG4L (Configuration 4 Low) .....	198
CONFIG5H (Configuration 5 High) .....	199
CONFIG5L (Configuration 5 Low) .....	199
CONFIG6H (Configuration 6 High) .....	200
CONFIG6L (Configuration 6 Low) .....	200
CONFIG7H (Configuration 7 High) .....	201
CONFIG7L (Configuration 7 Low) .....	201
DEVID1 (Device ID Register 1) .....	202
DEVID2 (Device ID Register 2) .....	202
EECON1 (Data EEPROM Control 1) .....	57, 66
File Summary .....	46–48
INTCON (Interrupt Control) .....	75
INTCON2 (Interrupt Control 2) .....	76
INTCON3 (Interrupt Control 3) .....	77
IPR1 (Peripheral Interrupt Priority 1) .....	82
IPR2 (Peripheral Interrupt Priority 2) .....	83
LVDCON (LVD Control) .....	191
OSCCON (Oscillator Control) .....	21
PIE1 (Peripheral Interrupt Enable 1) .....	80
PIE2 (Peripheral Interrupt Enable 2) .....	81
PIR1 (Peripheral Interrupt Request 1) .....	78
PIR2 (Peripheral Interrupt Request 2) .....	79
RCON (Register Control) .....	84
RCON (RESET Control) .....	53
RCSTA (Receive Status and Control) .....	167
SSPCON1 (MSSP Control 1) I <sup>2</sup> C Mode .....	136
SPI Mode .....	127
SSPCON2 (MSSP Control 2) I <sup>2</sup> C Mode .....	137
SSPSTAT (MSSP Status) I <sup>2</sup> C Mode .....	135
SPI Mode .....	126
STATUS .....	52
STKPTR (Stack Pointer) .....	38
T0CON (Timer0 Control) .....	103
T1CON (Timer 1 Control) .....	107
T2CON (Timer 2 Control) .....	111
T3CON (Timer3 Control) .....	113
TRISE .....	98
TXSTA (Transmit Status and Control) .....	166
WDTCON (Watchdog Timer Control) .....	203
RESET .....	25, 195, 241
Brown-out Reset (BOR) .....	195
MCLR Reset (During SLEEP) .....	25
MCLR Reset (Normal Operation) .....	25
Oscillator Start-up Timer (OST) .....	195
Power-on Reset (POR) .....	25, 195
Power-up Timer (PWRT) .....	195
Programmable Brown-out Reset (BOR) .....	25
RESET Instruction .....	25
Stack Full Reset .....	25
Stack Underflow Reset .....	25
Watchdog Timer (WDT) Reset .....	25

# PIC18FXX2

Example SPI Master Mode (CKE = 0)	278
Example SPI Master Mode (CKE = 1)	279
Example SPI Slave Mode (CKE = 0)	280
Example SPI Slave Mode (CKE = 1)	281
External Clock (All Modes except PLL)	271
First START Bit Timing	153
I <sup>2</sup> C Bus Data	282
I <sup>2</sup> C Bus START/STOP Bits	282
I <sup>2</sup> C Master Mode (Reception, 7-bit Address)	157
I <sup>2</sup> C Master Mode (Transmission, 7 or 10-bit Address)	156
I <sup>2</sup> C Slave Mode Timing (10-bit Reception, SEN = 0)	142
I <sup>2</sup> C Slave Mode Timing (10-bit Transmission)	143
I <sup>2</sup> C Slave Mode Timing (7-bit Reception, SEN = 0)	140
I <sup>2</sup> C Slave Mode Timing (7-bit Reception, SEN = 1)	146, 147
I <sup>2</sup> C Slave Mode Timing (7-bit Transmission)	141
Low Voltage Detect	192
Master SSP I <sup>2</sup> C Bus Data	284
Master SSP I <sup>2</sup> C Bus START/STOP Bits	284
Parallel Slave Port (PIC18F4X2)	277
Parallel Slave Port (Read)	101
Parallel Slave Port (Write)	100
PWM Output	122
Repeat START Condition	154
RESET, Watchdog Timer (WDT), Oscillator Start-up Timer (OST) and Power-up Timer (PWRT)	273
Slave Synchronization	131
Slaver Mode General Call Address Sequence (7 or 10-bit Address Mode)	148
Slow Rise Time (MCLR Tied to VDD)	33
SPI Mode (Master Mode)	130
SPI Mode (Slave Mode with CKE = 0)	132
SPI Mode (Slave Mode with CKE = 1)	132
Stop Condition Receive or Transmit Mode	158
Time-out Sequence on POR w/PLL Enabled (MCLR Tied to VDD)	33
Time-out Sequence on Power-up (MCLR Not Tied to VDD) Case 1	32
Case 2	32
Time-out Sequence on Power-up (MCLR Tied to VDD)	32
Timer0 and Timer1 External Clock	275
Timing for Transition Between Timer1 and OSC1 (HS with PLL)	23
Transition Between Timer1 and OSC1 (HS, XT, LP)	22
Transition Between Timer1 and OSC1 (RC, EC)	23
Transition from OSC1 to Timer1 Oscillator	22
USART Asynchronous Master Transmission	173
USART Asynchronous Master Transmission (Back to Back)	173
USART Asynchronous Reception	175
USART Synchronous Receive (Master/Slave)	286
USART Synchronous Reception (Master Mode, SREN)	178
USART Synchronous Transmission	177
USART Synchronous Transmission (Master/Slave)	286

USART Synchronous Transmission (Through TXEN)	177
Wake-up from SLEEP via Interrupt	206
Timing Diagrams Requirements Master SSP I <sup>2</sup> C Bus START/STOP Bits	284
Timing Requirements	
A/D Conversion	288
Capture/Compare/PWM (CCP1 and CCP2)	276
CLKO and I/O	273
Example SPI Mode (Master Mode, CKE = 0)	278
Example SPI Mode (Master Mode, CKE = 1)	279
Example SPI Mode (Slave Mode, CKE = 0)	280
Example SPI Slave Mode (CKE = 1)	281
External Clock	271
I <sup>2</sup> C Bus Data (Slave Mode)	283
Master SSP I <sup>2</sup> C Bus Data	285
Parallel Slave Port (PIC18F4X2)	277
RESET, Watchdog Timer, Oscillator Start-up Timer, Power-up Timer and Brown-out Reset Requirements	274
Timer0 and Timer1 External Clock	275
USART Synchronous Receive	286
USART Synchronous Transmission	286
Timing Specifications	
PLL Clock	272
TRISE Register	
PSPMODE Bit	95, 100
TSTFSZ	251
Two-Word Instructions Example Cases	41
TXSTA Register	
BRGH Bit	168

## U

Universal Synchronous Asynchronous Receiver Transmitter. See USART	
USART	165
Asynchronous Mode	172
Associated Registers, Receive	175
Associated Registers, Transmit	173
Receiver	174
Transmitter	172
Baud Rate Generator (BRG)	168
Associated Registers	168
Baud Rate Error, Calculating	168
Baud Rate Formula	168
Baud Rates for Asynchronous Mode (BRGH = 0)	170
Baud Rates for Asynchronous Mode (BRGH = 1)	171
Baud Rates for Synchronous Mode	169
High Baud Rate Select (BRGH Bit)	168
Sampling	168
Serial Port Enable (SPEN Bit)	165
Synchronous Master Mode	176
Associated Registers, Reception	178
Associated Registers, Transmit	176
Reception	178
Transmission	176
Synchronous Slave Mode	179
Associated Registers, Receive	180
Associated Registers, Transmit	179
Reception	180
Transmission	179



## WORLDWIDE SALES AND SERVICE

### AMERICAS

#### Corporate Office

2355 West Chandler Blvd.  
Chandler, AZ 85224-6199  
Tel: 480-792-7200  
Fax: 480-792-7277  
Technical Support:  
<http://support.microchip.com>  
Web Address:  
[www.microchip.com](http://www.microchip.com)

#### Atlanta

Alpharetta, GA  
Tel: 770-640-0034  
Fax: 770-640-0307

#### Boston

Westborough, MA  
Tel: 774-760-0087  
Fax: 774-760-0088

#### Chicago

Itasca, IL  
Tel: 630-285-0071  
Fax: 630-285-0075

#### Dallas

Addison, TX  
Tel: 972-818-7423  
Fax: 972-818-2924

#### Detroit

Farmington Hills, MI  
Tel: 248-538-2250  
Fax: 248-538-2260

#### Kokomo

Kokomo, IN  
Tel: 765-864-8360  
Fax: 765-864-8387

#### Los Angeles

Mission Viejo, CA  
Tel: 949-462-9523  
Fax: 949-462-9608

#### Santa Clara

Santa Clara, CA  
Tel: 408-961-6444  
Fax: 408-961-6445

#### Toronto

Mississauga, Ontario,  
Canada  
Tel: 905-673-0699  
Fax: 905-673-6509

### ASIA/PACIFIC

#### Asia Pacific Office

Suites 3707-14, 37th Floor  
Tower 6, The Gateway  
Harbour City, Kowloon  
Hong Kong  
Tel: 852-2401-1200  
Fax: 852-2401-3431

#### Australia - Sydney

Tel: 61-2-9868-6733  
Fax: 61-2-9868-6755

#### China - Beijing

Tel: 86-10-8528-2100  
Fax: 86-10-8528-2104

#### China - Chengdu

Tel: 86-28-8665-5511  
Fax: 86-28-8665-7889

#### China - Fuzhou

Tel: 86-591-8750-3506  
Fax: 86-591-8750-3521

#### China - Hong Kong SAR

Tel: 852-2401-1200  
Fax: 852-2401-3431

#### China - Qingdao

Tel: 86-532-8502-7355  
Fax: 86-532-8502-7205

#### China - Shanghai

Tel: 86-21-5407-5533  
Fax: 86-21-5407-5066

#### China - Shenyang

Tel: 86-24-2334-2829  
Fax: 86-24-2334-2393

#### China - Shenzhen

Tel: 86-755-8203-2660  
Fax: 86-755-8203-1760

#### China - Shunde

Tel: 86-757-2839-5507  
Fax: 86-757-2839-5571

#### China - Wuhan

Tel: 86-27-5980-5300  
Fax: 86-27-5980-5118

#### China - Xian

Tel: 86-29-8833-7250  
Fax: 86-29-8833-7256

### ASIA/PACIFIC

#### India - Bangalore

Tel: 91-80-4182-8400  
Fax: 91-80-4182-8422

#### India - New Delhi

Tel: 91-11-4160-8631  
Fax: 91-11-4160-8632

#### India - Pune

Tel: 91-20-2566-1512  
Fax: 91-20-2566-1513

#### Japan - Yokohama

Tel: 81-45-471- 6166  
Fax: 81-45-471-6122

#### Korea - Gumi

Tel: 82-54-473-4301  
Fax: 82-54-473-4302

#### Korea - Seoul

Tel: 82-2-554-7200  
Fax: 82-2-558-5932 or  
82-2-558-5934

#### Malaysia - Penang

Tel: 60-4-646-8870  
Fax: 60-4-646-5086

#### Philippines - Manila

Tel: 63-2-634-9065  
Fax: 63-2-634-9069

#### Singapore

Tel: 65-6334-8870  
Fax: 65-6334-8850

#### Taiwan - Hsin Chu

Tel: 886-3-572-9526  
Fax: 886-3-572-6459

#### Taiwan - Kaohsiung

Tel: 886-7-536-4818  
Fax: 886-7-536-4803

#### Taiwan - Taipei

Tel: 886-2-2500-6610  
Fax: 886-2-2508-0102

#### Thailand - Bangkok

Tel: 66-2-694-1351  
Fax: 66-2-694-1350

### EUROPE

#### Austria - Wels

Tel: 43-7242-2244-3910  
Fax: 43-7242-2244-393

#### Denmark - Copenhagen

Tel: 45-4450-2828  
Fax: 45-4485-2829

#### France - Paris

Tel: 33-1-69-53-63-20  
Fax: 33-1-69-30-90-79

#### Germany - Munich

Tel: 49-89-627-144-0  
Fax: 49-89-627-144-44

#### Italy - Milan

Tel: 39-0331-742611  
Fax: 39-0331-466781

#### Netherlands - Drunen

Tel: 31-416-690399  
Fax: 31-416-690340

#### Spain - Madrid

Tel: 34-91-708-08-90  
Fax: 34-91-708-08-91

#### UK - Wokingham

Tel: 44-118-921-5869  
Fax: 44-118-921-5820