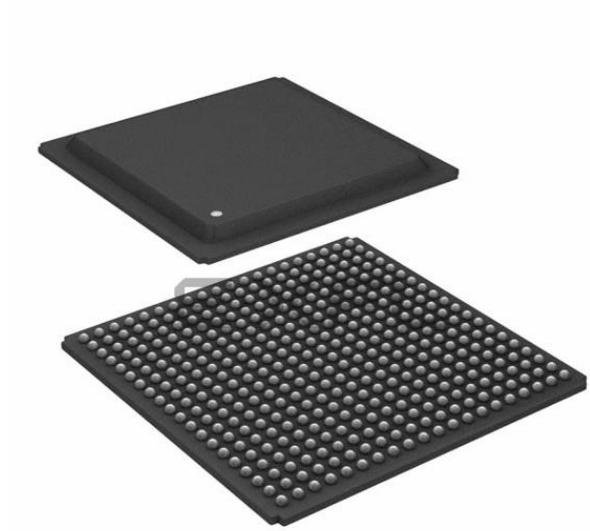

Welcome to E-XFL.COM

Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Floating Point
Interface	Host Interface, Link Port, Serial Port
Clock Rate	80MHz
Non-Volatile Memory	External
On-Chip RAM	512kB
Voltage - I/O	3.30V
Voltage - Core	2.50V
Operating Temperature	0°C ~ 85°C (TC)
Mounting Type	Surface Mount
Package / Case	400-BBGA
Supplier Device Package	400-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21160mkbz-80

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REVISION HISTORY

9/15—Rev. C to Rev. D

Removed model ADSP-21160NKB-100 (no longer available) from Ordering Guide 58

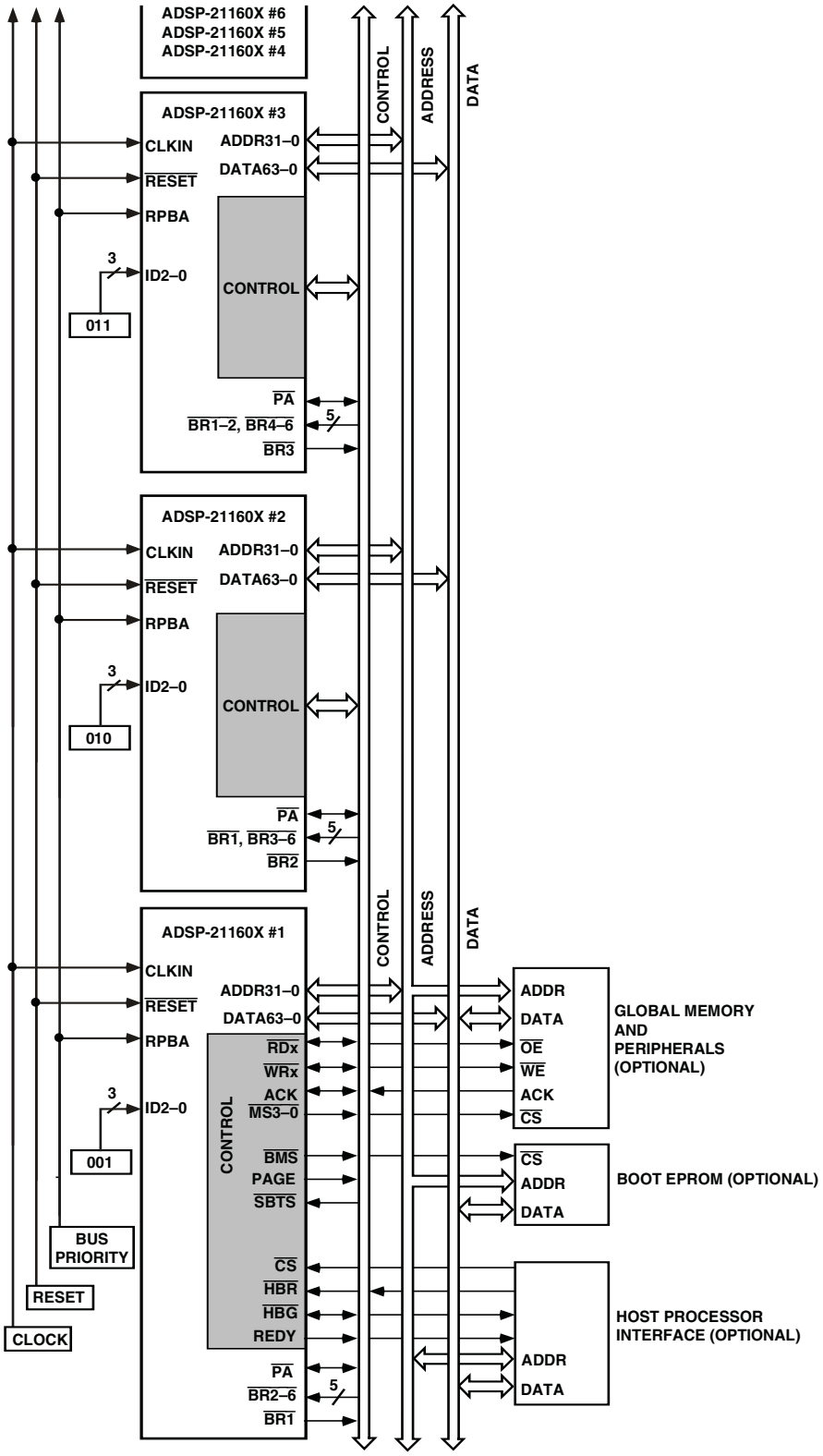

Figure 3. Shared Memory Multiprocessing System

located on the web page for the associated EZ-KIT or EZ-Extender product. The link is found in the *Product Download* area of the product web page.

Middleware Packages

Analog Devices separately offers middleware add-ins such as real time operating systems, file systems, USB stacks, and TCP/IP stacks. For more information, see the following web pages:

- www.analog.com/ucos3
- www.analog.com/ucfs
- www.analog.com/ucusbd
- www.analog.com/lwip

Algorithmic Modules

To speed development, Analog Devices offers add-ins that perform popular audio and video processing algorithms. These are available for use with both CrossCore Embedded Studio and VisualDSP++. For more information visit www.analog.com and search on "Blackfin software modules" or "SHARC software modules".

Designing an Emulator-Compatible DSP Board (Target)

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG Test Access Port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the processor's internal features via the processor's TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers. The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the DSP's JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see the application note (EE-68) "Analog Devices JTAG Emulation Technical Reference" (www.analog.com/ee-68). This document is updated regularly to keep pace with improvements to emulator support.

ADDITIONAL INFORMATION

This data sheet provides a general overview of the ADSP-21160x architecture and functionality. For detailed information on the Blackfin family core architecture and instruction set, refer to the *ADSP-21160 SHARC DSP Hardware Reference* and the *ADSP-21160 SHARC DSP Instruction Set Reference*. For detailed information on the development tools for this processor, see the *VisualDSP++ User's Guide*.

RELATED SIGNAL CHAINS

A signal chain is a series of signal conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next.

Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The application signal chains page in the Circuits from the Lab® site (http:\\www.analog.com\circuits) provides:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

PIN FUNCTION DESCRIPTIONS

ADSP-21160x pin definitions are listed below. Inputs identified as synchronous (S) must meet timing requirements with respect to CLKIN (or with respect to TCK for TMS, TDI). Inputs identified as asynchronous (A) can be asserted asynchronously to CLKIN (or to TCK for $\overline{\text{TRST}}$).

Tie or pull unused inputs to V_{DD} or GND, except for the following:

- ADDR31–0, DATA63–0, PAGE, BRST, CLKOUT (ID2–0 = 00x) (Note: These pins have a logic-level hold circuit enabled on the ADSP-21160x DSP with ID2–0 = 00x.)
- $\overline{\text{PA}}$, ACK, $\overline{\text{MS3–0}}$, $\overline{\text{RDx}}$, $\overline{\text{WRx}}$, $\overline{\text{CIF}}$, $\overline{\text{DMARx}}$, $\overline{\text{DMAGx}}$ (ID2–0 = 00x) (Note: These pins have a pull-up enabled on the ADSP-21160x with ID2–0 = 00x.)
- LxCLK, LxACK, LxDAT7–0 (LxPDRDE = 0) (Note: See Link Port Buffer Control Register Bit definitions in the *ADSP-21160 SHARC DSP Hardware Reference*.)
- DTx, DRx, TCLKx, RCLKx, $\overline{\text{EMU}}$, TMS, $\overline{\text{TRST}}$, TDI (Note: These pins have a pull-up.)

The following symbols appear in the Type column of Table 3: A = Asynchronous, G = Ground, I = Input, O = Output, P = Power Supply, S = Synchronous, (A/D) = Active Drive, (O/D) = Open Drain, and T = Three-State (when $\overline{\text{SBTS}}$ is asserted, or when the ADSP-21160x is a bus slave).

Table 3. Pin Function Descriptions

Pin	Type	Function
ADDR31–0	I/O/T	External Bus Address. The ADSP-21160x outputs addresses for external memory and peripherals on these pins. In a multiprocessor system, the bus master outputs addresses for read/writes of the internal memory or IOP registers of other ADSP-21160x DSPs. The ADSP-21160x inputs addresses when a host processor or multiprocessing bus master is reading or writing its internal memory or IOP registers. A keeper latch on the DSP's ADDR31–0 pins maintains the input at the level it was last driven (only enabled on the processor with ID2–0 = 00x).
DATA63–0	I/O/T	External Bus Data. The ADSP-21160x inputs and outputs data and instructions on these pins. Pull-up resistors on unused DATA pins are not necessary. A keeper latch on the DSP's DATA63-0 pins maintains the input at the level it was last driven (only enabled on the processor with ID2–0 = 00x).
$\overline{\text{MS3–0}}$	O/T	Memory Select Lines. These outputs are asserted (low) as chip selects for the corresponding banks of external memory. Memory bank size must be defined in the SYSCON control register. The $\overline{\text{MS3–0}}$ outputs are decoded memory address lines. In asynchronous access mode, the $\overline{\text{MS3–0}}$ outputs transition with the other address outputs. In synchronous access modes, the $\overline{\text{MS3–0}}$ outputs assert with the other address lines; however, they deassert after the first CLKIN cycle in which ACK is sampled asserted. $\overline{\text{MS3–0}}$ has a 20 kΩ internal pull-up resistor that is enabled on the ADSP-21160x with ID2–0 = 00x.
$\overline{\text{RDL}}$	I/O/T	Memory Read Low Strobe. $\overline{\text{RDL}}$ is asserted whenever ADSP-21160x reads from the low word of external memory or from the internal memory of other ADSP-21160x DSPs. External devices, including other ADSP-21160x DSPs, must assert $\overline{\text{RDL}}$ for reading from the low word of processor internal memory. In a multiprocessing system, $\overline{\text{RDL}}$ is driven by the bus master. $\overline{\text{RDL}}$ has a 20 kΩ internal pull-up resistor that is enabled on the processor with ID2–0 = 00x.
$\overline{\text{RDH}}$	I/O/T	Memory Read High Strobe. $\overline{\text{RDH}}$ is asserted whenever ADSP-21160x reads from the high word of external memory or from the internal memory of other ADSP-21160x DSPs. External devices, including other ADSP-21160x DSPs, must assert $\overline{\text{RDH}}$ for reading from the high word of ADSP-21160x internal memory. In a multiprocessing system, $\overline{\text{RDH}}$ is driven by the bus master. $\overline{\text{RDH}}$ has a 20 kΩ internal pull-up resistor that is enabled on the processor with ID2–0 = 00x.
$\overline{\text{WRL}}$	I/O/T	Memory Write Low Strobe. $\overline{\text{WRL}}$ is asserted when ADSP-21160x writes to the low word of external memory or internal memory of other ADSP-21160x DSPs. External devices must assert $\overline{\text{WRL}}$ for writing to ADSP-21160x DSP's low word of internal memory. In a multiprocessing system, $\overline{\text{WRL}}$ is driven by the bus master. $\overline{\text{WRL}}$ has a 20 kΩ internal pull-up resistor that is enabled on the processor with ID2–0 = 00x.
$\overline{\text{WRH}}$	I/O/T	Memory Write High Strobe. $\overline{\text{WRH}}$ is asserted when ADSP-21160x writes to the high word of external memory or internal memory of other ADSP-21160x DSPs. External devices must assert $\overline{\text{WRH}}$ for writing to ADSP-21160x DSP's high word of internal memory. In a multiprocessing system, $\overline{\text{WRH}}$ is driven by the bus master. $\overline{\text{WRH}}$ has a 20 kΩ internal pull-up resistor that is enabled on the processor with ID2–0 = 00x.

Table 3. Pin Function Descriptions (Continued)

Pin	Type	Function
PAGE	O/T	DRAM Page Boundary. The processor asserts this pin to an external DRAM controller, to signal that an external DRAM page boundary has been crossed. DRAM page size must be defined in the processor's memory control register (WAIT). DRAM can only be implemented in external memory Bank 0; the PAGE signal can only be activated for Bank 0 accesses. In a multiprocessing system, PAGE is output by the bus master. A keeper latch on the DSP's PAGE pin maintains the output at the level it was last driven (only enabled on the processor with ID2–0 = 00x).
BRST	I/O/T	Sequential Burst Access. BRST is asserted by ADSP-21160x or a host to indicate that data associated with consecutive addresses is being read or written. A slave device samples the initial address and increments an internal address counter after each transfer. The incremented address is not pipelined on the bus. If the burst access is a read from the host to the processor, the processor automatically increments the address as long as BRST is asserted. BRST is asserted after the initial access of a burst transfer. It is asserted for every cycle after that, except for the last data request cycle (denoted by $\overline{RDx}$ or $\overline{WRx}$ asserted and BRST negated). A keeper latch on the DSP's BRST pin maintains the input at the level it was last driven (only enabled on the processor with ID2–0 = 00x).
ACK	I/O/S	Memory Acknowledge. External devices can deassert ACK (low) to add wait states to an external memory access. ACK is used by I/O devices, memory controllers, or other peripherals to hold off completion of an external memory access. The ADSP-21160x deasserts ACK as an output to add wait states to a synchronous access of its internal memory, by a synchronous host or another DSP in a multiprocessor configuration. ACK has a 2 kΩ internal pull-up resistor that is enabled on the processor with ID2–0 = 00x.
$\overline{SBTS}$	I/S	Suspend Bus and Three-State. External devices can assert $\overline{SBTS}$ (low) to place the external bus address, data, selects, and strobes in a high-impedance state for the following cycle. If the ADSP-21160x attempts to access external memory while $\overline{SBTS}$ is asserted, the processor will halt and the memory access will not be completed until $\overline{SBTS}$ is deasserted. $\overline{SBTS}$ should only be used to recover from host processor and/or ADSP-21160x deadlock or used with a DRAM controller.
$\overline{IRQ2–0}$	I/A	Interrupt Request Lines. These are sampled on the rising edge of CLKIN and may be either edge-triggered or level-sensitive.
FLAG3–0	I/O/A	Flag Pins. Each is configured via control bits as either an input or output. As an input, it can be tested as a condition. As an output, it can be used to signal external peripherals.
TIMEXP	O	Timer Expired. Asserted for four processor core clock (CCLK) cycles when the timer is enabled and TCOUNT decrements to zero.
$\overline{HBR}$	I/A	Host Bus Request. Must be asserted by a host processor to request control of the ADSP-21160x DSP's external bus. When $\overline{HBR}$ is asserted in a multiprocessing system, the processor that is bus master will relinquish the bus and assert $\overline{HBG}$. To relinquish the bus, the processor places the address, data, select, and strobe lines in a high-impedance state. $\overline{HBR}$ has priority over all processor bus requests ($\overline{BR6–1}$) in a multiprocessing system.
$\overline{HBG}$	I/O	Host Bus Grant. Acknowledges an $\overline{HBR}$ bus request, indicating that the host processor may take control of the external bus. $\overline{HBG}$ is asserted (held low) by the ADSP-21160x until $\overline{HBR}$ is released. In a multiprocessing system, $\overline{HBG}$ is output by the processor bus master and is monitored by all others. After $\overline{HBR}$ is asserted, and before $\overline{HBG}$ is given, $\overline{HBG}$ will float for 1 t_{CLK} (1 CLKIN cycle). To avoid erroneous grants, $\overline{HBG}$ should be pulled up with a 20 kΩ to 50 kΩ external resistor.
$\overline{CS}$	I/A	Chip Select. Asserted by host processor to select the ADSP-21160x, for asynchronous transfer protocol.
REDY	O (O/D)	Host Bus Acknowledge. The ADSP-21160x deasserts REDY (low) to add wait states to an asynchronous host access when $\overline{CS}$ and $\overline{HBR}$ inputs are asserted.
$\overline{DMAR1}$	I/A	DMA Request 1 (DMA Channel 11). Asserted by external port devices to request DMA services. $\overline{DMAR1}$ has a 20 kΩ internal pull-up resistor that is enabled on the ADSP-21160x with ID2–0 = 00x.
$\overline{DMAR2}$	I/A	DMA Request 2 (DMA Channel 12). Asserted by external port devices to request DMA services. $\overline{DMAR2}$ has a 20 kΩ internal pull-up resistor that is enabled on the ADSP-21160x with ID2–0 = 00x.

Table 3. Pin Function Descriptions (Continued)

Pin	Type	Function
ID2–0	I	Multiprocessing ID. Determines which multiprocessing bus request ($\overline{BR1}$–$\overline{BR6}$) is used by the ADSP-21160x. ID = 001 corresponds to $\overline{BR1}$, ID = 010 corresponds to $\overline{BR2}$, and so on. Use ID = 000 or ID = 001 in single-processor systems. These lines are a system configuration selection which should be hardwired or only changed at reset.
$\overline{DMAG1}$	O/T	DMA Grant 1 (DMA Channel 11). Asserted by ADSP-21160x to indicate that the requested DMA starts on the next cycle. Driven by bus master only. $\overline{DMAG1}$ has a 20 kΩ internal pull-up resistor that is enabled on the ADSP-21160x with ID2–0 = 00x.
$\overline{DMAG2}$	O/T	DMA Grant 2 (DMA Channel 12). Asserted by ADSP-21160x to indicate that the requested DMA starts on the next cycle. Driven by bus master only. $\overline{DMAG2}$ has a 20 kΩ internal pull-up resistor that is enabled on the ADSP-21160x with ID2–0 = 00x.
$\overline{BR6–1}$	I/O/S	Multiprocessing Bus Requests. Used by multiprocessing ADSP-21160x DSPs to arbitrate for bus mastership. An ADSP-21160x only drives its own $\overline{BRx}$ line (corresponding to the value of its ID2–0 inputs) and monitors all others. In a multiprocessor system with less than six ADSP-21160x DSPs, the unused $\overline{BRx}$ pins should be pulled high; the processor's own $\overline{BRx}$ line must not be pulled high or low because it is an output.
RPBA	I/S	Rotating Priority Bus Arbitration Select. When RPBA is high, rotating priority for multiprocessor bus arbitration is selected. When RPBA is low, fixed priority is selected. This signal is a system configuration selection which must be set to the same value on every ADSP-21160x. If the value of RPBA is changed during system operation, it must be changed in the same CLKIN cycle on every processor.
$\overline{PA}$	I/O/T	Priority Access. Asserting its $\overline{PA}$ pin allows an ADSP-21160x bus slave to interrupt background DMA transfers and gain access to the external bus. $\overline{PA}$ is connected to all ADSP-21160x DSPs in the system. If access priority is not required in a system, the $\overline{PA}$ pin should be left unconnected. $\overline{PA}$ has a 20 kΩ internal pull-up resistor that is enabled on the ADSP-21160x with ID2–0 = 00x.
DTx	O	Data Transmit (Serial Ports 0, 1). Each DT pin has a 50 kΩ internal pull-up resistor.
DRx	I	Data Receive (Serial Ports 0, 1). Each DR pin has a 50 kΩ internal pull-up resistor.
TCLKx	I/O	Transmit Clock (Serial Ports 0, 1). Each TCLK pin has a 50 kΩ internal pull-up resistor.
RCLKx	I/O	Receive Clock (Serial Ports 0, 1). Each RCLK pin has a 50 kΩ internal pull-up resistor.
TFSx	I/O	Transmit Frame Sync (Serial Ports 0, 1).
RFSx	I/O	Receive Frame Sync (Serial Ports 0, 1).
LxDAT7–0	I/O	Link Port Data (Link Ports 0–5). Each LxDAT pin has a 50 kΩ internal pull-down resistor that is enabled or disabled by the LPDRD bit of the LCTL0–1 register.
LxCLK	I/O	Link Port Clock (Link Ports 0–5). Each LxCLK pin has a 50 kΩ internal pull-down resistor that is enabled or disabled by the LPDRD bit of the LCTL0–1 register.
LxACK	I/O	Link Port Acknowledge (Link Ports 0–5). Each LxACK pin has a 50 kΩ internal pull-down resistor that is enabled or disabled by the LPDRD bit of the LCOM register.
EBOOT	I	EPROM Boot Select. For a description of how this pin operates, see Table 4. This signal is a system configuration selection that should be hardwired.
LBOOT	I	Link Boot. For a description of how this pin operates, see Table 4. This signal is a system configuration selection that should be hardwired.
$\overline{BMS}$	I/O/T	Boot Memory Select. Serves as an output or input as selected with the EBOOT and LBOOT pins; see Table 4. This input is a system configuration selection that should be hardwired.
CLKIN	I	Local Clock In. CLKIN is the ADSP-21160x clock input. The ADSP-21160x external port cycles at the frequency of CLKIN. The instruction cycle rate is a multiple of the CLKIN frequency; it is programmable at power-up. CLKIN may not be halted, changed, or operated below the specified frequency.
CLK_CFG3–0	I	Core/CLKIN Ratio Control. ADSP-21160x core clock (instruction cycle) rate is equal to n x CLKIN where n is user-selectable to 2, 3, or 4, using the CLK_CFG3–0 inputs. For clock configuration definitions, see the *$\overline{RESET}$ & CLKIN* section of the *System Design* chapter of the *ADSP-21160 SHARC DSP Hardware Reference*.

Table 3. Pin Function Descriptions (Continued)

Pin	Type	Function
CLKOUT	O/T	Local Clock Out. CLKOUT is driven at the CLKIN frequency by the processor. This output can be three-stated by setting the COD bit in the SYSCON register. A keeper latch on the DSP's CLKOUT pin maintains the output at the level it was last driven (only enabled on the processor with ID2-0 = 00x). Do not use CLKOUT in multiprocessing systems; use CLKIN instead.
$\overline{\text{RESET}}$	I/A	Processor Reset. Resets the ADSP-21160x to a known state and begins execution at the program memory location specified by the hardware reset vector address. The $\overline{\text{RESET}}$ input must be asserted (low) at power-up.
TCK	I	Test Clock (JTAG). Provides a clock for JTAG boundary scan.
TMS	I/S	Test Mode Select (JTAG). Used to control the test state machine. TMS has a 20 kΩ internal pull-up resistor.
TDI	I/S	Test Data Input (JTAG). Provides serial data for the boundary scan logic. TDI has a 20 kΩ internal pull-up resistor.
TDO	O	Test Data Output (JTAG). Serial scan output of the boundary scan path.
$\overline{\text{TRST}}$	I/A	Test Reset (JTAG). Resets the test state machine. $\overline{\text{TRST}}$ must be asserted (pulsed low) after power-up or held low for proper operation of the ADSP-21160x. $\overline{\text{TRST}}$ has a 20 kΩ internal pull-up resistor.
$\overline{\text{EMU}}$	O (O/D)	Emulation Status. Must be connected to the ADSP-21160x emulator target board connector only. $\overline{\text{EMU}}$ has a 50 kΩ internal pull-up resistor.
$\overline{\text{CIF}}$	O/T	Core Instruction Fetch. Signal is active low when an external instruction fetch is performed. Driven by bus master only. Three-state when host is bus master. $\overline{\text{CIF}}$ has a 20 kΩ internal pull-up resistor that is enabled on the ADSP-21160x with ID2–0 = 00x.
V_{DDINT}	P	Core Power Supply. Nominally 2.5 V (ADSP-21160M) or 1.9 V (ADSP-21160N) dc and supplies the DSP's core processor
V_{DDEXT}	P	I/O Power Supply. Nominally 3.3 V dc.
AV_{DD}	P	Analog Power Supply. Nominally 2.5 V (ADSP-21160M) or 1.9 V (ADSP-21160N) dc and supplies the DSP's internal PLL (clock generator). This pin has the same specifications as V_{DDINT}, except that added filtering circuitry is required. For more information, see Power Supplies on page 9.
AGND	G	Analog Power Supply Return.
GND	G	Power Supply Return.
NC		Do Not Connect. Reserved pins that must be left open and unconnected.

Table 4. Boot Mode Selection

EBOOT	LBOOT	$\overline{\text{BMS}}$	Booting Mode
1	0	Output	EPROM (Connect $\overline{\text{BMS}}$ to EPROM chip select.)
0	0	1 (Input)	Host Processor
0	1	1 (Input)	Link Port
0	0	0 (Input)	No Booting. Processor executes from external memory.
0	1	0 (Input)	Reserved
1	1	x (Input)	Reserved

ABSOLUTE MAXIMUM RATINGS

Stresses at or above those listed in Table 9 (ADSP-21160M) and Table 10 (ADSP-21160N) may cause permanent damage to the product. These are stress ratings only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 9. Absolute Maximum Ratings—ADSP-21160M

Parameter	Rating
Internal (Core) Supply Voltage (V_{DDINT})	–0.3 V to +3.0 V
Analog (PLL) Supply Voltage (A_{VDD})	–0.3 V to +3.0 V
External (I/O) Supply Voltage (V_{DDEXT})	–0.3 V to +4.6 V
Input Voltage	–0.5 V to V_{DDEXT} + 0.5 V
Output Voltage Swing	–0.5 V to V_{DDEXT} + 0.5 V
Load Capacitance	200 pF
Storage Temperature Range	–65°C to +150°C

Table 10. Absolute Maximum Ratings—ADSP-21160N

Parameter	Rating
Internal (Core) Supply Voltage (V_{DDINT})	–0.3 V to +2.3 V
Analog (PLL) Supply Voltage (A_{VDD})	–0.3 V to +2.3 V
External (I/O) Supply Voltage (V_{DDEXT})	–0.3 V to +4.6 V
Input Voltage	–0.5 V to V_{DDEXT} + 0.5 V
Output Voltage Swing	–0.5 V to V_{DDEXT} + 0.5 V
Load Capacitance	200 pF
Storage Temperature Range	–65°C to +150°C

ESD SENSITIVITY

ESD (electrostatic discharge sensitive device)
Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PACKAGE INFORMATION

The information presented in Figure 7 provides details about the package branding for the ADSP-21160M/ADSP-21160N processor. For a complete listing of product availability, see Ordering Guide on Page 58.

Figure 7. Typical Package Brand

Table 11. Package Brand Information

Brand Key	Field Description
a	ADSP-21160 Model (M or N)
t	Temperature Range
pp	Package Type
Z	RoHS Compliant Designation
cc	See Ordering Guide
vvvvvv.x	Assembly Lot Code
n.n	Silicon Revision
#	RoHS Compliant Designation
yyww	Date Code

Table 12. Power-Up Sequencing

Parameter		Min	Max	Unit
Timing Requirements				
t_{RSTVDD}	$\overline{\text{RESET}}$ Low Before V_{DDINT}/V_{DDEXT} on	0		ns
$t_{IVDDEVDD}$	V_{DDINT} on Before V_{DDEXT}	– 50	+200	ms
t_{CLKVDD}	CLKIN Running After valid V_{DDINT}/V_{DDEXT}[1]	0	200	ms
t_{CLKRST}	CLKIN Valid Before $\overline{\text{RESET}}$ Deasserted	10[2]		µs
t_{PLLRST}	PLL Control Setup Before $\overline{\text{RESET}}$ Deasserted	20[3]		µs
Switching Characteristics				
$t_{CORERST}$	DSP Core Reset Deasserted After $\overline{\text{RESET}}$ Deasserted	$4096t_{CK}$[3, 4]		

[1] Valid V_{DDINT}/V_{DDEXT} assumes that the supplies are fully ramped to their V_{DDINT} and V_{DDEXT} rails. Voltage ramp rates can vary from microseconds to hundreds of milliseconds, depending on the design of the power supply subsystem.

[2] Assumes a stable CLKIN signal after meeting worst-case start-up timing of oscillators. Refer to your oscillator manufacturer's data sheet for start-up time.

[3] Based on CLKIN cycles.

[4] $\overline{\text{CORERST}}$ is an internal signal only. The 4096 cycle count is dependent on t_{SRST} specification. If setup time is not met, one additional CLKIN cycle may be added to the core reset time, resulting in 4097 cycles maximum.

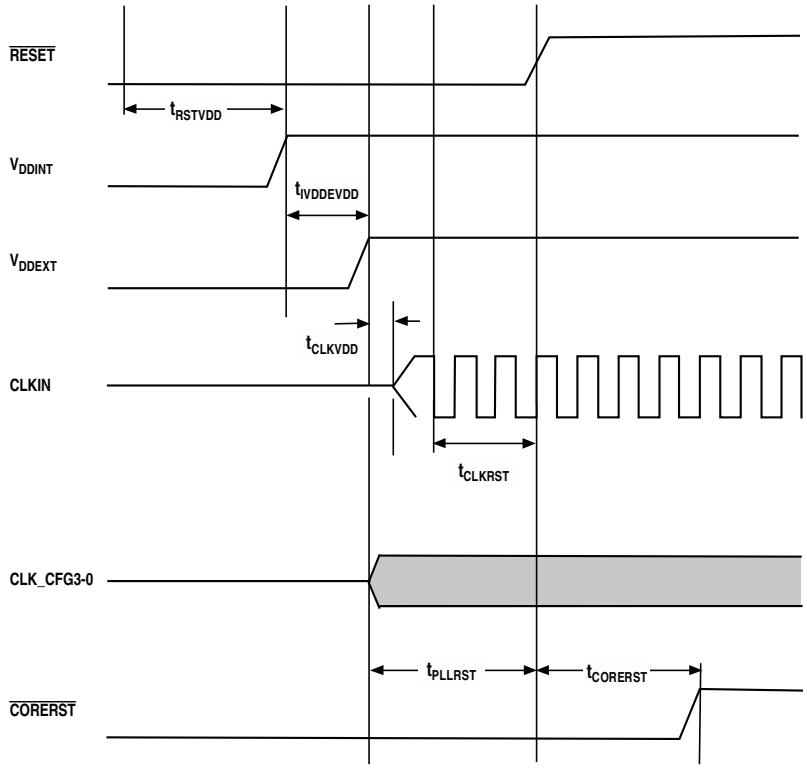

Figure 8. Power-Up Sequencing

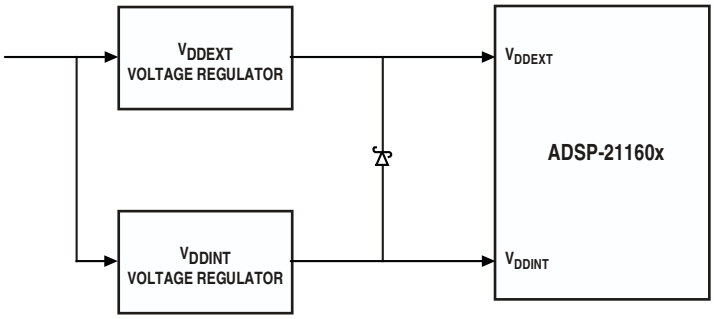

Figure 9. Dual Voltage Schottky Diode

Clock Input

For clock input, see Table 13 and Figure 10.

Table 13. Clock Input

Parameter		ADSP-21160M 80 MHz		ADSP-21160N 100 MHz		Unit
		Min	Max	Min	Max	
Timing Requirements						
t_{CK}	CLKIN Period	25	80	20	80	ns
t_{CKL}	CLKIN Width Low	10.5	40	7.5	40	ns
t_{CKH}	CLKIN Width High	10.5	40	7.5	40	ns
t_{CKRF}	CLKIN Rise/Fall (0.4 V–2.0 V)		3		3	ns
t_{CCLK}	Core Clock Period	12.5	40	10	30	ns

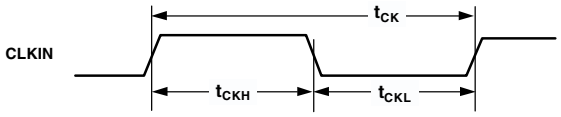

Figure 10. Clock Input

Reset

For reset, see Table 14 and Figure 11.

Table 14. Reset

Parameter		Min	Max	Unit
Timing Requirements				
t_{WRST}	$\overline{\text{RESET}}$ Pulsewidth Low[1]	$4t_{CK}$		ns
t_{SRST}	$\overline{\text{RESET}}$ Setup Before CLKIN High[2]	8		ns

[1] Applies after the power-up sequence is complete. At power-up, the processor's internal phase-locked loop requires no more than 100 µs while $\overline{\text{RESET}}$ is low, assuming stable V_{DD} and CLKIN (not including start-up time of external clock oscillator).

[2] Only required if multiple ADSP-21160x DSPs must come out of reset synchronous to CLKIN with program counters (PC) equal. Not required for multiple ADSP-21160x DSPs communicating over the shared bus (through the external port), because the bus arbitration logic automatically synchronizes itself after reset.

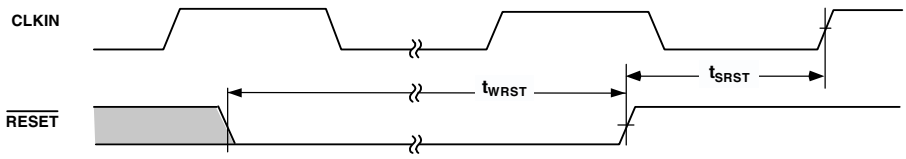

Figure 11. Reset

Interrupts

For interrupts, see Table 15 and Figure 12.

Table 15. Interrupts

Parameter		Min	Max	Unit
Timing Requirements				
t_{SIR}	$\overline{IRQ2–0}$ Setup Before CLKIN High[1]	6		ns
t_{HIR}	$\overline{IRQ2–0}$ Hold After CLKIN High[1]	0		ns
t_{IPW}	$\overline{IRQ2–0}$ Pulsewidth[2]	$2+t_{CK}$		ns

[1] Only required for $\overline{IRQx}$ recognition in the following cycle.
[2] Applies only if t_{SIR} and t_{HIR} requirements are not met.

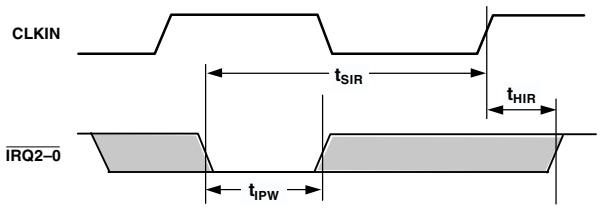

Figure 12. Interrupts

Timer

For timer, see Table 16 and Figure 13.

Table 16. Timer

Parameter		Min	Max	Unit
Switching Characteristic				
t_{DTEX}	CLKIN High to TIMEXP[1]	1	9	ns

[1] For ADSP-21160M, specification is 7 ns, maximum.

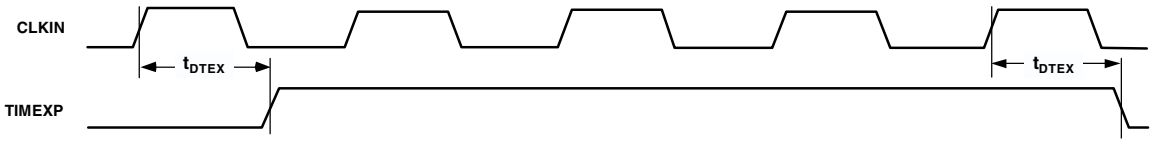

Figure 13. Timer

Memory Read—Bus Master

Use these specifications for asynchronous interfacing to memories (and memory-mapped peripherals) without reference to CLKIN except for the ACK pin requirements listed in note 6 of Table 18. These specifications apply when the ADSP-21160x is the bus master accessing external memory space in asynchronous access mode.

Table 18. Memory Read—Bus Master

Parameter		Min	Max	Unit
Timing Requirements				
t_{DAD}	Address, $\overline{CIF}$, Selects Delay to Data Valid[1, 2, 3, 4]		$t_{CK} - 0.25t_{CCLK} - 8.5 + W$	ns
t_{DRLD}	$\overline{RDx}$ Low to Data Valid[1, 4, 5]		$t_{CK} - 0.5t_{CCLK} + W$	ns
t_{HDA}	Data Hold from Address, Selects[6]	0		ns
t_{SDS}	Data Setup to $\overline{RDx}$ High[1]	8		ns
t_{HDRH}	Data Hold from $\overline{RDx}$ High[6]	1		ns
t_{DAAK}	ACK Delay from Address, Selects[2, 7]		$t_{CK} - 0.5t_{CCLK} - 12 + W$	ns
t_{DSAK}	ACK Delay from $\overline{RDx}$ Low[7]		$t_{CK} - 0.75t_{CCLK} - 11 + W$	ns
t_{SAKC}	ACK Setup to CLKIN[7]	$0.5t_{CCLK} + 3$		ns
t_{HAKC}	ACK Hold After CLKIN	1		ns
Switching Characteristics				
t_{DRHA}	Address, $\overline{CIF}$, Selects Hold After $\overline{RDx}$ High	$0.25t_{CCLK} - 1 + H$		ns
t_{DARL}	Address, $\overline{CIF}$, Selects to $\overline{RDx}$ Low[2]	$0.25t_{CCLK} - 3$		ns
t_{RW}	$\overline{RDx}$ Pulsewidth	$t_{CK} - 0.5t_{CCLK} - 1 + W$		ns
t_{RWR}	$\overline{RDx}$ High to $\overline{WRx}$, $\overline{RDx}$, $\overline{DMAGx}$ Low	$0.5t_{CCLK} - 1 + HI$		ns

W = (number of wait states specified in WAIT register) × t_{CK}.
HI = t_{CK} (if an address hold cycle or bus idle cycle occurs, as specified in WAIT register; otherwise HI = 0).
H = t_{CK} (if an address hold cycle occurs as specified in WAIT register; otherwise H = 0).

[1] Data Delay/Setup: User must meet t_{DAD}, t_{DRLD}, or t_{SDS}.
[2] The falling edge of $\overline{MSx}$, $\overline{BMS}$ is referenced.
[3] For ADSP-21160M, specification is t_{CK}–$0.25t_{CCLK}$–11+W ns, maximum.
[4] The maximum limit of timing requirement values for t_{DAD} and t_{DRLD} parameters are applicable for the case where AMI_ACK is always high.
[5] For ADSP-21160M, specification is $0.75t_{CK}$–11+W ns, maximum.
[6] Data Hold: User must meet t_{HDA} or t_{HDRH} in asynchronous access mode. See Example System Hold Time Calculation on page 49 for the calculation of hold times given capacitive and dc loads.
[7] For asynchronous access, ACK is sampled only after the programmed wait states for the access have been counted. For the first CLKIN cycle of a new external memory access, ACK must be driven low (deasserted) by t_{DAAK}, t_{DSAK}, or t_{SAKC}. For the second and subsequent cycles of an asynchronous external memory access, the t_{SAKC} and t_{HAKC} must be met for both assertion and deassertion of ACK signal.

Memory Write—Bus Master

Use these specifications for asynchronous interfacing to memories (and memory-mapped peripherals) without reference to CLKIN except for the ACK pin requirements listed in note 1 of Table 19. These specifications apply when the ADSP-21160x is the bus master accessing external memory space in asynchronous access mode.

Table 19. Memory Write—Bus Master

Parameter		Min	Max	Unit
Timing Requirements				
t_{DAAK}	ACK Delay from Address, Selects[1, 2]		$t_{CK} - 0.5t_{CCLK} - 12 + W$	ns
t_{DSAK}	ACK Delay from $\overline{WRx}$ Low[1]		$t_{CK} - 0.75t_{CCLK} - 11 + W$	ns
t_{SAKC}	ACK Setup to CLKIN[1]	$0.5t_{CCLK} + 3$		ns
t_{HAKC}	ACK Hold After CLKIN[1]	1		ns
Switching Characteristics				
t_{DAWH}	Address, $\overline{CIF}$, Selects to $\overline{WRx}$ Deasserted[2]	$t_{CK} - 0.25t_{CCLK} - 3 + W$		ns
t_{DAWL}	Address, $\overline{CIF}$, Selects to $\overline{WRx}$ Low[2]	$0.25t_{CCLK} - 3$		ns
t_{WW}	$\overline{WRx}$ Pulsewidth	$t_{CK} - 0.5t_{CCLK} - 1 + W$		ns
t_{DDWH}	Data Setup before $\overline{WRx}$ High[3]	$t_{CK} - 0.5t_{CCLK} - 1 + W$		ns
t_{DWHA}	Address Hold after $\overline{WRx}$ Deasserted	$0.25t_{CCLK} - 1 + H$		ns
t_{DWHD}	Data Hold after $\overline{WRx}$ Deasserted	$0.25t_{CCLK} - 1 + H$		ns
t_{DATRWH}	Data Disable after $\overline{WRx}$ Deasserted[4]	$0.25t_{CCLK} - 2 + H$	$0.25t_{CCLK} + 2 + H$	ns
t_{WWR}	$\overline{WRx}$ High to $\overline{WRx}$, $\overline{RDx}$, $\overline{DMAGx}$ Low	$0.5t_{CCLK} - 1 + HI$		ns
t_{DDWR}	Data Disable before $\overline{WRx}$ or $\overline{RDx}$ Low	$0.25t_{CCLK} - 1 + I$		ns
t_{WDE}	$\overline{WRx}$ Low to Data Enabled	$-0.25t_{CCLK} - 1$		ns

W = (number of wait states specified in WAIT register) × t_{CK}.
H = t_{CK} (if an address hold cycle occurs, as specified in WAIT register; otherwise H = 0).
HI = t_{CK} (if an address hold cycle or bus idle cycle occurs, as specified in WAIT register; otherwise HI = 0).
I = t_{CK} (if a bus idle cycle occurs, as specified in WAIT register; otherwise I = 0).

[1] For asynchronous access, ACK is sampled only after the programmed wait states for the access have been counted. For the first CLKIN cycle of a new external memory access, ACK must be driven low (deasserted) by t_{DAAK} or t_{DSAK} or t_{SAKC}. For the second and subsequent cycles of an asynchronous external memory access, the t_{SAKC} and t_{HAKC} must be met for both assertion and deassertion of ACK signal.
[2] The falling edge of $\overline{MSx}$, $\overline{BMS}$ is referenced.
[3] For ADSP-21160M, specification is $t_{CK} - 0.25t_{CCLK} - 12.5 + W$ ns, minimum.
[4] See Example System Hold Time Calculation on Page 49 for calculation of hold times given capacitive and dc loads.

Synchronous Read/Write—Bus Slave

See Table 21 and Figure 18. Use these specifications for ADSP-21160x bus master accesses of a slave's IOP registers or internal memory (in multiprocessor memory space). The bus master must meet these (bus slave) timing requirements.

Table 21. Synchronous Read/Write—Bus Slave

Parameter		Min	Max	Unit
Timing Requirements				
t_{SADDI}	Address, BRST Setup Before CLKIN	5		ns
t_{HADDI}	Address, BRST Hold After CLKIN	1		ns
t_{SRWI}	$\overline{RDx}$/$\overline{WRx}$ Setup Before CLKIN	5		ns
t_{HRWI}	$\overline{RDx}$/$\overline{WRx}$ Hold After CLKIN	1		ns
t_{SSDATI}	Data Setup Before CLKIN	5.5		ns
t_{HSDATI}	Data Hold After CLKIN	1		ns
Switching Characteristics				
t_{DDATO}	Data Delay After CLKIN[1]		0.25 t_{CCLK} + 9	ns
t_{HDATO}	Data Hold After CLKIN	1.5		ns
t_{DACKC}	ACK Delay After CLKIN		10	ns
t_{HACKO}	ACK Hold After CLKIN	1.5		ns

[1] For ADSP-21160M, specification is 12.5 ns, maximum.

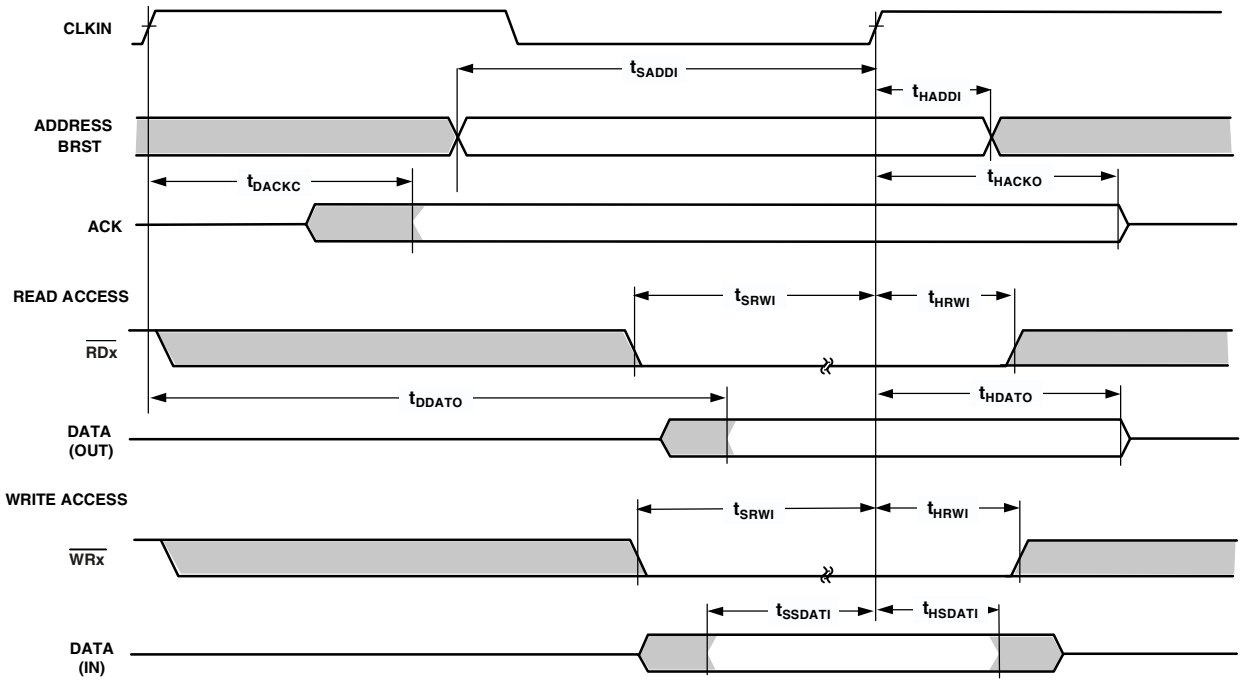

Figure 18. Synchronous Read/Write—Bus Slave

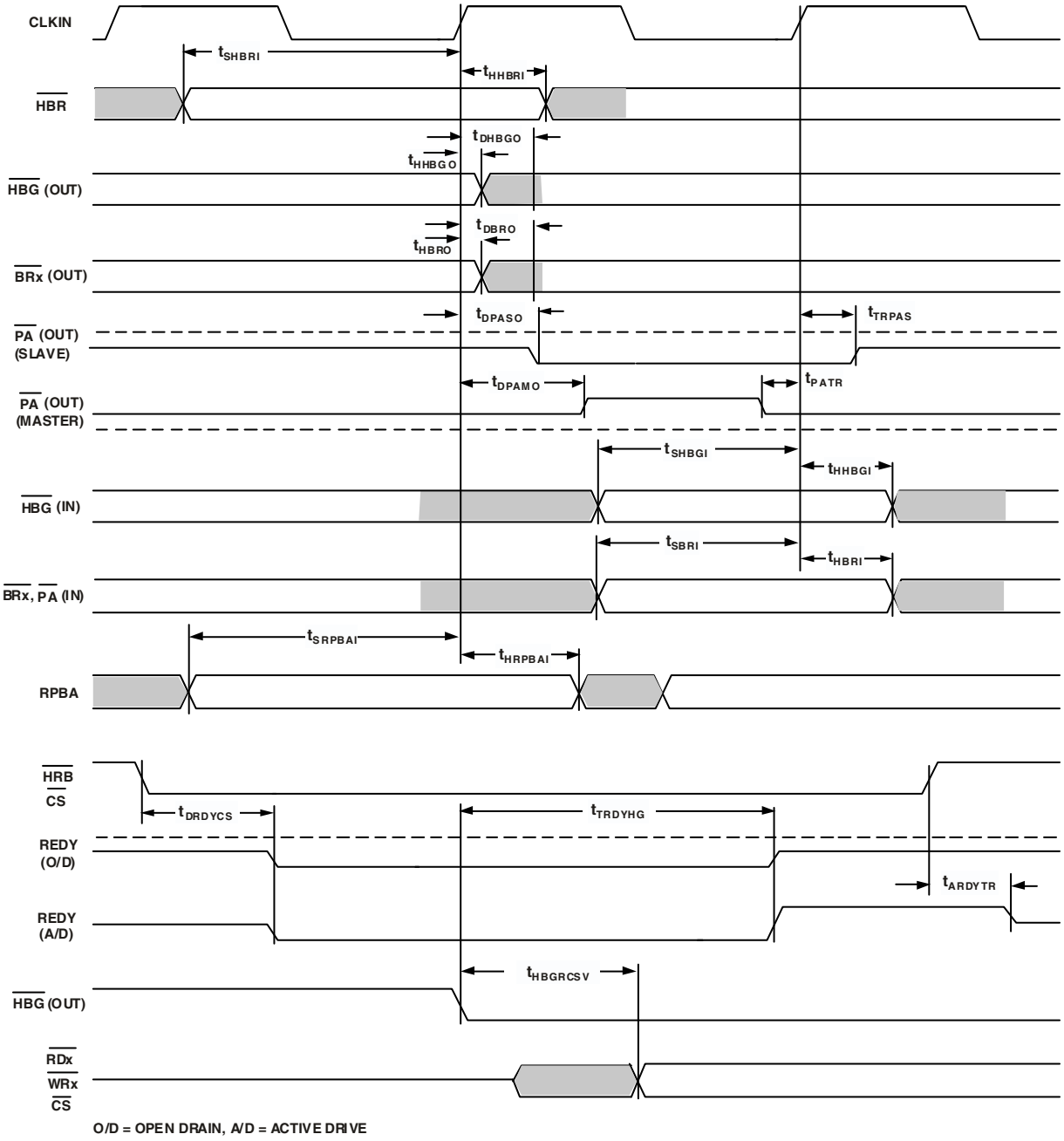

Figure 19. Multiprocessor Bus Request and Host Bus Request

Link Ports—Receive, Transmit

For link ports, see Table 27, Table 28, Figure 24, and Figure 25. Calculation of link receiver data setup and hold, relative to link clock, is required to determine the maximum allowable skew that can be introduced in the transmission path, between LDATA and LCLK. Setup skew is the maximum delay that can be introduced in LDATA, relative to LCLK (setup skew = $t_{LCLKTWH}$ minimum – t_{DLDCH} – t_{SLDCL}). Hold skew is the maximum delay that can be introduced in LCLK, relative to LDATA (hold skew = $t_{LCLKTWL}$ minimum + t_{HLDCH} – t_{HLDCL}). Calculations made directly from speed specifications result in unrealistically small skew times, because they include multiple tester guardbands.

Note that there is a two-cycle effect latency between the link port enable instruction and the DSP enabling the link port.

Table 27. Link Ports—Receive

Parameter		Min	Max	Unit
Timing Requirements				
t_{SLDCL}	Data Setup Before LCLK Low	2.5		ns
t_{HLDCL}	Data Hold After LCLK Low[1]	3		ns
t_{LCLKIW}	LCLK Period	t_{LCLK}		ns
$t_{LCLKRWL}$	LCLK Width Low[2]	4		ns
$t_{LCLKRWH}$	LCLK Width High[3]	4		ns
Switching Characteristics				
t_{DLALC}	LACK Low Delay After LCLK High[4, 5]	9	17	ns

[1] For ADSP-21160M, specification is 2.5 ns, minimum.
[2] For ADSP-21160M, specification is 6 ns, minimum.
[3] For ADSP-21160M, specification is 6 ns, minimum.
[4] LACK goes low with t_{DLALC} relative to rise of LCLK after first nibble, but does not go low if the receiver's link buffer is not about to fill.
[5] For ADSP-21160M, specification is 12 ns, minimum.

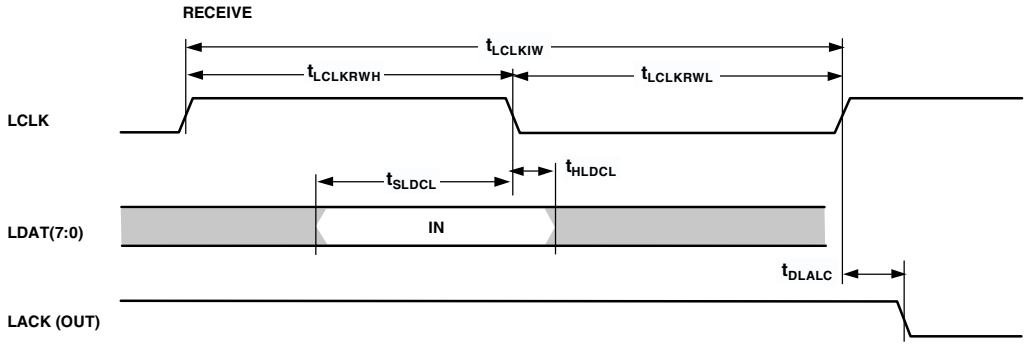

Figure 24. Link Ports—Receive

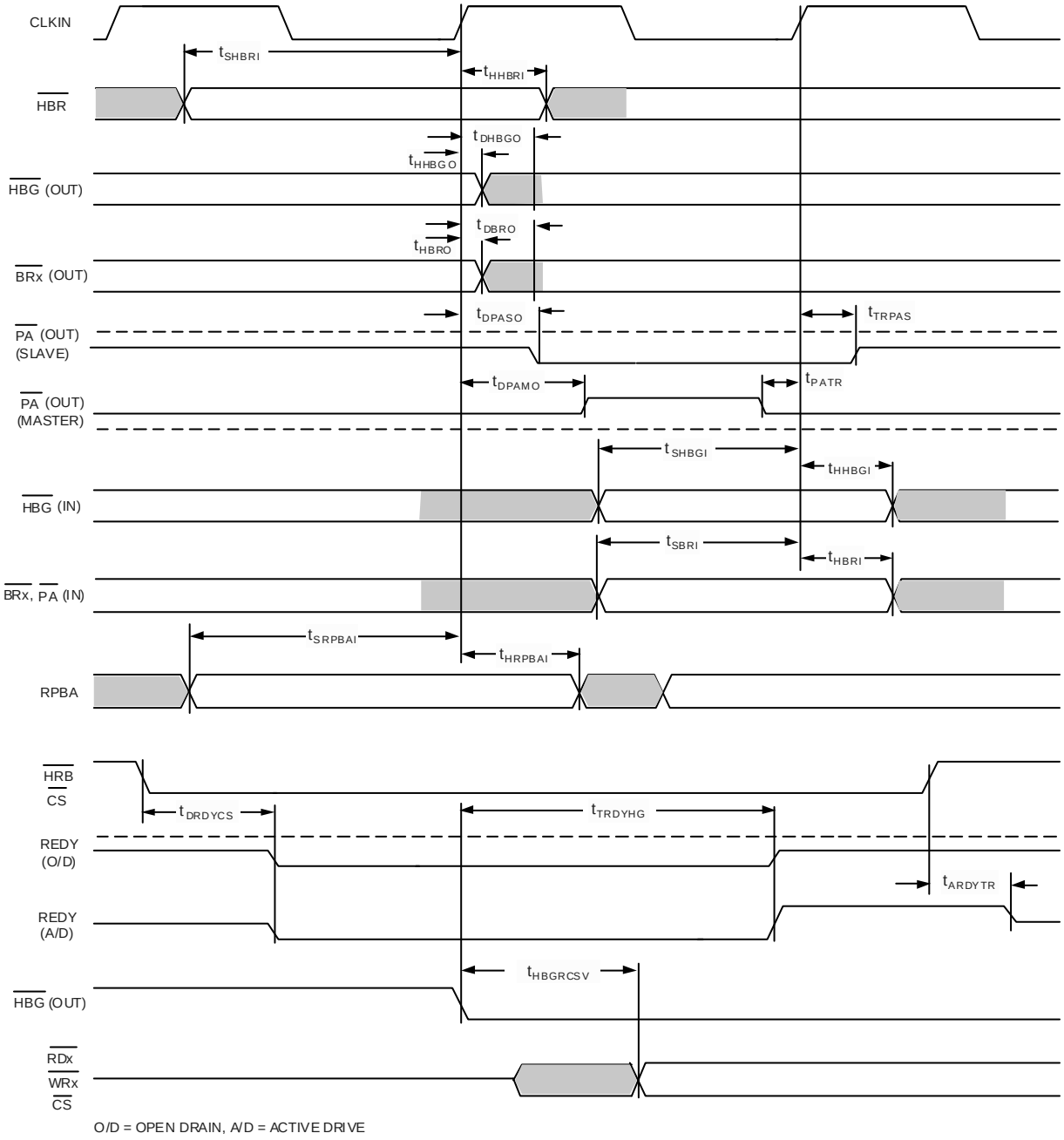

Figure 19. Multiprocessor Bus Request and Host Bus Request