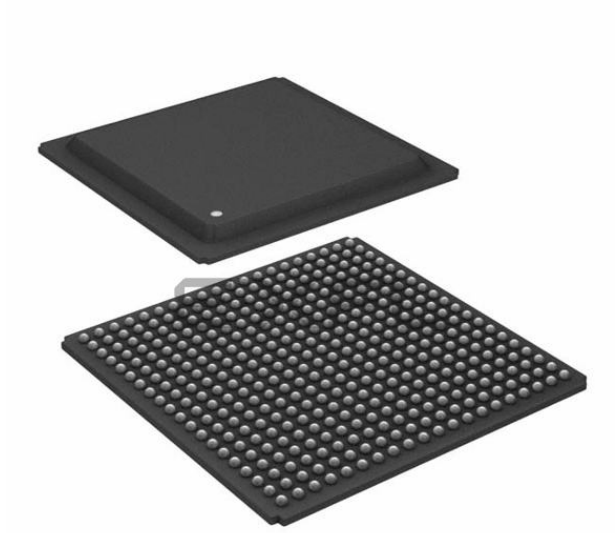

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Floating Point
Interface	Host Interface, Link Port, Serial Port
Clock Rate	100MHz
Non-Volatile Memory	External
On-Chip RAM	512kB
Voltage - I/O	3.30V
Voltage - Core	1.90V
Operating Temperature	-40°C ~ 100°C (TC)
Mounting Type	Surface Mount
Package / Case	400-BBGA
Supplier Device Package	400-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21160ncb-100

- **Single-instruction, multiple-data (SIMD) architecture provides**
  - **Two computational processing elements**
  - **Concurrent execution—each processing element executes the same instruction, but operates on different data**
  - **Code compatibility—at assembly level, uses the same instruction set as the ADSP-2106x SHARC DSPs**
- **Parallelism in buses and computational units allows**
  - **Single-cycle execution (with or without SIMD) of a multiply operation, an ALU operation, a dual memory read or write, and an instruction fetch**
  - **Transfers between memory and core at up to four 32-bit floating- or fixed-point words per cycle**
  - **Accelerated FFT butterfly computation through a multiply with add and subtract**
- **Memory attributes**
  - **4M bits on-chip dual-ported SRAM for independent access by core processor, host, and DMA**
  - **4G word address range for off-chip memory**
  - **Memory interface supports programmable wait state generation and page-mode for off-chip memory**
- **DMA controller supports**
  - **14 zero-overhead DMA channels for transfers between ADSP-21160x internal memory and external memory, external peripherals, host processor, serial ports, or link ports**
  - **64-bit background DMA transfers at core clock speed, in parallel with full-speed processor execution**
  - **Host processor interface to 16- and 32-bit microprocessors**
- **Multiprocessing support provides**
  - **Glueless connection for scalable DSP multiprocessing architecture**
  - **Distributed on-chip bus arbitration for parallel bus connect of up to 6 ADSP-21160x processors plus host**
  - **6 link ports for point-to-point connectivity and array multiprocessing**
- **Serial ports provide**
  - **Two synchronous serial ports with companding hardware**
  - **Independent transmit and receive functions**
  - **TDM support for T1 and E1 interfaces**
- **64-bit-wide synchronous external port provides**
  - **Glueless connection to asynchronous and SBSRAM external memories**

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REVISION HISTORY

9/15—Rev. C to Rev. D

Removed model ADSP-21160NKB-100 (no longer available) from Ordering Guide 58

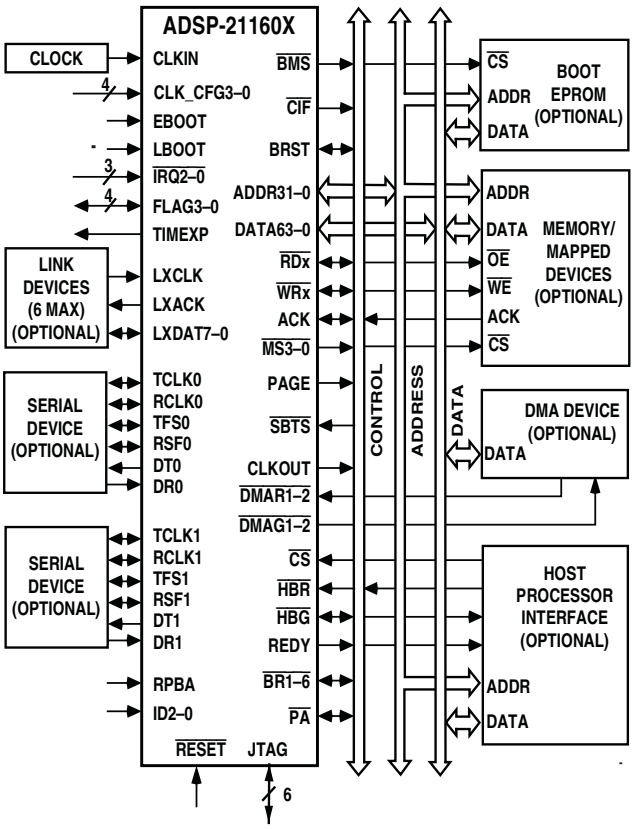

Figure 2. Single-Processor System

enabled, the same instruction is executed in both processing elements, but each processing element operates on different data. This architecture is efficient at executing math-intensive DSP algorithms.

Entering SIMD mode also has an effect on the way data is transferred between memory and the processing elements. In SIMD mode, twice the data bandwidth is required to sustain computational operation in the processing elements. Because of this requirement, entering SIMD mode also doubles the bandwidth between memory and the processing elements. When using the DAGs to transfer data in SIMD mode, two data values are transferred with each access of memory or the register file.

Independent, Parallel Computation Units

Within each processing element is a set of computational units. The computational units consist of an arithmetic/logic unit (ALU), multiplier, and shifter. These units perform single-cycle instructions. The three units within each processing element are arranged in parallel, maximizing computational throughput. Single multifunction instructions execute parallel ALU and multiplier operations. In SIMD mode, the parallel ALU and multiplier operations occur in both processing elements. These computation units support IEEE 32-bit single-precision floating-point, 40-bit extended-precision floating-point, and 32-bit fixed-point data formats.

Data Register File

A general-purpose data register file is contained in each processing element. The register files transfer data between the computation units and the data buses, and store intermediate results. These 10-port, 32-register (16 primary, 16 secondary) register files, combined with the ADSP-2116x enhanced Harvard architecture, allow unconstrained data flow between computation units and internal memory. The registers in PEX are referred to as R0–R15 and in PEY as S0–S15.

Single-Cycle Fetch of Instruction and Four Operands

The processor features an enhanced Harvard architecture in which the data memory (DM) bus transfers data, and the program memory (PM) bus transfers both instructions and data (see the functional block diagram 1). With the ADSP-21160x DSP's separate program and data memory buses and on-chip instruction cache, the processor can simultaneously fetch four operands and an instruction (from the cache), all in a single cycle.

Instruction Cache

The ADSP-21160x includes an on-chip instruction cache that enables three-bus operation for fetching an instruction and four data values. The cache is selective—only the instructions whose fetches conflict with PM bus data accesses are cached. This cache allows full-speed execution of core, providing looped operations, such as digital filter multiply- accumulates and FFT butterfly processing.

Data Address Generators with Hardware Circular Buffers

The ADSP-21160x DSP's two data address generators (DAGs) are used for indirect addressing and provide for implementing circular data buffers in hardware. Circular buffers allow efficient programming of delay lines and other data structures required in digital signal processing, and are commonly used in digital filters and Fourier transforms. The two DAGs of the product contain sufficient registers to allow the creation of up to 32 circular buffers (16 primary register sets, 16 secondary). The DAGs automatically handle address pointer wraparound, reducing overhead, increasing performance, and simplifying implementation. Circular buffers can start and end at any memory location.

Flexible Instruction Set

The 48-bit instruction word accommodates a variety of parallel operations for concise programming. For example, the processor can conditionally execute a multiply, an add, and subtract, in both processing elements, while branching, all in a single instruction.

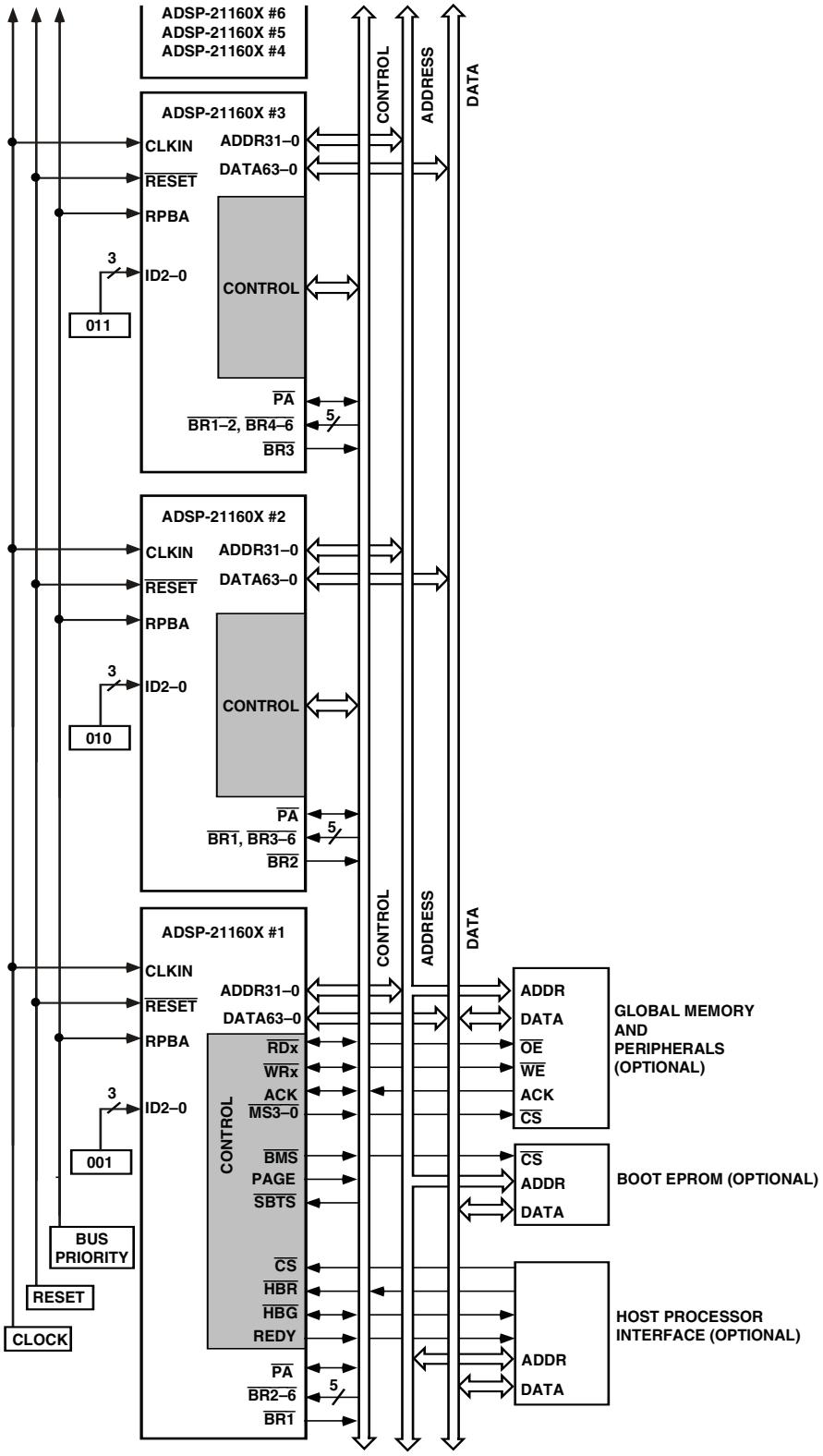

Figure 3. Shared Memory Multiprocessing System

MEMORY AND I/O INTERFACE FEATURES

Augmenting the ADSP-2116x family core, the ADSP-21160x adds the following architectural features.

Dual-Ported On-Chip Memory

The ADSP-21160x contains four megabits of on-chip SRAM, organized as two blocks of 2M bits each, which can be configured for different combinations of code and data storage (Figure 4). Each memory block is dual-ported for single-cycle, independent accesses by the core processor and I/O processor. The dual-ported memory in combination with three separate on-chip buses allows two data transfers from the core and one from I/O processor, in a single cycle. The ADSP-21160x memory can be configured as a maximum of 128K words of 32-bit data, 256K words of 16-bit data, 85K words of 48-bit instructions (or 40-bit data), or combinations of different word sizes up to four megabits. All of the memory can be accessed as 16-, 32-, 48-, or 64-bit words. A 16-bit floating-point storage format is supported that effectively doubles the amount of data that may be stored on-chip. Conversion between the 32-bit floating-point and 16-bit floating-point formats is done in a single instruction. While each memory block can store combinations of code and data, accesses are most efficient when one block stores data, using the DM bus for transfers, and the other block stores instructions and data, using the PM bus for transfers. Using the DM bus and PM bus in this way, with one dedicated to each memory block, assures single-cycle execution with two data transfers. In this case, the instruction must be available in the cache.

Off-Chip Memory and Peripherals Interface

The ADSP-21160x DSP's external port provides the processor's interface to off-chip memory and peripherals. The 4G word off-chip address space is included in the processor's unified address space. The separate on-chip buses—for PM addresses, PM data, DM addresses, DM data, I/O addresses, and I/O data—are multiplexed at the external port to create an external system bus with a single 32-bit address bus and a single 64-bit data bus. The lower 32 bits of the external data bus connect to even addresses, and the upper 32 bits of the 64 connect to odd addresses. Every access to external memory is based on an address that fetches a 32-bit word, and with the 64-bit bus, two address locations can be accessed at once. When fetching an instruction from external memory, two 32-bit data locations are being accessed (16 bits are unused). Figure 5 shows the alignment of various accesses to external memory.

The external port supports asynchronous, synchronous, and synchronous burst accesses. ZBT synchronous burst SRAM can be interfaced gluelessly. Addressing of external memory devices is facilitated by on-chip decoding of high-order address lines to generate memory bank select signals. Separate control lines are also generated for simplified addressing of page-mode DRAM. The ADSP-21160x provides programmable memory wait states and external memory acknowledge controls to allow interfacing to DRAM and peripherals with variable access, hold, and disable time requirements.

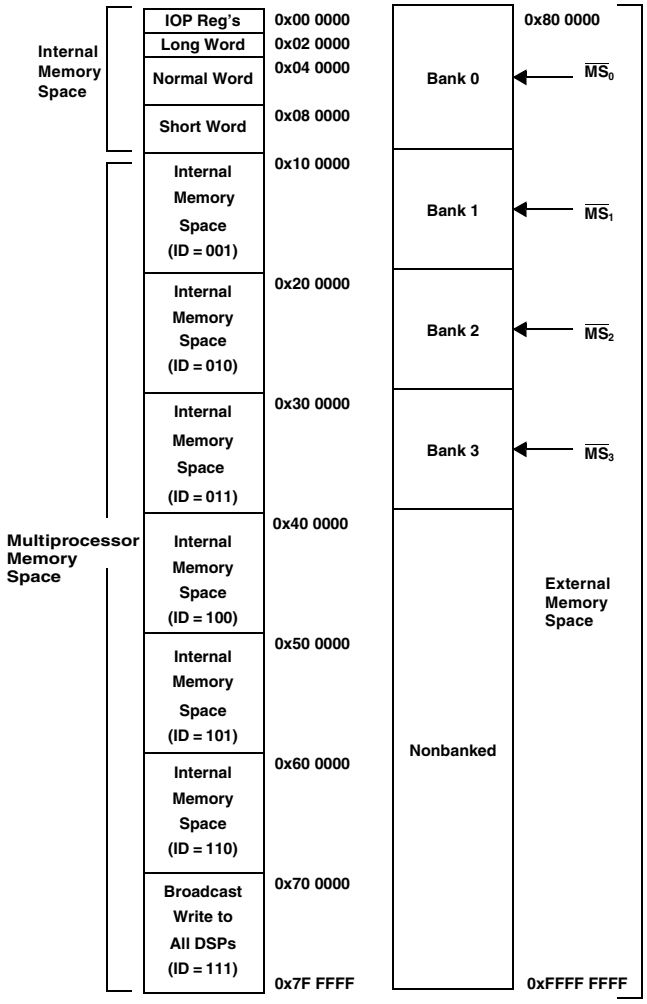

Figure 4. Memory Map

DMA Controller

The ADSP-21160x DSP's on-chip DMA controller allows zero-overhead data transfers without processor intervention. The DMA controller operates independently and invisibly to the processor core, allowing DMA operations to occur while the core is simultaneously executing its program instructions. DMA transfers can occur between the processor's internal memory and external memory, external peripherals, or a host processor. DMA transfers can also occur between the product's DSP's internal memory and its serial ports or link ports. External bus packing to 16-, 32-, 48-, or 64-bit words is performed during DMA transfers. Fourteen channels of DMA are available on the ADSP-21160x—six via the link ports, four via the serial ports, and four via the processor's external port (for either host processor, other ADSP-21160x processors, memory or I/O transfers). Programs can be downloaded to the processor using DMA transfers. Asynchronous off-chip peripherals can control two DMA channels using DMA Request/Grant lines ($\overline{\text{DMAR1–2}}$, $\overline{\text{DMAG1–2}}$). Other DMA features include

located on the web page for the associated EZ-KIT or EZ-Extender product. The link is found in the *Product Download* area of the product web page.

Middleware Packages

Analog Devices separately offers middleware add-ins such as real time operating systems, file systems, USB stacks, and TCP/IP stacks. For more information, see the following web pages:

- www.analog.com/ucos3
- www.analog.com/ucfs
- www.analog.com/ucusbd
- www.analog.com/lwip

Algorithmic Modules

To speed development, Analog Devices offers add-ins that perform popular audio and video processing algorithms. These are available for use with both CrossCore Embedded Studio and VisualDSP++. For more information visit www.analog.com and search on "Blackfin software modules" or "SHARC software modules".

Designing an Emulator-Compatible DSP Board (Target)

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG Test Access Port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the processor's internal features via the processor's TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers. The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the DSP's JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see the application note (EE-68) "Analog Devices JTAG Emulation Technical Reference" (www.analog.com/ee-68). This document is updated regularly to keep pace with improvements to emulator support.

ADDITIONAL INFORMATION

This data sheet provides a general overview of the ADSP-21160x architecture and functionality. For detailed information on the Blackfin family core architecture and instruction set, refer to the *ADSP-21160 SHARC DSP Hardware Reference* and the *ADSP-21160 SHARC DSP Instruction Set Reference*. For detailed information on the development tools for this processor, see the *VisualDSP++ User's Guide*.

RELATED SIGNAL CHAINS

A signal chain is a series of signal conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next.

Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The application signal chains page in the Circuits from the Lab® site (http:\\www.analog.com\circuits) provides:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

PIN FUNCTION DESCRIPTIONS

ADSP-21160x pin definitions are listed below. Inputs identified as synchronous (S) must meet timing requirements with respect to CLKIN (or with respect to TCK for TMS, TDI). Inputs identified as asynchronous (A) can be asserted asynchronously to CLKIN (or to TCK for $\overline{\text{TRST}}$).

Tie or pull unused inputs to V_{DD} or GND, except for the following:

- ADDR31–0, DATA63–0, PAGE, BRST, CLKOUT (ID2–0 = 00x) (Note: These pins have a logic-level hold circuit enabled on the ADSP-21160x DSP with ID2–0 = 00x.)
- $\overline{\text{PA}}$, ACK, $\overline{\text{MS3–0}}$, $\overline{\text{RDx}}$, $\overline{\text{WRx}}$, $\overline{\text{CIF}}$, $\overline{\text{DMARx}}$, $\overline{\text{DMAGx}}$ (ID2–0 = 00x) (Note: These pins have a pull-up enabled on the ADSP-21160x with ID2–0 = 00x.)
- LxCLK, LxACK, LxDAT7–0 (LxPDRDE = 0) (Note: See Link Port Buffer Control Register Bit definitions in the *ADSP-21160 SHARC DSP Hardware Reference*.)
- DTx, DRx, TCLKx, RCLKx, $\overline{\text{EMU}}$, TMS, $\overline{\text{TRST}}$, TDI (Note: These pins have a pull-up.)

The following symbols appear in the Type column of Table 3: A = Asynchronous, G = Ground, I = Input, O = Output, P = Power Supply, S = Synchronous, (A/D) = Active Drive, (O/D) = Open Drain, and T = Three-State (when $\overline{\text{SBTS}}$ is asserted, or when the ADSP-21160x is a bus slave).

Table 3. Pin Function Descriptions

Pin	Type	Function
ADDR31–0	I/O/T	External Bus Address. The ADSP-21160x outputs addresses for external memory and peripherals on these pins. In a multiprocessor system, the bus master outputs addresses for read/writes of the internal memory or IOP registers of other ADSP-21160x DSPs. The ADSP-21160x inputs addresses when a host processor or multiprocessing bus master is reading or writing its internal memory or IOP registers. A keeper latch on the DSP's ADDR31–0 pins maintains the input at the level it was last driven (only enabled on the processor with ID2–0 = 00x).
DATA63–0	I/O/T	External Bus Data. The ADSP-21160x inputs and outputs data and instructions on these pins. Pull-up resistors on unused DATA pins are not necessary. A keeper latch on the DSP's DATA63-0 pins maintains the input at the level it was last driven (only enabled on the processor with ID2–0 = 00x).
$\overline{\text{MS3–0}}$	O/T	Memory Select Lines. These outputs are asserted (low) as chip selects for the corresponding banks of external memory. Memory bank size must be defined in the SYSCON control register. The $\overline{\text{MS3–0}}$ outputs are decoded memory address lines. In asynchronous access mode, the $\overline{\text{MS3–0}}$ outputs transition with the other address outputs. In synchronous access modes, the $\overline{\text{MS3–0}}$ outputs assert with the other address lines; however, they deassert after the first CLKIN cycle in which ACK is sampled asserted. $\overline{\text{MS3–0}}$ has a 20 kΩ internal pull-up resistor that is enabled on the ADSP-21160x with ID2–0 = 00x.
$\overline{\text{RDL}}$	I/O/T	Memory Read Low Strobe. $\overline{\text{RDL}}$ is asserted whenever ADSP-21160x reads from the low word of external memory or from the internal memory of other ADSP-21160x DSPs. External devices, including other ADSP-21160x DSPs, must assert $\overline{\text{RDL}}$ for reading from the low word of processor internal memory. In a multiprocessing system, $\overline{\text{RDL}}$ is driven by the bus master. $\overline{\text{RDL}}$ has a 20 kΩ internal pull-up resistor that is enabled on the processor with ID2–0 = 00x.
$\overline{\text{RDH}}$	I/O/T	Memory Read High Strobe. $\overline{\text{RDH}}$ is asserted whenever ADSP-21160x reads from the high word of external memory or from the internal memory of other ADSP-21160x DSPs. External devices, including other ADSP-21160x DSPs, must assert $\overline{\text{RDH}}$ for reading from the high word of ADSP-21160x internal memory. In a multiprocessing system, $\overline{\text{RDH}}$ is driven by the bus master. $\overline{\text{RDH}}$ has a 20 kΩ internal pull-up resistor that is enabled on the processor with ID2–0 = 00x.
$\overline{\text{WRL}}$	I/O/T	Memory Write Low Strobe. $\overline{\text{WRL}}$ is asserted when ADSP-21160x writes to the low word of external memory or internal memory of other ADSP-21160x DSPs. External devices must assert $\overline{\text{WRL}}$ for writing to ADSP-21160x DSP's low word of internal memory. In a multiprocessing system, $\overline{\text{WRL}}$ is driven by the bus master. $\overline{\text{WRL}}$ has a 20 kΩ internal pull-up resistor that is enabled on the processor with ID2–0 = 00x.
$\overline{\text{WRH}}$	I/O/T	Memory Write High Strobe. $\overline{\text{WRH}}$ is asserted when ADSP-21160x writes to the high word of external memory or internal memory of other ADSP-21160x DSPs. External devices must assert $\overline{\text{WRH}}$ for writing to ADSP-21160x DSP's high word of internal memory. In a multiprocessing system, $\overline{\text{WRH}}$ is driven by the bus master. $\overline{\text{WRH}}$ has a 20 kΩ internal pull-up resistor that is enabled on the processor with ID2–0 = 00x.

Table 3. Pin Function Descriptions (Continued)

Pin	Type	Function
CLKOUT	O/T	Local Clock Out. CLKOUT is driven at the CLKIN frequency by the processor. This output can be three-stated by setting the COD bit in the SYSCON register. A keeper latch on the DSP's CLKOUT pin maintains the output at the level it was last driven (only enabled on the processor with ID2-0 = 00x). Do not use CLKOUT in multiprocessing systems; use CLKIN instead.
$\overline{\text{RESET}}$	I/A	Processor Reset. Resets the ADSP-21160x to a known state and begins execution at the program memory location specified by the hardware reset vector address. The $\overline{\text{RESET}}$ input must be asserted (low) at power-up.
TCK	I	Test Clock (JTAG). Provides a clock for JTAG boundary scan.
TMS	I/S	Test Mode Select (JTAG). Used to control the test state machine. TMS has a 20 kΩ internal pull-up resistor.
TDI	I/S	Test Data Input (JTAG). Provides serial data for the boundary scan logic. TDI has a 20 kΩ internal pull-up resistor.
TDO	O	Test Data Output (JTAG). Serial scan output of the boundary scan path.
$\overline{\text{TRST}}$	I/A	Test Reset (JTAG). Resets the test state machine. $\overline{\text{TRST}}$ must be asserted (pulsed low) after power-up or held low for proper operation of the ADSP-21160x. $\overline{\text{TRST}}$ has a 20 kΩ internal pull-up resistor.
$\overline{\text{EMU}}$	O (O/D)	Emulation Status. Must be connected to the ADSP-21160x emulator target board connector only. $\overline{\text{EMU}}$ has a 50 kΩ internal pull-up resistor.
$\overline{\text{CIF}}$	O/T	Core Instruction Fetch. Signal is active low when an external instruction fetch is performed. Driven by bus master only. Three-state when host is bus master. $\overline{\text{CIF}}$ has a 20 kΩ internal pull-up resistor that is enabled on the ADSP-21160x with ID2–0 = 00x.
V_{DDINT}	P	Core Power Supply. Nominally 2.5 V (ADSP-21160M) or 1.9 V (ADSP-21160N) dc and supplies the DSP's core processor
V_{DDEXT}	P	I/O Power Supply. Nominally 3.3 V dc.
AV_{DD}	P	Analog Power Supply. Nominally 2.5 V (ADSP-21160M) or 1.9 V (ADSP-21160N) dc and supplies the DSP's internal PLL (clock generator). This pin has the same specifications as V_{DDINT}, except that added filtering circuitry is required. For more information, see Power Supplies on page 9.
AGND	G	Analog Power Supply Return.
GND	G	Power Supply Return.
NC		Do Not Connect. Reserved pins that must be left open and unconnected.

Table 4. Boot Mode Selection

EBOOT	LBOOT	$\overline{\text{BMS}}$	Booting Mode
1	0	Output	EPROM (Connect $\overline{\text{BMS}}$ to EPROM chip select.)
0	0	1 (Input)	Host Processor
0	1	1 (Input)	Link Port
0	0	0 (Input)	No Booting. Processor executes from external memory.
0	1	0 (Input)	Reserved
1	1	x (Input)	Reserved

OPERATING CONDITIONS—ADSP-21160N

Table 7 shows recommended operating conditions for the ADSP-21160N. These specifications are subject to change without notice.

Table 7. Operating Conditions—ADSP-21160N

Parameter		C Grade Min	C Grade Max	K Grade Min	K Grade Max	Unit
V_{DDINT}	Internal (Core) Supply Voltage	1.8	2.0	1.8	2.0	V
AV_{DD}	Analog (PLL) Supply Voltage	1.8	2.0	1.8	2.0	V
V_{DDEXT}	External (I/O) Supply Voltage	3.13	3.47	3.13	3.47	V
T_{CASE}	Case Operating Temperature[1]	–40	+100	0	85	°C
V_{IH1}	High Level Input Voltage,[2] @ V_{DDEXT}=Max	2.0	V_{DDEXT}+0.5	2.0	V_{DDEXT}+0.5	V
V_{IH2}	High Level Input Voltage,[3] @ V_{DDEXT}=Max	2.0	V_{DDEXT}+0.5	2.0	V_{DDEXT}+0.5	V
V_{IL}	Low Level Input Voltage[2, 3] @ V_{DDEXT}=Min	–0.5	+0.8	–0.5	+0.8	V

[1] See Environmental Conditions on Page 51 for information on thermal specifications.

[2] Applies to input and bidirectional pins: DATA63–0, ADDR31–0, $\overline{RDx}$, $\overline{WRx}$, ACK, $\overline{SBTS}$, $\overline{IRQ2–0}$, FLAG3–0, $\overline{HBG}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $\overline{BR6–1}$, ID2–0, RPBA, $\overline{PA}$, BRST, TFS0, TFS1, RFS0, RFS1, LxDAT7–0, LxCLK, LxACK, EBOOT, LBOOT, $\overline{BMS}$, TMS, TDI, TCK, $\overline{HBR}$, DR0, DR1, TCLK0, TCLK1, RCLK0, and RCLK1.

[3] Applies to input pins: CLKIN, $\overline{RESET}$, and $\overline{TRST}$.

ELECTRICAL CHARACTERISTICS—ADSP-21160N

Table 8 shows the electrical characteristics. Note that these specifications are subject to change without notification.

Table 8. Electrical Characteristics—ADSP-21160N

Parameter		Test Conditions	Min	Max	Unit
V_{OH}	High Level Output Voltage[1]	@ V_{DDEXT} = Min, I_{OH} = –2.0 mA[2]	2.4		V
V_{OL}	Low Level Output Voltage[1]	@ V_{DDEXT} = Min, I_{OL} = 4.0 mA[2]		0.4	V
I_{IH}	High Level Input Current[3, 4, 5]	@ V_{DDEXT} = Max, V_{IN} = V_{DD} Max		10	µA
I_{IL}	Low Level Input Current[3]	@ V_{DDEXT} = Max, V_{IN} = 0 V		10	µA
I_{IHC}	CLKIN High Level Input Current[6]	@ V_{DDEXT} = Max, V_{IN} = V_{DDEXT} Max		25	µA
I_{ILC}	CLKIN Low Level Input Current[6]	@ V_{DDEXT} = Max, V_{IN} = 0 V		25	µA
I_{IKH}	Keeper High Load Current[7]	@ V_{DDEXT} = Max, V_{IN} = 2.0 V	–250	–50	µA
I_{IKL}	Keeper Low Load Current[7]	@ V_{DDEXT} = Max, V_{IN} = 0.8 V	50	200	µA
I_{IKH-OD}	Keeper High Overdrive Current[7, 8, 9]	@ V_{DDEXT} = Max	–300		µA
I_{IKL-OD}	Keeper Low Overdrive Current[7, 8, 9]	@ V_{DDEXT} = Max	300		µA
I_{ILPU1}	Low Level Input Current Pull-Up1[4]	@ V_{DDEXT} = Max, V_{IN} = 0 V		250	µA
I_{ILPU2}	Low Level Input Current Pull-Up2[5]	@ V_{DDEXT} = Max, V_{IN} = 0 V		500	µA
I_{OZH}	Three-State Leakage Current[10, 11, 12, 13]	@ V_{DDEXT} = Max, V_{IN} = V_{DD} Max		10	µA
I_{OZL}	Three-State Leakage Current[10]	@ V_{DDEXT} = Max, V_{IN} = 0 V		10	µA
I_{OZHPD}	Three-State Leakage Current Pull-Down[13]	@ V_{DDEXT} = Max, V_{IN} = V_{DD} Max		250	µA
I_{OZLPU1}	Three-State Leakage Current Pull-Up1[11]	@ V_{DDEXT} = Max, V_{IN} = 0 V		250	µA
I_{OZLPU2}	Three-State Leakage Current Pull-Up2[12]	@ V_{DDEXT} = Max, V_{IN} = 0 V		500	µA
I_{OZHA}	Three-State Leakage Current[14]	@ V_{DDEXT} = Max, V_{IN} = V_{DD} Max		25	µA
I_{OZLA}	Three-State Leakage Current[14]	@ V_{DDEXT} = Max, V_{IN} = 0 V		4	mA
$I_{DD-INPEAK}$	Supply Current (Internal)[15]	t_{CCLK} = 10.0 ns, V_{DDINT} = Max		960	mA
$I_{DD-INHIGH}$	Supply Current (Internal)[16]	t_{CCLK} = 10.0 ns, V_{DDINT} = Max		715	mA
$I_{DD-INLOW}$	Supply Current (Internal)[17]	t_{CCLK} = 10.0 ns, V_{DDINT} = Max		550	mA
$I_{DD-IDLE}$	Supply Current (Idle)[18]	t_{CCLK} = 10.0 ns, V_{DDINT} = Max		450	mA
AI_{DD}	Supply Current (Analog)[9]	@AV_{DD} = Max		10	mA
C_{IN}	Input Capacitance[19, 20]	f_{IN} = 1 MHz, T_{CASE} = 25°C, V_{IN} = 2.5 V		4.7	pF

[1] Applies to output and bidirectional pins: DATA63–0, ADDR31–0, $\overline{MS3–0}$, $\overline{RDx}$, $\overline{WRx}$, PAGE, CLKOUT, ACK, FLAG3–0, TIMEXP, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BR6–1}$, $\overline{PA}$, BRST, $\overline{CIF}$, DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, LxDAT7–0, LxCLK, LxACK, $\overline{BMS}$, TDO, and $\overline{EMU}$.

[2] See Output Drive Currents 47 for typical drive current capabilities.

[3] Applies to input pins: $\overline{SBTS}$, $\overline{IRQ2–0}$, $\overline{HBR}$, $\overline{CS}$, ID2–0, RPBA, EBOOT, LBOOT, CLKIN, $\overline{RESET}$, TCK, and CLK_CFG3-0.

[4] Applies to input pins with internal pull-ups: DR0, and DR1.

[5] Applies to input pins with internal pull-ups: $\overline{DMARx}$, TMS, TDI, and $\overline{TRST}$.

[6] Applies to CLKIN only.

[7] Applies to all pins with keeper latches: ADDR31–0, DATA63–0, PAGE, BRST, and CLKOUT.

[8] Current required to switch from kept high to low, or from kept low to high.

[9] Characterized, but not tested.

[10] Applies to three-statable pins: DATA63–0, ADDR31–0, PAGE, CLKOUT, ACK, FLAG3–0, REDY, $\overline{HBG}$, $\overline{BMS}$, $\overline{BR6–1}$, TFSx, RFSx, and TDO.

[11] Applies to three-statable pins with internal pull-ups: DTx, TCLKx, RCLKx, and $\overline{EMU}$.

[12] Applies to three-statable pins with internal pull-ups: $\overline{MS3–0}$,$\overline{RDx}$, $\overline{WRx}$, $\overline{DMAGx}$, $\overline{PA}$, and $\overline{CIF}$.

[13] Applies to three-statable pins with internal pull-downs: LxDAT7–0, LxCLK, and LxACK.

[14] Applies to ACK pulled up internally with 2 kΩ during reset or ID2–0 = 00x.

[15] The test program used to measure $I_{DD-INPEAK}$ represents worst-case processor operation and is not sustainable under normal application conditions. Actual internal power measurements made using typical applications are less than specified. For more information, see Power Dissipation on Page 47.

[16] $I_{DD-INHIGH}$ is a composite average based on a range of high activity code. For more information, see Power Dissipation on Page 47.

[17] $I_{DD-INLOW}$ is a composite average based on a range of low activity code. For more information, see Power Dissipation on Page 47.

[18] Idle denotes ADSP-21160N state during execution of IDLE instruction. For more information, see Power Dissipation on Page 47.

[19] Applies to all signal pins.

[20] Guaranteed, but not tested.

TIMING SPECIFICATIONS

The ADSP-21160x DSP's internal clock switches at higher frequencies than the system input clock (CLKIN). To generate the internal clock, the DSP uses an internal phase-locked loop (PLL). This PLL-based clocking minimizes the skew between the system clock (CLKIN) signal and the DSP's internal clock (the clock source for the external port logic and I/O pads).

The ADSP-21160x DSP's internal clock (a multiple of CLKIN) provides the clock signal for timing internal memory, processor core, link ports, serial ports, and external port (as required for read/write strobes in asynchronous access mode). During reset, program the ratio between the DSP's internal clock frequency and external (CLKIN) clock frequency with the CLK_CFG3–0 pins. Even though the internal clock is the clock source for the external port, the external port clock always switches at the CLKIN frequency. To determine switching frequencies for the serial and link ports, divide down the internal clock, using the programmable divider control of each port (TDIVx/RDIVx for the serial ports and LxCLKD1–0 for the link ports).

Note the following definitions of various clock periods that are a function of CLKIN and the appropriate ratio control:

- $t_{CCLK} = (t_{CK}) / CR$
- $t_{LCLK} = (t_{CCLK}) \times LR$
- $t_{SCLK} = (t_{CCLK}) \times SR$

where:

- LCLK = Link Port Clock
- SCLK = Serial Port Clock
- t_{CK} = CLKIN Clock Period
- t_{CCLK} = (Processor) Core Clock Period
- t_{LCLK} = Link Port Clock Period
- t_{SCLK} = Serial Port Clock Period
- CR = Core/CLKIN Ratio (2, 3, or 4:1, determined by CLK_CFG3–0 at reset)
- LR = Link Port/Core Clock Ratio (1, 2, 3, or 4:1, determined by LxCLKD)
- SR = Serial Port/Core Clock Ratio (wide range, determined by × CLKDIV)

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, it is not meaningful to add parameters to derive longer times.

See Figure 33 on Page 49 under Test Conditions for voltage reference levels.

Switching characteristics specify how the processor changes its signals. Circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics describe what the processor will do in a given circumstance. Use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

During processor reset ($\overline{RESET}$ pin low) or software reset (SRST bit in SYSCON register = 1), deassertion ($\overline{MS3–0}$, $\overline{HBG}$, $\overline{DMAGx}$, $\overline{RDx}$, $\overline{WRx}$, $\overline{CIF}$, PAGE, BRST) and three-state (FLAG3-0, LxCLK, LxACK, LxDAT7-0, ACK, REDY, $\overline{PA}$, TFSx, RFSx, TCLKx, RCLKx, DTx, $\overline{BMS}$, TDO, $\overline{EMU}$, DATA) timings differ. These occur asynchronously to CLKIN, and may not meet the specifications published in the timing requirements and switching characteristics tables. The maximum delay for deassertion and three-state is one t_{CK} from $\overline{RESET}$ pin assertion low or setting the SRST bit in SYSCON. During reset the DSP will not respond to $\overline{SBTS}$, $\overline{HBR}$, and MMS accesses. $\overline{HBR}$ asserted before reset will be recognized, but an $\overline{HBG}$ will not be returned by the DSP until after reset is deasserted and the DSP has completed bus synchronization.

Unless otherwise noted, all timing specifications (*Timing Requirements* and *Switching Characteristics*) listed on pages 21 through 46 apply to both ADSP-21160M and ADSP-21160N.

Power-Up Sequencing

For power-up sequencing, see Table 12 and Figure 8. During the power-up sequence of the DSP, differences in the ramp-up rates and activation time between the two power supplies can cause current to flow in the I/O ESD protection circuitry. To prevent this damage to the ESD diode protection circuitry, Analog Devices recommends including a bootstrap Schottky diode (see Figure 9). The bootstrap Schottky diode connected between the V_{DDINT} and V_{DDEXT} power supplies protects the ADSP-21160x from partially powering the V_{DDEXT} supply. Including a Schottky diode will shorten the delay between the supply ramps and thus prevent damage to the ESD diode protection circuitry. With this technique, if the V_{DDINT} rail rises ahead of the V_{DDEXT} rail, the Schottky diode pulls the V_{DDEXT} rail along with the V_{DDINT} rail.

Interrupts

For interrupts, see Table 15 and Figure 12.

Table 15. Interrupts

Parameter		Min	Max	Unit
Timing Requirements				
t_{SIR}	$\overline{IRQ2–0}$ Setup Before CLKIN High[1]	6		ns
t_{HIR}	$\overline{IRQ2–0}$ Hold After CLKIN High[1]	0		ns
t_{IPW}	$\overline{IRQ2–0}$ Pulsewidth[2]	$2+t_{CK}$		ns

[1] Only required for $\overline{IRQx}$ recognition in the following cycle.
[2] Applies only if t_{SIR} and t_{HIR} requirements are not met.

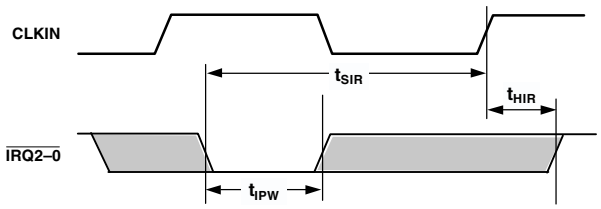

Figure 12. Interrupts

Timer

For timer, see Table 16 and Figure 13.

Table 16. Timer

Parameter		Min	Max	Unit
Switching Characteristic				
t_{DTEX}	CLKIN High to TIMEXP[1]	1	9	ns

[1] For ADSP-21160M, specification is 7 ns, maximum.

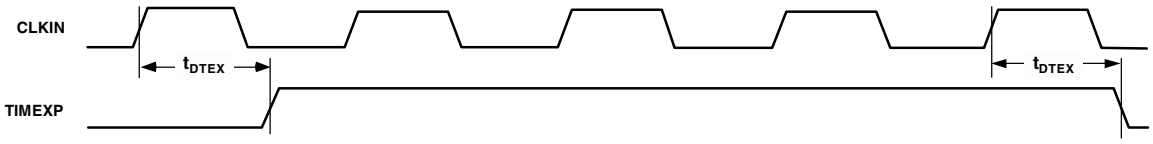

Figure 13. Timer

Flags

For flags, see Table 17 and Figure 14.

Table 17. Flags

Parameter		Min	Max	Unit
Timing Requirements				
t_{SFI}	FLAG3–0 IN Setup Before CLKIN High[1]	4		ns
t_{HFI}	FLAG3–0 IN Hold After CLKIN High[1]	1		ns
t_{DWRFI}	FLAG3–0 IN Delay After $\overline{RDx}$/$\overline{WRx}$ Low[1, 2]		10	ns
t_{HFIWR}	FLAG3–0 IN Hold After $\overline{RDx}$/$\overline{WRx}$ Deasserted[1]	0		ns
Switching Characteristics				
t_{DFO}	FLAG3–0 OUT Delay After CLKIN High		9	ns
t_{HFO}	FLAG3–0 OUT Hold After CLKIN High	1		ns
t_{DFOE}	CLKIN High to FLAG3–0 OUT Enable	1		ns
t_{DFOD}	CLKIN High to FLAG3–0 OUT Disable[3]		$t_{CK} - t_{CCLK} + 5$	ns

[1] Flag inputs meeting these setup and hold times for instruction cycle N will affect conditional instructions in instruction cycle N + 2.
[2] For ADSP-21160M, specification is 12 ns, maximum.
[3] For ADSP-21160M, specification is 5 ns, maximum.

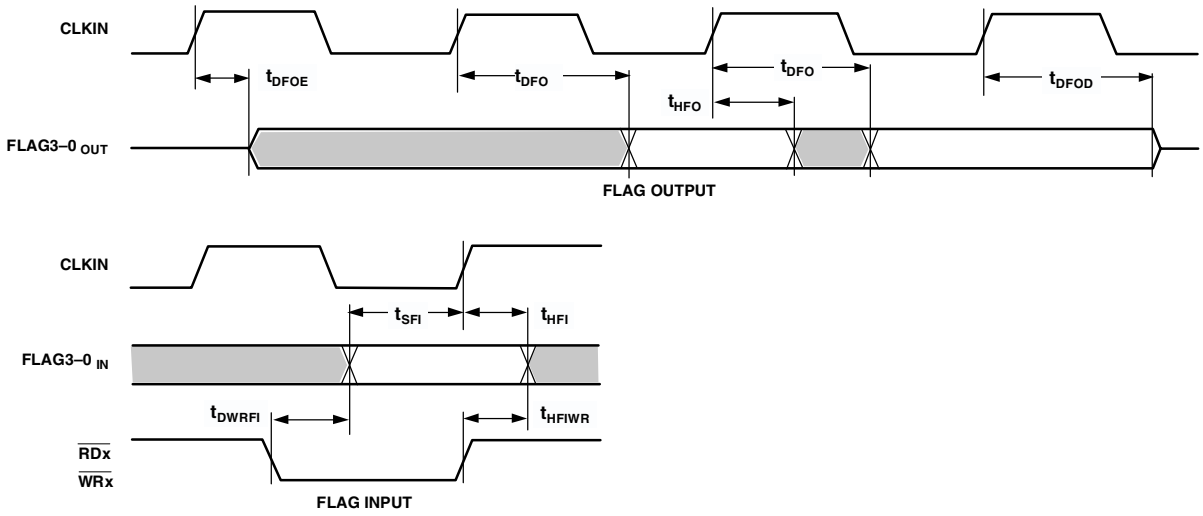

Figure 14. Flags

Memory Write—Bus Master

Use these specifications for asynchronous interfacing to memories (and memory-mapped peripherals) without reference to CLKIN except for the ACK pin requirements listed in note 1 of Table 19. These specifications apply when the ADSP-21160x is the bus master accessing external memory space in asynchronous access mode.

Table 19. Memory Write—Bus Master

Parameter		Min	Max	Unit
Timing Requirements				
t_{DAAK}	ACK Delay from Address, Selects[1, 2]		$t_{CK} - 0.5t_{CCLK} - 12 + W$	ns
t_{DSAK}	ACK Delay from $\overline{WRx}$ Low[1]		$t_{CK} - 0.75t_{CCLK} - 11 + W$	ns
t_{SAKC}	ACK Setup to CLKIN[1]	$0.5t_{CCLK} + 3$		ns
t_{HAKC}	ACK Hold After CLKIN[1]	1		ns
Switching Characteristics				
t_{DAWH}	Address, $\overline{CIF}$, Selects to $\overline{WRx}$ Deasserted[2]	$t_{CK} - 0.25t_{CCLK} - 3 + W$		ns
t_{DAWL}	Address, $\overline{CIF}$, Selects to $\overline{WRx}$ Low[2]	$0.25t_{CCLK} - 3$		ns
t_{WW}	$\overline{WRx}$ Pulsewidth	$t_{CK} - 0.5t_{CCLK} - 1 + W$		ns
t_{DDWH}	Data Setup before $\overline{WRx}$ High[3]	$t_{CK} - 0.5t_{CCLK} - 1 + W$		ns
t_{DWHA}	Address Hold after $\overline{WRx}$ Deasserted	$0.25t_{CCLK} - 1 + H$		ns
t_{DWHD}	Data Hold after $\overline{WRx}$ Deasserted	$0.25t_{CCLK} - 1 + H$		ns
t_{DATRWH}	Data Disable after $\overline{WRx}$ Deasserted[4]	$0.25t_{CCLK} - 2 + H$	$0.25t_{CCLK} + 2 + H$	ns
t_{WWR}	$\overline{WRx}$ High to $\overline{WRx}$, $\overline{RDx}$, $\overline{DMAGx}$ Low	$0.5t_{CCLK} - 1 + HI$		ns
t_{DDWR}	Data Disable before $\overline{WRx}$ or $\overline{RDx}$ Low	$0.25t_{CCLK} - 1 + I$		ns
t_{WDE}	$\overline{WRx}$ Low to Data Enabled	$-0.25t_{CCLK} - 1$		ns

W = (number of wait states specified in WAIT register) × t_{CK}.
H = t_{CK} (if an address hold cycle occurs, as specified in WAIT register; otherwise H = 0).
HI = t_{CK} (if an address hold cycle or bus idle cycle occurs, as specified in WAIT register; otherwise HI = 0).
I = t_{CK} (if a bus idle cycle occurs, as specified in WAIT register; otherwise I = 0).

[1] For asynchronous access, ACK is sampled only after the programmed wait states for the access have been counted. For the first CLKIN cycle of a new external memory access, ACK must be driven low (deasserted) by t_{DAAK} or t_{DSAK} or t_{SAKC}. For the second and subsequent cycles of an asynchronous external memory access, the t_{SAKC} and t_{HAKC} must be met for both assertion and deassertion of ACK signal.
[2] The falling edge of $\overline{MSx}$, $\overline{BMS}$ is referenced.
[3] For ADSP-21160M, specification is $t_{CK} - 0.25t_{CCLK} - 12.5 + W$ ns, minimum.
[4] See Example System Hold Time Calculation on Page 49 for calculation of hold times given capacitive and dc loads.

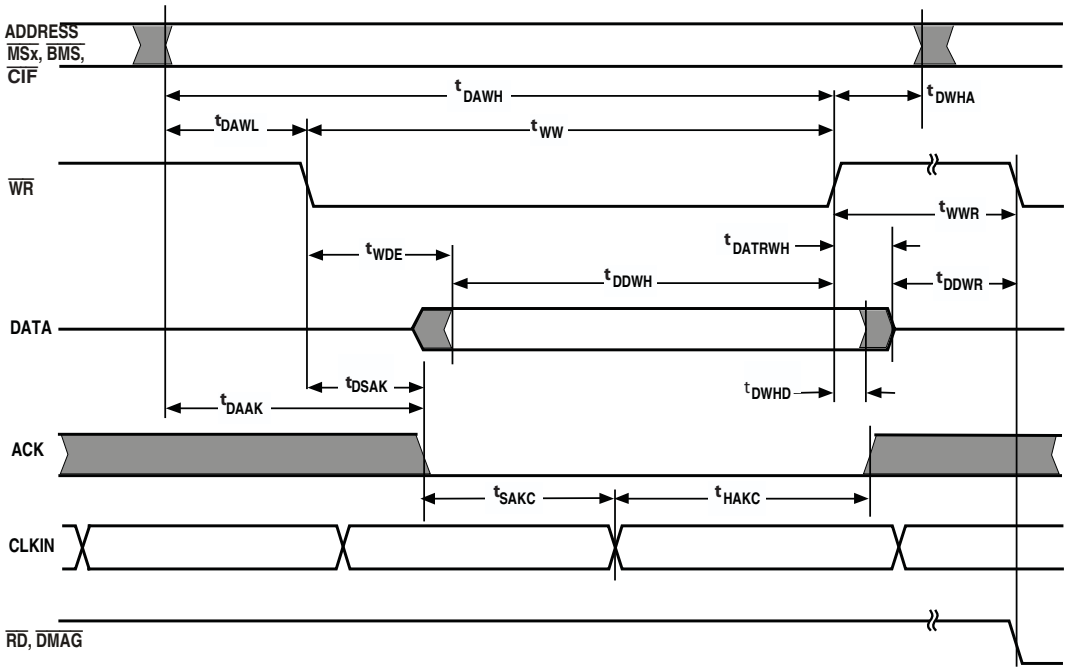

Figure 16. Memory Write—Bus Master

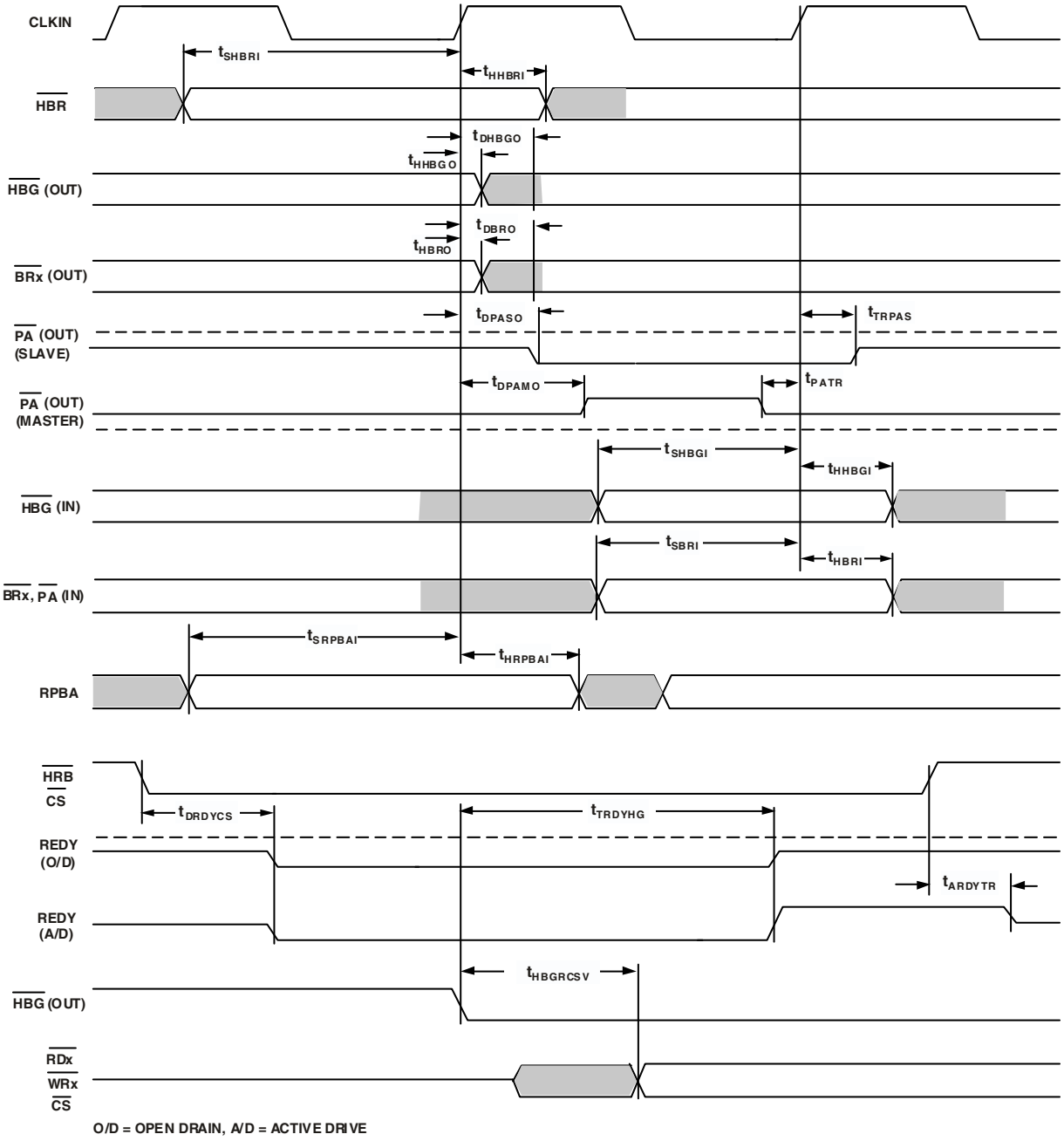

Figure 19. Multiprocessor Bus Request and Host Bus Request

Three-State Timing—Bus Master, Bus Slave

See Table 25 and Figure 22. These specifications show how the memory interface is disabled (stops driving) or enabled (resumes driving) relative to CLKIN and the $\overline{\text{SBTS}}$ pin. This timing is applicable to bus master transition cycles (BTC) and host transition cycles (HTC) as well as the $\overline{\text{SBTS}}$ pin.

Table 25. Three-State Timing—Bus Master, Bus Slave

Parameter		Min	Max	Unit
Timing Requirements				
t_{STSCK}	$\overline{\text{SBTS}}$ Setup Before CLKIN	6		ns
t_{HTSCK}	$\overline{\text{SBTS}}$ Hold After CLKIN[1]	2		ns
Switching Characteristics				
t_{MIENA}	Address/Select Enable After CLKIN	1.5	9	ns
t_{MIENS}	Strobes Enable After CLKIN[2]	1.5	9	ns
t_{MIENHG}	$\overline{\text{HBG}}$ Enable After CLKIN	1.5	9	ns
t_{MITRA}	Address/Select Disable After CLKIN[3]	0.5	9	ns
t_{MITRS}	Strobes Disable After CLKIN[2, 4, 5]	$0.25t_{CCLK} - 4$	$0.25t_{CCLK}+1.5$	ns
t_{MITRHG}	$\overline{\text{HBG}}$ Disable After CLKIN[6]	0.5	8	ns
t_{DATEN}	Data Enable After CLKIN[7, 8]	$0.25t_{CCLK} + 1$	$0.25t_{CCLK} + 7$	ns
t_{DATTR}	Data Disable After CLKIN[7, 9]	0.5	5	ns
t_{ACKEN}	ACK Enable After CLKIN[7]	1.5	9	ns
t_{ACKTR}	ACK Disable After CLKIN[7]	1.5	5	ns
t_{CDCEN}	CLKOUT Enable After CLKIN[10]	0.5	9	ns
t_{CDCTR}	CLKOUT Disable After CLKIN	$t_{CCLK} - 3$	$t_{CCLK}+1$	ns
t_{ATRHBG}	Address, $\overline{\text{MSx}}$ Disable Before $\overline{\text{HBG}}$ Low[11]	$1.5t_{CK} - 6$	$1.5t_{CK} + 5$	ns
t_{STRHBG}	$\overline{\text{RDx}}$, $\overline{\text{WRx}}$, $\overline{\text{DMAGx}}$ Disable Before $\overline{\text{HBG}}$ Low[11]	$t_{CK} + 0.25t_{CCLK} - 6$	$t_{CK} + 0.25t_{CCLK} + 5$	ns
t_{PTRHBG}	Page Disable Before $\overline{\text{HBG}}$ Low[11]	$t_{CK} - 6$	$t_{CK} + 5$	ns
t_{BTRHBG}	$\overline{\text{BMS}}$ Disable Before $\overline{\text{HBG}}$ Low[11]	$0.5t_{CK} - 6.5$	$0.5t_{CK} + 1.5$	ns
t_{MENHBG}	Memory Interface Enable After $\overline{\text{HBG}}$ High[12, 13]	$t_{CK} - 5$	$t_{CK}+6$	ns

[1] For ADSP-21160M, specification is 1 ns, minimum.
[2] Strobes = $\overline{\text{RDx}}$, $\overline{\text{WRx}}$, and $\overline{\text{DMAGx}}$.
[3] For ADSP-21160M, specification is $0.25t_{CCLK}$–1 ns (minimum) and $0.25t_{CCLK}$+4 ns (maximum).
[4] If access aborted by $\overline{\text{SBTS}}$, then strobes disable *before* CLKIN [$0.25t_{CCLK}$ + 1.5 (min.), $0.25t_{CCLK}$ + 5 (max.)]
[5] For ADSP-21160M, specification is $0.25t_{CCLK}$ ns (maximum).
[6] For ADSP-21160M, specification is 3.5 ns (minimum).
[7] In addition to bus master transition cycles, these specs also apply to bus master and bus slave synchronous read/write.
[8] For ADSP-21160M, specification is 1.5 ns (minimum) and 10 ns (maximum).
[9] For ADSP-21160M, specification is 1.5 ns (minimum).
[10] For ADSP-21160M, specification is 0.5 ns (minimum).
[11] Not specified for ADSP-21160M.
[12] Memory Interface = Address, $\overline{\text{RDx}}$, $\overline{\text{WRx}}$, $\overline{\text{MSx}}$, PAGE, $\overline{\text{DMAGx}}$, and $\overline{\text{BMS}}$ (in EPROM boot mode).
[13] For ADSP-21160M, specification is t_{CK}+5 ns (maximum).

DMA Handshake

See Table 26 and Figure 23. These specifications describe the three DMA handshake modes. In all three modes, $\overline{\text{DMARx}}$ is used to initiate transfers. For handshake mode, $\overline{\text{DMAGx}}$ controls the latching or enabling of data externally. For external handshake mode, the data transfer is controlled by the ADDR31–0, $\overline{\text{RDx}}$, $\overline{\text{WRx}}$, PAGE, $\overline{\text{MS3–0}}$, ACK, and $\overline{\text{DMAGx}}$ signals. For Paced Master mode, the data transfer is controlled by ADDR31–0, $\overline{\text{RDx}}$, $\overline{\text{WRx}}$, $\overline{\text{MS3–0}}$, and ACK (not $\overline{\text{DMAGx}}$). For Paced Master mode, the Memory Read-Bus Master, Memory Write-Bus Master, and Synchronous Read/Write-Bus Master timing specifications for ADDR31–0, $\overline{\text{RDx}}$, $\overline{\text{WRx}}$, $\overline{\text{MS3–0}}$, PAGE, DATA63–0, and ACK also apply.

Table 26. DMA Handshake

Parameter		Min	Max	Unit
Timing Requirements				
t_{SDRC}	$\overline{\text{DMARx}}$ Setup Before CLKIN[1]	3		ns
t_{WDR}	$\overline{\text{DMARx}}$ Width Low (Nonsynchronous)[2, 3]	$0.5t_{CCLK}+2.5$		ns
$t_{SDATDGL}$	Data Setup After $\overline{\text{DMAGx}}$ Low[4, 5]		$t_{CK}-0.5t_{CCLK}-7$	ns
$t_{HDATIDG}$	Data Hold After $\overline{\text{DMAGx}}$ High	2		ns
t_{DATDRH}	Data Valid After $\overline{\text{DMARx}}$ High[4, 6]		$t_{CK}+3$	ns
t_{DMARLL}	$\overline{\text{DMARx}}$ Low Edge to Low Edge[7]	t_{CK}		ns
t_{DMARH}	$\overline{\text{DMARx}}$ Width High[2, 8]	$0.5t_{CCLK}+1$		ns
Switching Characteristics				
t_{DDGL}	$\overline{\text{DMAGx}}$ Low Delay After CLKIN	$0.25t_{CCLK}+1$	$0.25t_{CCLK}+9$	ns
t_{WDGH}	$\overline{\text{DMAGx}}$ High Width	$0.5t_{CCLK}-1+\text{HI}$		ns
t_{WDGL}	$\overline{\text{DMAGx}}$ Low Width	$t_{CK}-0.5t_{CCLK}-1$		ns
t_{HDGC}	$\overline{\text{DMAGx}}$ High Delay After CLKIN	$t_{CK}-0.25t_{CCLK}+1.5$	$t_{CK}-0.25t_{CCLK}+9$	ns
$t_{VDATDGH}$	Data Valid Before $\overline{\text{DMAGx}}$ High[9]	$t_{CK}-0.25t_{CCLK}-8$	$t_{CK}-0.25t_{CCLK}+5$	ns
$t_{DATRDGH}$	Data Disable After $\overline{\text{DMAGx}}$ High[10]	$0.25t_{CCLK}-3$	$0.25t_{CCLK}+1.5$	ns
t_{DGWRL}	$\overline{\text{WRx}}$ Low Before $\overline{\text{DMAGx}}$ Low	–1.5	2	ns
t_{DGWRH}	$\overline{\text{DMAGx}}$ Low Before $\overline{\text{WRx}}$ High	$t_{CK}-0.5t_{CCLK}-2+W$		ns
t_{DGWRR}	$\overline{\text{WRx}}$ High Before $\overline{\text{DMAGx}}$ High[11]	–1.5	2	ns
t_{DGRDL}	$\overline{\text{RDx}}$ Low Before $\overline{\text{DMAGx}}$ Low	–1.5	2	ns
t_{DRDGH}	$\overline{\text{RDx}}$ Low Before $\overline{\text{DMAGx}}$ High	$t_{CK}-0.5t_{CCLK}-2+W$		ns
t_{DGRDR}	$\overline{\text{RDx}}$ High Before $\overline{\text{DMAGx}}$ High[11]	–1.5	2	ns
t_{DGWR}	$\overline{\text{DMAGx}}$ High to $\overline{\text{WRx}}$, $\overline{\text{RDx}}$, $\overline{\text{DMAGx}}$ Low	$0.5t_{CCLK}-2+\text{HI}$		ns
t_{DADGH}	Address/Select Valid to $\overline{\text{DMAGx}}$ High[12]	15.5		ns
t_{DDGHA}	Address/Select Hold after $\overline{\text{DMAGx}}$ High	1		ns

W = (number of wait states specified in WAIT register) × t_{CK}.
HI = t_{CK} (if data bus idle cycle occurs, as specified in WAIT register; otherwise HI = 0).

[1] Only required for recognition in the current cycle.
[2] Maximum throughput using $\overline{\text{DMARx}}$ / $\overline{\text{DMAGx}}$ handshaking equals $t_{WDR} + t_{DMARH} = (0.5t_{CCLK}+1) + (0.5t_{CCLK}+1) = 10.0$ ns (100 MHz). This throughput limit applies to non-synchronous access mode only.
[3] For ADSP-21160M, specification is $t_{CCLK}+4.5$ ns, minimum.
[4] $t_{SDATDGL}$ is the data setup requirement if $\overline{\text{DMARx}}$ is not being used to hold off completion of a write. Otherwise, if $\overline{\text{DMARx}}$ low holds off completion of the write, the data can be driven t_{DATDRH} after $\overline{\text{DMARx}}$ is brought high.
[5] For ADSP-21160M, specification is $0.75t_{CCLK}-7$ ns, maximum.
[6] For ADSP-21160M, specification is $t_{CLK}+10$ ns, maximum.
[7] Use t_{DMARLL} if $\overline{\text{DMARx}}$ transitions synchronous with CLKIN. Otherwise, use t_{WDR} and t_{DMARH}.
[8] For ADSP-21160M, specification is $t_{CCLK}+4.5$ ns, minimum.
[9] $t_{VDATDGH}$ is valid if $\overline{\text{DMARx}}$ is not being used to hold off completion of a read. If $\overline{\text{DMARx}}$ is used to prolong the read, then $t_{VDATDGH} = t_{CK} - 0.25t_{CCLK} - 8 + (n \times t_{CK})$ where n equals the number of extra cycles that the access is prolonged.
[10] See Example System Hold Time Calculation on page 49 for calculation of hold times given capacitive and dc loads.
[11] This parameter applies for synchronous access mode only.
[12] For ADSP-21160M, specification is 18 ns, minimum.

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high impedance state to when they start driving. The output enable time t_{ENA} is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in the output enable/disable diagram (Figure 31). If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

Example System Hold Time Calculation

To determine the data output hold time in a particular system, first calculate t_{DECAY} using the equation given above. Choose ΔV to be the difference between the ADSP-21160x DSP's output voltage and the input threshold for the device requiring the hold time. A typical ΔV will be 0.4 V. C_L is the total bus capacitance (per data line), and I_L is the total leakage or three-state current (per data line). The hold time will be t_{DECAY} plus the minimum disable time (i.e., t_{DATRWH} for the write cycle).

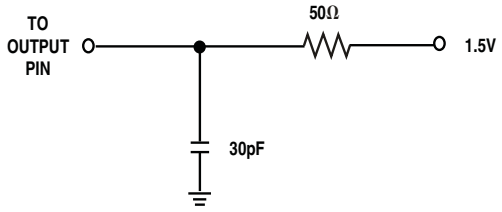

Figure 32. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

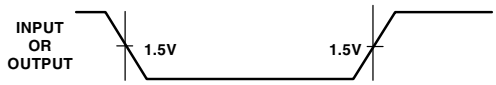

Figure 33. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Capacitive Loading

Output delays and holds are based on standard capacitive loads: 30 pF on all pins (see Figure 32). Figure 34, Figure 35, Figure 37, and Figure 38 show how output rise time varies with capacitance. Figure 36 and Figure 39 graphically show how output delays and holds vary with load capacitance. (Note that this graph or derating does not apply to output disable delays; see Output Disable Time on Page 48.) The graphs of Figure 34 through Figure 39 may not be linear outside the ranges shown.

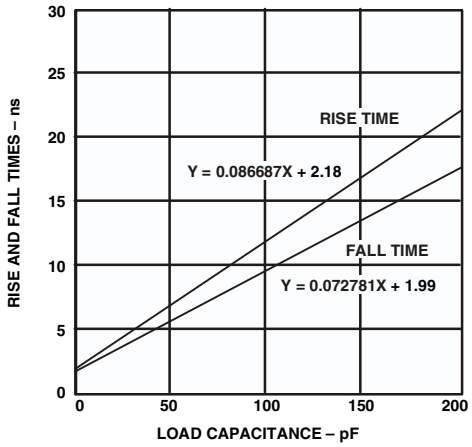

Figure 34. ADSP-21160M Typical Output Rise Time (10%–90%, V_{DDEXT} = Max) vs. Load Capacitance

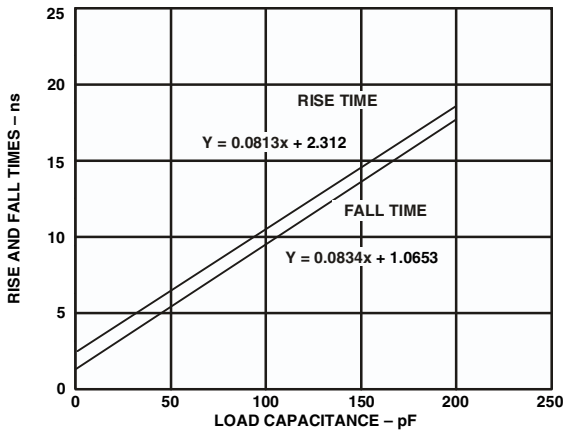

Figure 35. ADSP-21160M Typical Output Rise Time (10%–90%, V_{DDEXT} = Min) vs. Load Capacitance

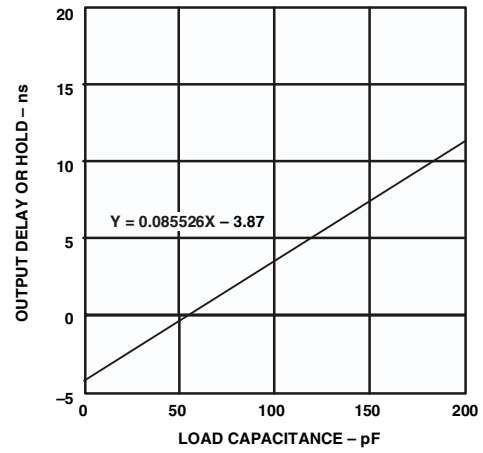

Figure 36. ADSP-21160M Typical Output Delay or Hold vs. Load Capacitance (at Max Case Temperature)

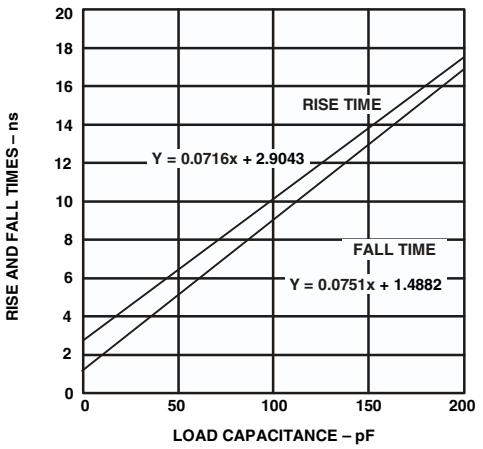

Figure 37. ADSP-21160N Typical Output Rise Time (20%–80%, V_{DDEXT} = Max) vs. Load Capacitance

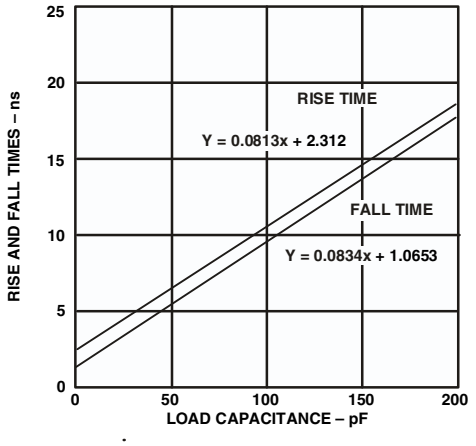

Figure 38. ADSP-21160N Typical Output Rise Time (20%–80%, V_{DDEXT} = Min) vs. Load Capacitance

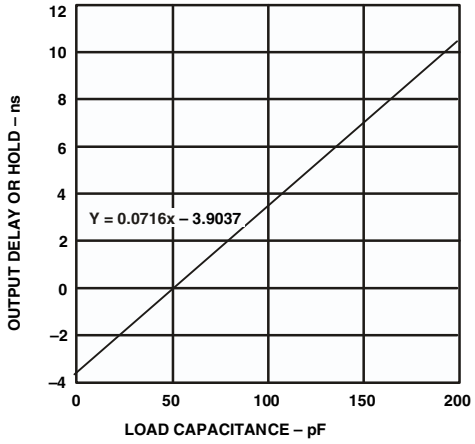

Figure 39. ADSP-21160N Typical Output Delay or Hold vs. Load Capacitance (at Max Case Temperature)