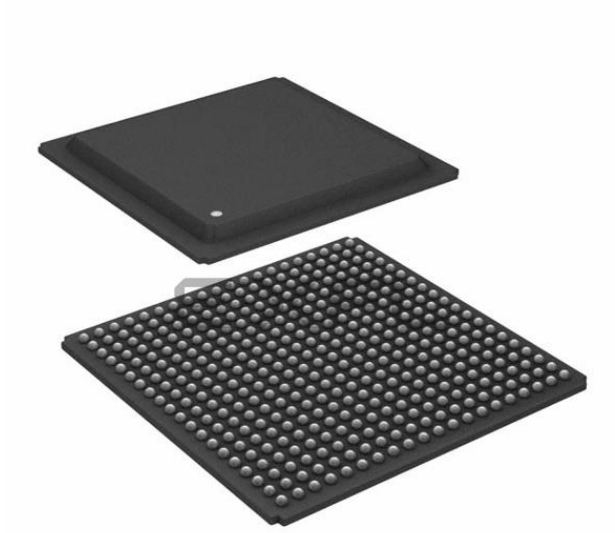

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Floating Point
Interface	Host Interface, Link Port, Serial Port
Clock Rate	100MHz
Non-Volatile Memory	External
On-Chip RAM	512kB
Voltage - I/O	3.30V
Voltage - Core	1.90V
Operating Temperature	-40°C ~ 100°C (TC)
Mounting Type	Surface Mount
Package / Case	400-BBGA
Supplier Device Package	400-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21160ncbz-100

located on the web page for the associated EZ-KIT or EZ-Extender product. The link is found in the *Product Download* area of the product web page.

Middleware Packages

Analog Devices separately offers middleware add-ins such as real time operating systems, file systems, USB stacks, and TCP/IP stacks. For more information, see the following web pages:

- www.analog.com/ucos3
- www.analog.com/ucfs
- www.analog.com/ucusbd
- www.analog.com/lwip

Algorithmic Modules

To speed development, Analog Devices offers add-ins that perform popular audio and video processing algorithms. These are available for use with both CrossCore Embedded Studio and VisualDSP++. For more information visit www.analog.com and search on "Blackfin software modules" or "SHARC software modules".

Designing an Emulator-Compatible DSP Board (Target)

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG Test Access Port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the processor's internal features via the processor's TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers. The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the DSP's JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see the application note (EE-68) "Analog Devices JTAG Emulation Technical Reference" (www.analog.com/ee-68). This document is updated regularly to keep pace with improvements to emulator support.

ADDITIONAL INFORMATION

This data sheet provides a general overview of the ADSP-21160x architecture and functionality. For detailed information on the Blackfin family core architecture and instruction set, refer to the *ADSP-21160 SHARC DSP Hardware Reference* and the *ADSP-21160 SHARC DSP Instruction Set Reference*. For detailed information on the development tools for this processor, see the *VisualDSP++ User's Guide*.

RELATED SIGNAL CHAINS

A signal chain is a series of signal conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next.

Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The application signal chains page in the Circuits from the Lab® site (http:\\www.analog.com\circuits) provides:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

Table 3. Pin Function Descriptions (Continued)

Pin	Type	Function
CLKOUT	O/T	Local Clock Out. CLKOUT is driven at the CLKIN frequency by the processor. This output can be three-stated by setting the COD bit in the SYSCON register. A keeper latch on the DSP's CLKOUT pin maintains the output at the level it was last driven (only enabled on the processor with ID2-0 = 00x). Do not use CLKOUT in multiprocessing systems; use CLKIN instead.
$\overline{\text{RESET}}$	I/A	Processor Reset. Resets the ADSP-21160x to a known state and begins execution at the program memory location specified by the hardware reset vector address. The $\overline{\text{RESET}}$ input must be asserted (low) at power-up.
TCK	I	Test Clock (JTAG). Provides a clock for JTAG boundary scan.
TMS	I/S	Test Mode Select (JTAG). Used to control the test state machine. TMS has a 20 kΩ internal pull-up resistor.
TDI	I/S	Test Data Input (JTAG). Provides serial data for the boundary scan logic. TDI has a 20 kΩ internal pull-up resistor.
TDO	O	Test Data Output (JTAG). Serial scan output of the boundary scan path.
$\overline{\text{TRST}}$	I/A	Test Reset (JTAG). Resets the test state machine. $\overline{\text{TRST}}$ must be asserted (pulsed low) after power-up or held low for proper operation of the ADSP-21160x. $\overline{\text{TRST}}$ has a 20 kΩ internal pull-up resistor.
$\overline{\text{EMU}}$	O (O/D)	Emulation Status. Must be connected to the ADSP-21160x emulator target board connector only. $\overline{\text{EMU}}$ has a 50 kΩ internal pull-up resistor.
$\overline{\text{CIF}}$	O/T	Core Instruction Fetch. Signal is active low when an external instruction fetch is performed. Driven by bus master only. Three-state when host is bus master. $\overline{\text{CIF}}$ has a 20 kΩ internal pull-up resistor that is enabled on the ADSP-21160x with ID2–0 = 00x.
V_{DDINT}	P	Core Power Supply. Nominally 2.5 V (ADSP-21160M) or 1.9 V (ADSP-21160N) dc and supplies the DSP's core processor
V_{DDEXT}	P	I/O Power Supply. Nominally 3.3 V dc.
AV_{DD}	P	Analog Power Supply. Nominally 2.5 V (ADSP-21160M) or 1.9 V (ADSP-21160N) dc and supplies the DSP's internal PLL (clock generator). This pin has the same specifications as V_{DDINT}, except that added filtering circuitry is required. For more information, see Power Supplies on page 9.
AGND	G	Analog Power Supply Return.
GND	G	Power Supply Return.
NC		Do Not Connect. Reserved pins that must be left open and unconnected.

Table 4. Boot Mode Selection

EBOOT	LBOOT	$\overline{\text{BMS}}$	Booting Mode
1	0	Output	EPROM (Connect $\overline{\text{BMS}}$ to EPROM chip select.)
0	0	1 (Input)	Host Processor
0	1	1 (Input)	Link Port
0	0	0 (Input)	No Booting. Processor executes from external memory.
0	1	0 (Input)	Reserved
1	1	x (Input)	Reserved

ELECTRICAL CHARACTERISTICS—ADSP-21160M

Table 6 shows ADSP-21160M electrical characteristics. These specifications are subject to change without notification.

Table 6. Electrical Characteristics—ADSP-21160M

Parameter		Test Conditions	Min	Max	Unit
V_{OH}	High Level Output Voltage[1]	@ V_{DDEXT} = Min, I_{OH} = –2.0 mA[2]	2.4		V
V_{OL}	Low Level Output Voltage[1]	@ V_{DDEXT} = Min, I_{OL} = 4.0 mA[2]		0.4	V
I_{IH}	High Level Input Current[3, 4, 5]	@ V_{DDEXT} = Max, V_{IN} = V_{DD} Max		10	µA
I_{IL}	Low Level Input Current[3]	@ V_{DDEXT} = Max, V_{IN} = 0 V		10	µA
I_{ILPU1}	Low Level Input Current Pull-Up1[4]	@ V_{DDEXT} = Max, V_{IN} = 0 V		250	µA
I_{ILPU2}	Low Level Input Current Pull-Up2[5]	@ V_{DDEXT} = Max, V_{IN} = 0 V		500	µA
I_{OZH}	Three-State Leakage Current[6, 7, 8, 9]	@ V_{DDEXT} = Max, V_{IN} = V_{DD} Max		10	µA
I_{OZL}	Three-State Leakage Current[6]	@ V_{DDEXT} = Max, V_{IN} = 0 V		10	µA
I_{OZHPD}	Three-State Leakage Current Pull-Down[9]	@ V_{DDEXT} = Max, V_{IN} = V_{DD} Max		250	µA
I_{OZLPU1}	Three-State Leakage Current Pull-Up1[7]	@ V_{DDEXT} = Max, V_{IN} = 0 V		250	µA
I_{OZLPU2}	Three-State Leakage Current Pull-Up2[8]	@ V_{DDEXT} = Max, V_{IN} = 0 V		500	µA
I_{OZHA}	Three-State Leakage Current[10]	@ V_{DDEXT} = Max, V_{IN} = V_{DD} Max		25	µA
I_{OZLA}	Three-State Leakage Current[10]	@ V_{DDEXT} = Max, V_{IN} = 0 V		4	mA
$I_{DD-INPEAK}$	Supply Current (Internal)[11]	t_{CCLK} = 12.5 ns, V_{DDINT} = Max		1400	mA
$I_{DD-INHIGH}$	Supply Current (Internal)[12]	t_{CCLK} = 12.5 ns, V_{DDINT} = Max		875	mA
$I_{DD-INLOW}$	Supply Current (Internal)[13]	t_{CCLK} = 12.5 ns, V_{DDINT} = Max		625	mA
$I_{DD-IDLE}$	Supply Current (Idle)[14]	t_{CCLK} = 12.5 ns, V_{DDINT} = Max		400	mA
AI_{DD}	Supply Current (Analog)[15]	@AV_{DD} = Max		10	mA
C_{IN}	Input Capacitance[16, 17]	f_{IN} = 1 MHz, T_{CASE} = 25°C, V_{IN} = 2.5 V		4.7	pF

[1] Applies to output and bidirectional pins: DATA63–0, ADDR31–0, $\overline{MS3–0}$, $\overline{RDx}$, $\overline{WRx}$, PAGE, CLKOUT, ACK, FLAG3–0, TIMEXP, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BR6–1}$, $\overline{PA}$, BRST, $\overline{CIF}$, DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, LxDAT7–0, LxCLK, LxACK, $\overline{BMS}$, TDO, and $\overline{EMU}$.

[2] See Output Drive Currents—ADSP-21160M on Page 47 for typical drive current capabilities.

[3] Applies to input pins: $\overline{SBTS}$, $\overline{IRQ2–0}$, $\overline{HBR}$, $\overline{CS}$, ID2–0, RPBA, EBOOT, LBOOT, CLKIN, $\overline{RESET}$, TCK, and CLK_CFG3-0.

[4] Applies to input pins with internal pull-ups: DR0, and DR1.

[5] Applies to input pins with internal pull-ups: $\overline{DMARx}$, TMS, TDI, and $\overline{TRST}$.

[6] Applies to three-statable pins: DATA63–0, ADDR31–0, PAGE, CLKOUT, ACK, FLAG3–0, REDY, $\overline{HBG}$, $\overline{BMS}$, $\overline{BR6–1}$, TFSx, RFSx, and TDO.

[7] Applies to three-statable pins with internal pull-ups: DTx, TCLKx, RCLKx, and $\overline{EMU}$.

[8] Applies to three-statable pins with internal pull-ups: $\overline{MS3–0}$,$\overline{RDx}$, $\overline{WRx}$, $\overline{DMAGx}$, $\overline{PA}$, and $\overline{CIF}$.

[9] Applies to three-statable pins with internal pull-downs: LxDAT7–0, LxCLK, and LxACK.

[10] Applies to ACK pulled up internally with 2 kΩ during reset or ID2–0 = 00x.

[11] The test program used to measure $I_{DD-INPEAK}$ represents worst-case processor operation and is not sustainable under normal application conditions. Actual internal power measurements made using typical applications are less than specified. For more information, see Power Dissipation on Page 47.

[12] $I_{DD-INHIGH}$ is a composite average based on a range of high activity code. For more information, see Power Dissipation on Page 47.

[13] $I_{DD-INLOW}$ is a composite average based on a range of low activity code. For more information, see Power Dissipation on Page 47.

[14] Idle denotes ADSP-21160M state during execution of IDLE instruction. For more information, see Power Dissipation on Page 47.

[15] Characterized, but not tested.

[16] Applies to all signal pins.

[17] Guaranteed, but not tested.

OPERATING CONDITIONS—ADSP-21160N

Table 7 shows recommended operating conditions for the ADSP-21160N. These specifications are subject to change without notice.

Table 7. Operating Conditions—ADSP-21160N

Parameter		C Grade Min	C Grade Max	K Grade Min	K Grade Max	Unit
V_{DDINT}	Internal (Core) Supply Voltage	1.8	2.0	1.8	2.0	V
AV_{DD}	Analog (PLL) Supply Voltage	1.8	2.0	1.8	2.0	V
V_{DDEXT}	External (I/O) Supply Voltage	3.13	3.47	3.13	3.47	V
T_{CASE}	Case Operating Temperature[1]	–40	+100	0	85	°C
V_{IH1}	High Level Input Voltage,[2] @ V_{DDEXT}=Max	2.0	V_{DDEXT}+0.5	2.0	V_{DDEXT}+0.5	V
V_{IH2}	High Level Input Voltage,[3] @ V_{DDEXT}=Max	2.0	V_{DDEXT}+0.5	2.0	V_{DDEXT}+0.5	V
V_{IL}	Low Level Input Voltage[2, 3] @ V_{DDEXT}=Min	–0.5	+0.8	–0.5	+0.8	V

[1] See Environmental Conditions on Page 51 for information on thermal specifications.

[2] Applies to input and bidirectional pins: DATA63–0, ADDR31–0, $\overline{RDx}$, $\overline{WRx}$, ACK, $\overline{SBTS}$, $\overline{IRQ2–0}$, FLAG3–0, $\overline{HBG}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $\overline{BR6–1}$, ID2–0, RPBA, $\overline{PA}$, BRST, TFS0, TFS1, RFS0, RFS1, LxDAT7–0, LxCLK, LxACK, EBOOT, LBOOT, $\overline{BMS}$, TMS, TDI, TCK, $\overline{HBR}$, DR0, DR1, TCLK0, TCLK1, RCLK0, and RCLK1.

[3] Applies to input pins: CLKIN, $\overline{RESET}$, and $\overline{TRST}$.

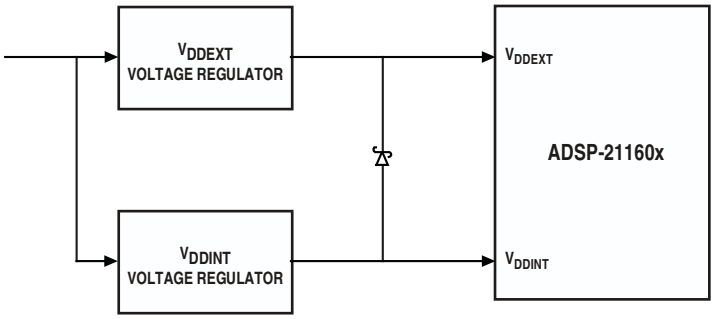


Figure 9. Dual Voltage Schottky Diode

Clock Input

For clock input, see Table 13 and Figure 10.

Table 13. Clock Input

Parameter		ADSP-21160M 80 MHz		ADSP-21160N 100 MHz		Unit
		Min	Max	Min	Max	
Timing Requirements						
t_{CK}	CLKIN Period	25	80	20	80	ns
t_{CKL}	CLKIN Width Low	10.5	40	7.5	40	ns
t_{CKH}	CLKIN Width High	10.5	40	7.5	40	ns
t_{CKRF}	CLKIN Rise/Fall (0.4 V–2.0 V)		3		3	ns
t_{CCLK}	Core Clock Period	12.5	40	10	30	ns

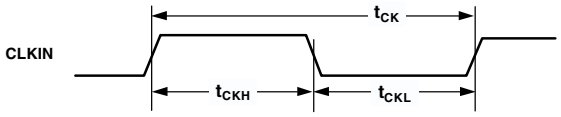


Figure 10. Clock Input

Reset

For reset, see Table 14 and Figure 11.

Table 14. Reset

Parameter		Min	Max	Unit
Timing Requirements				
t_{WRST}	$\overline{\text{RESET}}$ Pulsewidth Low[1]	$4t_{CK}$		ns
t_{SRST}	$\overline{\text{RESET}}$ Setup Before CLKIN High[2]	8		ns

[1] Applies after the power-up sequence is complete. At power-up, the processor's internal phase-locked loop requires no more than 100 µs while $\overline{\text{RESET}}$ is low, assuming stable V_{DD} and CLKIN (not including start-up time of external clock oscillator).

[2] Only required if multiple ADSP-21160x DSPs must come out of reset synchronous to CLKIN with program counters (PC) equal. Not required for multiple ADSP-21160x DSPs communicating over the shared bus (through the external port), because the bus arbitration logic automatically synchronizes itself after reset.

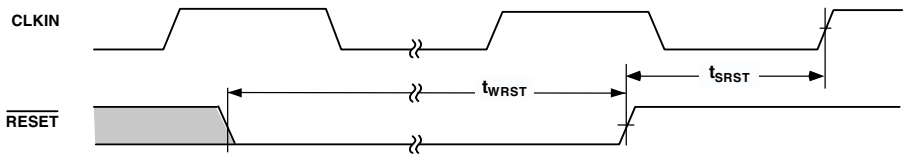


Figure 11. Reset

Interrupts

For interrupts, see Table 15 and Figure 12.

Table 15. Interrupts

Parameter		Min	Max	Unit
Timing Requirements				
t_{SIR}	$\overline{IRQ2–0}$ Setup Before CLKIN High[1]	6		ns
t_{HIR}	$\overline{IRQ2–0}$ Hold After CLKIN High[1]	0		ns
t_{IPW}	$\overline{IRQ2–0}$ Pulsewidth[2]	$2+t_{CK}$		ns

[1] Only required for $\overline{IRQx}$ recognition in the following cycle.
[2] Applies only if t_{SIR} and t_{HIR} requirements are not met.

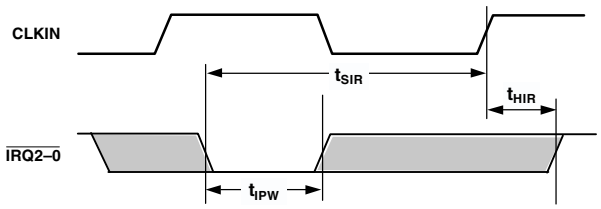


Figure 12. Interrupts

Timer

For timer, see Table 16 and Figure 13.

Table 16. Timer

Parameter		Min	Max	Unit
Switching Characteristic				
t_{DTEX}	CLKIN High to TIMEXP[1]	1	9	ns

[1] For ADSP-21160M, specification is 7 ns, maximum.

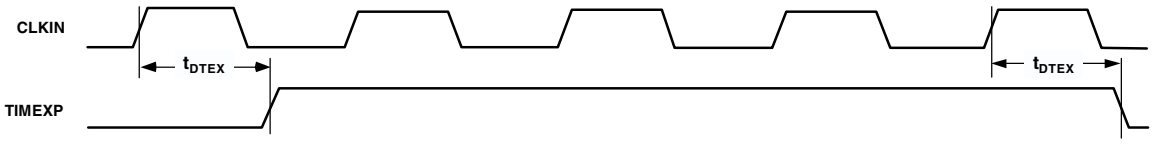


Figure 13. Timer

Memory Write—Bus Master

Use these specifications for asynchronous interfacing to memories (and memory-mapped peripherals) without reference to CLKIN except for the ACK pin requirements listed in note 1 of Table 19. These specifications apply when the ADSP-21160x is the bus master accessing external memory space in asynchronous access mode.

Table 19. Memory Write—Bus Master

Parameter		Min	Max	Unit
Timing Requirements				
t_{DAAK}	ACK Delay from Address, Selects[1, 2]		$t_{CK} - 0.5t_{CCLK} - 12 + W$	ns
t_{DSAK}	ACK Delay from $\overline{WRx}$ Low[1]		$t_{CK} - 0.75t_{CCLK} - 11 + W$	ns
t_{SAKC}	ACK Setup to CLKIN[1]	$0.5t_{CCLK} + 3$		ns
t_{HAKC}	ACK Hold After CLKIN[1]	1		ns
Switching Characteristics				
t_{DAWH}	Address, $\overline{CIF}$, Selects to $\overline{WRx}$ Deasserted[2]	$t_{CK} - 0.25t_{CCLK} - 3 + W$		ns
t_{DAWL}	Address, $\overline{CIF}$, Selects to $\overline{WRx}$ Low[2]	$0.25t_{CCLK} - 3$		ns
t_{WW}	$\overline{WRx}$ Pulsewidth	$t_{CK} - 0.5t_{CCLK} - 1 + W$		ns
t_{DDWH}	Data Setup before $\overline{WRx}$ High[3]	$t_{CK} - 0.5t_{CCLK} - 1 + W$		ns
t_{DWHA}	Address Hold after $\overline{WRx}$ Deasserted	$0.25t_{CCLK} - 1 + H$		ns
t_{DWHD}	Data Hold after $\overline{WRx}$ Deasserted	$0.25t_{CCLK} - 1 + H$		ns
t_{DATRWH}	Data Disable after $\overline{WRx}$ Deasserted[4]	$0.25t_{CCLK} - 2 + H$	$0.25t_{CCLK} + 2 + H$	ns
t_{WWR}	$\overline{WRx}$ High to $\overline{WRx}$, $\overline{RDx}$, $\overline{DMAGx}$ Low	$0.5t_{CCLK} - 1 + HI$		ns
t_{DDWR}	Data Disable before $\overline{WRx}$ or $\overline{RDx}$ Low	$0.25t_{CCLK} - 1 + I$		ns
t_{WDE}	$\overline{WRx}$ Low to Data Enabled	$-0.25t_{CCLK} - 1$		ns

W = (number of wait states specified in WAIT register) × t_{CK}.
H = t_{CK} (if an address hold cycle occurs, as specified in WAIT register; otherwise H = 0).
HI = t_{CK} (if an address hold cycle or bus idle cycle occurs, as specified in WAIT register; otherwise HI = 0).
I = t_{CK} (if a bus idle cycle occurs, as specified in WAIT register; otherwise I = 0).

[1] For asynchronous access, ACK is sampled only after the programmed wait states for the access have been counted. For the first CLKIN cycle of a new external memory access, ACK must be driven low (deasserted) by t_{DAAK} or t_{DSAK} or t_{SAKC}. For the second and subsequent cycles of an asynchronous external memory access, the t_{SAKC} and t_{HAKC} must be met for both assertion and deassertion of ACK signal.
[2] The falling edge of $\overline{MSx}$, $\overline{BMS}$ is referenced.
[3] For ADSP-21160M, specification is $t_{CK} - 0.25t_{CCLK} - 12.5 + W$ ns, minimum.
[4] See Example System Hold Time Calculation on Page 49 for calculation of hold times given capacitive and dc loads.

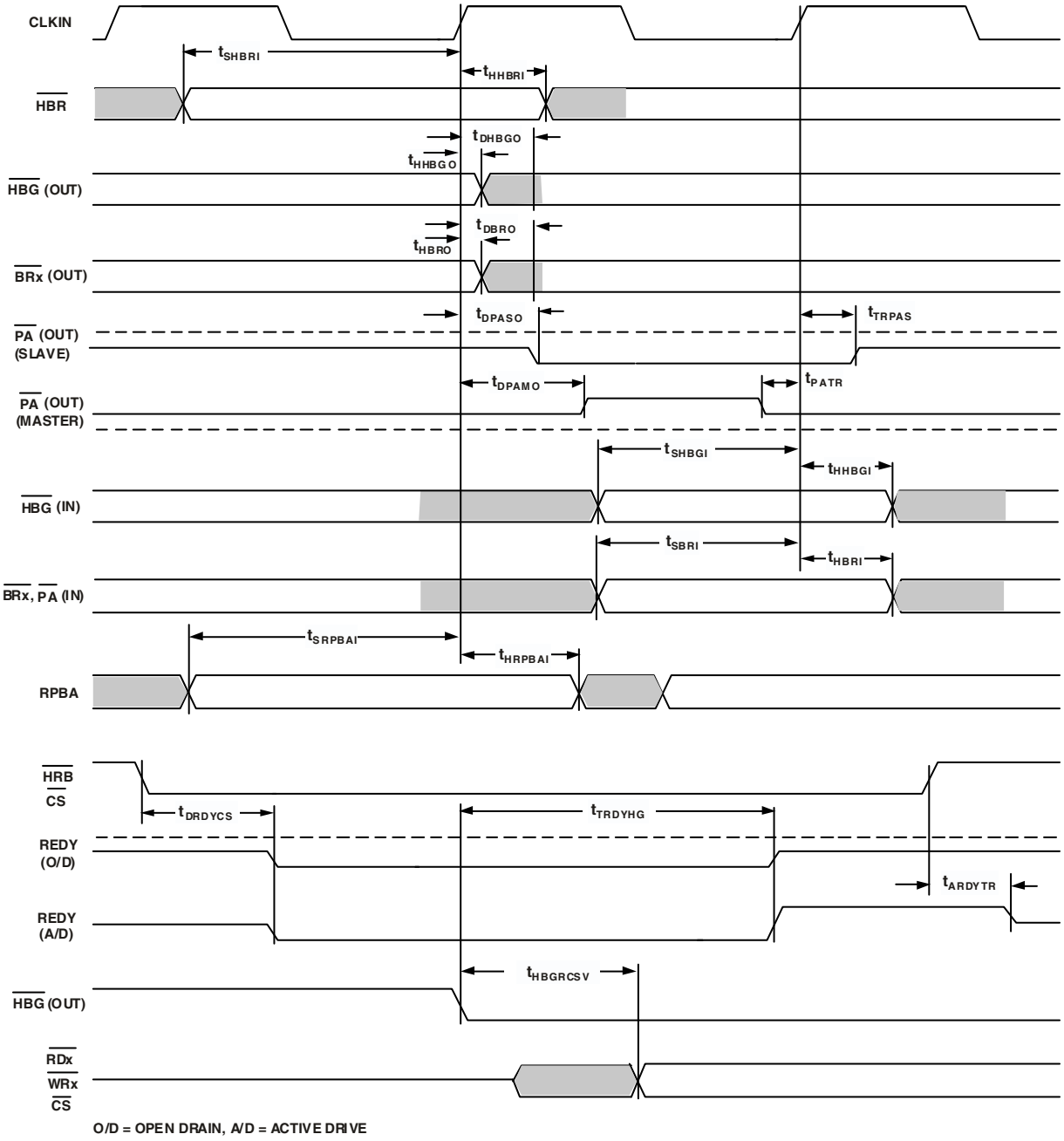


Figure 19. Multiprocessor Bus Request and Host Bus Request

Asynchronous Read/Write—Host to ADSP-21160x

Use these specifications (Table 23, Table 24, Figure 20, and Figure 21) for asynchronous host processor accesses of an ADSP-21160x, after the host has asserted $\overline{CS}$ and $\overline{HBR}$ (low). After $\overline{HBG}$ is returned by the ADSP-21160x, the host can drive the $\overline{RDx}$ and $\overline{WRx}$ pins to access the ADSP-21160x DSP's internal memory or IOP registers. $\overline{HBR}$ and $\overline{HBG}$ are assumed low for this timing.

Table 23. Read Cycle

Parameter		Min	Max	Unit
Timing Requirements				
t_{SADRDL}	Address Setup/$\overline{CS}$ Low Before $\overline{RDx}$ Low	0		ns
t_{HADRDH}	Address Hold/$\overline{CS}$ Hold Low After $\overline{RDx}$	2		ns
t_{WRWH}	$\overline{RDx}$/$\overline{WRx}$ High Width	5		ns
$t_{DRDHRDY}$	$\overline{RDx}$ High Delay After REDY (O/D) Disable	0		ns
$t_{DRDHRDY}$	$\overline{RDx}$ High Delay After REDY (A/D) Disable	0		ns
Switching Characteristics				
$t_{SDATRDY}$	Data Valid Before REDY Disable from Low	2		ns
$t_{DRDYRDL}$	REDY (O/D) or (A/D) Low Delay After $\overline{RDx}$ Low[1]		11	ns
t_{RDYPRD}	REDY (O/D) or (A/D) Low Pulsewidth for Read[2]	t_{CK} – 4		ns
t_{HDARWH}	Data Disable After $\overline{RDx}$ High[3]	1.5	6	ns

[1] For ADSP-21160M, specification is 7 ns, minimum.
[2] For ADSP-21160M, specification is t_{CK} ns, minimum.
[3] For ADSP-21160M, specification is 2 ns, minimum.

Table 24. Write Cycle

Parameter		Min	Max	Unit
Timing Requirements				
t_{SCSWRL}	$\overline{CS}$ Low Setup Before $\overline{WRx}$ Low	0		ns
t_{HCSWRH}	$\overline{CS}$ Low Hold After $\overline{WRx}$ High	0		ns
t_{SADWRH}	Address Setup Before $\overline{WRx}$ High	6		ns
t_{HADWRH}	Address Hold After $\overline{WRx}$ High	2		ns
t_{WWRL}	$\overline{WRx}$ Low Width[1]	t_{CCLK}+1		ns
t_{WRWH}	$\overline{RDx}$/$\overline{WRx}$ High Width	5		ns
$t_{DWRHRDY}$	$\overline{WRx}$ High Delay After REDY (O/D) or (A/D) Disable	0		ns
t_{SDATWH}	Data Setup Before $\overline{WRx}$ High	5		ns
t_{HDATWH}	Data Hold After $\overline{WRx}$ High	4		ns
Switching Characteristics				
$t_{DRDYWRL}$	REDY (O/D) or (A/D) Low Delay After $\overline{WRx}$/$\overline{CS}$ Low		11	ns
t_{RDYPWR}	REDY (O/D) or (A/D) Low Pulsewidth for Write[2]	5.75 + 0.5t_{CCLK}		ns

[1] For ADSP-21160M, specification is 7 ns, minimum.
[2] For ADSP-21160M, specification is 12 ns, minimum.

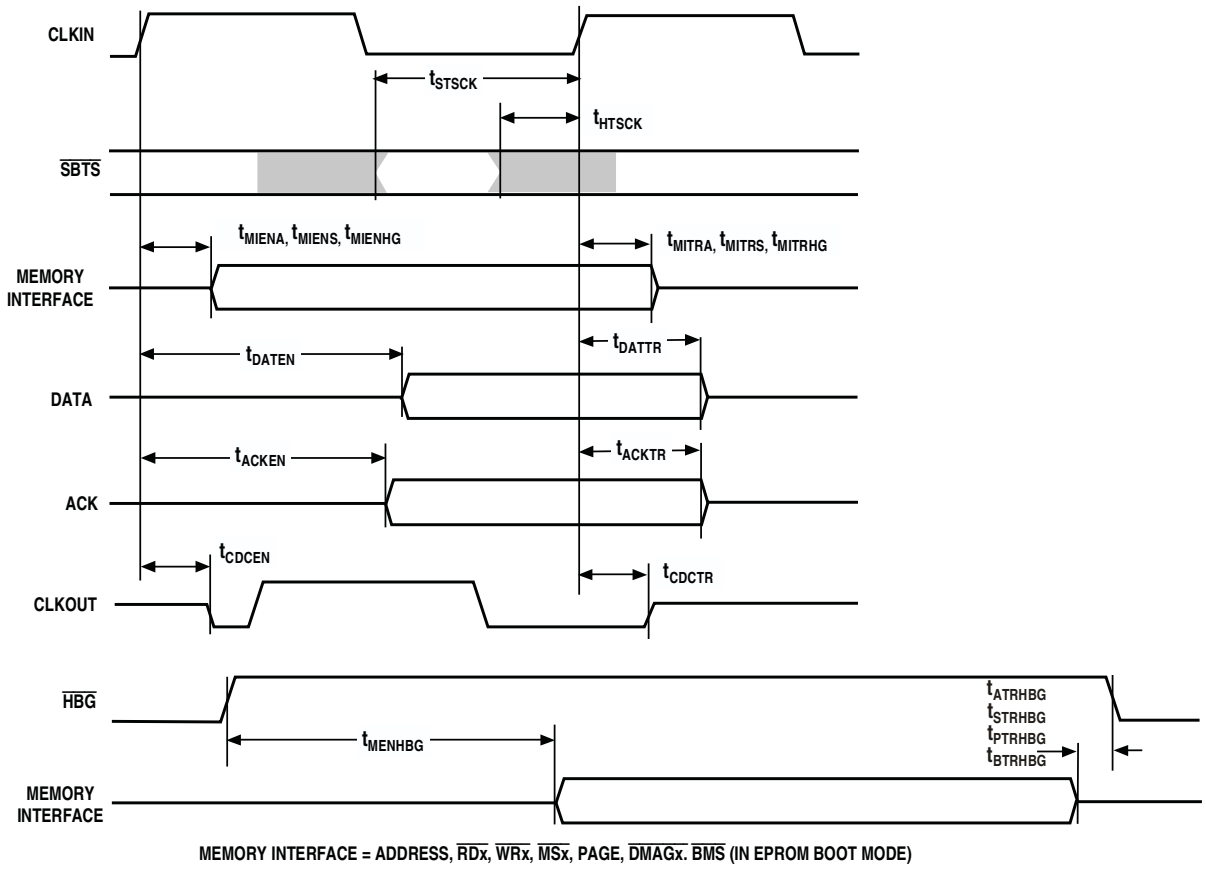
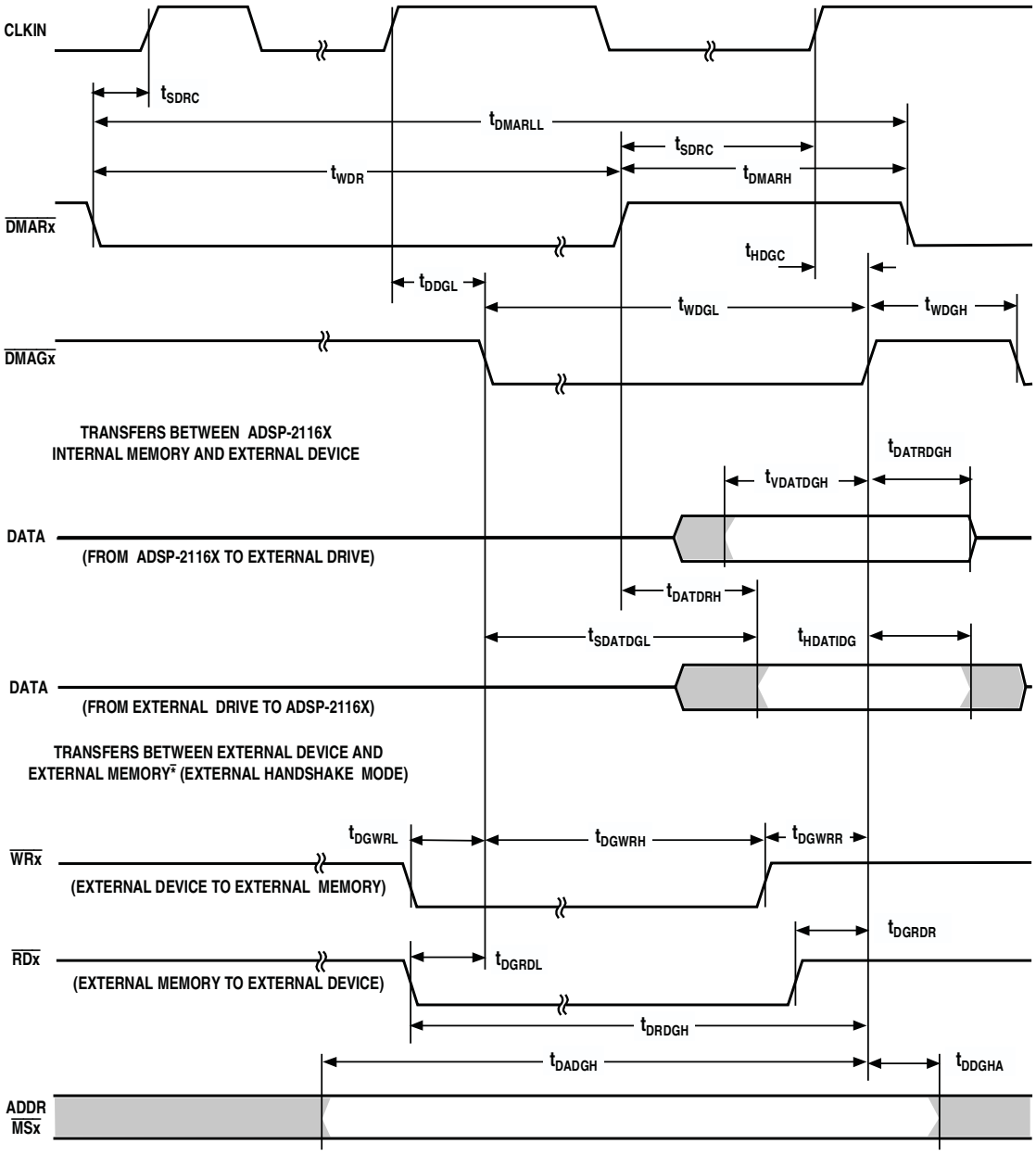


Figure 22. Three-State Timing—Bus Master, Bus Slave



* MEMORY READ BUS MASTER, MEMORY WRITE BUS MASTER, OR SYNCHRONOUS READ/WRITE BUS MASTER TIMING SPECIFICATIONS FOR ADDR31–0, RDx, WRx, MS3–0 AND ACK ALSO APPLY HERE.

Figure 23. DMA Handshake

Table 33. Serial Ports—Enable and Three-State

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DDTEN}	Data Enable from External TCLK[1]	4		ns
t_{DDTTE}	Data Disable from External TCLK[1]		10	ns
t_{DDTIN}	Data Enable from Internal TCLK[1]	0		ns
t_{DDTTI}	Data Disable from Internal TCLK[1]		3	ns

[1] Referenced to drive edge.

Table 34. Serial Ports—Internal Clock

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DFSI}	TFS Delay After TCLK (Internally Generated TFS)[1]		4.5	ns
t_{HOFSI}	TFS Hold After TCLK (Internally Generated TFS)[1]	–1.5		ns
t_{DDTI}	Transmit Data Delay After TCLK[1]		7.5	ns
t_{HDTI}	Transmit Data Hold After TCLK[1]	0		ns
t_{SCLKIW}	TCLK/RCLK Width[2]	$0.5t_{SCLK}$ –1.5	$0.5t_{SCLK}$+1.5	ns

[1] Referenced to drive edge.
[2] For ADSP-21160M, specification is $0.5t_{SCLK}$–2.5 ns (minimum) and $0.5t_{SCLK}$+2 ns (maximum)

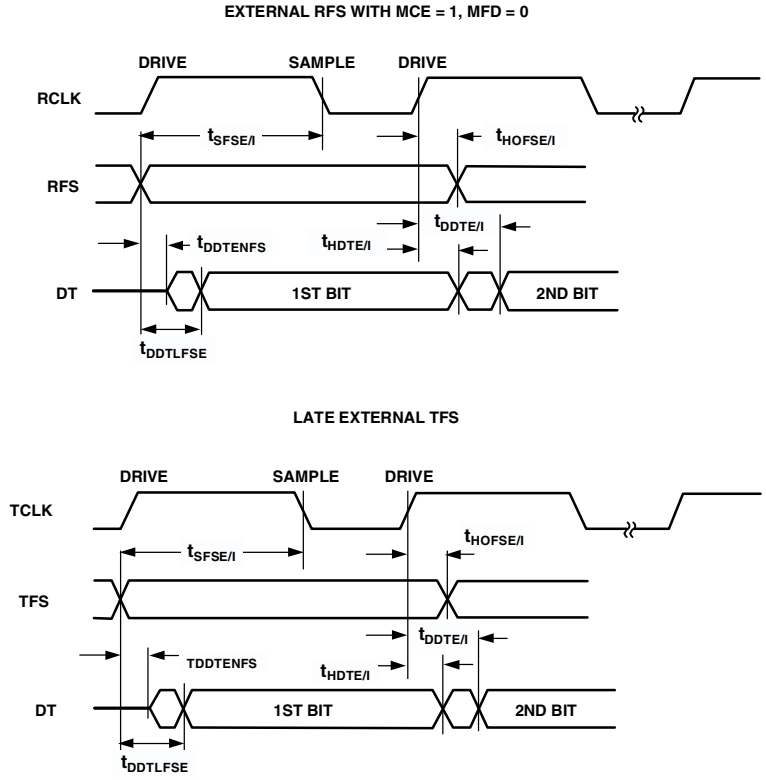


Figure 26. Serial Ports—External Late Frame Sync

JTAG Test Access Port and Emulation

For JTAG Test Access Port and emulation, see Table 36 and Figure 28.

Table 36. JTAG Test Access Port and Emulation

Parameter		Min	Max	Unit
Timing Requirements				
t_{TCK}	TCK Period	t_{CK}		ns
t_{STAP}	TDI, TMS Setup Before TCK High	5		ns
t_{HTAP}	TDI, TMS Hold After TCK High	6		ns
t_{SSYS}	System Inputs Setup Before TCK Low[1]	7		ns
t_{HSYS}	System Inputs Hold After TCK Low[1]	18		ns
t_{TRSTW}	$\overline{TRST}$ Pulsewidth	$4t_{CK}$		ns
Switching Characteristics				
t_{DTDO}	TDO Delay from TCK Low		13	ns
t_{DSYS}	System Outputs Delay After TCK Low[2]		30	ns

[1] System Inputs = DATA63–0, ADDR31–0, $\overline{RDx}$, $\overline{WRx}$, ACK, $\overline{SBTS}$, $\overline{HBR}$, $\overline{HBG}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $\overline{BR6–1}$, ID2–0, RPBA, $\overline{IRQ2–0}$, FLAG3–0, $\overline{PA}$, BRST, DR0, DR1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, LxDAT7–0, LxCLK, LxACK, EBOOT, LBOOT, $\overline{BMS}$, CLKIN, and $\overline{RESET}$.

[2] System Outputs = DATA63–0, ADDR31–0, $\overline{MS3–0}$, $\overline{RDx}$, $\overline{WRx}$, ACK, PAGE, CLKOUT, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BR6–1}$, $\overline{PA}$, BRST, $\overline{CIF}$, FLAG3–0, TIMEXP, DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, LxDAT7–0, LxCLK, LxACK, and $\overline{BMS}$.

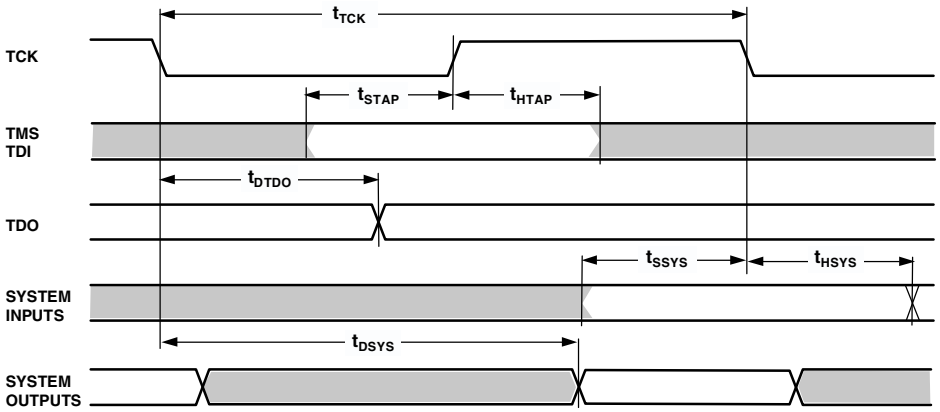


Figure 28. JTAG Test Access Port and Emulation

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high impedance state to when they start driving. The output enable time t_{ENA} is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in the output enable/disable diagram (Figure 31). If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

Example System Hold Time Calculation

To determine the data output hold time in a particular system, first calculate t_{DECAY} using the equation given above. Choose ΔV to be the difference between the ADSP-21160x DSP's output voltage and the input threshold for the device requiring the hold time. A typical ΔV will be 0.4 V. C_L is the total bus capacitance (per data line), and I_L is the total leakage or three-state current (per data line). The hold time will be t_{DECAY} plus the minimum disable time (i.e., t_{DATRWH} for the write cycle).

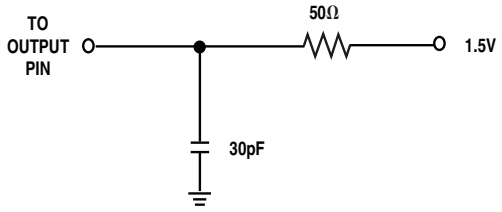


Figure 32. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

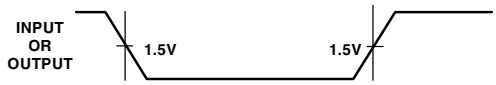


Figure 33. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Capacitive Loading

Output delays and holds are based on standard capacitive loads: 30 pF on all pins (see Figure 32). Figure 34, Figure 35, Figure 37, and Figure 38 show how output rise time varies with capacitance. Figure 36 and Figure 39 graphically show how output delays and holds vary with load capacitance. (Note that this graph or derating does not apply to output disable delays; see Output Disable Time on Page 48.) The graphs of Figure 34 through Figure 39 may not be linear outside the ranges shown.

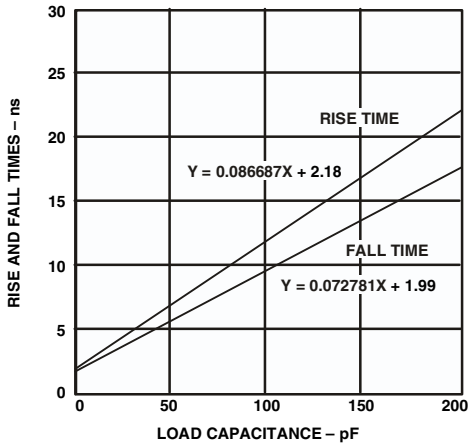


Figure 34. ADSP-21160M Typical Output Rise Time (10%–90%, V_{DDEXT} = Max) vs. Load Capacitance

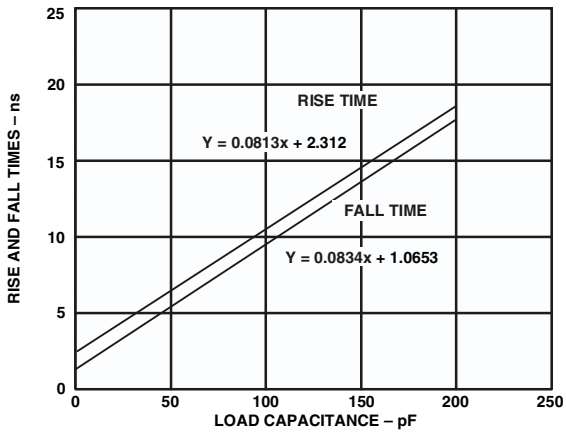


Figure 35. ADSP-21160M Typical Output Rise Time (10%–90%, V_{DDEXT} = Min) vs. Load Capacitance

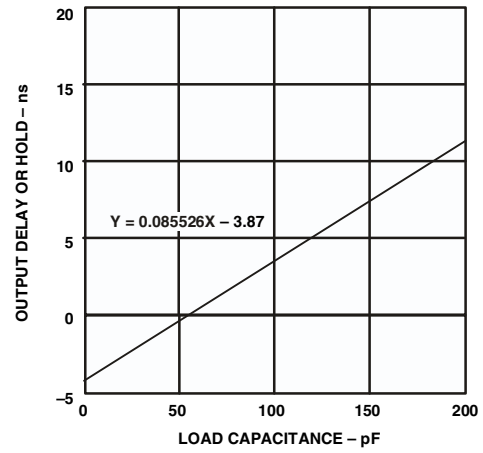


Figure 36. ADSP-21160M Typical Output Delay or Hold vs. Load Capacitance (at Max Case Temperature)

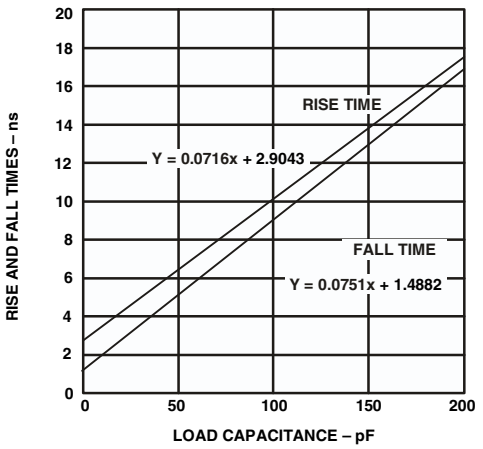


Figure 37. ADSP-21160N Typical Output Rise Time (20%–80%, V_{DDEXT} = Max) vs. Load Capacitance

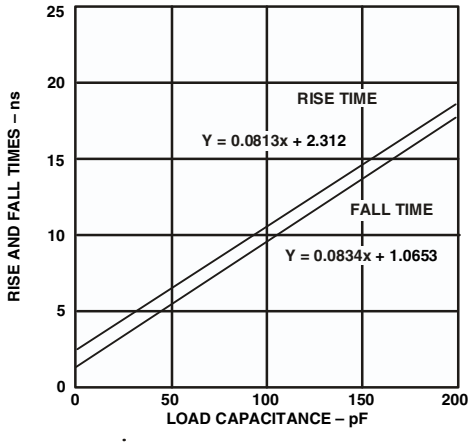


Figure 38. ADSP-21160N Typical Output Rise Time (20%–80%, V_{DDEXT} = Min) vs. Load Capacitance

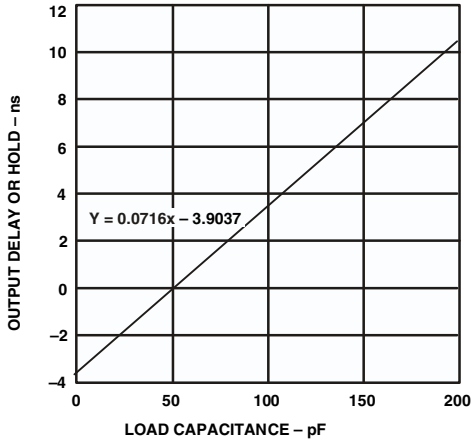


Figure 39. ADSP-21160N Typical Output Delay or Hold vs. Load Capacitance (at Max Case Temperature)

Table 40. 400-Ball PBGA Pin Assignments (Continued)

(See Footnotes 1 and 2)							
Pin Name	**Pin No.**	**Pin Name**	**Pin No.**	**Pin Name**	**Pin No.**	**Pin Name**	**Pin No.**
DATA[44]	J01	CLK_CFG_0	K01	CLKIN	L01	AV_{DD}	M01
DATA[43]	J02	DATA[46]	K02	CLK_CFG_1	L02	CLK_CFG_3	M02
DATA[42]	J03	DATA[45]	K03	AGND	L03	CLKOUT	M03
DATA[41]	J04	DATA[47]	K04	CLK_CFG_2	L04	NC[2]	M04
V_{DDEXT}	J05	V_{DDEXT}	K05	V_{DDEXT}	L05	V_{DDEXT}	M05
V_{DDINT}	J06	V_{DDINT}	K06	V_{DDINT}	L06	V_{DDINT}	M06
GND	J07	GND	K07	GND	L07	GND	M07
GND	J08	GND	K08	GND	L08	GND	M08
GND	J09	GND	K09	GND	L09	GND	M09
GND	J10	GND	K10	GND	L10	GND	M10
GND	J11	GND	K11	GND	L11	GND	M11
GND	J12	GND	K12	GND	L12	GND	M12
GND	J13	GND	K13	GND	L13	GND	M13
GND	J14	GND	K14	GND	L14	GND	M14
V_{DDINT}	J15	V_{DDINT}	K15	V_{DDINT}	L15	V_{DDINT}	M15
V_{DDEXT}	J16	V_{DDEXT}	K16	V_{DDEXT}	L16	V_{DDEXT}	M16
L2DAT[2]	J17	$\overline{BR6}$	K17	$\overline{BR2}$	L17	PAGE	M17
L2DAT[0]	J18	$\overline{BR5}$	K18	$\overline{BR1}$	L18	$\overline{SBTS}$	M18
$\overline{HBG}$	J19	$\overline{BR4}$	K19	ACK	L19	$\overline{PA}$	M19
$\overline{HBR}$	J20	$\overline{BR3}$	K20	REDY	L20	L3DAT[7]	M20
NC	N01	DATA[49]	P01	DATA[53]	R01	DATA[56]	T01
NC	N02	DATA[50]	P02	DATA[54]	R02	DATA[58]	T02
DATA[48]	N03	DATA[52]	P03	DATA[57]	R03	DATA[59]	T03
DATA[51]	N04	DATA[55]	P04	DATA[60]	R04	DATA[63]	T04
V_{DDEXT}	N05	V_{DDEXT}	P05	V_{DDEXT}	R05	V_{DDEXT}	T05
V_{DDINT}	N06	V_{DDINT}	P06	V_{DDINT}	R06	V_{DDINT}	T06
GND	N07	GND	P07	GND	R07	V_{DDINT}	T07
GND	N08	GND	P08	GND	R08	V_{DDINT}	T08
GND	N09	GND	P09	GND	R09	V_{DDINT}	T09
GND	N10	GND	P10	GND	R10	V_{DDINT}	T10
GND	N11	GND	P11	GND	R11	V_{DDINT}	T11
GND	N12	GND	P12	GND	R12	V_{DDINT}	T12
GND	N13	GND	P13	GND	R13	V_{DDINT}	T13
GND	N14	GND	P14	GND	R14	V_{DDINT}	T14
V_{DDINT}	N15	V_{DDINT}	P15	GND	R15	V_{DDINT}	T15
V_{DDEXT}	N16	V_{DDEXT}	P16	V_{DDEXT}	R16	V_{DDEXT}	T16
L3DAT[5]	N17	L3DAT[2]	P17	L4DAT[5]	R17	L4DAT[3]	T17
L3DAT[6]	N18	L3DAT[1]	P18	L4DAT[6]	R18	L4ACK	T18
L3DAT[4]	N19	L3DAT[3]	P19	L4DAT[7]	R19	L4CLK	T19
L3CLK	N20	L3ACK	P20	L3DAT[0]	R20	L4DAT[4]	T20
DATA[61]	U01	ADDR[4]	V01	ADDR[5]	W01	ADDR[8]	Y01
DATA[62]	U02	ADDR[6]	V02	ADDR[9]	W02	ADDR[11]	Y02
ADDR[3]	U03	ADDR[7]	V03	ADDR[12]	W03	ADDR[13]	Y03
ADDR[2]	U04	ADDR[10]	V04	ADDR[15]	W04	ADDR[16]	Y04
V_{DDEXT}	U05	ADDR[14]	V05	ADDR[17]	W05	ADDR[19]	Y05
V_{DDEXT}	U06	ADDR[18]	V06	ADDR[20]	W06	ADDR[21]	Y06

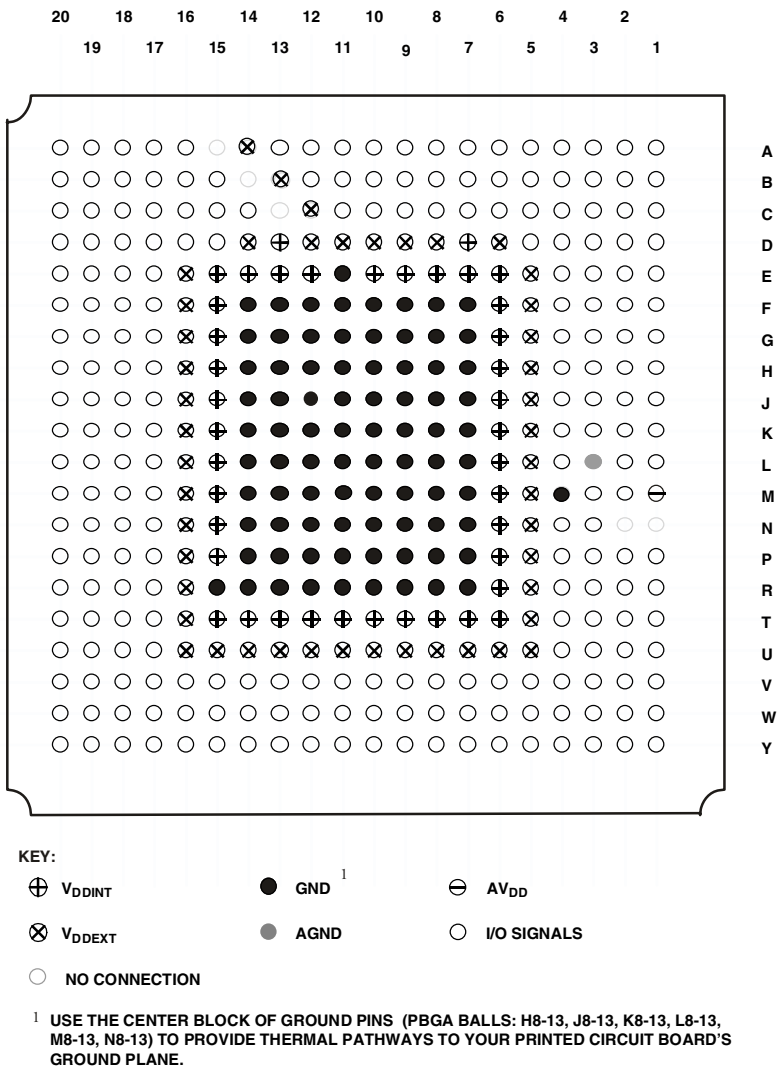


Figure 40. ADSP-21160M 400-Ball PBGA Pin Configurations (Bottom View, Summary)

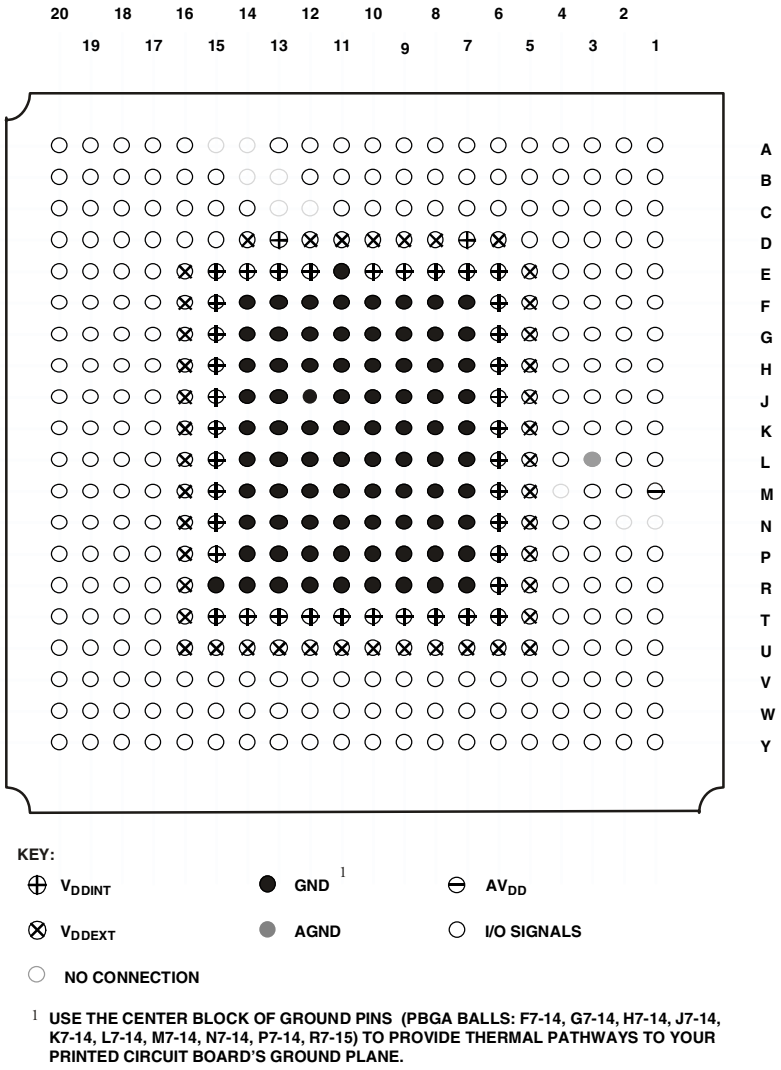


Figure 41. ADSP-21160N 400-Ball PBGA Pin Configurations (Bottom View, Summary)

ORDERING GUIDE

Model	Notes	Temperature Range	Instruction Rate	On-Chip SRAM	Package Description	Package Option
ADSP-21160MKBZ-80	[1]	0°C to +85°C	80 MHz	4M bits	400-Ball Plastic Ball Grid Array (PBGA)	B-400
ADSP-21160MKB-80		0°C to +85°C	80 MHz	4M bits	400-Ball Plastic Ball Grid Array (PBGA)	B-400
ADSP-21160NCBZ-100	[1]	–40°C to +100°C	100 MHz	4M bits	400-Ball Plastic Ball Grid Array (PBGA)	B-400
ADSP-21160NCB-100		–40°C to +100°C	100 MHz	4M bits	400-Ball Plastic Ball Grid Array (PBGA)	B-400
ADSP-21160NKBZ-100	[1]	0°C to +85°C	100 MHz	4M bits	400-Ball Plastic Ball Grid Array (PBGA)	B-400

[1] Z = RoHS Compliant Part.