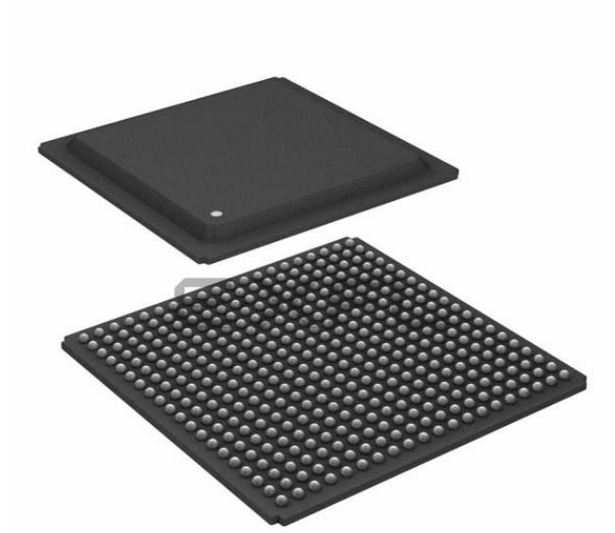

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Floating Point
Interface	Host Interface, Link Port, Serial Port
Clock Rate	100MHz
Non-Volatile Memory	External
On-Chip RAM	512kB
Voltage - I/O	3.30V
Voltage - Core	1.90V
Operating Temperature	0°C ~ 85°C (TC)
Mounting Type	Surface Mount
Package / Case	400-BBGA
Supplier Device Package	400-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21160nkb-100

GENERAL DESCRIPTION

The ADSP-21160x SHARC® DSP family has two members: ADSP-21160M and ADSP-21160N. The ADSP-21160M is fabricated in a 0.25 micron CMOS process. The ADSP-21160N is fabricated in a 0.18 micron CMOS process. The ADSP-21160N offers higher performance and lower power consumption than the ADSP-21160M. Easing portability, the ADSP-21160x is application source code compatible with first generation ADSP-2106x SHARC DSPs in SISD (single instruction, single data) mode. To take advantage of the processor's SIMD (single-instruction, multiple-data) capability, some code changes are needed. Like other SHARC DSPs, the ADSP-21160x is a 32-bit processor that is optimized for high performance DSP applications. The ADSP-21160x includes a core running up to 100 MHz, a dual-ported on-chip SRAM, an integrated I/O processor with multiprocessing support, and multiple internal buses to eliminate I/O bottlenecks.

Table 1 shows major differences between the ADSP-21160M and ADSP-21160N processors.

Table 1. ADSP-21160x SHARC Processor Family Features

Feature	ADSP-21160M	ADSP-21160N
SRAM	4 Mbits	4 Mbits
Operating Voltage	3.3 V I/O 2.5 V Core	3.3 V I/O 1.9 V Core
Instruction Rate	80 MHz	100 MHz
Link Port Transfer Rate (6)	80 MBytes/s	100 MBytes/s
Serial Port Transfer Rate (2)	40 Mbits/s	50 Mbits/s

The ADSP-21160x introduces single-instruction, multiple-data (SIMD) processing. Using two computational units (ADSP-2106x SHARC DSPs have one), the ADSP-21160x can double performance versus the ADSP-2106x on a range of DSP algorithms.

Fabricated in a state-of-the-art, high speed, low power CMOS process, the ADSP-21160N has a 10 ns instruction cycle time. With its SIMD computational hardware running at 100 MHz, the ADSP-21160N can perform 600 million math operations per second (480 million operations for ADSP-21160M at a 12.5 ns instruction cycle time).

Table 2 shows performance benchmarks for the ADSP-21160x.

These benchmarks provide single-channel extrapolations of measured dual-channel (SIMD) processing performance. For more information on benchmarking and optimizing DSP code for single- and dual-channel processing, see the Analog Devices website (www.analog.com).

The ADSP-21160x continues the SHARC family's industry-leading standards of integration for DSPs, combining a high performance 32-bit DSP core with integrated, on-chip system features. These features include a 4M-bit dual-ported SRAM memory, host processor interface, I/O processor that supports 14 DMA channels, two serial ports, six link ports, external parallel bus, and glueless multiprocessing.

Table 2. ADSP-21160x Benchmarks

Benchmark Algorithm	ADSP-21160M 80 MHz	ADSP-21160N 100 MHz
1024 Point Complex FFT (Radix 4, with reversal)	115 µs	92 µs
FIR Filter (per tap)	6.25 ns	5 ns
IIR Filter (per biquad)	25 ns	20 ns
Matrix Multiply (pipelined)		
[3×3] × [3×1]	56.25 ns	45 ns
[4×4] × [4×1]	100 ns	80 ns
Divide (y/x)	37.5 ns	30 ns
Inverse Square Root	56.25 ns	45 ns
DMA Transfer Rate	560M bytes/s	800M bytes/s

The functional block diagram (Figure 1 on Page 1) of the ADSP-21160x illustrates the following architectural features:

- Two processing elements, each made up of an ALU, multiplier, shifter, and data register file
- Data address generators (DAG1, DAG2)
- Program sequencer with instruction cache
- PM and DM buses capable of supporting four 32-bit data transfers between memory and the core every core processor cycle
- Interval timer
- On-chip SRAM (4M bits)
- External port that supports:
  - Interfacing to off-chip memory peripherals
  - Glueless multiprocessing support for six ADSP-21160x SHARC DSPs
  - Host port
- DMA controller
- Serial ports and link ports
- JTAG test access port

Figure 2 shows a typical single-processor system. A multiprocessing system appears in Figure 3 on Page 6.

ADSP-21160X FAMILY CORE ARCHITECTURE

The ADSP-21160x processor includes the following architectural features of the ADSP-2116x family core. The ADSP-21160x is code compatible at the assembly level with the ADSP-2106x and ADSP-21161.

SIMD Computational Engine

The ADSP-21160x contains two computational processing elements that operate as a single-instruction multiple-data (SIMD) engine. The processing elements are referred to as PEX and PEY, and each contains an ALU, multiplier, shifter, and register file. PEX is always active, and PEY may be enabled by setting the PEYEN mode bit in the MODE1 register. When this mode is

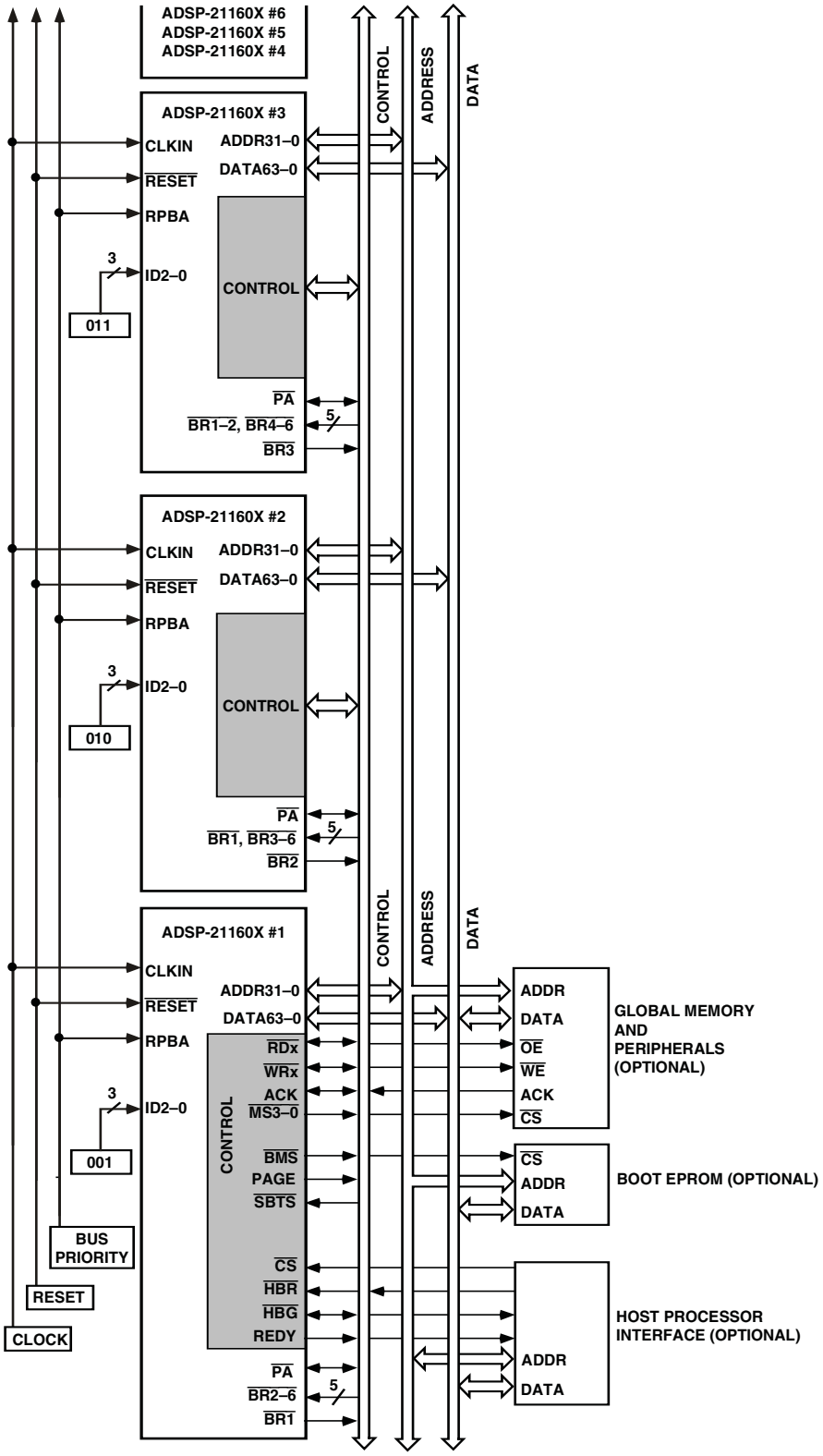

Figure 3. Shared Memory Multiprocessing System

Program Booting

The internal memory of the ADSP-21160x can be booted at system power-up from an 8-bit EPROM, a host processor, or through one of the link ports. Selection of the boot source is controlled by the $\overline{\text{BMS}}$ (Boot Memory Select), EBOOT (EPROM Boot), and LBOOT (Link/Host Boot) pins. 32-bit and 16-bit host processors can be used for booting.

Phase-Locked Loop

The processor uses an on-chip PLL to generate the internal clock for the core. Ratios of 2:1, 3:1, and 4:1 between the core and CLKIN are supported. The CLK_CFG pins are used to select the ratio. The CLKIN rate is the rate at which the synchronous external port operates.

Power Supplies

The processor has separate power supply connections for the internal (V_{DDINT}), external (V_{DDEXT}), and analog (AV_{DD} and AGND) power supplies. The internal and analog supplies must meet the V_{DDINT} and AV_{DD} requirement. The external supply must meet the 3.3 V requirement. All external supply pins must be connected to the same supply.

The PLL filter, Figure 6, must be added for each ADSP-21160x in the system. V_{DDINT} is the digital core supply. It is recommended that the capacitors be connected directly to AGND using short thick trace. It is recommended that the capacitors be placed as close to AV_{DD} and AGND as possible. The connection from AGND to the (digital) ground plane should be made after the capacitors. The use of a thick trace for AGND is reasonable only because the PLL is a relatively low power circuit—it does not apply to any other ADSP-21160x GND connection.

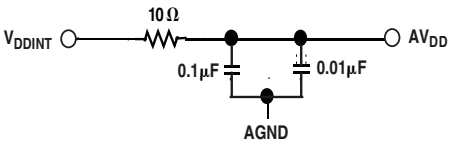

Figure 6. Analog Power (AV_{DD}) Filter Circuit

DEVELOPMENT TOOLS

Analog Devices supports its processors with a complete line of software and hardware development tools, including integrated development environments (which include CrossCore® Embedded Studio and/or VisualDSP++®), evaluation products, emulators, and a wide variety of software add-ins.

Integrated Development Environments (IDEs)

For C/C++ software writing and editing, code generation, and debug support, Analog Devices offers two IDEs.

The newest IDE, CrossCore Embedded Studio, is based on the Eclipse™ framework. Supporting most Analog Devices processor families, it is the IDE of choice for future processors, including multicore devices. CrossCore Embedded Studio seamlessly integrates available software add-ins to support real time operating systems, file systems, TCP/IP stacks, USB stacks, algorithmic software modules, and evaluation hardware board support packages. For more information visit www.analog.com/cces.

The other Analog Devices IDE, VisualDSP++, supports processor families introduced prior to the release of CrossCore Embedded Studio. This IDE includes the Analog Devices VDK real time operating system and an open source TCP/IP stack. For more information visit www.analog.com/visualdsp. Note that VisualDSP++ will not support future Analog Devices processors.

EZ-KIT Lite Evaluation Board

For processor evaluation, Analog Devices provides wide range of EZ-KIT Lite® evaluation boards. Including the processor and key peripherals, the evaluation board also supports on-chip emulation capabilities and other evaluation and development features. Also available are various EZ-Extenders®, which are daughter cards delivering additional specialized functionality, including audio and video processing. For more information visit www.analog.com and search on “ezkit” or “ezextender”.

EZ-KIT Lite Evaluation Kits

For a cost-effective way to learn more about developing with Analog Devices processors, Analog Devices offer a range of EZ-KIT Lite evaluation kits. Each evaluation kit includes an EZ-KIT Lite evaluation board, directions for downloading an evaluation version of the available IDE(s), a USB cable, and a power supply. The USB controller on the EZ-KIT Lite board connects to the USB port of the user’s PC, enabling the chosen IDE evaluation suite to emulate the on-board processor in-circuit. This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also supports in-circuit programming of the on-board Flash device to store user-specific boot code, enabling standalone operation. With the full version of CrossCore Embedded Studio or VisualDSP++ installed (sold separately), engineers can develop software for supported EZ-KITs or any custom system utilizing supported Analog Devices processors.

Software Add-Ins for CrossCore Embedded Studio

Analog Devices offers software add-ins which seamlessly integrate with CrossCore Embedded Studio to extend its capabilities and reduce development time. Add-ins include board support packages for evaluation hardware, various middleware packages, and algorithmic modules. Documentation, help, configuration dialogs, and coding examples present in these add-ins are viewable through the CrossCore Embedded Studio IDE once the add-in is installed.

Board Support Packages for Evaluation Hardware

Software support for the EZ-KIT Lite evaluation boards and EZ-Extender daughter cards is provided by software add-ins called Board Support Packages (BSPs). The BSPs contain the required drivers, pertinent release notes, and select example code for the given evaluation hardware. A download link for a specific BSP is

located on the web page for the associated EZ-KIT or EZ-Extender product. The link is found in the *Product Download* area of the product web page.

Middleware Packages

Analog Devices separately offers middleware add-ins such as real time operating systems, file systems, USB stacks, and TCP/IP stacks. For more information, see the following web pages:

- www.analog.com/ucos3
- www.analog.com/ucfs
- www.analog.com/ucusbd
- www.analog.com/lwip

Algorithmic Modules

To speed development, Analog Devices offers add-ins that perform popular audio and video processing algorithms. These are available for use with both CrossCore Embedded Studio and VisualDSP++. For more information visit www.analog.com and search on "Blackfin software modules" or "SHARC software modules".

Designing an Emulator-Compatible DSP Board (Target)

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG Test Access Port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the processor's internal features via the processor's TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers. The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the DSP's JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see the application note (EE-68) "Analog Devices JTAG Emulation Technical Reference" (www.analog.com/ee-68). This document is updated regularly to keep pace with improvements to emulator support.

ADDITIONAL INFORMATION

This data sheet provides a general overview of the ADSP-21160x architecture and functionality. For detailed information on the Blackfin family core architecture and instruction set, refer to the *ADSP-21160 SHARC DSP Hardware Reference* and the *ADSP-21160 SHARC DSP Instruction Set Reference*. For detailed information on the development tools for this processor, see the *VisualDSP++ User's Guide*.

RELATED SIGNAL CHAINS

A signal chain is a series of signal conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next.

Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The application signal chains page in the Circuits from the Lab® site (http:\\www.analog.com\circuits) provides:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

Table 3. Pin Function Descriptions (Continued)

Pin	Type	Function
ID2–0	I	Multiprocessing ID. Determines which multiprocessing bus request ($\overline{BR1}$–$\overline{BR6}$) is used by the ADSP-21160x. ID = 001 corresponds to $\overline{BR1}$, ID = 010 corresponds to $\overline{BR2}$, and so on. Use ID = 000 or ID = 001 in single-processor systems. These lines are a system configuration selection which should be hardwired or only changed at reset.
$\overline{DMAG1}$	O/T	DMA Grant 1 (DMA Channel 11). Asserted by ADSP-21160x to indicate that the requested DMA starts on the next cycle. Driven by bus master only. $\overline{DMAG1}$ has a 20 kΩ internal pull-up resistor that is enabled on the ADSP-21160x with ID2–0 = 00x.
$\overline{DMAG2}$	O/T	DMA Grant 2 (DMA Channel 12). Asserted by ADSP-21160x to indicate that the requested DMA starts on the next cycle. Driven by bus master only. $\overline{DMAG2}$ has a 20 kΩ internal pull-up resistor that is enabled on the ADSP-21160x with ID2–0 = 00x.
$\overline{BR6–1}$	I/O/S	Multiprocessing Bus Requests. Used by multiprocessing ADSP-21160x DSPs to arbitrate for bus mastership. An ADSP-21160x only drives its own $\overline{BRx}$ line (corresponding to the value of its ID2–0 inputs) and monitors all others. In a multiprocessor system with less than six ADSP-21160x DSPs, the unused $\overline{BRx}$ pins should be pulled high; the processor's own $\overline{BRx}$ line must not be pulled high or low because it is an output.
RPBA	I/S	Rotating Priority Bus Arbitration Select. When RPBA is high, rotating priority for multiprocessor bus arbitration is selected. When RPBA is low, fixed priority is selected. This signal is a system configuration selection which must be set to the same value on every ADSP-21160x. If the value of RPBA is changed during system operation, it must be changed in the same CLKIN cycle on every processor.
$\overline{PA}$	I/O/T	Priority Access. Asserting its $\overline{PA}$ pin allows an ADSP-21160x bus slave to interrupt background DMA transfers and gain access to the external bus. $\overline{PA}$ is connected to all ADSP-21160x DSPs in the system. If access priority is not required in a system, the $\overline{PA}$ pin should be left unconnected. $\overline{PA}$ has a 20 kΩ internal pull-up resistor that is enabled on the ADSP-21160x with ID2–0 = 00x.
DTx	O	Data Transmit (Serial Ports 0, 1). Each DT pin has a 50 kΩ internal pull-up resistor.
DRx	I	Data Receive (Serial Ports 0, 1). Each DR pin has a 50 kΩ internal pull-up resistor.
TCLKx	I/O	Transmit Clock (Serial Ports 0, 1). Each TCLK pin has a 50 kΩ internal pull-up resistor.
RCLKx	I/O	Receive Clock (Serial Ports 0, 1). Each RCLK pin has a 50 kΩ internal pull-up resistor.
TFSx	I/O	Transmit Frame Sync (Serial Ports 0, 1).
RFSx	I/O	Receive Frame Sync (Serial Ports 0, 1).
LxDAT7–0	I/O	Link Port Data (Link Ports 0–5). Each LxDAT pin has a 50 kΩ internal pull-down resistor that is enabled or disabled by the LPDRD bit of the LCTL0–1 register.
LxCLK	I/O	Link Port Clock (Link Ports 0–5). Each LxCLK pin has a 50 kΩ internal pull-down resistor that is enabled or disabled by the LPDRD bit of the LCTL0–1 register.
LxACK	I/O	Link Port Acknowledge (Link Ports 0–5). Each LxACK pin has a 50 kΩ internal pull-down resistor that is enabled or disabled by the LPDRD bit of the LCOM register.
EBOOT	I	EPROM Boot Select. For a description of how this pin operates, see Table 4. This signal is a system configuration selection that should be hardwired.
LBOOT	I	Link Boot. For a description of how this pin operates, see Table 4. This signal is a system configuration selection that should be hardwired.
$\overline{BMS}$	I/O/T	Boot Memory Select. Serves as an output or input as selected with the EBOOT and LBOOT pins; see Table 4. This input is a system configuration selection that should be hardwired.
CLKIN	I	Local Clock In. CLKIN is the ADSP-21160x clock input. The ADSP-21160x external port cycles at the frequency of CLKIN. The instruction cycle rate is a multiple of the CLKIN frequency; it is programmable at power-up. CLKIN may not be halted, changed, or operated below the specified frequency.
CLK_CFG3–0	I	Core/CLKIN Ratio Control. ADSP-21160x core clock (instruction cycle) rate is equal to n x CLKIN where n is user-selectable to 2, 3, or 4, using the CLK_CFG3–0 inputs. For clock configuration definitions, see the *$\overline{RESET}$ & CLKIN* section of the *System Design* chapter of the *ADSP-21160 SHARC DSP Hardware Reference*.

SPECIFICATIONS

OPERATING CONDITIONS—ADSP-21160M

Table 5 shows the recommended operating conditions for the ADSP-21160M. Specifications are subject to change without notice.

Table 5. Operating Conditions—ADSP-21160M

		K Grade		
Parameter		**Min**	**Max**	**Unit**
V_{DDINT}	Internal (Core) Supply Voltage	2.37	2.63	V
AV_{DD}	Analog (PLL) Supply Voltage	2.37	2.63	V
V_{DDEXT}	External (I/O) Supply Voltage	3.13	3.47	V
T_{CASE}	Case Operating Temperature[1]	0	85	°C
V_{IH1}	High Level Input Voltage,[2] @ V_{DDEXT}=Max	2.2	V_{DDEXT}+0.5	V
V_{IH2}	High Level Input Voltage,[3] @ V_{DDEXT}=Max	2.3	V_{DDEXT}+0.5	V
V_{IL}	Low Level Input Voltage[2, 3] @ V_{DDEXT}=Min	−0.5	+0.8	V

[1] See Environmental Conditions on Page 51 for information on thermal specifications.

[2] Applies to input and bidirectional pins: DATA63–0, ADDR31–0, $\overline{RDx}$, $\overline{WRx}$, ACK, $\overline{SBTS}$, $\overline{IRQ2–0}$, FLAG3–0, $\overline{HBG}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $\overline{BR6–1}$, ID2–0, RPBA, $\overline{PA}$, BRST, TFS0, TFS1, RFS0, RFS1, LxDAT7–0, LxCLK, LxACK, EBOOT, LBOOT, $\overline{BMS}$, TMS, TDI, TCK, $\overline{HBR}$, DR0, DR1, TCLK0, TCLK1, RCLK0, and RCLK1.

[3] Applies to input pins: CLKIN, $\overline{RESET}$, and $\overline{TRST}$.

ELECTRICAL CHARACTERISTICS—ADSP-21160M

Table 6 shows ADSP-21160M electrical characteristics. These specifications are subject to change without notification.

Table 6. Electrical Characteristics—ADSP-21160M

Parameter		Test Conditions	Min	Max	Unit
V_{OH}	High Level Output Voltage[1]	@ V_{DDEXT} = Min, I_{OH} = –2.0 mA[2]	2.4		V
V_{OL}	Low Level Output Voltage[1]	@ V_{DDEXT} = Min, I_{OL} = 4.0 mA[2]		0.4	V
I_{IH}	High Level Input Current[3, 4, 5]	@ V_{DDEXT} = Max, V_{IN} = V_{DD} Max		10	µA
I_{IL}	Low Level Input Current[3]	@ V_{DDEXT} = Max, V_{IN} = 0 V		10	µA
I_{ILPU1}	Low Level Input Current Pull-Up1[4]	@ V_{DDEXT} = Max, V_{IN} = 0 V		250	µA
I_{ILPU2}	Low Level Input Current Pull-Up2[5]	@ V_{DDEXT} = Max, V_{IN} = 0 V		500	µA
I_{OZH}	Three-State Leakage Current[6, 7, 8, 9]	@ V_{DDEXT} = Max, V_{IN} = V_{DD} Max		10	µA
I_{OZL}	Three-State Leakage Current[6]	@ V_{DDEXT} = Max, V_{IN} = 0 V		10	µA
I_{OZHPD}	Three-State Leakage Current Pull-Down[9]	@ V_{DDEXT} = Max, V_{IN} = V_{DD} Max		250	µA
I_{OZLPU1}	Three-State Leakage Current Pull-Up1[7]	@ V_{DDEXT} = Max, V_{IN} = 0 V		250	µA
I_{OZLPU2}	Three-State Leakage Current Pull-Up2[8]	@ V_{DDEXT} = Max, V_{IN} = 0 V		500	µA
I_{OZHA}	Three-State Leakage Current[10]	@ V_{DDEXT} = Max, V_{IN} = V_{DD} Max		25	µA
I_{OZLA}	Three-State Leakage Current[10]	@ V_{DDEXT} = Max, V_{IN} = 0 V		4	mA
$I_{DD-INPEAK}$	Supply Current (Internal)[11]	t_{CCLK} = 12.5 ns, V_{DDINT} = Max		1400	mA
$I_{DD-INHIGH}$	Supply Current (Internal)[12]	t_{CCLK} = 12.5 ns, V_{DDINT} = Max		875	mA
$I_{DD-INLOW}$	Supply Current (Internal)[13]	t_{CCLK} = 12.5 ns, V_{DDINT} = Max		625	mA
$I_{DD-IDLE}$	Supply Current (Idle)[14]	t_{CCLK} = 12.5 ns, V_{DDINT} = Max		400	mA
AI_{DD}	Supply Current (Analog)[15]	@AV_{DD} = Max		10	mA
C_{IN}	Input Capacitance[16, 17]	f_{IN} = 1 MHz, T_{CASE} = 25°C, V_{IN} = 2.5 V		4.7	pF

[1] Applies to output and bidirectional pins: DATA63–0, ADDR31–0, $\overline{MS3–0}$, $\overline{RDx}$, $\overline{WRx}$, PAGE, CLKOUT, ACK, FLAG3–0, TIMEXP, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BR6–1}$, $\overline{PA}$, BRST, $\overline{CIF}$, DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, LxDAT7–0, LxCLK, LxACK, $\overline{BMS}$, TDO, and $\overline{EMU}$.

[2] See Output Drive Currents—ADSP-21160M on Page 47 for typical drive current capabilities.

[3] Applies to input pins: $\overline{SBTS}$, $\overline{IRQ2–0}$, $\overline{HBR}$, $\overline{CS}$, ID2–0, RPBA, EBOOT, LBOOT, CLKIN, $\overline{RESET}$, TCK, and CLK_CFG3-0.

[4] Applies to input pins with internal pull-ups: DR0, and DR1.

[5] Applies to input pins with internal pull-ups: $\overline{DMARx}$, TMS, TDI, and $\overline{TRST}$.

[6] Applies to three-statable pins: DATA63–0, ADDR31–0, PAGE, CLKOUT, ACK, FLAG3–0, REDY, $\overline{HBG}$, $\overline{BMS}$, $\overline{BR6–1}$, TFSx, RFSx, and TDO.

[7] Applies to three-statable pins with internal pull-ups: DTx, TCLKx, RCLKx, and $\overline{EMU}$.

[8] Applies to three-statable pins with internal pull-ups: $\overline{MS3–0}$,$\overline{RDx}$, $\overline{WRx}$, $\overline{DMAGx}$, $\overline{PA}$, and $\overline{CIF}$.

[9] Applies to three-statable pins with internal pull-downs: LxDAT7–0, LxCLK, and LxACK.

[10] Applies to ACK pulled up internally with 2 kΩ during reset or ID2–0 = 00x.

[11] The test program used to measure $I_{DD-INPEAK}$ represents worst-case processor operation and is not sustainable under normal application conditions. Actual internal power measurements made using typical applications are less than specified. For more information, see Power Dissipation on Page 47.

[12] $I_{DD-INHIGH}$ is a composite average based on a range of high activity code. For more information, see Power Dissipation on Page 47.

[13] $I_{DD-INLOW}$ is a composite average based on a range of low activity code. For more information, see Power Dissipation on Page 47.

[14] Idle denotes ADSP-21160M state during execution of IDLE instruction. For more information, see Power Dissipation on Page 47.

[15] Characterized, but not tested.

[16] Applies to all signal pins.

[17] Guaranteed, but not tested.

OPERATING CONDITIONS—ADSP-21160N

Table 7 shows recommended operating conditions for the ADSP-21160N. These specifications are subject to change without notice.

Table 7. Operating Conditions—ADSP-21160N

Parameter		C Grade Min	C Grade Max	K Grade Min	K Grade Max	Unit
V_{DDINT}	Internal (Core) Supply Voltage	1.8	2.0	1.8	2.0	V
AV_{DD}	Analog (PLL) Supply Voltage	1.8	2.0	1.8	2.0	V
V_{DDEXT}	External (I/O) Supply Voltage	3.13	3.47	3.13	3.47	V
T_{CASE}	Case Operating Temperature[1]	–40	+100	0	85	°C
V_{IH1}	High Level Input Voltage,[2] @ V_{DDEXT}=Max	2.0	V_{DDEXT}+0.5	2.0	V_{DDEXT}+0.5	V
V_{IH2}	High Level Input Voltage,[3] @ V_{DDEXT}=Max	2.0	V_{DDEXT}+0.5	2.0	V_{DDEXT}+0.5	V
V_{IL}	Low Level Input Voltage[2, 3] @ V_{DDEXT}=Min	–0.5	+0.8	–0.5	+0.8	V

[1] See Environmental Conditions on Page 51 for information on thermal specifications.

[2] Applies to input and bidirectional pins: DATA63–0, ADDR31–0, $\overline{RDx}$, $\overline{WRx}$, ACK, $\overline{SBTS}$, $\overline{IRQ2–0}$, FLAG3–0, $\overline{HBG}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $\overline{BR6–1}$, ID2–0, RPBA, $\overline{PA}$, BRST, TFS0, TFS1, RFS0, RFS1, LxDAT7–0, LxCLK, LxACK, EBOOT, LBOOT, $\overline{BMS}$, TMS, TDI, TCK, $\overline{HBR}$, DR0, DR1, TCLK0, TCLK1, RCLK0, and RCLK1.

[3] Applies to input pins: CLKIN, $\overline{RESET}$, and $\overline{TRST}$.

ABSOLUTE MAXIMUM RATINGS

Stresses at or above those listed in Table 9 (ADSP-21160M) and Table 10 (ADSP-21160N) may cause permanent damage to the product. These are stress ratings only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 9. Absolute Maximum Ratings—ADSP-21160M

Parameter	Rating
Internal (Core) Supply Voltage (V_{DDINT})	–0.3 V to +3.0 V
Analog (PLL) Supply Voltage (A_{VDD})	–0.3 V to +3.0 V
External (I/O) Supply Voltage (V_{DDEXT})	–0.3 V to +4.6 V
Input Voltage	–0.5 V to V_{DDEXT} + 0.5 V
Output Voltage Swing	–0.5 V to V_{DDEXT} + 0.5 V
Load Capacitance	200 pF
Storage Temperature Range	–65°C to +150°C

Table 10. Absolute Maximum Ratings—ADSP-21160N

Parameter	Rating
Internal (Core) Supply Voltage (V_{DDINT})	–0.3 V to +2.3 V
Analog (PLL) Supply Voltage (A_{VDD})	–0.3 V to +2.3 V
External (I/O) Supply Voltage (V_{DDEXT})	–0.3 V to +4.6 V
Input Voltage	–0.5 V to V_{DDEXT} + 0.5 V
Output Voltage Swing	–0.5 V to V_{DDEXT} + 0.5 V
Load Capacitance	200 pF
Storage Temperature Range	–65°C to +150°C

ESD SENSITIVITY

ESD (electrostatic discharge sensitive device)
Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PACKAGE INFORMATION

The information presented in Figure 7 provides details about the package branding for the ADSP-21160M/ADSP-21160N processor. For a complete listing of product availability, see Ordering Guide on Page 58.

Figure 7. Typical Package Brand

Table 11. Package Brand Information

Brand Key	Field Description
a	ADSP-21160 Model (M or N)
t	Temperature Range
pp	Package Type
Z	RoHS Compliant Designation
cc	See Ordering Guide
vvvvvv.x	Assembly Lot Code
n.n	Silicon Revision
#	RoHS Compliant Designation
yyww	Date Code

TIMING SPECIFICATIONS

The ADSP-21160x DSP's internal clock switches at higher frequencies than the system input clock (CLKIN). To generate the internal clock, the DSP uses an internal phase-locked loop (PLL). This PLL-based clocking minimizes the skew between the system clock (CLKIN) signal and the DSP's internal clock (the clock source for the external port logic and I/O pads).

The ADSP-21160x DSP's internal clock (a multiple of CLKIN) provides the clock signal for timing internal memory, processor core, link ports, serial ports, and external port (as required for read/write strobes in asynchronous access mode). During reset, program the ratio between the DSP's internal clock frequency and external (CLKIN) clock frequency with the CLK_CFG3–0 pins. Even though the internal clock is the clock source for the external port, the external port clock always switches at the CLKIN frequency. To determine switching frequencies for the serial and link ports, divide down the internal clock, using the programmable divider control of each port (TDIVx/RDIVx for the serial ports and LxCLKD1–0 for the link ports).

Note the following definitions of various clock periods that are a function of CLKIN and the appropriate ratio control:

- $t_{CCLK} = (t_{CK}) / CR$
- $t_{LCLK} = (t_{CCLK}) \times LR$
- $t_{SCLK} = (t_{CCLK}) \times SR$

where:

- LCLK = Link Port Clock
- SCLK = Serial Port Clock
- t_{CK} = CLKIN Clock Period
- t_{CCLK} = (Processor) Core Clock Period
- t_{LCLK} = Link Port Clock Period
- t_{SCLK} = Serial Port Clock Period
- CR = Core/CLKIN Ratio (2, 3, or 4:1, determined by CLK_CFG3–0 at reset)
- LR = Link Port/Core Clock Ratio (1, 2, 3, or 4:1, determined by LxCLKD)
- SR = Serial Port/Core Clock Ratio (wide range, determined by × CLKDIV)

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, it is not meaningful to add parameters to derive longer times.

See Figure 33 on Page 49 under Test Conditions for voltage reference levels.

Switching characteristics specify how the processor changes its signals. Circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics describe what the processor will do in a given circumstance. Use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

During processor reset ($\overline{RESET}$ pin low) or software reset (SRST bit in SYSCON register = 1), deassertion ($\overline{MS3–0}$, $\overline{HBG}$, $\overline{DMAGx}$, $\overline{RDx}$, $\overline{WRx}$, $\overline{CIF}$, PAGE, BRST) and three-state (FLAG3-0, LxCLK, LxACK, LxDAT7-0, ACK, REDY, $\overline{PA}$, TFSx, RFSx, TCLKx, RCLKx, DTx, $\overline{BMS}$, TDO, $\overline{EMU}$, DATA) timings differ. These occur asynchronously to CLKIN, and may not meet the specifications published in the timing requirements and switching characteristics tables. The maximum delay for deassertion and three-state is one t_{CK} from $\overline{RESET}$ pin assertion low or setting the SRST bit in SYSCON. During reset the DSP will not respond to $\overline{SBTS}$, $\overline{HBR}$, and MMS accesses. $\overline{HBR}$ asserted before reset will be recognized, but an $\overline{HBG}$ will not be returned by the DSP until after reset is deasserted and the DSP has completed bus synchronization.

Unless otherwise noted, all timing specifications (*Timing Requirements* and *Switching Characteristics*) listed on pages 21 through 46 apply to both ADSP-21160M and ADSP-21160N.

Power-Up Sequencing

For power-up sequencing, see Table 12 and Figure 8. During the power-up sequence of the DSP, differences in the ramp-up rates and activation time between the two power supplies can cause current to flow in the I/O ESD protection circuitry. To prevent this damage to the ESD diode protection circuitry, Analog Devices recommends including a bootstrap Schottky diode (see Figure 9). The bootstrap Schottky diode connected between the V_{DDINT} and V_{DDEXT} power supplies protects the ADSP-21160x from partially powering the V_{DDEXT} supply. Including a Schottky diode will shorten the delay between the supply ramps and thus prevent damage to the ESD diode protection circuitry. With this technique, if the V_{DDINT} rail rises ahead of the V_{DDEXT} rail, the Schottky diode pulls the V_{DDEXT} rail along with the V_{DDINT} rail.

Table 12. Power-Up Sequencing

Parameter		Min	Max	Unit
Timing Requirements				
t_{RSTVDD}	$\overline{\text{RESET}}$ Low Before V_{DDINT}/V_{DDEXT} on	0		ns
$t_{IVDDEVDD}$	V_{DDINT} on Before V_{DDEXT}	– 50	+200	ms
t_{CLKVDD}	CLKIN Running After valid V_{DDINT}/V_{DDEXT}[1]	0	200	ms
t_{CLKRST}	CLKIN Valid Before $\overline{\text{RESET}}$ Deasserted	10[2]		µs
t_{PLLRST}	PLL Control Setup Before $\overline{\text{RESET}}$ Deasserted	20[3]		µs
Switching Characteristics				
$t_{CORERST}$	DSP Core Reset Deasserted After $\overline{\text{RESET}}$ Deasserted	$4096t_{CK}$[3, 4]		

[1] Valid V_{DDINT}/V_{DDEXT} assumes that the supplies are fully ramped to their V_{DDINT} and V_{DDEXT} rails. Voltage ramp rates can vary from microseconds to hundreds of milliseconds, depending on the design of the power supply subsystem.

[2] Assumes a stable CLKIN signal after meeting worst-case start-up timing of oscillators. Refer to your oscillator manufacturer's data sheet for start-up time.

[3] Based on CLKIN cycles.

[4] $\overline{\text{CORERST}}$ is an internal signal only. The 4096 cycle count is dependent on t_{SRST} specification. If setup time is not met, one additional CLKIN cycle may be added to the core reset time, resulting in 4097 cycles maximum.

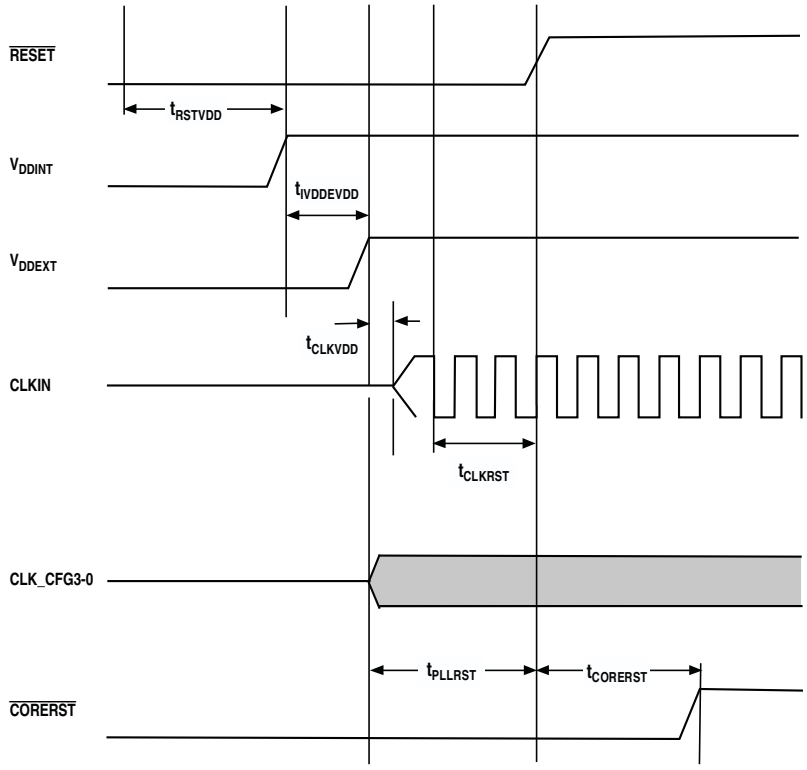

Figure 8. Power-Up Sequencing

Reset

For reset, see Table 14 and Figure 11.

Table 14. Reset

Parameter		Min	Max	Unit
Timing Requirements				
t_{WRST}	$\overline{\text{RESET}}$ Pulsewidth Low[1]	$4t_{CK}$		ns
t_{SRST}	$\overline{\text{RESET}}$ Setup Before CLKIN High[2]	8		ns

[1] Applies after the power-up sequence is complete. At power-up, the processor's internal phase-locked loop requires no more than 100 µs while $\overline{\text{RESET}}$ is low, assuming stable V_{DD} and CLKIN (not including start-up time of external clock oscillator).

[2] Only required if multiple ADSP-21160x DSPs must come out of reset synchronous to CLKIN with program counters (PC) equal. Not required for multiple ADSP-21160x DSPs communicating over the shared bus (through the external port), because the bus arbitration logic automatically synchronizes itself after reset.

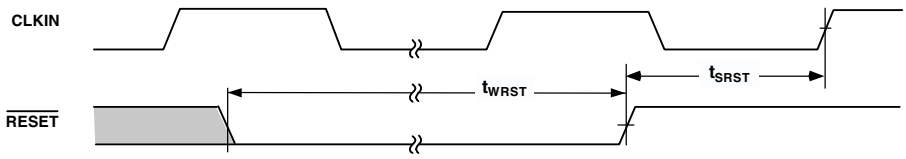

Figure 11. Reset

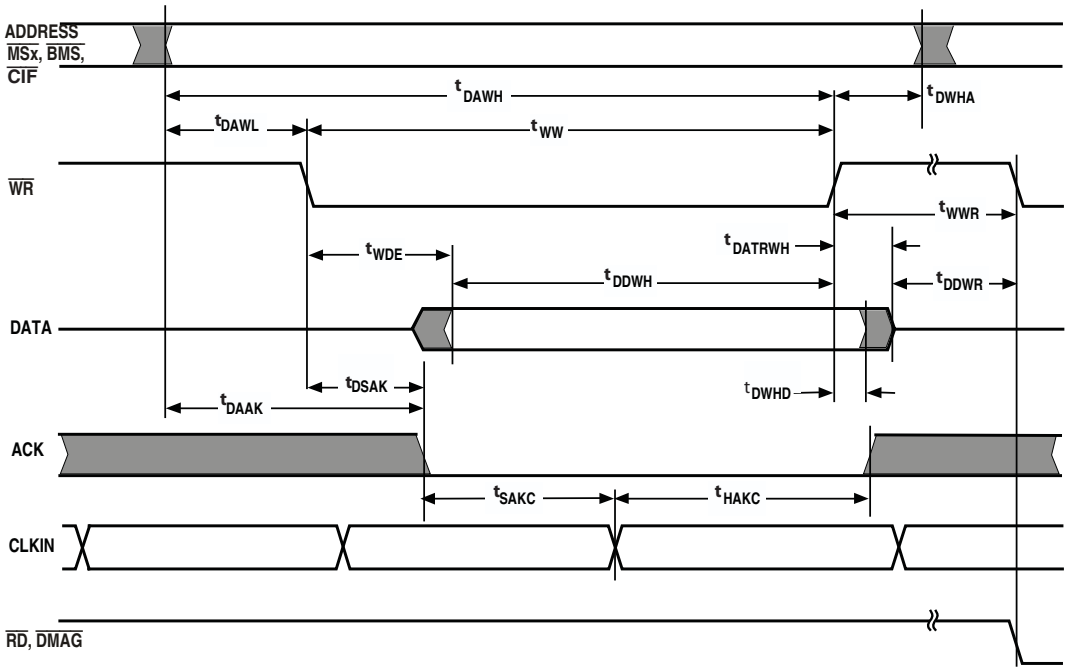

Figure 16. Memory Write—Bus Master

Asynchronous Read/Write—Host to ADSP-21160x

Use these specifications (Table 23, Table 24, Figure 20, and Figure 21) for asynchronous host processor accesses of an ADSP-21160x, after the host has asserted $\overline{CS}$ and $\overline{HBR}$ (low). After $\overline{HBG}$ is returned by the ADSP-21160x, the host can drive the $\overline{RDx}$ and $\overline{WRx}$ pins to access the ADSP-21160x DSP's internal memory or IOP registers. $\overline{HBR}$ and $\overline{HBG}$ are assumed low for this timing.

Table 23. Read Cycle

Parameter		Min	Max	Unit
Timing Requirements				
t_{SADRDL}	Address Setup/$\overline{CS}$ Low Before $\overline{RDx}$ Low	0		ns
t_{HADRDH}	Address Hold/$\overline{CS}$ Hold Low After $\overline{RDx}$	2		ns
t_{WRWH}	$\overline{RDx}$/$\overline{WRx}$ High Width	5		ns
$t_{DRDHRDY}$	$\overline{RDx}$ High Delay After REDY (O/D) Disable	0		ns
$t_{DRDHRDY}$	$\overline{RDx}$ High Delay After REDY (A/D) Disable	0		ns
Switching Characteristics				
$t_{SDATRDY}$	Data Valid Before REDY Disable from Low	2		ns
$t_{DRDYRDL}$	REDY (O/D) or (A/D) Low Delay After $\overline{RDx}$ Low[1]		11	ns
t_{RDYPRD}	REDY (O/D) or (A/D) Low Pulsewidth for Read[2]	t_{CK} – 4		ns
t_{HDARWH}	Data Disable After $\overline{RDx}$ High[3]	1.5	6	ns

[1] For ADSP-21160M, specification is 7 ns, minimum.
[2] For ADSP-21160M, specification is t_{CK} ns, minimum.
[3] For ADSP-21160M, specification is 2 ns, minimum.

Table 24. Write Cycle

Parameter		Min	Max	Unit
Timing Requirements				
t_{SCSWRL}	$\overline{CS}$ Low Setup Before $\overline{WRx}$ Low	0		ns
t_{HCSWRH}	$\overline{CS}$ Low Hold After $\overline{WRx}$ High	0		ns
t_{SADWRH}	Address Setup Before $\overline{WRx}$ High	6		ns
t_{HADWRH}	Address Hold After $\overline{WRx}$ High	2		ns
t_{WWRL}	$\overline{WRx}$ Low Width[1]	t_{CCLK}+1		ns
t_{WRWH}	$\overline{RDx}$/$\overline{WRx}$ High Width	5		ns
$t_{DWRHRDY}$	$\overline{WRx}$ High Delay After REDY (O/D) or (A/D) Disable	0		ns
t_{SDATWH}	Data Setup Before $\overline{WRx}$ High	5		ns
t_{HDATWH}	Data Hold After $\overline{WRx}$ High	4		ns
Switching Characteristics				
$t_{DRDYWRL}$	REDY (O/D) or (A/D) Low Delay After $\overline{WRx}$/$\overline{CS}$ Low		11	ns
t_{RDYPWR}	REDY (O/D) or (A/D) Low Pulsewidth for Write[2]	5.75 + 0.5t_{CCLK}		ns

[1] For ADSP-21160M, specification is 7 ns, minimum.
[2] For ADSP-21160M, specification is 12 ns, minimum.

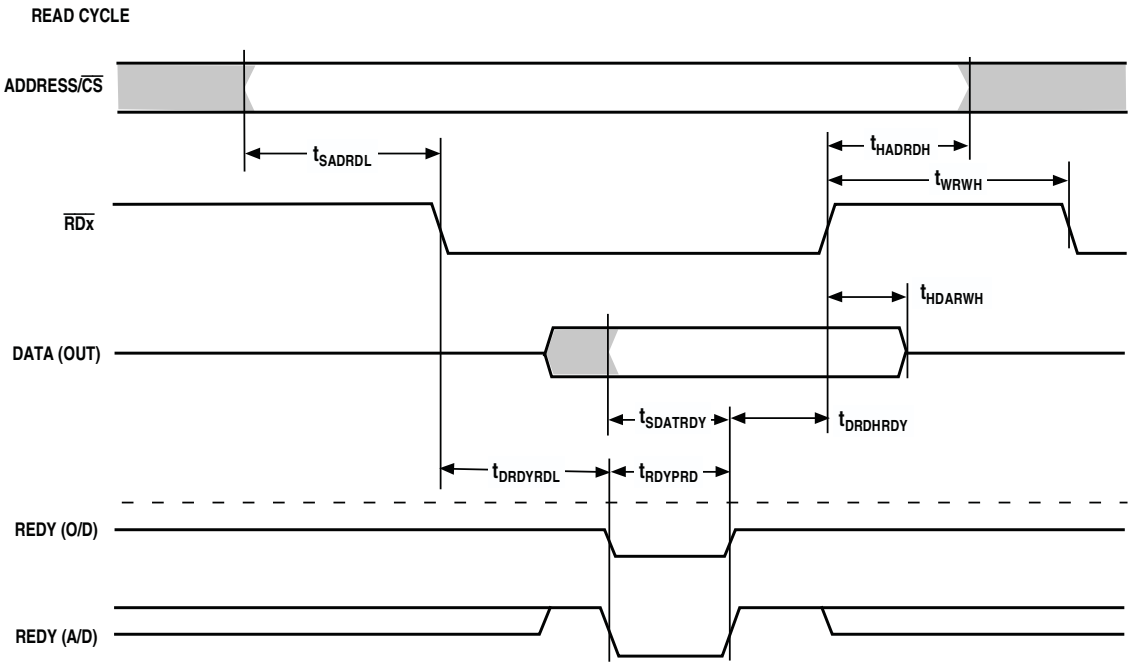

Figure 20. Asynchronous Read—Host to ADSP-21160x

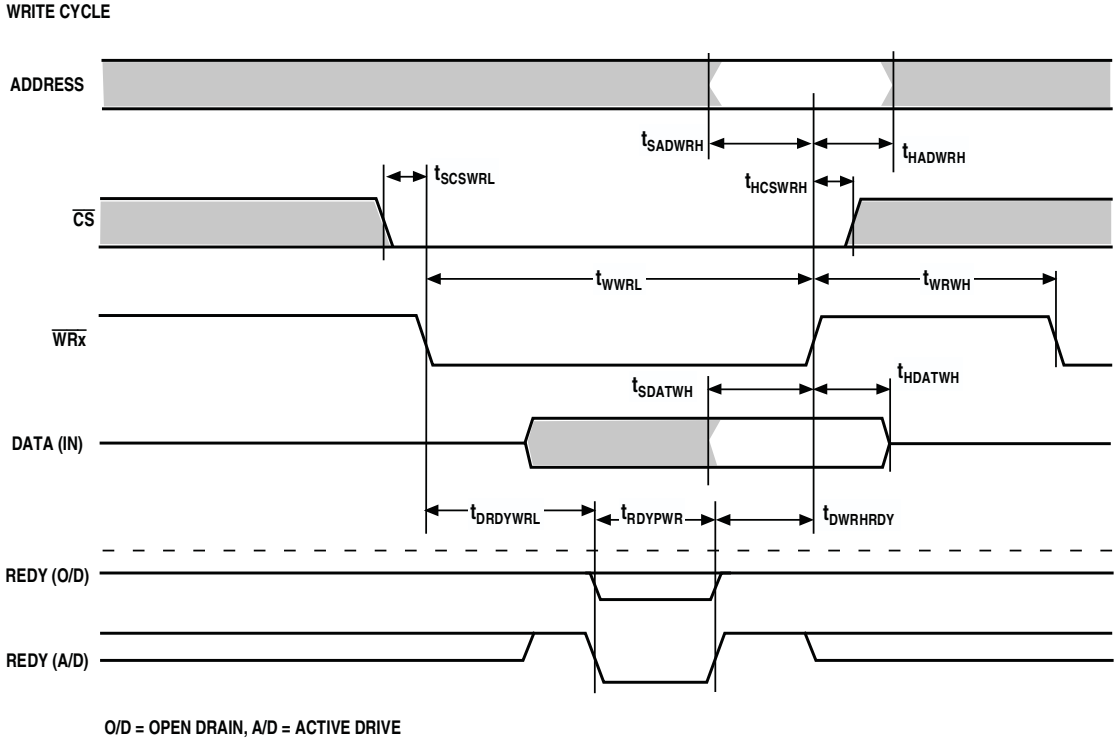

Figure 21. Asynchronous Write—Host to ADSP-21160x

OUTPUT DRIVE CURRENTS—ADSP-21160M

Figure 29 shows typical I–V characteristics for the output drivers of the ADSP-21160M. The curves represent the current drive capability of the output drivers as a function of output voltage.

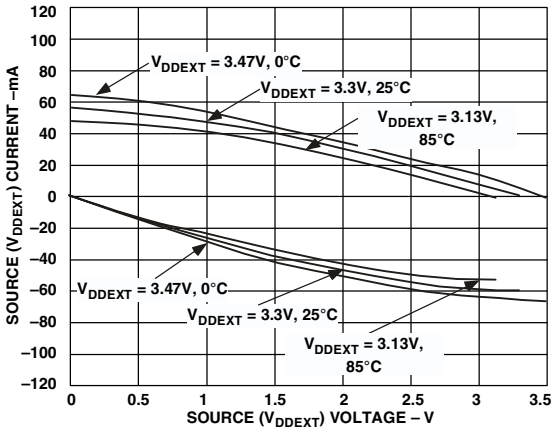

Figure 29. ADSP-21160M Typical Drive Currents

OUTPUT DRIVE CURRENTS—ADSP-21160N

Figure 30 shows typical I–V characteristics for the output drivers of the ADSP-21160N. The curves represent the current drive capability of the output drivers as a function of output voltage.

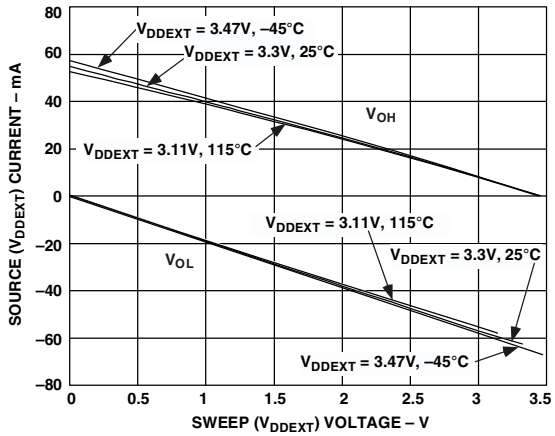

Figure 30. ADSP-21160N Typical Drive Currents

POWER DISSIPATION

Total power dissipation has two components: one due to internal circuitry and one due to the switching of external output drivers.

Internal power dissipation is dependent on the instruction execution sequence and the data operands involved. Using the current specifications ($I_{DD\text{-}INPEAK}$, $I_{DD\text{-}INHIGH}$, $I_{DD\text{-}INLOW}$, and $I_{DD\text{-}IDLE}$) from Electrical Characteristics—ADSP-21160M on Page 16 and Electrical Characteristics—ADSP-21160N on Page 18 and the current-versus-operation information in Table 37, engineers can estimate the ADSP-21160x DSP's internal power supply (V_{DDINT}) input current for a specific application, according to the formula:

$$\begin{aligned} &\%\ \text{Peak} \times I_{DD\text{-}INPEAK} \\ &\%\ \text{High} \times I_{DD\text{-}INHIGH} \\ &\%\ \text{Low} \times I_{DD\text{-}INLOW} \\ +\ &\%\ \text{Peak} \times I_{DD\text{-}IDLE} \\ &= I_{DDINT} \end{aligned}$$

The external component of total power dissipation is caused by the switching of output pins. Its magnitude depends on:

- The number of output pins that switch during each cycle (O)
- The maximum frequency at which they can switch (f)
- Their load capacitance (C)
- Their voltage swing (V_{DD})

and is calculated by:

$$P_{EXT} = O \times C \times V_{DD}^2 \times f$$

The load capacitance should include the processor's package capacitance (C_{IN}). The switching frequency includes driving the load high and then back low. Address and data pins can drive high and low at a maximum rate of $1/(2t_{CK})$. The write strobe can switch every cycle at a frequency of $1/t_{CK}$. Select pins switch at $1/(2t_{CK})$, but selects can switch on each cycle.

Example for ADSP-21160N: Estimate P_{EXT} with the following assumptions:

- A system with one bank of external data memory—asynchronous RAM (64-bit)
- Four 64K × 16 RAM chips are used, each with a load of 10 pF
- External data memory writes occur every other cycle, a rate of $1/(2\ t_{CK})$, with 50% of the pins switching
- The bus cycle time is 50 MHz (t_{CK} = 20 ns).

The P_{EXT} equation is calculated for each class of pins that can drive, as shown in Table 38.

A typical power consumption can now be calculated for these conditions by adding a typical internal power dissipation:

$$P_{TOTAL} = P_{EXT} + P_{INT} + P_{PLL}$$

where:

- P_{EXT} is from Table 38
- P_{INT} is $I_{DDINT} \times 1.9$ V, using the calculation I_{DDINT} listed in Power Dissipation on page 47
- P_{PLL} is $AI_{DD} \times 1.9$ V, using the value for AI_{DD} listed in Electrical Characteristics—ADSP-21160M on Page 16 and Electrical Characteristics—ADSP-21160N on Page 18

ENVIRONMENTAL CONDITIONS

Thermal Characteristics

The ADSP-21160x DSPs are provided in a 400-Ball PBGA (Plastic Ball Grid Array) package.

The ADSP-21160x is specified for a case temperature (T_{CASE}). To ensure that the T_{CASE} data sheet specification is not exceeded, a heatsink and/or an air flow source may be used. Use the centerblock of ground pins (for ADSP-21160M, PBGA balls: H8-13, J8-13, K8-13, L8-13, M8-13, N8-13; for ADSP-21160N, PBGA balls: F7-14, G7-14, H7-14, J7-14, K7-14, L7-14, M-14, N7-14, P7-14, R7-15) to provide thermal pathways to the printed circuit board's ground plane. A heatsink should be attached to the ground plane (as close as possible to the thermal pathways) with a thermal adhesive.

$$T_{CASE} = T_{AMB} + (PD \times \theta_{CA})$$

- T_{CASE} = Case temperature (measured on top surface of package)
- T_{AMB} = Ambient temperature °C
- PD = Power dissipation in W (this value depends upon the specific application; a method for calculating PD is shown under Power Dissipation).
- θ_{CA} = Value from Table 39.
- θ_{JB} = 6.46°C/W

Table 39. Airflow Over Package Versus θ_{CA}

Airflow (Linear Ft./Min.)	0	200	400
θ_{CA} (°C/W)[1]	12.13	9.86	8.7

[1] θ_{JC} = 3.6 °C/W

400-BALL PBGA PIN CONFIGURATIONS

Table 40 lists the pin assignments for the PBGA package, and the pin configurations diagram in Figure 40 (ADSP-21160M) and Figure 41 (ADSP-21160N) show the pin assignment summary.

Table 40. 400-Ball PBGA Pin Assignments

(See Footnotes 1 and 2)							
Pin Name	**Pin No.**	**Pin Name**	**Pin No.**	**Pin Name**	**Pin No.**	**Pin Name**	**Pin No.**
DATA[14]	A01	DATA[22]	B01	DATA[24]	C01	DATA[28]	D01
DATA[13]	A02	DATA[16]	B02	DATA[18]	C02	DATA[25]	D02
DATA[10]	A03	DATA[15]	B03	DATA[17]	C03	DATA[20]	D03
DATA[8]	A04	DATA[9]	B04	DATA[11]	C04	DATA[19]	D04
DATA[4]	A05	DATA[6]	B05	DATA[7]	C05	DATA[12]	D05
DATA[2]	A06	DATA[3]	B06	DATA[5]	C06	V_{DDEXT}	D06
TDI	A07	DATA[0]	B07	DATA[1]	C07	V_{DDINT}	D07
$\overline{TRST}$	A08	TCK	B08	TMS	C08	V_{DDEXT}	D08
$\overline{RESET}$	A09	$\overline{EMU}$	B09	TD0	C09	V_{DDEXT}	D09
RPBA	A10	$\overline{IRQ2}$	B10	$\overline{IRQ1}$	C10	V_{DDEXT}	D10
$\overline{IRQ0}$	A11	FLAG3	B11	FLAG2	C11	V_{DDEXT}	D11
FLAG1	A12	FLAG0	B12	NC[1]	C12	V_{DDEXT}	D12
TIMEXP	A13	NC[1]	B13	NC	C13	V_{DDINT}	D13
NC[1]	A14	NC	B14	TCLK1	C14	V_{DDEXT}	D14
NC	A15	DT1	B15	DR1	C15	TFS0	D15
TFS1	A16	RCLK1	B16	DR0	C16	L1DAT[7]	D16
RFS1	A17	RFS0	B17	L0DAT[7]	C17	L0CLK	D17
RCLK0	A18	TCLK0	B18	L0DAT[6]	C18	L0DAT[3]	D18
DT0	A19	L0DAT[5]	B19	L0ACK	C19	L0DAT[1]	D19
L0DAT[4]	A20	L0DAT[2]	B20	L0DAT[0]	C20	L1CLK	D20
DATA[30]	E01	DATA[34]	F01	DATA[38]	G01	DATA[40]	H01
DATA[29]	E02	DATA[33]	F02	DATA[35]	G02	DATA[39]	H02
DATA[23]	E03	DATA[27]	F03	DATA[32]	G03	DATA[37]	H03
DATA[21]	E04	DATA[26]	F04	DATA[31]	G04	DATA[36]	H04
V_{DDEXT}	E05	V_{DDEXT}	F05	V_{DDEXT}	G05	V_{DDEXT}	H05
V_{DDINT}	E06	V_{DDINT}	F06	V_{DDINT}	G06	V_{DDINT}	H06
V_{DDINT}	E07	GND	F07	GND	G07	GND	H07
V_{DDINT}	E08	GND	F08	GND	G08	GND	H08
V_{DDINT}	E09	GND	F09	GND	G09	GND	H09
V_{DDINT}	E10	GND	F10	GND	G10	GND	H10
GND	E11	GND	F11	GND	G11	GND	H11
V_{DDINT}	E12	GND	F12	GND	G12	GND	H12
V_{DDINT}	E13	GND	F13	GND	G13	GND	H13
V_{DDINT}	E14	GND	F14	GND	G14	GND	H14
V_{DDINT}	E15	V_{DDINT}	F15	V_{DDINT}	G15	V_{DDINT}	H15
V_{DDEXT}	E16	V_{DDEXT}	F16	V_{DDEXT}	G16	V_{DDEXT}	H16
L1DAT[6]	E17	L1DAT[4]	F17	L1DAT[2]	G17	L2DAT[5]	H17
L1DAT[5]	E18	L1DAT[3]	F18	L2DAT[6]	G18	L2ACK	H18
L1ACK	E19	L1DAT[0]	F19	L2DAT[4]	G19	L2DAT[3]	H19
L1DAT[1]	E20	L2DAT[7]	F20	L2CLK	G20	L2DAT[1]	H20

Table 40. 400-Ball PBGA Pin Assignments (Continued)

(See Footnotes 1 and 2)							
Pin Name	**Pin No.**	**Pin Name**	**Pin No.**	**Pin Name**	**Pin No.**	**Pin Name**	**Pin No.**
DATA[44]	J01	CLK_CFG_0	K01	CLKIN	L01	AV_{DD}	M01
DATA[43]	J02	DATA[46]	K02	CLK_CFG_1	L02	CLK_CFG_3	M02
DATA[42]	J03	DATA[45]	K03	AGND	L03	CLKOUT	M03
DATA[41]	J04	DATA[47]	K04	CLK_CFG_2	L04	NC[2]	M04
V_{DDEXT}	J05	V_{DDEXT}	K05	V_{DDEXT}	L05	V_{DDEXT}	M05
V_{DDINT}	J06	V_{DDINT}	K06	V_{DDINT}	L06	V_{DDINT}	M06
GND	J07	GND	K07	GND	L07	GND	M07
GND	J08	GND	K08	GND	L08	GND	M08
GND	J09	GND	K09	GND	L09	GND	M09
GND	J10	GND	K10	GND	L10	GND	M10
GND	J11	GND	K11	GND	L11	GND	M11
GND	J12	GND	K12	GND	L12	GND	M12
GND	J13	GND	K13	GND	L13	GND	M13
GND	J14	GND	K14	GND	L14	GND	M14
V_{DDINT}	J15	V_{DDINT}	K15	V_{DDINT}	L15	V_{DDINT}	M15
V_{DDEXT}	J16	V_{DDEXT}	K16	V_{DDEXT}	L16	V_{DDEXT}	M16
L2DAT[2]	J17	$\overline{BR6}$	K17	$\overline{BR2}$	L17	PAGE	M17
L2DAT[0]	J18	$\overline{BR5}$	K18	$\overline{BR1}$	L18	$\overline{SBTS}$	M18
$\overline{HBG}$	J19	$\overline{BR4}$	K19	ACK	L19	$\overline{PA}$	M19
$\overline{HBR}$	J20	$\overline{BR3}$	K20	REDY	L20	L3DAT[7]	M20
NC	N01	DATA[49]	P01	DATA[53]	R01	DATA[56]	T01
NC	N02	DATA[50]	P02	DATA[54]	R02	DATA[58]	T02
DATA[48]	N03	DATA[52]	P03	DATA[57]	R03	DATA[59]	T03
DATA[51]	N04	DATA[55]	P04	DATA[60]	R04	DATA[63]	T04
V_{DDEXT}	N05	V_{DDEXT}	P05	V_{DDEXT}	R05	V_{DDEXT}	T05
V_{DDINT}	N06	V_{DDINT}	P06	V_{DDINT}	R06	V_{DDINT}	T06
GND	N07	GND	P07	GND	R07	V_{DDINT}	T07
GND	N08	GND	P08	GND	R08	V_{DDINT}	T08
GND	N09	GND	P09	GND	R09	V_{DDINT}	T09
GND	N10	GND	P10	GND	R10	V_{DDINT}	T10
GND	N11	GND	P11	GND	R11	V_{DDINT}	T11
GND	N12	GND	P12	GND	R12	V_{DDINT}	T12
GND	N13	GND	P13	GND	R13	V_{DDINT}	T13
GND	N14	GND	P14	GND	R14	V_{DDINT}	T14
V_{DDINT}	N15	V_{DDINT}	P15	GND	R15	V_{DDINT}	T15
V_{DDEXT}	N16	V_{DDEXT}	P16	V_{DDEXT}	R16	V_{DDEXT}	T16
L3DAT[5]	N17	L3DAT[2]	P17	L4DAT[5]	R17	L4DAT[3]	T17
L3DAT[6]	N18	L3DAT[1]	P18	L4DAT[6]	R18	L4ACK	T18
L3DAT[4]	N19	L3DAT[3]	P19	L4DAT[7]	R19	L4CLK	T19
L3CLK	N20	L3ACK	P20	L3DAT[0]	R20	L4DAT[4]	T20
DATA[61]	U01	ADDR[4]	V01	ADDR[5]	W01	ADDR[8]	Y01
DATA[62]	U02	ADDR[6]	V02	ADDR[9]	W02	ADDR[11]	Y02
ADDR[3]	U03	ADDR[7]	V03	ADDR[12]	W03	ADDR[13]	Y03
ADDR[2]	U04	ADDR[10]	V04	ADDR[15]	W04	ADDR[16]	Y04
V_{DDEXT}	U05	ADDR[14]	V05	ADDR[17]	W05	ADDR[19]	Y05
V_{DDEXT}	U06	ADDR[18]	V06	ADDR[20]	W06	ADDR[21]	Y06

Table 40. 400-Ball PBGA Pin Assignments (Continued)

(See Footnotes 1 and 2)							
Pin Name	**Pin No.**	**Pin Name**	**Pin No.**	**Pin Name**	**Pin No.**	**Pin Name**	**Pin No.**
V_{DDEXT}	U07	ADDR[22]	V07	ADDR[23]	W07	ADDR[24]	Y07
V_{DDEXT}	U08	ADDR[25]	V08	ADDR[26]	W08	ADDR[27]	Y08
V_{DDEXT}	U09	ADDR[28]	V09	ADDR[29]	W09	ADDR[30]	Y09
V_{DDEXT}	U10	ID0	V10	ID1	W10	ADDR[31]	Y10
V_{DDEXT}	U11	ADDR[1]	V11	ADDR[0]	W11	ID2	Y11
V_{DDEXT}	U12	$\overline{MS1}$	V12	$\overline{BMS}$	W12	BRST	Y12
V_{DDEXT}	U13	$\overline{CS}$	V13	$\overline{MS2}$	W13	$\overline{MS0}$	Y13
V_{DDEXT}	U14	$\overline{RDL}$	V14	$\overline{CIF}$	W14	$\overline{MS3}$	Y14
V_{DDEXT}	U15	$\overline{DMAR2}$	V15	$\overline{RDH}$	W15	$\overline{WRH}$	Y15
V_{DDEXT}	U16	L5DAT[0]	V16	$\overline{DMAG2}$	W16	$\overline{WRL}$	Y16
L5DAT[7]	U17	L5DAT[2]	V17	LBOOT	W17	$\overline{DMAG1}$	Y17
L4DAT[0]	U18	L5ACK	V18	L5DAT[1]	W18	$\overline{DMAR1}$	Y18
L4DAT[1]	U19	L5DAT[4]	V19	L5DAT[3]	W19	EBOOT	Y19
L4DAT[2]	U20	L5DAT[6]	V20	L5DAT[5]	W20	L5CLK	Y20

[1] For ADSP-21160M, Pin Name and function is defined as V_{DDEXT}. For ADSP-21160N, Pin Name and function is defined as No Connect (NC).
[2] For ADSP-21160M, Pin Name and function is defined as GND. For ADSP-21160N, Pin Name and function is defined as No Connect (NC).