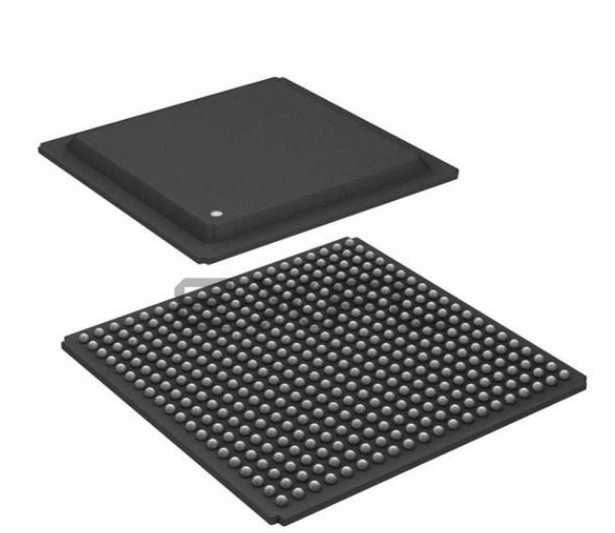

Welcome to E-XFL.COM

Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Floating Point
Interface	Host Interface, Link Port, Serial Port
Clock Rate	100MHz
Non-Volatile Memory	External
On-Chip RAM	512kB
Voltage - I/O	3.30V
Voltage - Core	1.90V
Operating Temperature	0°C ~ 85°C (TC)
Mounting Type	Surface Mount
Package / Case	400-BBGA
Supplier Device Package	400-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21160nkbz-100

- **Single-instruction, multiple-data (SIMD) architecture provides**
  - **Two computational processing elements**
  - **Concurrent execution—each processing element executes the same instruction, but operates on different data**
  - **Code compatibility—at assembly level, uses the same instruction set as the ADSP-2106x SHARC DSPs**
- **Parallelism in buses and computational units allows**
  - **Single-cycle execution (with or without SIMD) of a multiply operation, an ALU operation, a dual memory read or write, and an instruction fetch**
  - **Transfers between memory and core at up to four 32-bit floating- or fixed-point words per cycle**
  - **Accelerated FFT butterfly computation through a multiply with add and subtract**
- **Memory attributes**
  - **4M bits on-chip dual-ported SRAM for independent access by core processor, host, and DMA**
  - **4G word address range for off-chip memory**
  - **Memory interface supports programmable wait state generation and page-mode for off-chip memory**
- **DMA controller supports**
  - **14 zero-overhead DMA channels for transfers between ADSP-21160x internal memory and external memory, external peripherals, host processor, serial ports, or link ports**
  - **64-bit background DMA transfers at core clock speed, in parallel with full-speed processor execution**
  - **Host processor interface to 16- and 32-bit microprocessors**
- **Multiprocessing support provides**
  - **Glueless connection for scalable DSP multiprocessing architecture**
  - **Distributed on-chip bus arbitration for parallel bus connect of up to 6 ADSP-21160x processors plus host**
  - **6 link ports for point-to-point connectivity and array multiprocessing**
- **Serial ports provide**
  - **Two synchronous serial ports with companding hardware**
  - **Independent transmit and receive functions**
  - **TDM support for T1 and E1 interfaces**
- **64-bit-wide synchronous external port provides**
  - **Glueless connection to asynchronous and SBSRAM external memories**

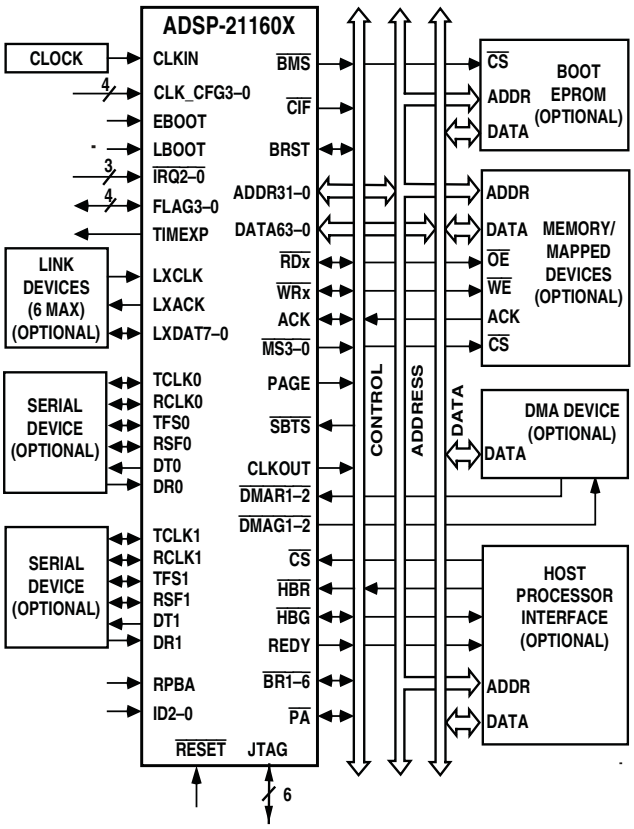

Figure 2. Single-Processor System

enabled, the same instruction is executed in both processing elements, but each processing element operates on different data. This architecture is efficient at executing math-intensive DSP algorithms.

Entering SIMD mode also has an effect on the way data is transferred between memory and the processing elements. In SIMD mode, twice the data bandwidth is required to sustain computational operation in the processing elements. Because of this requirement, entering SIMD mode also doubles the bandwidth between memory and the processing elements. When using the DAGs to transfer data in SIMD mode, two data values are transferred with each access of memory or the register file.

Independent, Parallel Computation Units

Within each processing element is a set of computational units. The computational units consist of an arithmetic/logic unit (ALU), multiplier, and shifter. These units perform single-cycle instructions. The three units within each processing element are arranged in parallel, maximizing computational throughput. Single multifunction instructions execute parallel ALU and multiplier operations. In SIMD mode, the parallel ALU and multiplier operations occur in both processing elements. These computation units support IEEE 32-bit single-precision floating-point, 40-bit extended-precision floating-point, and 32-bit fixed-point data formats.

Data Register File

A general-purpose data register file is contained in each processing element. The register files transfer data between the computation units and the data buses, and store intermediate results. These 10-port, 32-register (16 primary, 16 secondary) register files, combined with the ADSP-2116x enhanced Harvard architecture, allow unconstrained data flow between computation units and internal memory. The registers in PEX are referred to as R0–R15 and in PEY as S0–S15.

Single-Cycle Fetch of Instruction and Four Operands

The processor features an enhanced Harvard architecture in which the data memory (DM) bus transfers data, and the program memory (PM) bus transfers both instructions and data (see the functional block diagram 1). With the ADSP-21160x DSP's separate program and data memory buses and on-chip instruction cache, the processor can simultaneously fetch four operands and an instruction (from the cache), all in a single cycle.

Instruction Cache

The ADSP-21160x includes an on-chip instruction cache that enables three-bus operation for fetching an instruction and four data values. The cache is selective—only the instructions whose fetches conflict with PM bus data accesses are cached. This cache allows full-speed execution of core, providing looped operations, such as digital filter multiply- accumulates and FFT butterfly processing.

Data Address Generators with Hardware Circular Buffers

The ADSP-21160x DSP's two data address generators (DAGs) are used for indirect addressing and provide for implementing circular data buffers in hardware. Circular buffers allow efficient programming of delay lines and other data structures required in digital signal processing, and are commonly used in digital filters and Fourier transforms. The two DAGs of the product contain sufficient registers to allow the creation of up to 32 circular buffers (16 primary register sets, 16 secondary). The DAGs automatically handle address pointer wraparound, reducing overhead, increasing performance, and simplifying implementation. Circular buffers can start and end at any memory location.

Flexible Instruction Set

The 48-bit instruction word accommodates a variety of parallel operations for concise programming. For example, the processor can conditionally execute a multiply, an add, and subtract, in both processing elements, while branching, all in a single instruction.

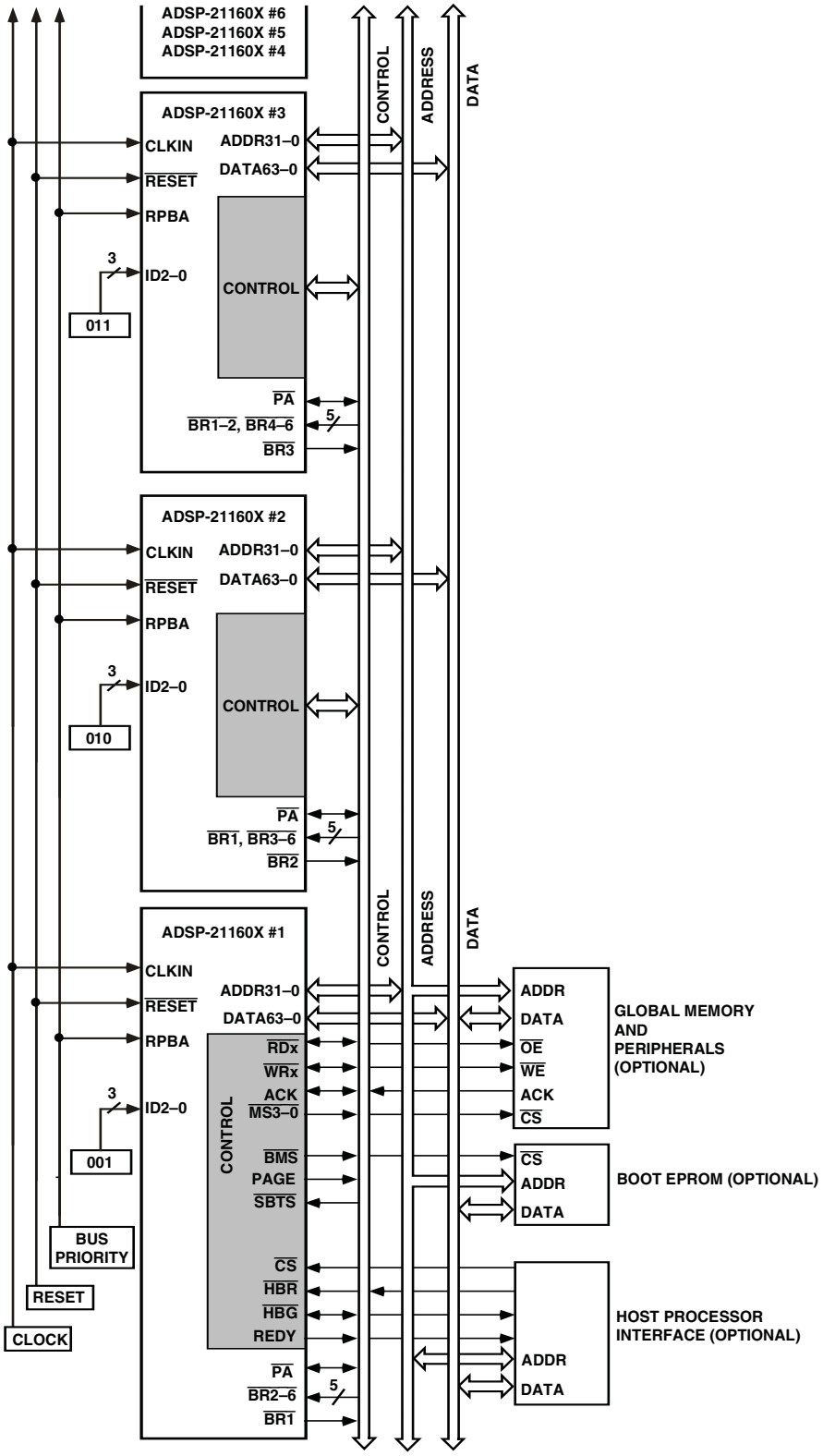

Figure 3. Shared Memory Multiprocessing System

MEMORY AND I/O INTERFACE FEATURES

Augmenting the ADSP-2116x family core, the ADSP-21160x adds the following architectural features.

Dual-Ported On-Chip Memory

The ADSP-21160x contains four megabits of on-chip SRAM, organized as two blocks of 2M bits each, which can be configured for different combinations of code and data storage (Figure 4). Each memory block is dual-ported for single-cycle, independent accesses by the core processor and I/O processor. The dual-ported memory in combination with three separate on-chip buses allows two data transfers from the core and one from I/O processor, in a single cycle. The ADSP-21160x memory can be configured as a maximum of 128K words of 32-bit data, 256K words of 16-bit data, 85K words of 48-bit instructions (or 40-bit data), or combinations of different word sizes up to four megabits. All of the memory can be accessed as 16-, 32-, 48-, or 64-bit words. A 16-bit floating-point storage format is supported that effectively doubles the amount of data that may be stored on-chip. Conversion between the 32-bit floating-point and 16-bit floating-point formats is done in a single instruction. While each memory block can store combinations of code and data, accesses are most efficient when one block stores data, using the DM bus for transfers, and the other block stores instructions and data, using the PM bus for transfers. Using the DM bus and PM bus in this way, with one dedicated to each memory block, assures single-cycle execution with two data transfers. In this case, the instruction must be available in the cache.

Off-Chip Memory and Peripherals Interface

The ADSP-21160x DSP's external port provides the processor's interface to off-chip memory and peripherals. The 4G word off-chip address space is included in the processor's unified address space. The separate on-chip buses—for PM addresses, PM data, DM addresses, DM data, I/O addresses, and I/O data—are multiplexed at the external port to create an external system bus with a single 32-bit address bus and a single 64-bit data bus. The lower 32 bits of the external data bus connect to even addresses, and the upper 32 bits of the 64 connect to odd addresses. Every access to external memory is based on an address that fetches a 32-bit word, and with the 64-bit bus, two address locations can be accessed at once. When fetching an instruction from external memory, two 32-bit data locations are being accessed (16 bits are unused). Figure 5 shows the alignment of various accesses to external memory.

The external port supports asynchronous, synchronous, and synchronous burst accesses. ZBT synchronous burst SRAM can be interfaced gluelessly. Addressing of external memory devices is facilitated by on-chip decoding of high-order address lines to generate memory bank select signals. Separate control lines are also generated for simplified addressing of page-mode DRAM. The ADSP-21160x provides programmable memory wait states and external memory acknowledge controls to allow interfacing to DRAM and peripherals with variable access, hold, and disable time requirements.

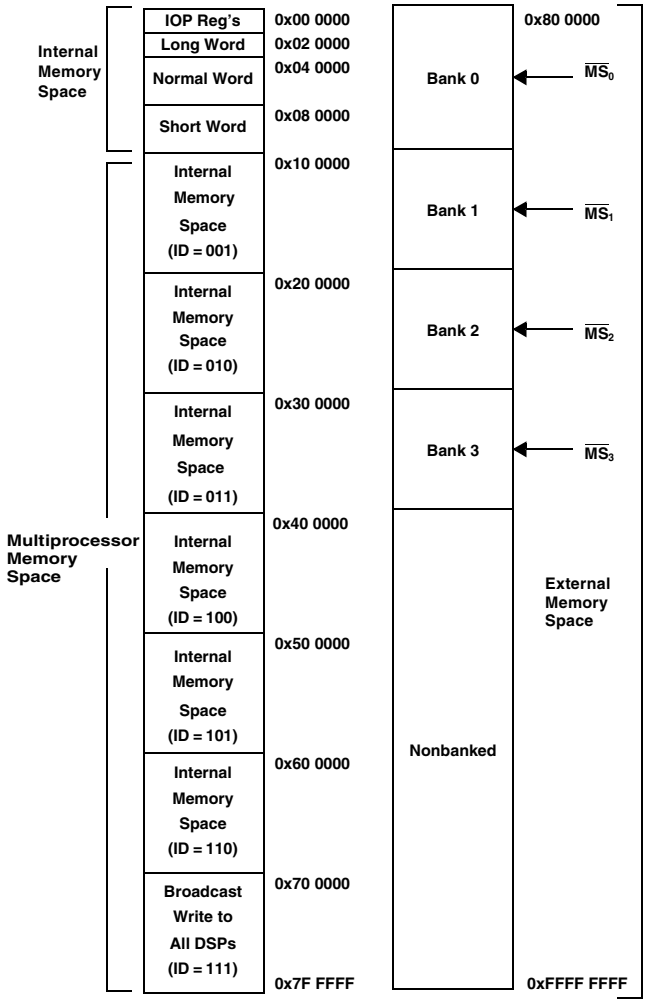

Figure 4. Memory Map

DMA Controller

The ADSP-21160x DSP's on-chip DMA controller allows zero-overhead data transfers without processor intervention. The DMA controller operates independently and invisibly to the processor core, allowing DMA operations to occur while the core is simultaneously executing its program instructions. DMA transfers can occur between the processor's internal memory and external memory, external peripherals, or a host processor. DMA transfers can also occur between the product's DSP's internal memory and its serial ports or link ports. External bus packing to 16-, 32-, 48-, or 64-bit words is performed during DMA transfers. Fourteen channels of DMA are available on the ADSP-21160x—six via the link ports, four via the serial ports, and four via the processor's external port (for either host processor, other ADSP-21160x processors, memory or I/O transfers). Programs can be downloaded to the processor using DMA transfers. Asynchronous off-chip peripherals can control two DMA channels using DMA Request/Grant lines ($\overline{\text{DMAR1–2}}$, $\overline{\text{DMAG1–2}}$). Other DMA features include

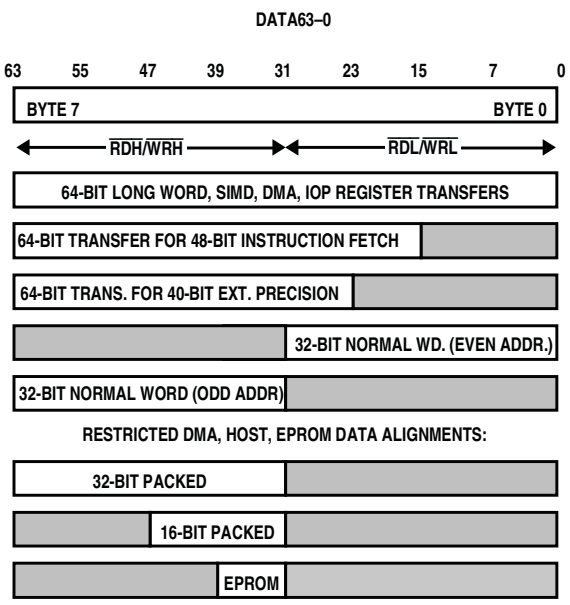

Figure 5. External Data Alignment Options

interrupt generation upon completion of DMA transfers, two-dimensional DMA, and DMA chaining for automatic linked DMA transfers.

Multiprocessing

The ADSP-21160x offers powerful features tailored to multiprocessing DSP systems as shown in M. The external port and link ports provide integrated glueless multiprocessing support.

The external port supports a unified address space (see Figure 4) that allows direct interprocessor accesses of each processor's internal memory. Distributed bus arbitration logic is included on-chip for simple, glueless connection of systems containing up to six ADSP-21160x processors and a host processor. Master processor changeover incurs only one cycle of overhead. Bus arbitration is selectable as either fixed or rotating priority. Bus lock allows indivisible read-modify-write sequences for semaphores. A vector interrupt is provided for interprocessor commands. Maximum throughput for interprocessor data transfer is 400M bytes/s (ADSP-21160N) over the external port. Broadcast writes allow simultaneous transmission of data to all ADSP-21160x DSPs and can be used to implement reflective semaphores.

Six link ports provide for a second method of multiprocessing communications. Each link port can support communications to another ADSP-21160x. Using the links, a large multiprocessor system can be constructed in a 2D or 3D fashion. Systems can use the link ports and cluster multiprocessing concurrently or independently.

Link Ports

The processor features six 8-bit link ports that provide additional I/O capabilities. With the capability of running at 100 MHz rates, each link port can support 100M bytes/s (ADSP-21160N). Link port I/O is especially useful for point-to-point interprocessor communication in multiprocessing systems. The link ports can operate independently and simultaneously. Link port data is packed into 48- or 32-bit words, and can be directly read by the core processor or DMA-transferred to on-chip memory. Each link port has its own double-buffered input and output registers. Clock/acknowledge handshaking controls link port transfers. Transfers are programmable as transmit or receive.

Serial Ports

The processor features two synchronous serial ports that provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices. The serial ports can operate up to half the clock rate of the core, providing each with a maximum data rate of 50M bits/s (ADSP-21160N). Independent transmit and receive functions provide greater flexibility for serial communications. Serial port data can be automatically transferred to and from on-chip memory via a dedicated DMA. Each of the serial ports offers a TDM multichannel mode. The serial ports can operate with little-endian or big-endian transmission formats, with word lengths selectable from 3 bits to 32 bits. They offer selectable synchronization and transmit modes as well as optional μ-law or A-law companding. Serial port clocks and frame syncs can be generated internally or externally.

Host Processor Interface

The ADSP-21160x host interface allows easy connection to standard microprocessor buses, both 16- and 32-bit, with little additional hardware required. The host interface is accessed through the ADSP-21160x DSP's external port and is memory-mapped into the unified address space. Four channels of DMA are available for the host interface; code and data transfers are accomplished with low software overhead. The host processor communicates with the ADSP-21160x DSP's external bus with host bus request ($\overline{HBR}$), host bus grant ($\overline{HBG}$), ready (REDY), acknowledge (ACK), and chip select (CS) signals. The host can directly read and write the internal memory of the processor, and can access the DMA channel setup and mailbox registers. Vector interrupt support provides efficient execution of host commands.

The host processor interface can be used in either multiprocessor or uniprocessor systems. For multiprocessor systems, host access to the SHARC requires that address pins ADDR17, ADDR18, ADDR19, and ADDR20 be driven low. It is not enough to tie these pins to ground through a resistor (for example, 10 kΩ). These pins must be driven low with a strong enough drive strength (10 Ω to 50 Ω) to overcome the SHARC keeper latches present on these pins. If the drive strength provided is not strong enough, data access failures can occur.

For uniprocessor SHARC systems using this host access feature, address pins ADDR17, ADDR18, ADDR19, and ADDR20 may be tied low (for example, through a 10 kΩ ohm resistor), driven low by a buffer/driver, or left floating. Any of these options is sufficient.

located on the web page for the associated EZ-KIT or EZ-Extender product. The link is found in the *Product Download* area of the product web page.

Middleware Packages

Analog Devices separately offers middleware add-ins such as real time operating systems, file systems, USB stacks, and TCP/IP stacks. For more information, see the following web pages:

- www.analog.com/ucos3
- www.analog.com/ucfs
- www.analog.com/ucusbd
- www.analog.com/lwip

Algorithmic Modules

To speed development, Analog Devices offers add-ins that perform popular audio and video processing algorithms. These are available for use with both CrossCore Embedded Studio and VisualDSP++. For more information visit www.analog.com and search on "Blackfin software modules" or "SHARC software modules".

Designing an Emulator-Compatible DSP Board (Target)

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG Test Access Port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the processor's internal features via the processor's TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers. The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the DSP's JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see the application note (EE-68) "Analog Devices JTAG Emulation Technical Reference" (www.analog.com/ee-68). This document is updated regularly to keep pace with improvements to emulator support.

ADDITIONAL INFORMATION

This data sheet provides a general overview of the ADSP-21160x architecture and functionality. For detailed information on the Blackfin family core architecture and instruction set, refer to the *ADSP-21160 SHARC DSP Hardware Reference* and the *ADSP-21160 SHARC DSP Instruction Set Reference*. For detailed information on the development tools for this processor, see the *VisualDSP++ User's Guide*.

RELATED SIGNAL CHAINS

A signal chain is a series of signal conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next.

Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The application signal chains page in the Circuits from the Lab® site (http:\\www.analog.com\circuits) provides:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

ABSOLUTE MAXIMUM RATINGS

Stresses at or above those listed in Table 9 (ADSP-21160M) and Table 10 (ADSP-21160N) may cause permanent damage to the product. These are stress ratings only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 9. Absolute Maximum Ratings—ADSP-21160M

Parameter	Rating
Internal (Core) Supply Voltage (V_{DDINT})	–0.3 V to +3.0 V
Analog (PLL) Supply Voltage (A_{VDD})	–0.3 V to +3.0 V
External (I/O) Supply Voltage (V_{DDEXT})	–0.3 V to +4.6 V
Input Voltage	–0.5 V to V_{DDEXT} + 0.5 V
Output Voltage Swing	–0.5 V to V_{DDEXT} + 0.5 V
Load Capacitance	200 pF
Storage Temperature Range	–65°C to +150°C

Table 10. Absolute Maximum Ratings—ADSP-21160N

Parameter	Rating
Internal (Core) Supply Voltage (V_{DDINT})	–0.3 V to +2.3 V
Analog (PLL) Supply Voltage (A_{VDD})	–0.3 V to +2.3 V
External (I/O) Supply Voltage (V_{DDEXT})	–0.3 V to +4.6 V
Input Voltage	–0.5 V to V_{DDEXT} + 0.5 V
Output Voltage Swing	–0.5 V to V_{DDEXT} + 0.5 V
Load Capacitance	200 pF
Storage Temperature Range	–65°C to +150°C

ESD SENSITIVITY

ESD (electrostatic discharge sensitive device)
Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PACKAGE INFORMATION

The information presented in Figure 7 provides details about the package branding for the ADSP-21160M/ADSP-21160N processor. For a complete listing of product availability, see Ordering Guide on Page 58.

Figure 7. Typical Package Brand

Table 11. Package Brand Information

Brand Key	Field Description
a	ADSP-21160 Model (M or N)
t	Temperature Range
pp	Package Type
Z	RoHS Compliant Designation
cc	See Ordering Guide
vvvvvv.x	Assembly Lot Code
n.n	Silicon Revision
#	RoHS Compliant Designation
yyww	Date Code

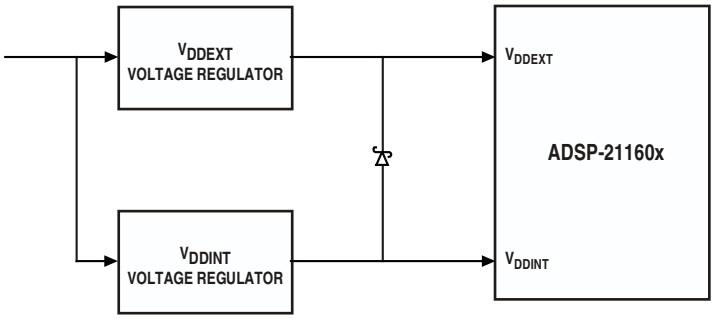

Figure 9. Dual Voltage Schottky Diode

Clock Input

For clock input, see Table 13 and Figure 10.

Table 13. Clock Input

Parameter		ADSP-21160M 80 MHz		ADSP-21160N 100 MHz		Unit
		Min	Max	Min	Max	
Timing Requirements						
t_{CK}	CLKIN Period	25	80	20	80	ns
t_{CKL}	CLKIN Width Low	10.5	40	7.5	40	ns
t_{CKH}	CLKIN Width High	10.5	40	7.5	40	ns
t_{CKRF}	CLKIN Rise/Fall (0.4 V–2.0 V)		3		3	ns
t_{CCLK}	Core Clock Period	12.5	40	10	30	ns

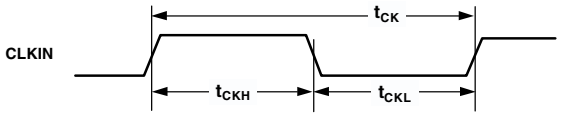

Figure 10. Clock Input

Interrupts

For interrupts, see Table 15 and Figure 12.

Table 15. Interrupts

Parameter		Min	Max	Unit
Timing Requirements				
t_{SIR}	$\overline{IRQ2–0}$ Setup Before CLKIN High[1]	6		ns
t_{HIR}	$\overline{IRQ2–0}$ Hold After CLKIN High[1]	0		ns
t_{IPW}	$\overline{IRQ2–0}$ Pulsewidth[2]	$2+t_{CK}$		ns

[1] Only required for $\overline{IRQx}$ recognition in the following cycle.
[2] Applies only if t_{SIR} and t_{HIR} requirements are not met.

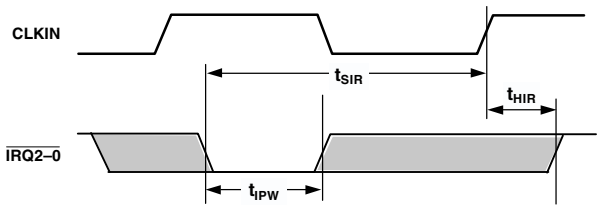

Figure 12. Interrupts

Timer

For timer, see Table 16 and Figure 13.

Table 16. Timer

Parameter		Min	Max	Unit
Switching Characteristic				
t_{DTEX}	CLKIN High to TIMEXP[1]	1	9	ns

[1] For ADSP-21160M, specification is 7 ns, maximum.

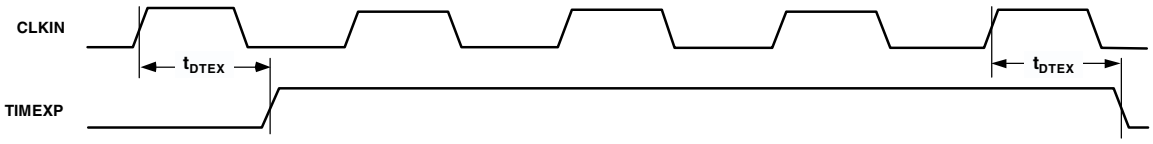

Figure 13. Timer

Flags

For flags, see Table 17 and Figure 14.

Table 17. Flags

Parameter		Min	Max	Unit
Timing Requirements				
t_{SFI}	FLAG3–0 IN Setup Before CLKIN High[1]	4		ns
t_{HFI}	FLAG3–0 IN Hold After CLKIN High[1]	1		ns
t_{DWRFI}	FLAG3–0 IN Delay After $\overline{RDx}$/$\overline{WRx}$ Low[1, 2]		10	ns
t_{HFIWR}	FLAG3–0 IN Hold After $\overline{RDx}$/$\overline{WRx}$ Deasserted[1]	0		ns
Switching Characteristics				
t_{DFO}	FLAG3–0 OUT Delay After CLKIN High		9	ns
t_{HFO}	FLAG3–0 OUT Hold After CLKIN High	1		ns
t_{DFOE}	CLKIN High to FLAG3–0 OUT Enable	1		ns
t_{DFOD}	CLKIN High to FLAG3–0 OUT Disable[3]		$t_{CK} - t_{CCLK} + 5$	ns

[1] Flag inputs meeting these setup and hold times for instruction cycle N will affect conditional instructions in instruction cycle N + 2.
[2] For ADSP-21160M, specification is 12 ns, maximum.
[3] For ADSP-21160M, specification is 5 ns, maximum.

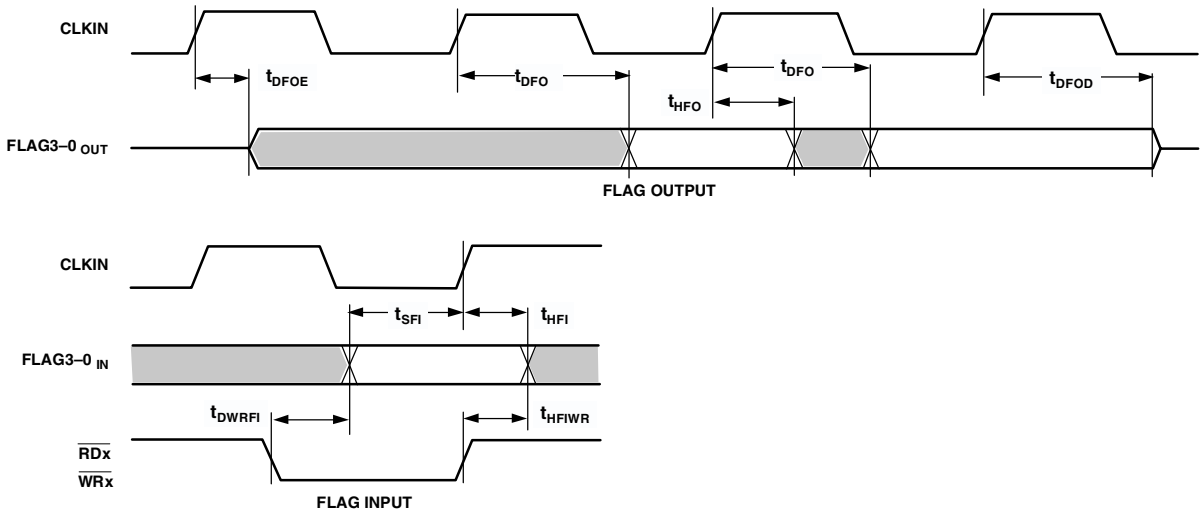

Figure 14. Flags

Synchronous Read/Write—Bus Master

See Table 20 and Figure 17. Use these specifications for interfacing to external memory systems that require CLKIN—relative timing or for accessing a slave ADSP-21160x (in multiprocessor memory space). These synchronous switching characteristics are also valid during asynchronous memory reads and writes except where noted (see Memory Read–Bus Master on page 26 and Memory Write–Bus Master on page 28).

When accessing a slave ADSP-21160x, these switching characteristics must meet the slave's timing requirements for synchronous read/writes (see Synchronous Read/Write–Bus Slave on page 32). The slave ADSP-21160x must also meet these (bus master) timing requirements for data and acknowledge setup and hold times.

Table 20. Synchronous Read/Write—Bus Master

Parameter		Min	Max	Unit
Timing Requirements				
t_{SSDATI}	Data Setup Before CLKIN	5.5		ns
t_{HSDATI}	Data Hold After CLKIN	1		ns
t_{SACKC}	ACK Setup Before CLKIN	$0.5t_{CCLK}+3$		ns
t_{HACKC}	ACK Hold After CLKIN	1		ns
Switching Characteristics				
t_{DADDO}	Address, $\overline{MSx}$, $\overline{BMS}$, BRST, $\overline{CIF}$ Delay After CLKIN		10	ns
t_{HADDO}	Address, $\overline{MSx}$, $\overline{BMS}$, BRST, $\overline{CIF}$ Hold After CLKIN	1.5		ns
t_{DPGO}	PAGE Delay After CLKIN	1.5	11	ns
t_{DRDO}	$\overline{RDx}$ High Delay After CLKIN	$0.25t_{CCLK}-1$	$0.25t_{CCLK}+9$	ns
t_{DWRO}	$\overline{WRx}$ High Delay After CLKIN	$0.25t_{CCLK}-1$	$0.25t_{CCLK}+9$	ns
t_{DRWL}	$\overline{RDx}$/$\overline{WRx}$ Low Delay After CLKIN	$0.25t_{CCLK}-1$	$0.25t_{CCLK}+9$	ns
t_{DDATO}	Data Delay After CLKIN[1]		$0.25t_{CCLK}+9$	ns
t_{HDATO}	Data Hold After CLKIN	1.5		ns
t_{DACKMO}	ACK Delay After CLKIN[2, 3]	3	9	ns
t_{ACKMTR}	ACK Disable Before CLKIN[2]	−3		ns
t_{DCKOO}	CLKOUT Delay After CLKIN[4]	0.5	5	ns
t_{CKOP}	CLKOUT Period	$t_{CK}-1$	t_{CK}[5] $+1$	ns
t_{CKWH}	CLKOUT Width High	$t_{CK}/2-2$	$t_{CK}/2+2$[2]	ns
t_{CKWL}	CLKOUT Width Low	$t_{CK}/2-2$	$t_{CK}/2+2$[2]	ns

[1] For ADSP-21160M, specification is 12.5 ns, maximum.
[2] Applies to broadcast write, master precharge of ACK.
[3] For ADSP-21160M, specification is $0.25t_{CCLK}+3$ ns (minimum) and $.25t_{CCLK}+9$ ns (maximum).
[4] For ADSP-21160M, specification is 2 ns, minimum.
[5] Applies only when the DSP drives a bus operation; CLKOUT held inactive or three-state otherwise. For more information, see the System Design chapter in the *ADSP-21160 SHARC DSP Hardware Reference*.

Asynchronous Read/Write—Host to ADSP-21160x

Use these specifications (Table 23, Table 24, Figure 20, and Figure 21) for asynchronous host processor accesses of an ADSP-21160x, after the host has asserted $\overline{CS}$ and $\overline{HBR}$ (low). After $\overline{HBG}$ is returned by the ADSP-21160x, the host can drive the $\overline{RDx}$ and $\overline{WRx}$ pins to access the ADSP-21160x DSP's internal memory or IOP registers. $\overline{HBR}$ and $\overline{HBG}$ are assumed low for this timing.

Table 23. Read Cycle

Parameter		Min	Max	Unit
Timing Requirements				
t_{SADRDL}	Address Setup/$\overline{CS}$ Low Before $\overline{RDx}$ Low	0		ns
t_{HADRDH}	Address Hold/$\overline{CS}$ Hold Low After $\overline{RDx}$	2		ns
t_{WRWH}	$\overline{RDx}$/$\overline{WRx}$ High Width	5		ns
$t_{DRDHRDY}$	$\overline{RDx}$ High Delay After REDY (O/D) Disable	0		ns
$t_{DRDHRDY}$	$\overline{RDx}$ High Delay After REDY (A/D) Disable	0		ns
Switching Characteristics				
$t_{SDATRDY}$	Data Valid Before REDY Disable from Low	2		ns
$t_{DRDYRDL}$	REDY (O/D) or (A/D) Low Delay After $\overline{RDx}$ Low[1]		11	ns
t_{RDYPRD}	REDY (O/D) or (A/D) Low Pulsewidth for Read[2]	t_{CK} – 4		ns
t_{HDARWH}	Data Disable After $\overline{RDx}$ High[3]	1.5	6	ns

[1] For ADSP-21160M, specification is 7 ns, minimum.
[2] For ADSP-21160M, specification is t_{CK} ns, minimum.
[3] For ADSP-21160M, specification is 2 ns, minimum.

Table 24. Write Cycle

Parameter		Min	Max	Unit
Timing Requirements				
t_{SCSWRL}	$\overline{CS}$ Low Setup Before $\overline{WRx}$ Low	0		ns
t_{HCSWRH}	$\overline{CS}$ Low Hold After $\overline{WRx}$ High	0		ns
t_{SADWRH}	Address Setup Before $\overline{WRx}$ High	6		ns
t_{HADWRH}	Address Hold After $\overline{WRx}$ High	2		ns
t_{WWRL}	$\overline{WRx}$ Low Width[1]	t_{CCLK}+1		ns
t_{WRWH}	$\overline{RDx}$/$\overline{WRx}$ High Width	5		ns
$t_{DWRHRDY}$	$\overline{WRx}$ High Delay After REDY (O/D) or (A/D) Disable	0		ns
t_{SDATWH}	Data Setup Before $\overline{WRx}$ High	5		ns
t_{HDATWH}	Data Hold After $\overline{WRx}$ High	4		ns
Switching Characteristics				
$t_{DRDYWRL}$	REDY (O/D) or (A/D) Low Delay After $\overline{WRx}$/$\overline{CS}$ Low		11	ns
t_{RDYPWR}	REDY (O/D) or (A/D) Low Pulsewidth for Write[2]	5.75 + 0.5t_{CCLK}		ns

[1] For ADSP-21160M, specification is 7 ns, minimum.
[2] For ADSP-21160M, specification is 12 ns, minimum.

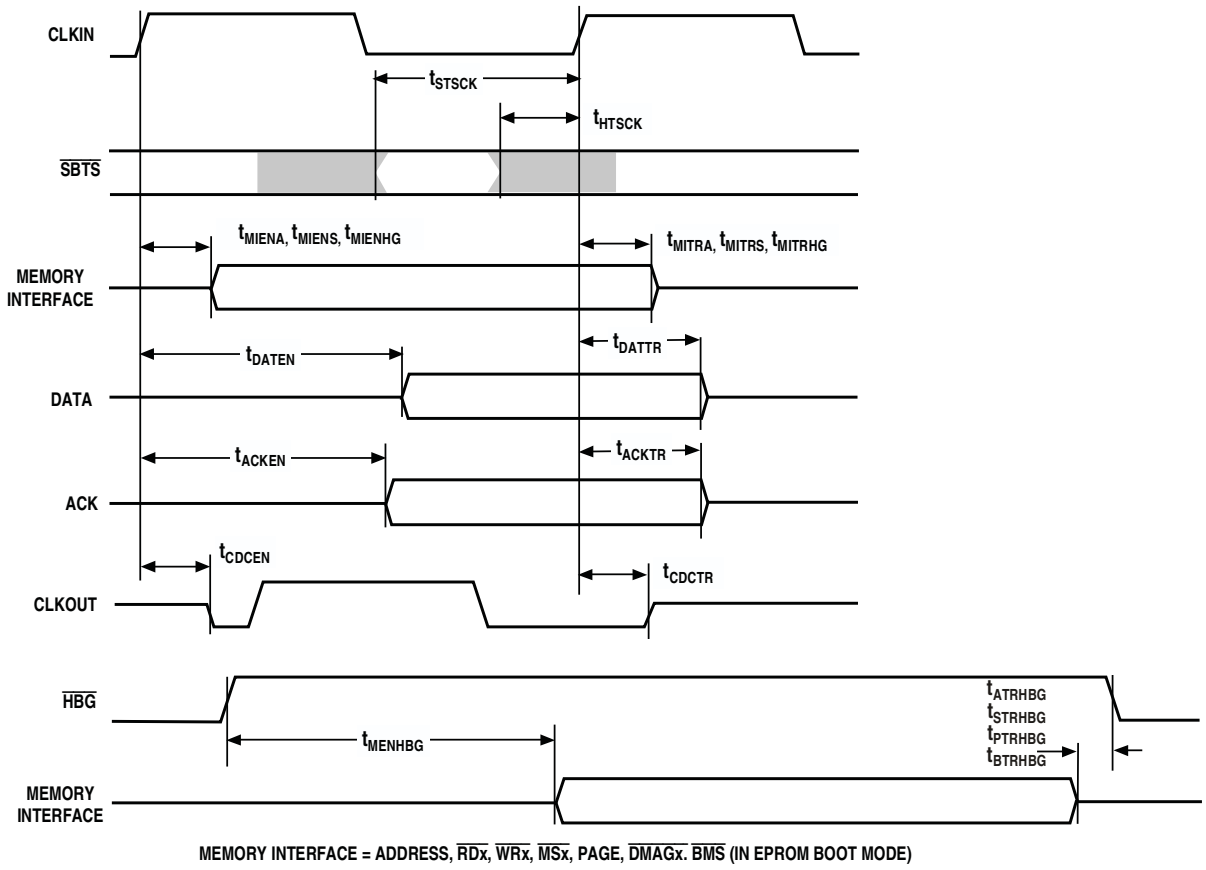

Figure 22. Three-State Timing—Bus Master, Bus Slave

Link Ports—Receive, Transmit

For link ports, see Table 27, Table 28, Figure 24, and Figure 25. Calculation of link receiver data setup and hold, relative to link clock, is required to determine the maximum allowable skew that can be introduced in the transmission path, between LDATA and LCLK. Setup skew is the maximum delay that can be introduced in LDATA, relative to LCLK (setup skew = $t_{LCLKTWH}$ minimum – t_{DLDCH} – t_{SLDCL}). Hold skew is the maximum delay that can be introduced in LCLK, relative to LDATA (hold skew = $t_{LCLKTWL}$ minimum + t_{HLDCH} – t_{HLDCL}). Calculations made directly from speed specifications result in unrealistically small skew times, because they include multiple tester guardbands.

Note that there is a two-cycle effect latency between the link port enable instruction and the DSP enabling the link port.

Table 27. Link Ports—Receive

Parameter		Min	Max	Unit
Timing Requirements				
t_{SLDCL}	Data Setup Before LCLK Low	2.5		ns
t_{HLDCL}	Data Hold After LCLK Low[1]	3		ns
t_{LCLKIW}	LCLK Period	t_{LCLK}		ns
$t_{LCLKRWL}$	LCLK Width Low[2]	4		ns
$t_{LCLKRWH}$	LCLK Width High[3]	4		ns
Switching Characteristics				
t_{DLALC}	LACK Low Delay After LCLK High[4, 5]	9	17	ns

[1] For ADSP-21160M, specification is 2.5 ns, minimum.
[2] For ADSP-21160M, specification is 6 ns, minimum.
[3] For ADSP-21160M, specification is 6 ns, minimum.
[4] LACK goes low with t_{DLALC} relative to rise of LCLK after first nibble, but does not go low if the receiver's link buffer is not about to fill.
[5] For ADSP-21160M, specification is 12 ns, minimum.

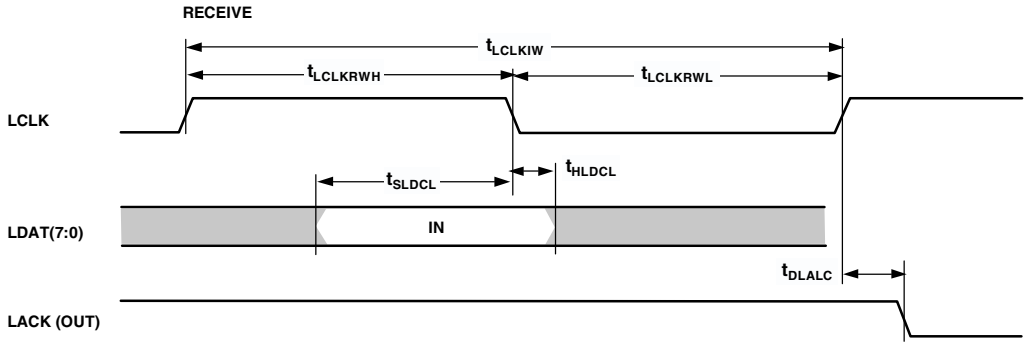

Figure 24. Link Ports—Receive

Table 33. Serial Ports—Enable and Three-State

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DDTEN}	Data Enable from External TCLK[1]	4		ns
t_{DDTTE}	Data Disable from External TCLK[1]		10	ns
t_{DDTIN}	Data Enable from Internal TCLK[1]	0		ns
t_{DDTTI}	Data Disable from Internal TCLK[1]		3	ns

[1] Referenced to drive edge.

Table 34. Serial Ports—Internal Clock

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DFSI}	TFS Delay After TCLK (Internally Generated TFS)[1]		4.5	ns
t_{HOFSI}	TFS Hold After TCLK (Internally Generated TFS)[1]	–1.5		ns
t_{DDTI}	Transmit Data Delay After TCLK[1]		7.5	ns
t_{HDTI}	Transmit Data Hold After TCLK[1]	0		ns
t_{SCLKIW}	TCLK/RCLK Width[2]	$0.5t_{SCLK}$ –1.5	$0.5t_{SCLK}$+1.5	ns

[1] Referenced to drive edge.
[2] For ADSP-21160M, specification is $0.5t_{SCLK}$–2.5 ns (minimum) and $0.5t_{SCLK}$+2 ns (maximum)

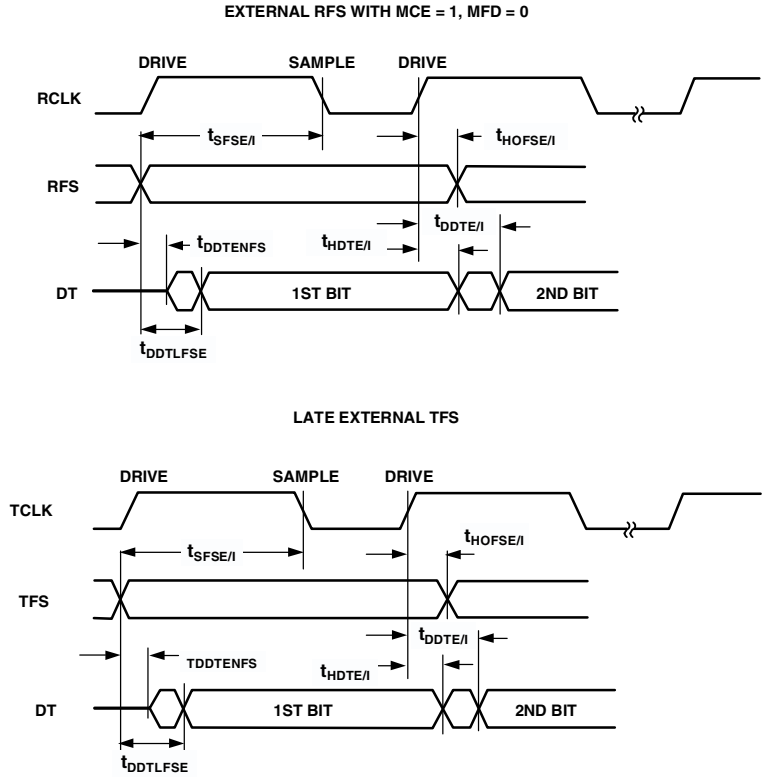

Figure 26. Serial Ports—External Late Frame Sync

Table 35. Serial Ports—External Late Frame Sync

Parameter		Min	Max	Unit
Switching Characteristics				
$t_{DDTLFSE}$	Data Delay from Late External TFS or External RFS with MCE = 1, MFD = 0[1]		13	ns
$t_{DDTENFS}$	Data Enable from Late FS or MCE = 1, MFD = 0[1]	1.0		ns

[1] MCE = 1, TFS enable and TFS valid follow $t_{DDTLFSE}$ and $t_{DDTENFS}$.

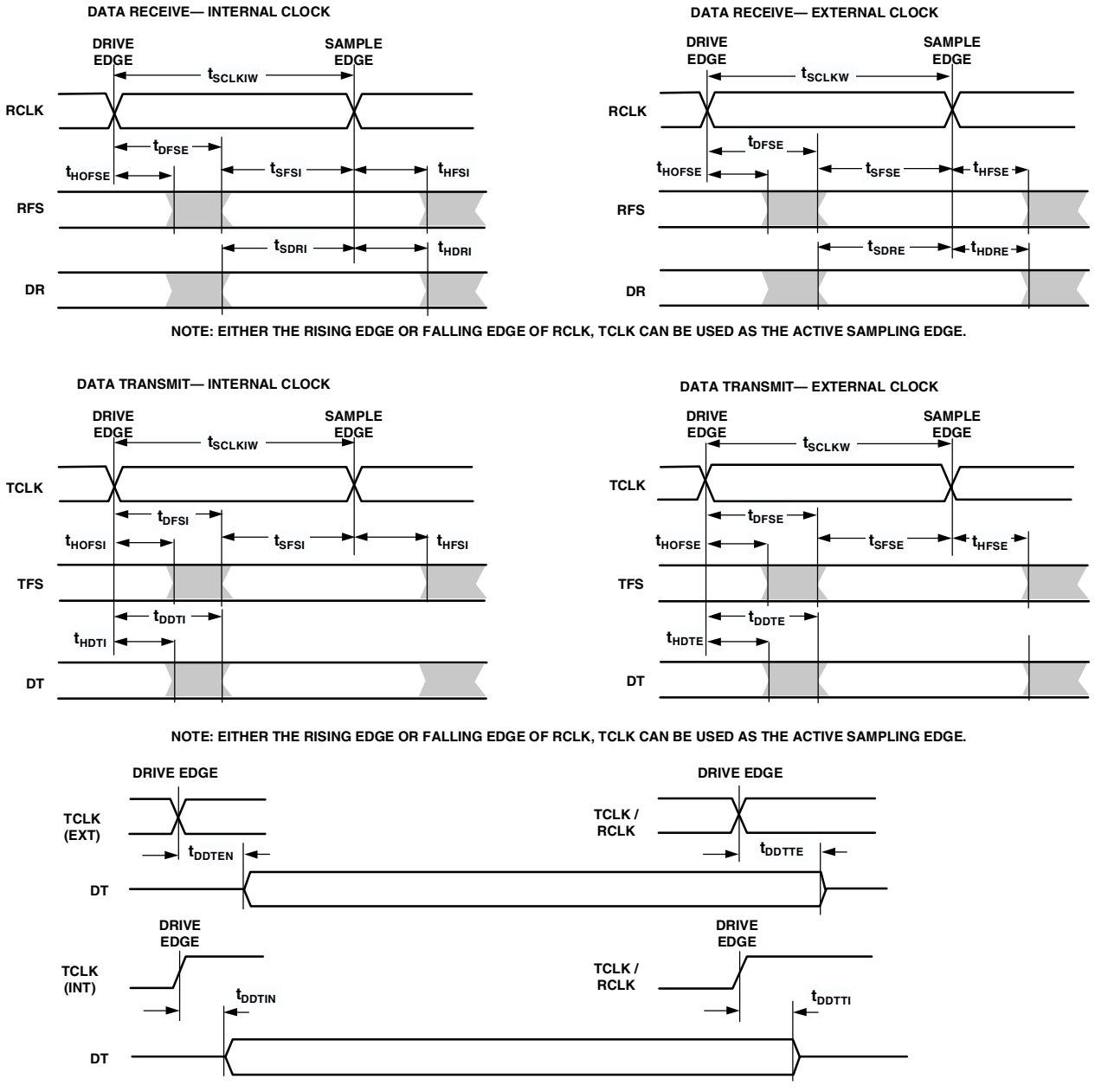

Figure 27. Serial Ports

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high impedance state to when they start driving. The output enable time t_{ENA} is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in the output enable/disable diagram (Figure 31). If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

Example System Hold Time Calculation

To determine the data output hold time in a particular system, first calculate t_{DECAY} using the equation given above. Choose ΔV to be the difference between the ADSP-21160x DSP's output voltage and the input threshold for the device requiring the hold time. A typical ΔV will be 0.4 V. C_L is the total bus capacitance (per data line), and I_L is the total leakage or three-state current (per data line). The hold time will be t_{DECAY} plus the minimum disable time (i.e., t_{DATRWH} for the write cycle).

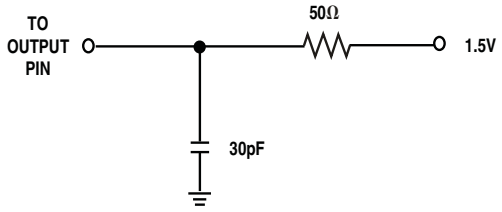

Figure 32. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

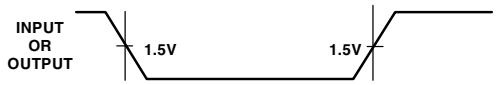

Figure 33. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Capacitive Loading

Output delays and holds are based on standard capacitive loads: 30 pF on all pins (see Figure 32). Figure 34, Figure 35, Figure 37, and Figure 38 show how output rise time varies with capacitance. Figure 36 and Figure 39 graphically show how output delays and holds vary with load capacitance. (Note that this graph or derating does not apply to output disable delays; see Output Disable Time on Page 48.) The graphs of Figure 34 through Figure 39 may not be linear outside the ranges shown.

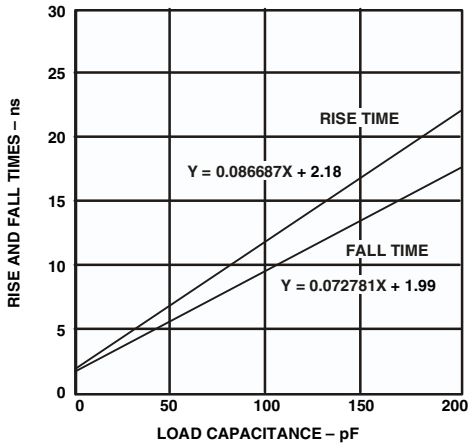

Figure 34. ADSP-21160M Typical Output Rise Time (10%–90%, V_{DDEXT} = Max) vs. Load Capacitance

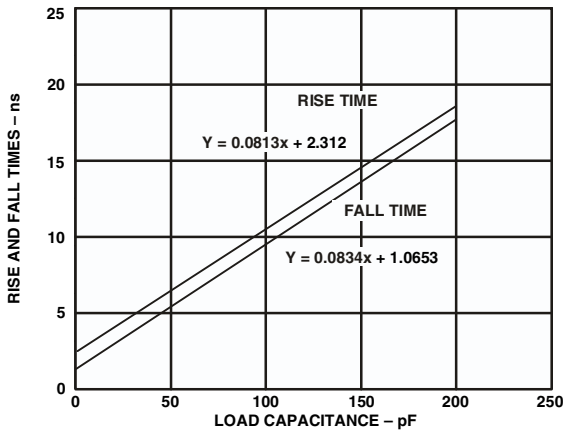

Figure 35. ADSP-21160M Typical Output Rise Time (10%–90%, V_{DDEXT} = Min) vs. Load Capacitance

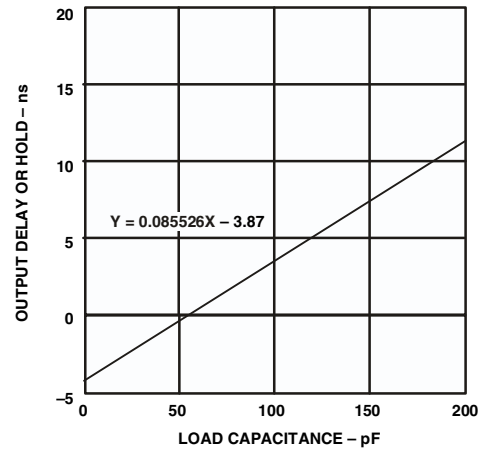

Figure 36. ADSP-21160M Typical Output Delay or Hold vs. Load Capacitance (at Max Case Temperature)

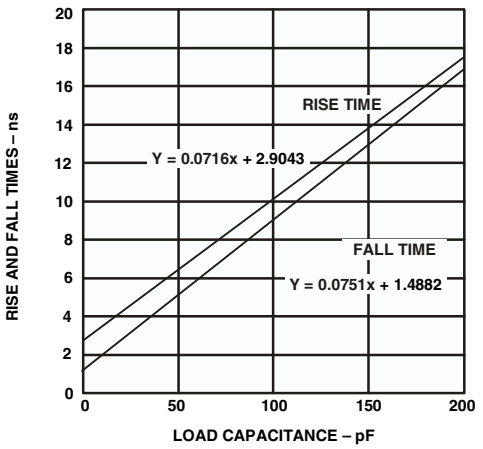

Figure 37. ADSP-21160N Typical Output Rise Time (20%–80%, V_{DDEXT} = Max) vs. Load Capacitance

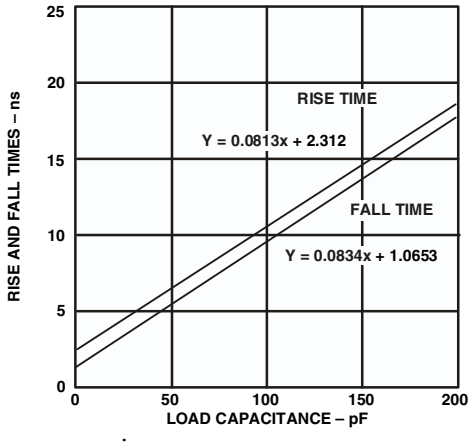

Figure 38. ADSP-21160N Typical Output Rise Time (20%–80%, V_{DDEXT} = Min) vs. Load Capacitance

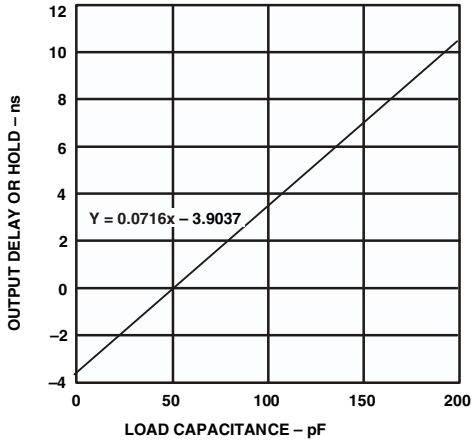

Figure 39. ADSP-21160N Typical Output Delay or Hold vs. Load Capacitance (at Max Case Temperature)

Table 40. 400-Ball PBGA Pin Assignments (Continued)

(See Footnotes 1 and 2)							
Pin Name	**Pin No.**	**Pin Name**	**Pin No.**	**Pin Name**	**Pin No.**	**Pin Name**	**Pin No.**
DATA[44]	J01	CLK_CFG_0	K01	CLKIN	L01	AV_{DD}	M01
DATA[43]	J02	DATA[46]	K02	CLK_CFG_1	L02	CLK_CFG_3	M02
DATA[42]	J03	DATA[45]	K03	AGND	L03	CLKOUT	M03
DATA[41]	J04	DATA[47]	K04	CLK_CFG_2	L04	NC[2]	M04
V_{DDEXT}	J05	V_{DDEXT}	K05	V_{DDEXT}	L05	V_{DDEXT}	M05
V_{DDINT}	J06	V_{DDINT}	K06	V_{DDINT}	L06	V_{DDINT}	M06
GND	J07	GND	K07	GND	L07	GND	M07
GND	J08	GND	K08	GND	L08	GND	M08
GND	J09	GND	K09	GND	L09	GND	M09
GND	J10	GND	K10	GND	L10	GND	M10
GND	J11	GND	K11	GND	L11	GND	M11
GND	J12	GND	K12	GND	L12	GND	M12
GND	J13	GND	K13	GND	L13	GND	M13
GND	J14	GND	K14	GND	L14	GND	M14
V_{DDINT}	J15	V_{DDINT}	K15	V_{DDINT}	L15	V_{DDINT}	M15
V_{DDEXT}	J16	V_{DDEXT}	K16	V_{DDEXT}	L16	V_{DDEXT}	M16
L2DAT[2]	J17	$\overline{BR6}$	K17	$\overline{BR2}$	L17	PAGE	M17
L2DAT[0]	J18	$\overline{BR5}$	K18	$\overline{BR1}$	L18	$\overline{SBTS}$	M18
$\overline{HBG}$	J19	$\overline{BR4}$	K19	ACK	L19	$\overline{PA}$	M19
$\overline{HBR}$	J20	$\overline{BR3}$	K20	REDY	L20	L3DAT[7]	M20
NC	N01	DATA[49]	P01	DATA[53]	R01	DATA[56]	T01
NC	N02	DATA[50]	P02	DATA[54]	R02	DATA[58]	T02
DATA[48]	N03	DATA[52]	P03	DATA[57]	R03	DATA[59]	T03
DATA[51]	N04	DATA[55]	P04	DATA[60]	R04	DATA[63]	T04
V_{DDEXT}	N05	V_{DDEXT}	P05	V_{DDEXT}	R05	V_{DDEXT}	T05
V_{DDINT}	N06	V_{DDINT}	P06	V_{DDINT}	R06	V_{DDINT}	T06
GND	N07	GND	P07	GND	R07	V_{DDINT}	T07
GND	N08	GND	P08	GND	R08	V_{DDINT}	T08
GND	N09	GND	P09	GND	R09	V_{DDINT}	T09
GND	N10	GND	P10	GND	R10	V_{DDINT}	T10
GND	N11	GND	P11	GND	R11	V_{DDINT}	T11
GND	N12	GND	P12	GND	R12	V_{DDINT}	T12
GND	N13	GND	P13	GND	R13	V_{DDINT}	T13
GND	N14	GND	P14	GND	R14	V_{DDINT}	T14
V_{DDINT}	N15	V_{DDINT}	P15	GND	R15	V_{DDINT}	T15
V_{DDEXT}	N16	V_{DDEXT}	P16	V_{DDEXT}	R16	V_{DDEXT}	T16
L3DAT[5]	N17	L3DAT[2]	P17	L4DAT[5]	R17	L4DAT[3]	T17
L3DAT[6]	N18	L3DAT[1]	P18	L4DAT[6]	R18	L4ACK	T18
L3DAT[4]	N19	L3DAT[3]	P19	L4DAT[7]	R19	L4CLK	T19
L3CLK	N20	L3ACK	P20	L3DAT[0]	R20	L4DAT[4]	T20
DATA[61]	U01	ADDR[4]	V01	ADDR[5]	W01	ADDR[8]	Y01
DATA[62]	U02	ADDR[6]	V02	ADDR[9]	W02	ADDR[11]	Y02
ADDR[3]	U03	ADDR[7]	V03	ADDR[12]	W03	ADDR[13]	Y03
ADDR[2]	U04	ADDR[10]	V04	ADDR[15]	W04	ADDR[16]	Y04
V_{DDEXT}	U05	ADDR[14]	V05	ADDR[17]	W05	ADDR[19]	Y05
V_{DDEXT}	U06	ADDR[18]	V06	ADDR[20]	W06	ADDR[21]	Y06

ORDERING GUIDE

Model	Notes	Temperature Range	Instruction Rate	On-Chip SRAM	Package Description	Package Option
ADSP-21160MKBZ-80	[1]	0°C to +85°C	80 MHz	4M bits	400-Ball Plastic Ball Grid Array (PBGA)	B-400
ADSP-21160MKB-80		0°C to +85°C	80 MHz	4M bits	400-Ball Plastic Ball Grid Array (PBGA)	B-400
ADSP-21160NCBZ-100	[1]	–40°C to +100°C	100 MHz	4M bits	400-Ball Plastic Ball Grid Array (PBGA)	B-400
ADSP-21160NCB-100		–40°C to +100°C	100 MHz	4M bits	400-Ball Plastic Ball Grid Array (PBGA)	B-400
ADSP-21160NKBZ-100	[1]	0°C to +85°C	100 MHz	4M bits	400-Ball Plastic Ball Grid Array (PBGA)	B-400

[1] Z = RoHS Compliant Part.