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Details

Product Status	Obsolete
Core Processor	AVR
Core Size	8-Bit
Speed	4MHz
Connectivity	SPI, UART/USART
Peripherals	PWM, WDT
Number of I/O	32
Program Memory Size	4KB (2K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.6x16.6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at90s4414-4jc

Port B (PB7..PB0)

Port B is an 8-bit bidirectional I/O port with internal pull-up resistors. The Port B output buffers can sink 20 mA. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not active.

Port B also serves the functions of various special features of the AT90S4414/8515 as listed on page 58.

Port C (PC7..PC0)

Port C is an 8-bit bidirectional I/O port with internal pull-up resistors. The Port C output buffers can sink 20 mA. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not active.

Port C also serves as Address output when using external SRAM.

Port D (PD7..PD0)

Port D is an 8-bit bidirectional I/O port with internal pull-up resistors. The Port D output buffers can sink 20 mA. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not active.

Port D also serves the functions of various special features of the AT90S4414/8515 as listed on page 64.

RESET

Reset input. A low level on this pin for more than 50 ns will generate a reset, even if the clock is not running. Shorter pulses are not guaranteed to generate a reset.

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2

Output from the inverting oscillator amplifier

ICP

ICP is the input pin for the Timer/Counter1 Input Capture function.

OC1B

OC1B is the output pin for the Timer/Counter1 Output CompareB function

ALE

ALE is the Address Latch Enable used when the External Memory is enabled. The ALE strobe is used to latch the low-order address (8 bits) into an address latch during the first access cycle, and the AD0-7 pins are used for data during the second access cycle.

Crystal Oscillator

XTAL1 and XTAL2 are input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 2. Either a quartz crystal or a ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven as shown in Figure 3.

I/O Memory

The I/O space definition of the AT90S4414/8515 is shown in the following table:

Table 2. AT90S4414/8515 I/O Space

Address Hex	Name	Function
\$3F (\$5F)	SREG	Status Register
\$3E (\$5E)	SPH	Stack Pointer High
\$3D (\$5D)	SPL	Stack Pointer Low
\$3B (\$5B)	GIMSK	General Interrupt Mask register
\$3A (\$5A)	GIFR	General Interrupt Flag Register
\$39 (\$59)	TIMSK	Timer/Counter Interrupt Mask register
\$38 (\$58)	TIFR	Timer/Counter Interrupt Flag register
\$35 (\$55)	MCUCR	MCU general Control Register
\$33 (\$53)	TCCR0	Timer/Counter0 Control Register
\$32 (\$52)	TCNT0	Timer/Counter0 (8-bit)
\$2F (\$4F)	TCCR1A	Timer/Counter1 Control Register A
\$2E (\$4E)	TCCR1B	Timer/Counter1 Control Register B
\$2D (\$4D)	TCNT1H	Timer/Counter1 High Byte
\$2C (\$4C)	TCNT1L	Timer/Counter1 Low Byte
\$2B (\$4B)	OCR1AH	Timer/Counter1 Output Compare Register A High Byte
\$2A (\$4A)	OCR1AL	Timer/Counter1 Output Compare Register A Low Byte
\$29 (\$49)	OCR1BH	Timer/Counter1 Output Compare Register B High Byte
\$28 (\$48)	OCR1BL	Timer/Counter1 Output Compare Register B Low Byte
\$25 (\$45)	ICR1H	T/C 1 Input Capture Register High Byte
\$24 (\$44)	ICR1L	T/C 1 Input Capture Register Low Byte
\$21 (\$41)	WDTCR	Watchdog Timer Control Register
\$1F (\$3E)	EEARH	EEPROM Address Register High Byte (AT90S8515)
\$1E (\$3E)	EEARL	EEPROM Address Register Low Byte
\$1D (\$3D)	EEDR	EEPROM Data Register
\$1C (\$3C)	EEDR	EEPROM Control Register
\$1B (\$3B)	PORTA	Data Register, Port A
\$1A (\$3A)	DDRA	Data Direction Register, Port A
\$19 (\$39)	PINA	Input Pins, Port A
\$18 (\$38)	PORTB	Data Register, Port B
\$17 (\$37)	DDRB	Data Direction Register, Port B
\$16 (\$36)	PINB	Input Pins, Port B
\$15 (\$35)	PORTC	Data Register, Port C
\$14 (\$34)	DDRC	Data Direction Register, Port C
\$13 (\$33)	PINC	Input Pins, Port C

Table 3. Reset and Interrupt Vectors

Vector No.	Program Address	Source	Interrupt Definition
1	\$000	RESET	External Reset, Power-on Reset and Watchdog Reset
2	\$001	INT0	External Interrupt Request 0
3	\$002	INT1	External Interrupt Request 1
4	\$003	TIMER1 CAPT	Timer/Counter1 Capture Event
5	\$004	TIMER1 COMPA	Timer/Counter1 Compare Match A
6	\$005	TIMER1 COMPB	Timer/Counter1 Compare Match B
7	\$006	TIMER1 OVF	Timer/Counter1 Overflow
8	\$007	TIMER0, OVF	Timer/Counter0 Overflow
9	\$008	SPI, STC	Serial Transfer Complete
10	\$009	UART, RX	UART, Rx Complete
11	\$00A	UART, UDRE	UART Data Register Empty
12	\$00B	UART, TX	UART, Tx Complete
13	\$00C	ANA_COMP	Analog Comparator

The most typical and general program setup for the Reset and Interrupt Vector Addresses are:

Address	Labels	Code	Comments
\$000		rjmp RESET	; Reset Handler
\$001		rjmp EXT_INT0	; IRQ0 Handler
\$002		rjmp EXT_INT1	; IRQ1 Handler
\$003		rjmp TIM1_CAPT	; Timer1 Capture Handler
\$004		rjmp TIM1_COMPA	; Timer1 CompareA Handler
\$005		rjmp TIM1_COMPB	; Timer1 CompareB Handler
\$006		rjmp TIM1_OVF	; Timer1 Overflow Handler
\$007		rjmp TIM0_OVF	; Timer0 Overflow Handler
\$008		rjmp SPI_STC	; SPI Transfer Complete Handler
\$009		rjmp UART_RXC	; UART RX Complete Handler
\$00a		rjmp UART_DRE	; UDR Empty Handler
\$00b		rjmp UART_TXC	; UART TX Complete Handler
\$00c		rjmp ANA_COMP	; Analog Comparator Handler
;			
\$00d	MAIN:	ldi r16,high(RAMEND);	Main program start
\$00e		out SPH,r16	
\$00f		ldi r16,low(RAMEND)	
\$010		out SPL,r16	
\$011		<instr> xxx	
...

Reset Sources

The AT90S4414/8515 has three sources of reset:

- Power-On Reset. The MCU is reset when the supply voltage is below the power-on reset threshold (V_{POT}).
- External Reset. The MCU is reset when a low level is present on the \overline{RESET} pin for more than 50 ns.
- Watchdog Reset. The MCU is reset when the Watchdog timer period expires and the Watchdog is enabled.

During reset, all I/O registers are then set to their initial values, and the program starts execution from address \$000. The instruction placed in address \$000 must be an RJMP - relative jump - instruction to the reset handling routine. If the program never enables an interrupt source, the interrupt vectors are not used, and regular program code can be placed at these locations. The circuit diagram in Figure 23 shows the reset logic. Table 4 defines the timing and electrical parameters of the reset circuitry.

Figure 23. Reset Logic

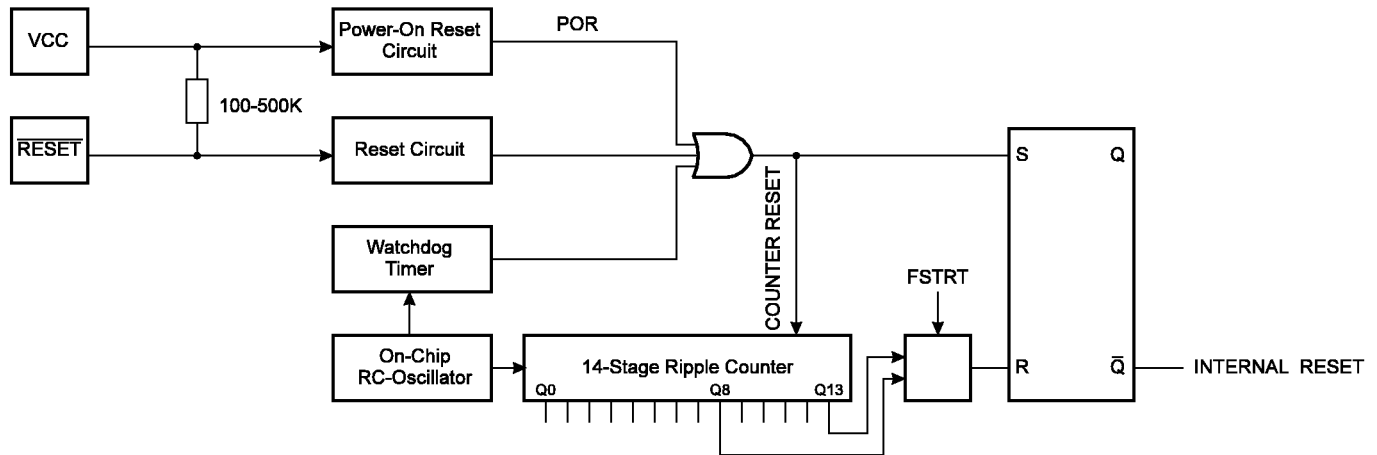


Table 4. Reset Characteristics

Symbol	Parameter	Min	Typ	Max	Units
$V_{POT}^{(1)}$	Power-on Reset Threshold Voltage (rising)	0.8	1.2	1.6	V
	Power-on Reset Threshold Voltage (falling)	0.2	0.4	0.6	V
V_{RST}	\overline{RESET} Pin Threshold Voltage	-	-	$0.9 V_{CC}$	V
t_{TOUT}	Reset Delay Time-out Period FSTRT Unprogrammed	11	16	21	ms
t_{TOUT}	Reset Delay Time-out Period FSTRT Programmed	1.0	1.1	1.2	ms

Notes: 1. The Power-on Reset will not work unless the supply voltage has been below V_{POT} (falling).

The user can select the start-up time according to typical oscillator start-up. The number of WDT oscillator cycles used for each time-out is shown in Table 5. The frequency of the watchdog oscillator is voltage dependent as shown in "Typical Characteristics" on page 86.

Table 5. Number of Watchdog Oscillator Cycles

FSTRT	Time-out at $V_{CC} = 5V$	Number of WDT cycles
Programmed	1.1 ms	1K
Unprogrammed	16.0 ms	16K

Table 7. Interrupt 0 Sense Control

ISC01	ISC00	Description
0	0	The low level of INT0 generates an interrupt request.
0	1	Reserved
1	0	The falling edge of INT0 generates an interrupt request.
1	1	The rising edge of INT0 generates an interrupt request.

Note: When changing the ISC01/ISC00 bits, INT0 must be disabled by clearing its Interrupt Enable bit in the GIMSK Register. Otherwise an interrupt can occur when the bits are changed.

The value on the INTn pin is sampled before detecting edges. If edge interrupt is selected, pulses with a duration longer than one CPU clock period will generate an interrupt. Shorter pulses are not guaranteed to generate an interrupt. If low level interrupt is selected, the low level must be held until the completion of the currently executing instruction to generate an interrupt. If enabled, a level triggered interrupt will generate an interrupt request as long as the pin is held low.

Sleep Modes

To enter the sleep modes, the SE bit in MCUCR must be set (one) and a SLEEP instruction must be executed. If an enabled interrupt occurs while the MCU is in a sleep mode, the MCU awakes, executes the interrupt routine, and resumes execution from the instruction following SLEEP. The contents of the register file, SRAM and I/O memory are unaltered. If a reset occurs during sleep mode, the MCU wakes up and executes from the Reset vector.

Idle Mode

When the SM bit is cleared (zero), the SLEEP instruction forces the MCU into the Idle Mode stopping the CPU but allowing Timer/Counters, Watchdog and the interrupt system to continue operating. This enables the MCU to wake up from external triggered interrupts as well as internal ones like Timer Overflow interrupt and watchdog reset. If wakeup from the Analog Comparator interrupt is not required, the analog comparator can be powered down by setting the ACD-bit in the Analog Comparator Control and Status register - ACSR. This will reduce power consumption in Idle Mode. When the MCU wakes up from Idle mode, the CPU starts program execution immediately.

Power Down Mode

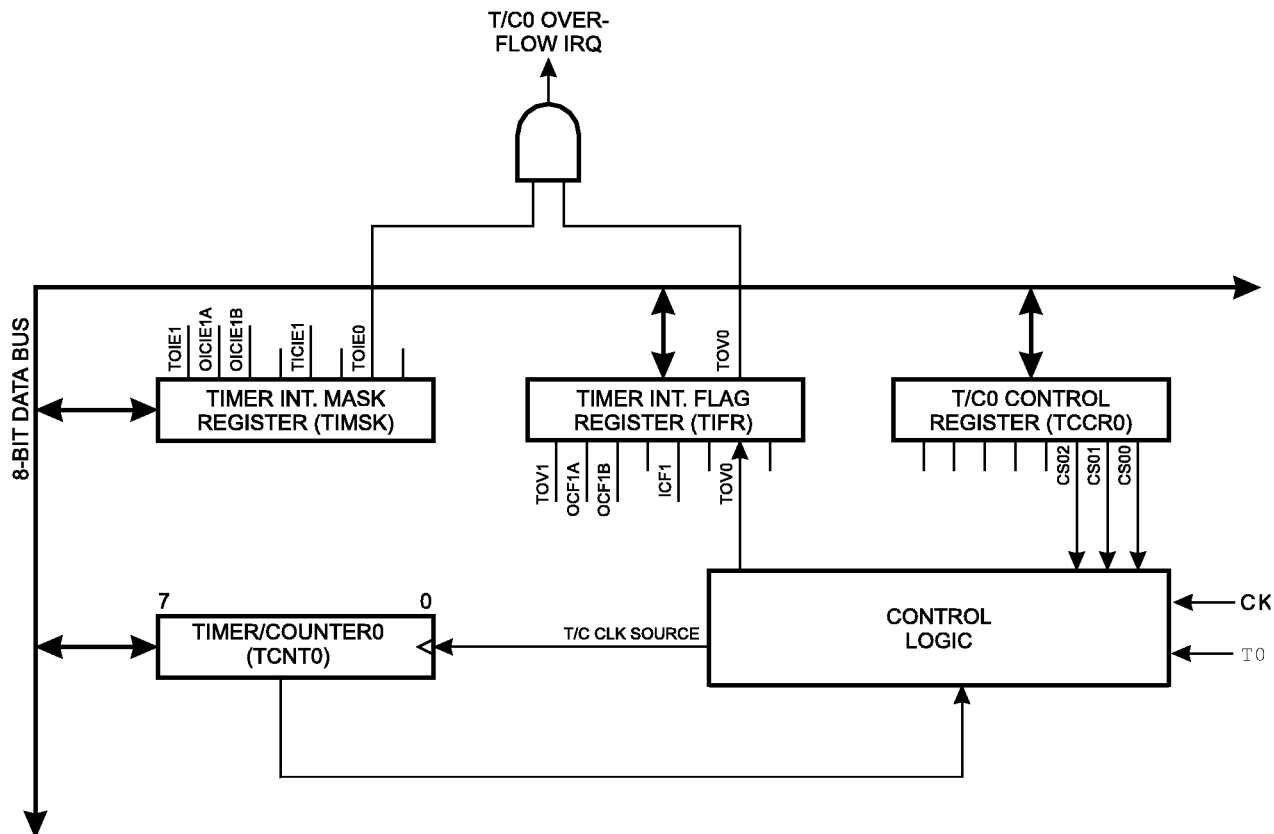
When the SM bit is set (one), the SLEEP instruction forces the MCU into the Power Down Mode. In this mode, the external oscillator is stopped, while the external interrupts and the Watchdog (if enabled) continue operating. Only an external reset, a watchdog reset (if enabled), an external level interrupt on INT0 or INT1, can wake up the MCU.

Note that when a level triggered interrupt is used for wake-up from power down, the low level must be held for a time longer than the reset delay time-out period t_{TOUT} . Otherwise, the MCU will fail to wake up.

Timer/Counters

The AT90S4414/8515 provides two general purpose Timer/Counters - one 8-bit T/C and one 16-bit T/C. The Timer/Counters have individual prescaling selection from the same 10-bit prescaling timer. Both Timer/Counters can either be used as a timer with an internal clock timebase or as a counter with an external pin connection which triggers the counting.

Figure 29. Timer/Counter0 Block Diagram



Timer/Counter0 Control Register - TCCR0

Bit	7	6	5	4	3	2	1	0	
\$33 (\$53)	-	-	-	-	-	CS02	CS01	CS00	TCCR0
Read/Write	R	R	R	R	R	R/W	R/W	R/W	
Initial value	0	0	0	0	0	0	0	0	

- **Bits 7..3 - Res: Reserved bits**

These bits are reserved bits in the AT90S4414/8515 and always read as zero.

- **Bits 2,1,0 - CS02, CS01, CS00: Clock Select0, bit 2,1 and 0**

The Clock Select0 bits 2,1 and 0 define the prescaling source of Timer/Counter0.

Table 8. Clock 0 Prescale Select

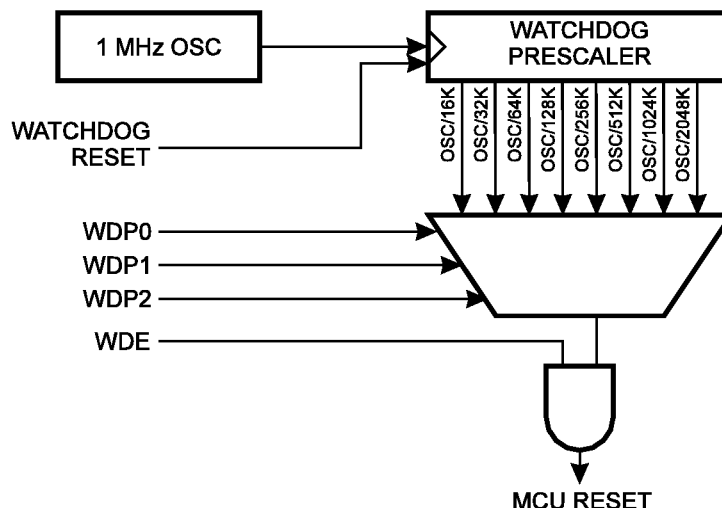
CS02	CS01	CS00	Description
0	0	0	Stop, the Timer/Counter0 is stopped.
0	0	1	CK
0	1	0	CK/8
0	1	1	CK/64
1	0	0	CK/256
1	0	1	CK/1024
1	1	0	External Pin T0, falling edge
1	1	1	External Pin T0, rising edge

Watchdog Timer

The Watchdog Timer is clocked from a separate on-chip oscillator which runs at 1MHz. This is the typical value at $V_{CC} = 5V$. See characterization data for typical values at other V_{CC} levels. By controlling the Watchdog Timer prescaler, the Watchdog reset interval can be adjusted, see Table 15 for a detailed description. The WDR - Watchdog Reset - instruction resets the Watchdog Timer. Eight different clock cycle periods can be selected to determine the reset period. If the reset period expires without another Watchdog reset, the AT90S4414/8515 resets and executes from the reset vector. For timing details on the Watchdog reset, refer to page 23.

To prevent unintentional disabling of the watchdog, a special turn-off sequence must be followed when the watchdog is disabled. Refer to the description of the Watchdog Timer Control Register for details.

Figure 33. Watchdog Timer



Watchdog Timer Control Register - WDTCR

Bit	7	6	5	4	3	2	1	0	
\$21 (\$41)	-	-	-	WDTOE	WDE	WDP2	WDP1	WDP0	WDTCR
Read/Write	R	R	R	R/W	R/W	R/W	R/W	R/W	
Initial value	0	0	0	0	0	0	0	0	

- Bits 7..5 - Res: Reserved bits**

These bits are reserved bits in the AT90S4414/8515 and will always read as zero.

- Bit 4 - WDTOE: Watch Dog Turn-Off Enable**

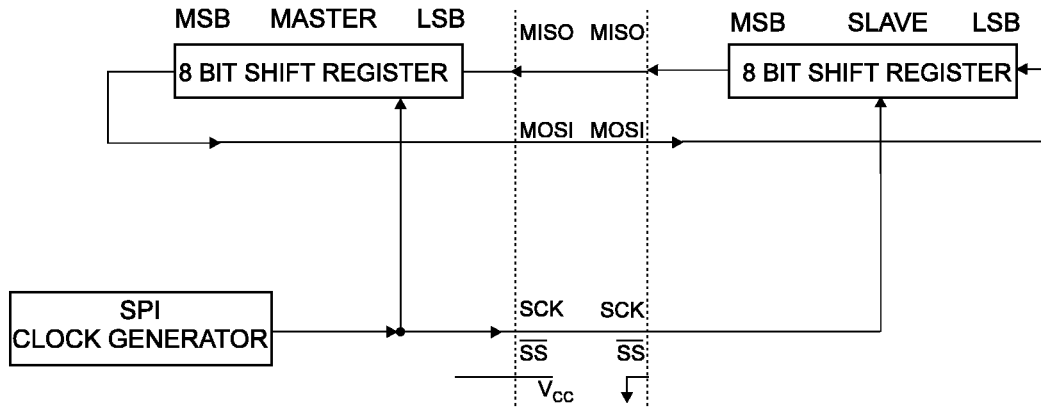
This bit must be set (one) when the WDE bit is cleared. Otherwise, the watchdog will not be disabled. Once set, hardware will clear this bit to zero after four clock cycles. Refer to the description of the WDE bit for a watchdog disable procedure.

- Bit 3 - WDE: Watch Dog Enable**

When the WDE is set (one) the Watchdog Timer is enabled, and if the WDE is cleared (zero) the Watchdog Timer function is disabled. WDE can only be cleared if the WDTOE bit is set(one). To disable an enabled watchdog timer, the following procedure must be followed:

1. In the same operation, write a logical one to WDTOE and WDE. A logical one must be written to WDE even though it is set to one before the disable operation starts.
2. Within the next four clock cycles, write a logical 0 to WDE. This disables the watchdog.

Figure 35. SPI Master-slave Interconnection



The system is single buffered in the transmit direction and double buffered in the receive direction. This means that bytes to be transmitted cannot be written to the SPI Data Register before the entire shift cycle is completed. When receiving data, however, a received byte must be read from the SPI Data Register before the next byte has been completely shifted in. Otherwise, the first byte is lost.

When the SPI is enabled, the data direction of the MOSI, MISO, SCK and \overline{SS} pins is overridden according to the following table:

Table 16. SPI Pin Overrides

Pin	Direction, Master SPI	Direction, Slave SPI
MOSI	User Defined	Input
MISO	Input	User Defined
SCK	User Defined	Input
\overline{SS}	User Defined	Input

Note: See "Alternate Functions of PortB" on page 58 for a detailed description of how to define the direction of the user defined SPI pins.

\overline{SS} Pin Functionality

When the SPI is configured as a master (MSTR in SPCR is set), the user can determine the direction of the \overline{SS} pin. If \overline{SS} is configured as an output, the pin is a general output pin which does not affect the SPI system. If \overline{SS} is configured as an input, it must be held high to ensure Master SPI operation. If the \overline{SS} pin is driven low by peripheral circuitry when the SPI is configured as master with the \overline{SS} pin defined as an input, the SPI system interprets this as another master selecting the SPI as a slave and starting to send data to it. To avoid bus contention, the SPI system takes the following actions:

1. The MSTR bit in SPCR is cleared and the SPI system becomes a slave. As a result of the SPI becoming a slave, the MOSI and SCK pins become inputs.
2. The SPIF flag in SPSR is set, and if the SPI interrupt is enabled and the I-bit in SREG are set, the interrupt routine will be executed.

Thus, when interrupt-driven SPI transmittal is used in master mode, and there exists a possibility that \overline{SS} is driven low, the interrupt should always check that the MSTR bit is still set. Once the MSTR bit has been cleared by a slave select, it must be set by the user to re-enable SPI master mode.

When the SPI is configured as a slave, the \overline{SS} pin is always input. When \overline{SS} is held low, the SPI is activated and MISO becomes an output if configured so by the user. All other pins are inputs. When \overline{SS} is driven high, all pins are inputs, and the SPI is passive, which means that it will not receive incoming data. Note that the SPI logic will be reset once the \overline{SS} pin is brought high. If the \overline{SS} pin is brought high during a transmission, the SPI will stop sending and receiving immediately and both data received and data sent must be considered as lost.

Data transmission is initiated by writing the data to be transmitted to the UART I/O Data Register, UDR. Data is transferred from UDR to the Transmit shift register when:

- A new character has been written to UDR after the stop bit from the previous character has been shifted out. The shift register is loaded immediately.
- A new character has been written to UDR before the stop bit from the previous character has been shifted out. The shift register is loaded when the stop bit of the character currently being transmitted has been shifted out.

If the 10(11)-bit Transmitter shift register is empty, data is transferred from UDR to the shift register. At this time the UDRE (UART Data Register Empty) bit in the UART Status Register, USR, is set. When this bit is set (one), the UART is ready to receive the next character. At the same time as the data is transferred from UDR to the 10(11)-bit shift register, bit 0 of the shift register is cleared (start bit) and bit 9 or 10 is set (stop bit). If 9 bit data word is selected (the CHR9 bit in the UART Control Register, UCR is set), the TXB8 bit in UCR is transferred to bit 9 in the Transmit shift register.

On the Baud Rate clock following the transfer operation to the shift register, the start bit is shifted out on the TXD pin. Then follows the data, LSB first. When the stop bit has been shifted out, the shift register is loaded if any new data has been written to the UDR during the transmission. During loading, UDRE is set. If there is no new data in the UDR register to send when the stop bit is shifted out, the UDRE flag will remain set until UDR is written again. When no new data has been written, and the stop bit has been present on TXD for one bit length, the TX Complete Flag, TXC, in USR is set.

The TXEN bit in UCR enables the UART transmitter when set (one). When this bit is cleared (zero), the PD1 pin can be used for general I/O. When TXEN is set, the UART Transmitter will be connected to PD1, which is forced to be an output pin regardless of the setting of the DDD1 bit in DDRD.

Data Reception

Figure 39 shows a block diagram of the UART Receiver.

Figure 39. UART Receiver

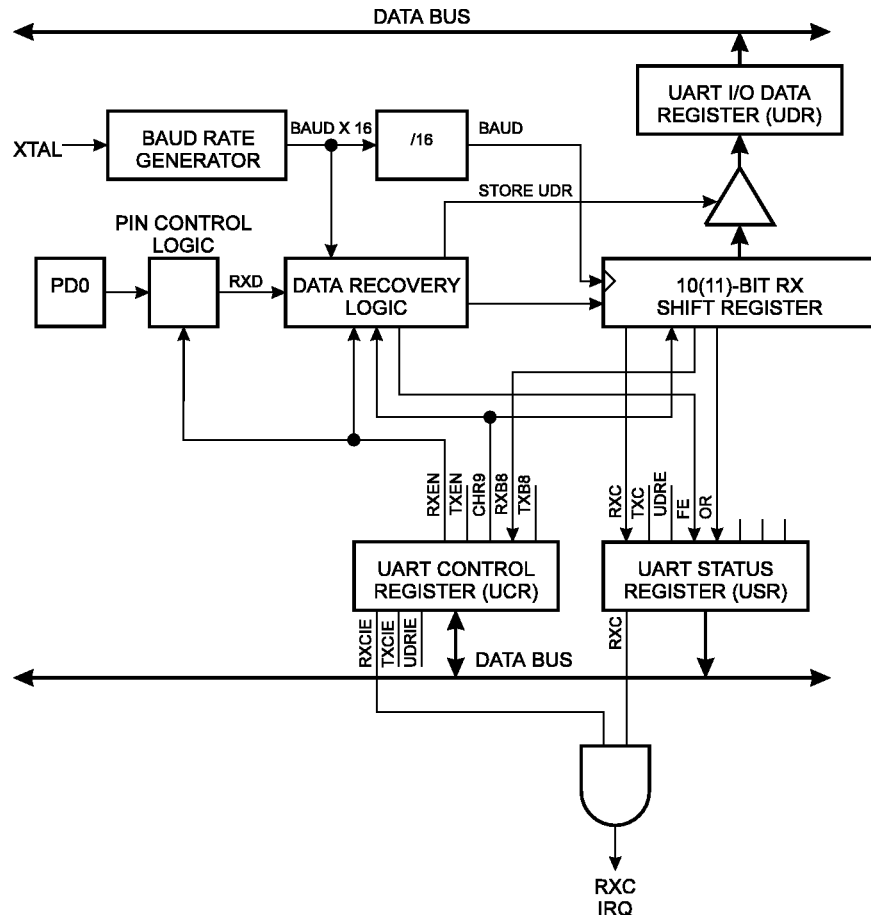


Table 18. UBRR Settings at Various Crystal Frequencies

Baud Rate	1 MHz	%Error	1.8432 MHz	%Error	2 MHz	%Error	2.4576 MHz	%Error
2400	UBRR= 25	0.2	UBRR= 47	0.0	UBRR= 51	0.2	UBRR= 63	0.0
4800	UBRR= 12	0.2	UBRR= 23	0.0	UBRR= 25	0.2	UBRR= 31	0.0
9600	UBRR= 6	7.5	UBRR= 11	0.0	UBRR= 12	0.2	UBRR= 15	0.0
14400	UBRR= 3	7.8	UBRR= 7	0.0	UBRR= 8	3.7	UBRR= 10	3.1
19200	UBRR= 2	7.8	UBRR= 5	0.0	UBRR= 6	7.5	UBRR= 7	0.0
28800	UBRR= 1	7.8	UBRR= 3	0.0	UBRR= 3	7.8	UBRR= 4	6.3
38400	UBRR= 1	22.9	UBRR= 2	0.0	UBRR= 2	7.8	UBRR= 3	0.0
57600	UBRR= 0	7.8	UBRR= 1	0.0	UBRR= 1	7.8	UBRR= 2	12.5
76800	UBRR= 0	22.9	UBRR= 1	33.3	UBRR= 1	22.9	UBRR= 1	0.0
115200	UBRR= 0	84.3	UBRR= 0	0.0	UBRR= 0	7.8	UBRR= 0	25.0

Baud Rate	3.2768 MHz	%Error	3.6864 MHz	%Error	4 MHz	%Error	4.608 MHz	%Error
2400	UBRR= 84	0.4	UBRR= 95	0.0	UBRR= 103	0.2	UBRR= 119	0.0
4800	UBRR= 42	0.8	UBRR= 47	0.0	UBRR= 51	0.2	UBRR= 59	0.0
9600	UBRR= 20	1.6	UBRR= 23	0.0	UBRR= 25	0.2	UBRR= 29	0.0
14400	UBRR= 13	1.6	UBRR= 15	0.0	UBRR= 16	2.1	UBRR= 19	0.0
19200	UBRR= 10	3.1	UBRR= 11	0.0	UBRR= 12	0.2	UBRR= 14	0.0
28800	UBRR= 6	1.6	UBRR= 7	0.0	UBRR= 8	3.7	UBRR= 9	0.0
38400	UBRR= 4	6.3	UBRR= 5	0.0	UBRR= 6	7.5	UBRR= 7	6.7
57600	UBRR= 3	12.5	UBRR= 3	0.0	UBRR= 3	7.8	UBRR= 4	0.0
76800	UBRR= 2	12.5	UBRR= 2	0.0	UBRR= 2	7.8	UBRR= 3	6.7
115200	UBRR= 1	12.5	UBRR= 1	0.0	UBRR= 1	7.8	UBRR= 2	20.0

Baud Rate	7.3728 MHz	%Error	8 MHz	%Error	9.216 MHz	%Error	11.059 MHz	%Error
2400	UBRR= 191	0.0	UBRR= 207	0.2	UBRR= 239	0.0	UBRR= 287	-
4800	UBRR= 95	0.0	UBRR= 103	0.2	UBRR= 119	0.0	UBRR= 143	0.0
9600	UBRR= 47	0.0	UBRR= 51	0.2	UBRR= 59	0.0	UBRR= 71	0.0
14400	UBRR= 31	0.0	UBRR= 34	0.8	UBRR= 39	0.0	UBRR= 47	0.0
19200	UBRR= 23	0.0	UBRR= 25	0.2	UBRR= 29	0.0	UBRR= 35	0.0
28800	UBRR= 15	0.0	UBRR= 16	2.1	UBRR= 19	0.0	UBRR= 23	0.0
38400	UBRR= 11	0.0	UBRR= 12	0.2	UBRR= 14	0.0	UBRR= 17	0.0
57600	UBRR= 7	0.0	UBRR= 8	3.7	UBRR= 9	0.0	UBRR= 11	0.0
76800	UBRR= 5	0.0	UBRR= 6	7.5	UBRR= 7	6.7	UBRR= 8	0.0
115200	UBRR= 3	0.0	UBRR= 3	7.8	UBRR= 4	0.0	UBRR= 5	0.0

UART BAUD Rate Register - UBRR

Bit	7	6	5	4	3	2	1	0	
\$09 (\$29)	MSB							LSB	UBRR
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	0	0	0	0	0	0	0	0	

The UBRR register is an 8-bit read/write register which specifies the UART Baud Rate according to the equation on the previous page.

• **Bit 2 - ACIC: Analog Comparator Input Capture Enable**

When set (one), this bit enables the Input Capture function in Timer/Counter1 to be triggered by the analog comparator. The comparator output is in this case directly connected to the Input Capture front-end logic, making the comparator utilize the noise canceler and edge select features of the Timer/Counter1 Input Capture interrupt. When cleared (zero), no connection between the analog comparator and the Input Capture function is given. To make the comparator trigger the Timer/Counter1 Input Capture interrupt, the TICIE1 bit in the Timer Interrupt Mask Register (TIMSK) must be set (one).

• **Bits 1,0 - ACIS1, ACIS0: Analog Comparator Interrupt Mode Select**

These bits determine which comparator events that trigger the Analog Comparator interrupt. The different settings are shown in Table 19.

Table 19. ACIS1/ACIS0 Settings

ACIS1	ACIS0	Interrupt Mode
0	0	Comparator Interrupt on Output Toggle
0	1	Reserved
1	0	Comparator Interrupt on Falling Output Edge
1	1	Comparator Interrupt on Rising Output Edge

Note: When changing the ACIS1/ACIS0 bits, The Analog Comparator Interrupt must be disabled by clearing its Interrupt Enable bit in the ACSR register. Otherwise an interrupt can occur when the bits are changed.

Interface to External SRAM

The interface to the SRAM consists of:

- Port A: Multiplexed low-order address bus and data bus
- Port C: High-order address bus
- The ALE-pin: Address latch enable
- The \overline{RD} and \overline{WR} -pin: Read and write strobes.

The external data SRAM is enabled by setting the SRE - External SRAM enable bit of the MCUCR - MCU control register, and will override the setting of the data direction register DDRA. When the SRE bit is cleared (zero), the external data SRAM is disabled, and the normal pin and data direction settings are used. When SRE is cleared (zero), the address space above the internal SRAM boundary is not mapped into the internal SRAM, as in AVR parts not having interface to the external SRAM.

When ALE goes from high to low, there is a valid address on Port A. ALE is low during a data transfer. \overline{RD} and \overline{WR} are active when accessing the external SRAM only.

When the external SRAM is enabled, the ALE signal may have short pulses when accessing the internal RAM, but the ALE signal is stable when accessing the external SRAM.

Figure 42 sketches how to connect an external SRAM to the AVR using 8 latches which are transparent when G is high.

Default, the external SRAM access is a three-cycle scheme as depicted in Figure 43. When one extra wait state is needed in the access cycle, set the SRW bit (one) in the MCUCR register. The resulting access scheme is shown in Figure 44. In both cases, note that PORTA is data bus in one cycle only. As soon as the data access finishes, PORTA becomes a low order address bus again.

For details in the timing for the SRAM interface, please refer to Figure 68, Table 38, Table 39, Table 40, and Table 41 in section "Absolute Maximum Ratings*" on page 81.

Port B Schematics

Note that all port pins are synchronized. The synchronization latches are however, not shown in the figures.

Figure 46. Port B Schematic Diagram (Pins PB0 and PB1)

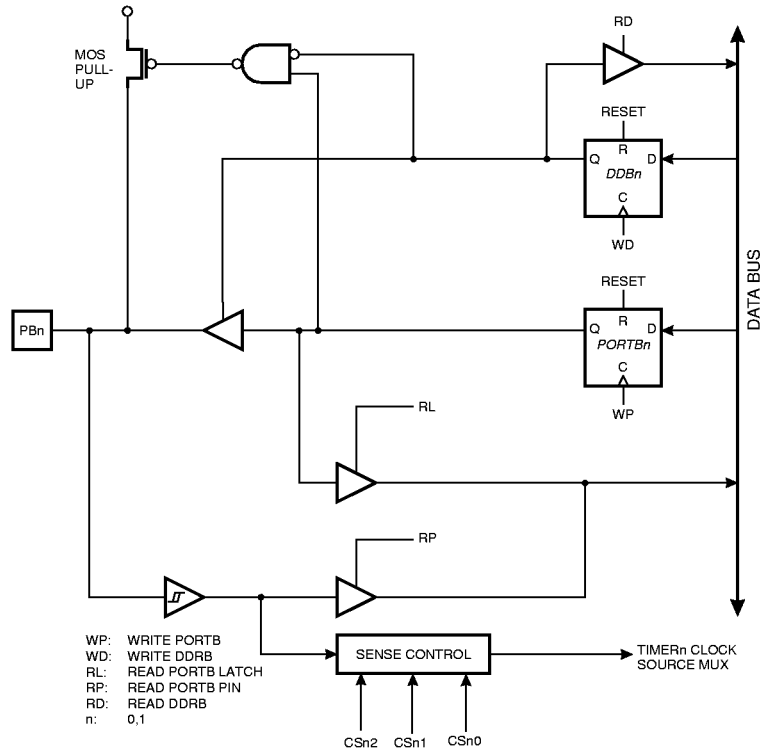
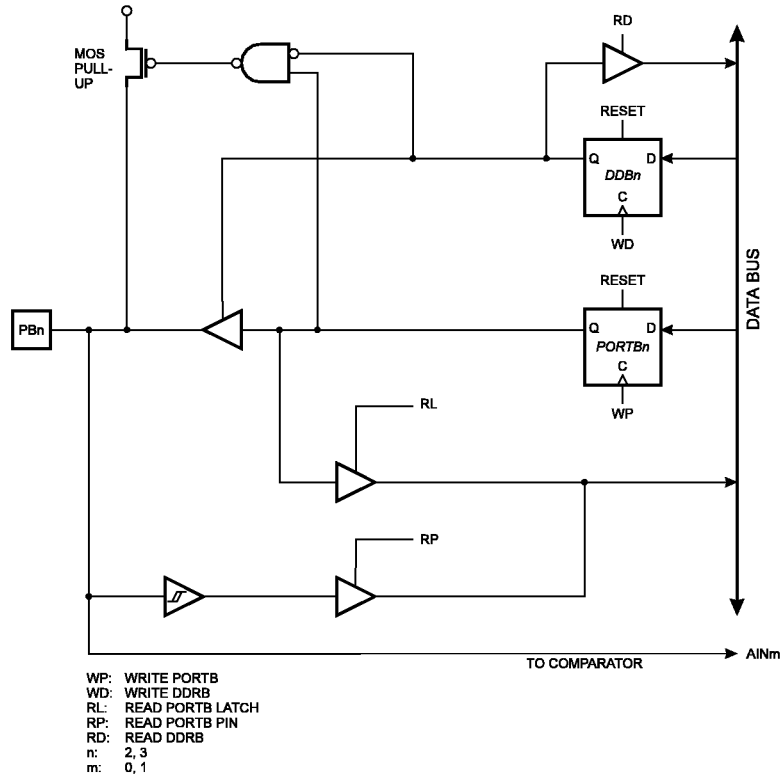


Figure 47. Port B Schematic Diagram (Pins PB2 and PB3)



Port C

Port C is an 8-bit bi-directional I/O port. Three I/O memory address locations are allocated for the Port C, one each for the Data Register - PORTC, \$15(\$35), Data Direction Register - DDRC, \$14(\$34) and the Port C Input Pins - PINC, \$13(\$33). The Port C Input Pins address is read only, while the Data Register and the Data Direction Register are read/write.

All port pins have individually selectable pull-up resistors. The Port C output buffers can sink 20mA and thus drive LED displays directly. When pins PC0 to PC7 are used as inputs and are externally pulled low, they will source current if the internal pull-up resistors are activated.

The Port C pins have alternate functions related to the optional external data SRAM. Port C can be configured to be the high-order address byte during accesses to external data memory. When Port C is set to the alternate function by the SRE - External SRAM Enable - bit in the MCUCR - MCU Control Register, the alternate settings override the data direction register.

Port C Data Register - PORTC

Bit	7	6	5	4	3	2	1	0									
\$15 (\$35)	<table><tr><td>PORTC7</td><td>PORTC6</td><td>PORTC5</td><td>PORTC4</td><td>PORTC3</td><td>PORTC2</td><td>PORTC1</td><td>PORTC0</td></tr></table>								PORTC7	PORTC6	PORTC5	PORTC4	PORTC3	PORTC2	PORTC1	PORTC0	PORTC
PORTC7	PORTC6	PORTC5	PORTC4	PORTC3	PORTC2	PORTC1	PORTC0										
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W									
Initial value	0	0	0	0	0	0	0	0									

Port C Data Direction Register - DDRC

Bit	7	6	5	4	3	2	1	0									
\$14 (\$34)	<table><tr><td>DDC7</td><td>DDC6</td><td>DDC5</td><td>DDC4</td><td>DDC3</td><td>DDC2</td><td>DDC1</td><td>DDC0</td></tr></table>								DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0	DDRC
DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0										
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W									
Initial value	0	0	0	0	0	0	0	0									

Port C Input Pins Address - PINC

Bit	7	6	5	4	3	2	1	0									
\$13 (\$33)	<table><tr><td>PINC7</td><td>PINC6</td><td>PINC5</td><td>PINC4</td><td>PINC3</td><td>PINC2</td><td>PINC1</td><td>PINC0</td></tr></table>								PINC7	PINC6	PINC5	PINC4	PINC3	PINC2	PINC1	PINC0	PINC
PINC7	PINC6	PINC5	PINC4	PINC3	PINC2	PINC1	PINC0										
Read/Write	R	R	R	R	R	R	R	R									
Initial value	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z									

The Port C Input Pins address - PINC - is not a register, and this address enables access to the physical value on each Port C pin. When reading PORTC, the Port C Data Latch is read, and when reading PINC, the logical values present on the pins are read.

PortC as General Digital I/O

All 8 pins in Port C have equal functionality when used as digital I/O pins.

PCn, General I/O pin: The DDcn bit in the DDRC register selects the direction of this pin, if DDcn is set (one), PCn is configured as an output pin. If DDcn is cleared (zero), PCn is configured as an input pin. If PORTCn is set (one) when the pin configured as an input pin, the MOS pull up resistor is activated. To switch the pull up resistor off, PORTCn has to be cleared (zero) or the pin has to be configured as an output pin. The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not active.

Table 23. DDcn Effects on Port C Pins

DDCn	PORTCn	I/O	Pull up	Comment
0	0	Input	No	Tri-state (Hi-Z)
0	1	Input	Yes	PCn will source current if ext. pulled low.
1	0	Output	No	Push-Pull Zero Output
1	1	Output	No	Push-Pull One Output

n: 7...0, pin number

Port D Data Register - PORTD

Bit	7	6	5	4	3	2	1	0	
\$12 (\$32)	PORTD7	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0	PORTD
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	0	0	0	0	0	0	0	0	

Port D Data Direction Register - DDRD

Bit	7	6	5	4	3	2	1	0	
\$11 (\$31)	DDD7	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	DDRD
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	0	0	0	0	0	0	0	0	

Port D Input Pins Address - PIND

Bit	7	6	5	4	3	2	1	0	
\$10 (\$30)	PIND7	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0	PIND
Read/Write	R	R	R	R	R	R	R	R	
Initial value	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	

The Port D Input Pins address - PIND - is not a register, and this address enables access to the physical value on each Port D pin. When reading PORTD, the Port D Data Latch is read, and when reading PIND, the logical values present on the pins are read.

PortD as General Digital I/O

PD_n, General I/O pin: The DDD_n bit in the DDRD register selects the direction of this pin. If DDD_n is set (one), PD_n is configured as an output pin. If DDD_n is cleared (zero), PD_n is configured as an input pin. If PD_n is set (one) when configured as an input pin the MOS pull up resistor is activated. To switch the pull up resistor off the PD_n has to be cleared (zero) or the pin has to be configured as an output pin. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not active.

Table 25. DDD_n Bits on Port D Pins

DDD _n	PORTD _n	I/O	Pull up	Comment
0	0	Input	No	Tri-state (Hi-Z)
0	1	Input	Yes	PD _n will source current if ext. pulled low.
1	0	Output	No	Push-pull Zero Output
1	1	Output	No	Push-pull One Output

n: 7,6...0, pin number.

Alternate Functions Of Port D

• \overline{RD} - Port D, Bit 7

\overline{RD} is the external data memory read control strobe. See "Interface to External SRAM" on page 53 for detailed information.

• \overline{WR} - Port D, Bit 6

\overline{WR} is the external data memory write control strobe. See "Interface to External SRAM" on page 53 for detailed information.

• OC1A- Port D, Bit 5

OC1A, Output compare match output: The PD5 pin can serve as an external output when the Timer/Counter1 compare matches. The PD5 pin has to be configured as an output (DDD5 set (one)) to serve this function. See the Timer/Counter1 description for further details, and how to enable the output. The OC1A pin is also the output pin for the PWM mode timer function.

Memory Programming

Program and Data Memory Lock Bits

The AT90S4414/8515 MCU provides two Lock bits which can be left unprogrammed ('1') or can be programmed ('0') to obtain the additional features listed in Table 26. The Lock Bits can only be erased with the Chip Erase command.

Table 26. Lock Bit Protection Modes

Memory Lock Bits			Protection Type
Mode	LB1	LB2	
1	1	1	No memory lock features enabled.
2	0	1	Further programming of the Flash and EEPROM is disabled. ⁽¹⁾
3	0	0	Same as mode 2, and verify is also disabled.

Note: 1. In Parallel mode, further programming of the Fuse bits are also disabled. Program the Fuse bits before programming the Lock bits.

Fuse Bits

The AT90S4414/8515 has two Fuse bits, SPIEN and FSTRT.

- When the SPIEN Fuse is programmed ('0'), Serial Program and Data Downloading is enabled. Default value is programmed ("0").
- When the FSTRT Fuse is programmed ('0'), the short start-up time is selected. Default value is unprogrammed ("1"). Parts with this bit pre-programmed ('0') can be delivered on demand.

The Fuse bits are not accessible in Serial Programming Mode. The status of the Fuse bits is not affected by Chip Erase.

Signature Bytes

All Atmel microcontrollers have a three-byte signature code which identifies the device. This code can be read in both serial and parallel mode. The three bytes reside in a separate address space.

For the AT90S8515⁽¹⁾ they are:

1. \$000: \$1E (indicates manufactured by Atmel)
2. \$001: \$93 (indicates 8KB Flash memory)
3. \$002: \$01 (indicates AT90S8515 device when signature byte \$001 is \$93)

For the AT90S4414⁽¹⁾ they are:

1. \$000: \$1E (indicates manufactured by Atmel)
2. \$001: \$92 (indicates 4KB Flash memory)
3. \$002: \$01 (indicates AT90S4414 device when signature byte \$001 is \$92)

Note: 1. When both Lock bits are programmed (Lock mode 3), the signature bytes can not be read in serial mode. Reading the signature bytes will return: \$00, \$01 and \$02.

Programming the Flash and EEPROM

Atmel's AT90S4414/8515 offers 4K/8K bytes of In-System Reprogrammable Flash Program memory and 256/512 bytes of EEPROM Data memory.

The AT90S4414/8515 is shipped with the on-chip Flash Program and EEPROM Data memory arrays in the erased state (i.e. contents = \$FF) and ready to be programmed. This device supports a High-voltage (12V) Parallel programming mode and a Low-voltage Serial programming mode. The +12V is used for programming enable only, and no current of significance is drawn by this pin. The serial programming mode provides a convenient way to download program and data into the AT90S4414/8515 inside the user's system.

Table 28. Pin Name Mapping

Signal Name in Programming Mode	Pin Name	I/O	Function
RDY/BSY	PD1	O	0: Device is busy programming, 1: Device is ready for new command
\overline{OE}	PD2	I	Output Enable (Active low)
\overline{WR}	PD3	I	Write Pulse (Active low)
BS	PD4	I	Byte Select ("0" selects low byte, "1" selects high byte)
XA0	PD5	I	XTAL Action Bit 0
XA1	PD6	I	XTAL Action Bit 1
DATA	PB7-0	I/O	Bidirectional Databus (Output when \overline{OE} is low)

Table 29. XA1 and XA0 Coding

XA1	XA0	Action when XTAL1 is Pulsed
0	0	Load Flash or EEPROM Address (High or low address byte determined by BS)
0	1	Load Data (High or Low data byte for Flash determined by BS)
1	0	Load Command
1	1	No Action, Idle

Table 30. Command Byte Bit Coding

Command Byte	Command Executed
1000 0000	Chip Erase
0100 0000	Write Fuse Bits
0010 0000	Write Lock Bits
0001 0000	Write Flash
0001 0001	Write EEPROM
0000 1000	Read Signature Bytes
0000 0100	Read Lock and Fuse Bits
0000 0010	Read Flash
0000 0011	Read EEPROM

Enter Programming Mode

The following algorithm puts the device in parallel programming mode:

1. Apply supply voltage according to Table 27, between V_{CC} and GND.
2. Set the \overline{RESET} and BS pin to "0" and wait at least 100 ns.
3. Apply 11.5 - 12.5V to \overline{RESET} . Any activity on BS within 100 ns after +12V has been applied to \overline{RESET} , will cause the device to fail entering programming mode.

DC Characteristics

$T_A = -40^{\circ}\text{C}$ to 85°C , $V_{CC} = 2.7\text{V}$ to 6.0V (unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IL}	Input Low Voltage	(Except XTAL1)	-0.5		$0.3 V_{CC}^{(1)}$	V
V_{IL1}	Input Low Voltage	(XTAL1)	-0.5		$0.2 V_{CC}^{(1)}$	V
V_{IH}	Input High Voltage	(Except XTAL1, $\overline{\text{RESET}}$)	$0.6 V_{CC}^{(2)}$		$V_{CC} + 0.5$	V
V_{IH1}	Input High Voltage	(XTAL1)	$0.8 V_{CC}^{(2)}$		$V_{CC} + 0.5$	V
V_{IH2}	Input High Voltage	($\overline{\text{RESET}}$)	$0.9 V_{CC}^{(2)}$		$V_{CC} + 0.5$	V
V_{OL}	Output Low Voltage ⁽³⁾ (Ports A,B,C,D)	$I_{OL} = 20 \text{ mA}$, $V_{CC} = 5\text{V}$			0.6	V
		$I_{OL} = 10 \text{ mA}$, $V_{CC} = 3\text{V}$			0.5	V
V_{OH}	Output High Voltage ⁽⁴⁾ (Ports A,B,C,D)	$I_{OH} = -3 \text{ mA}$, $V_{CC} = 5\text{V}$	4.2			V
		$I_{OH} = -1.5 \text{ mA}$, $V_{CC} = 3\text{V}$	2.3			V
I_{IL}	Input Leakage Current I/O pin	$V_{CC} = 6\text{V}$, pin low (absolute value)			8.0	μA
I_{IH}	Input Leakage Current I/O pin	$V_{CC} = 6\text{V}$, pin high (absolute value)			980	nA
RRST	Reset Pull-Up Resistor		100		500	k Ω
$R_{I/O}$	I/O Pin Pull-Up Resistor		35		120	k Ω
I_{CC}	Power Supply Current	Active Mode, $V_{CC} = 3\text{V}$, 4MHz			3.0	mA
		Idle Mode $V_{CC} = 3\text{V}$, 4MHz			1.2	mA
	Power Down Mode ⁽⁵⁾	WDT enabled, $V_{CC} = 3\text{V}$		9	15.0	μA
		WDT disabled, $V_{CC} = 3\text{V}$		<1	2.0	μA
V_{ACIO}	Analog Comparator Input Offset Voltage	$V_{CC} = 5\text{V}$			40	mV
I_{ACLK}	Analog Comparator Input Leakage Current	$V_{CC} = 5\text{V}$ $V_{in} = V_{CC}/2$	-50		50	nA
t_{ACPD}	Analog Comparator Propagation Delay	$V_{CC} = 2.7\text{V}$ $V_{CC} = 4.0\text{V}$		750 500		ns

- Notes:
1. "Max" means the highest value where the pin is guaranteed to be read as low.
 2. "Min" means the lowest value where the pin is guaranteed to be read as high.
 3. Although each I/O port can sink more than the test conditions (20mA at $V_{CC} = 5\text{V}$, 10mA at $V_{CC} = 3\text{V}$) under steady state conditions (non-transient), the following must be observed:
 - 1) The sum of all I_{OL} , for all ports, should not exceed 200 mA.
 - 2) The sum of all I_{OL} , for ports B0-B7, D0-D7 and XTAL2, should not exceed 100 mA.
 - 3) The sum of all I_{OL} , for ports A0-A7, ALE, OC1B and C0-C7 should not exceed 100 mA.
 If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test condition.
 4. Although each I/O port can source more than the test conditions (3mA at $V_{CC} = 5\text{V}$, 1.5mA at $V_{CC} = 3\text{V}$) under steady state conditions (non-transient), the following must be observed:
 - 1) The sum of all I_{OH} , for all ports, should not exceed 200 mA.
 - 2) The sum of all I_{OH} , for ports B0-B7, D0-D7 and XTAL2, should not exceed 100 mA.
 - 3) The sum of all I_{OH} , for ports A0-A7, ALE, OC1B and C0-C7 should not exceed 100 mA.
 If I_{OH} exceeds the test condition, V_{OH} may exceed the related specification. Pins are not guaranteed to source current greater than the listed test condition.
 5. Minimum V_{CC} for Power Down is 2V.

Figure 74. Power Down Supply Current vs. V_{CC}

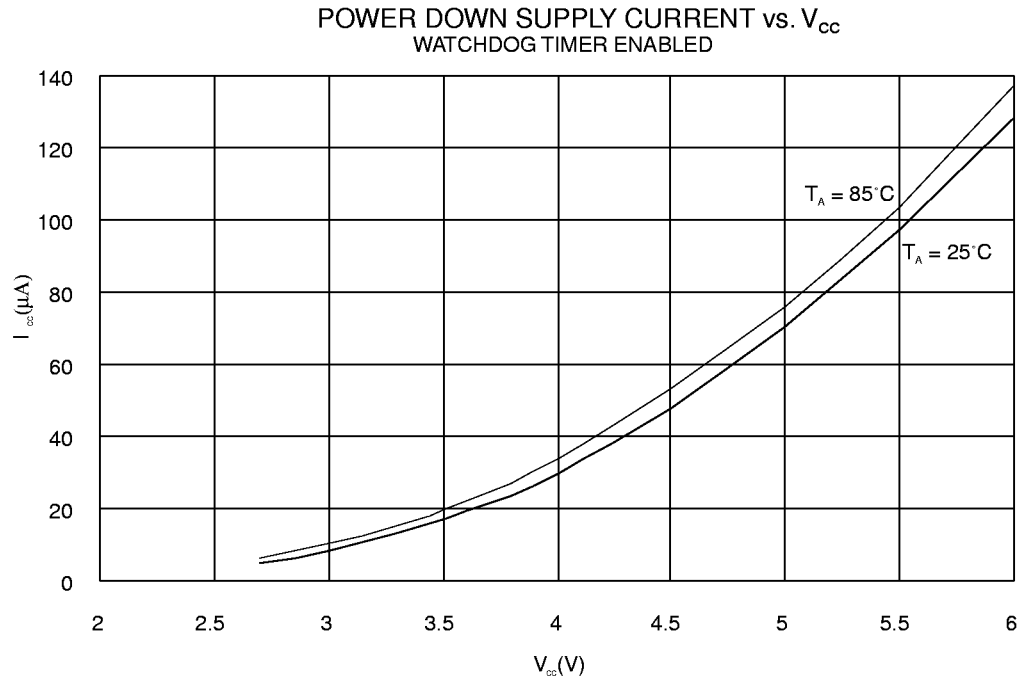


Figure 75. Analog Comparator Current vs. V_{CC}

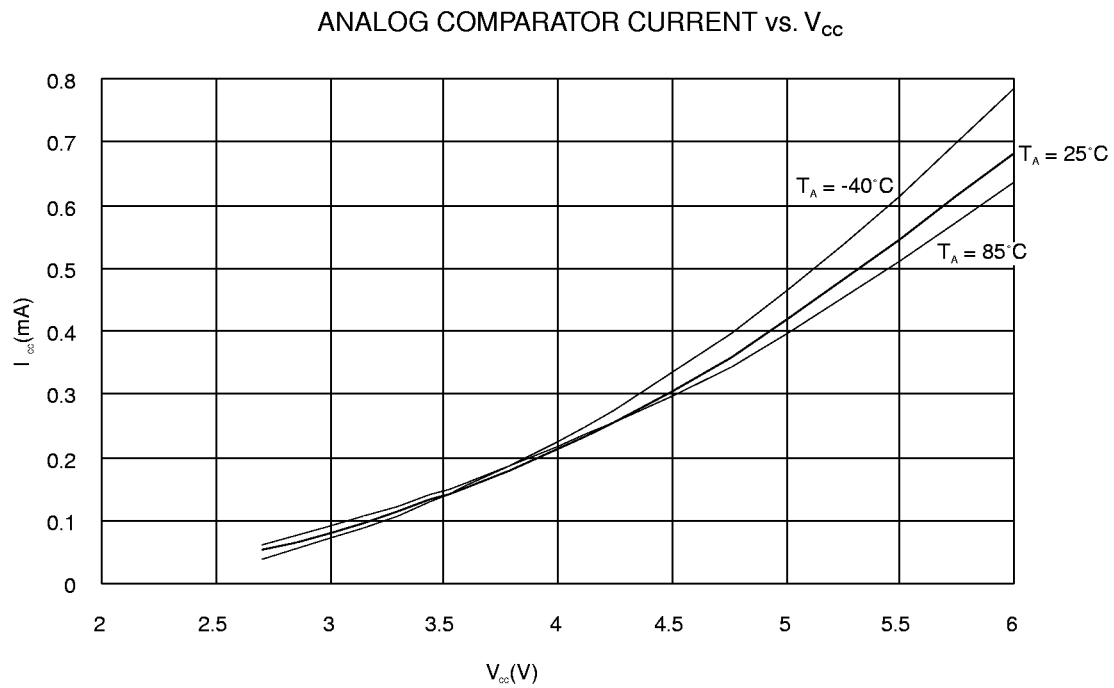


Figure 82. I/O Pin Sink Current vs. Output Voltage

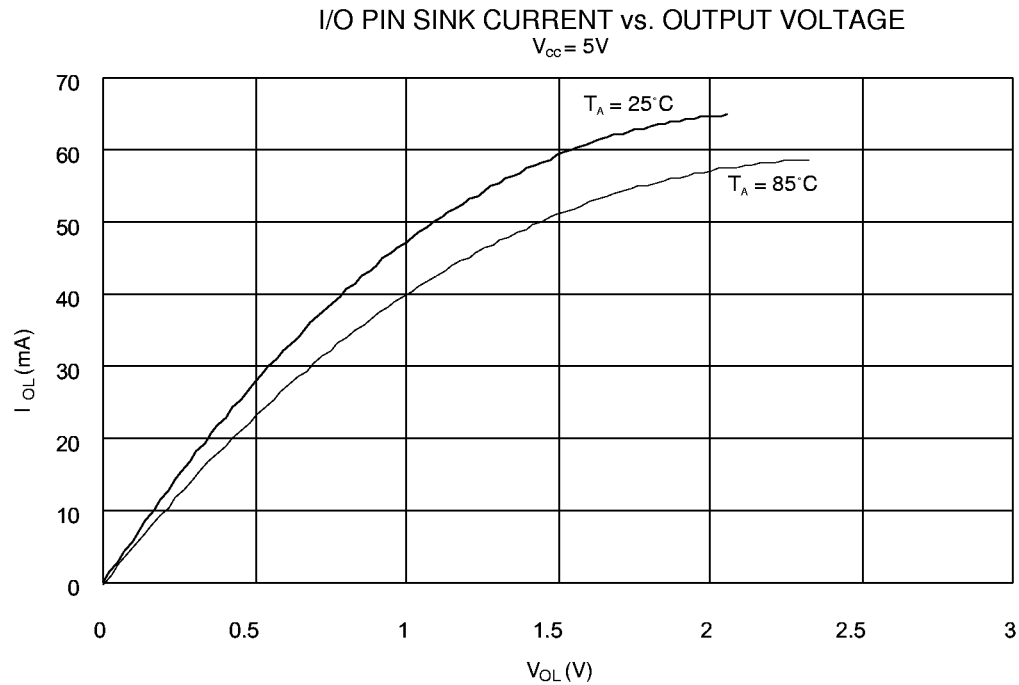
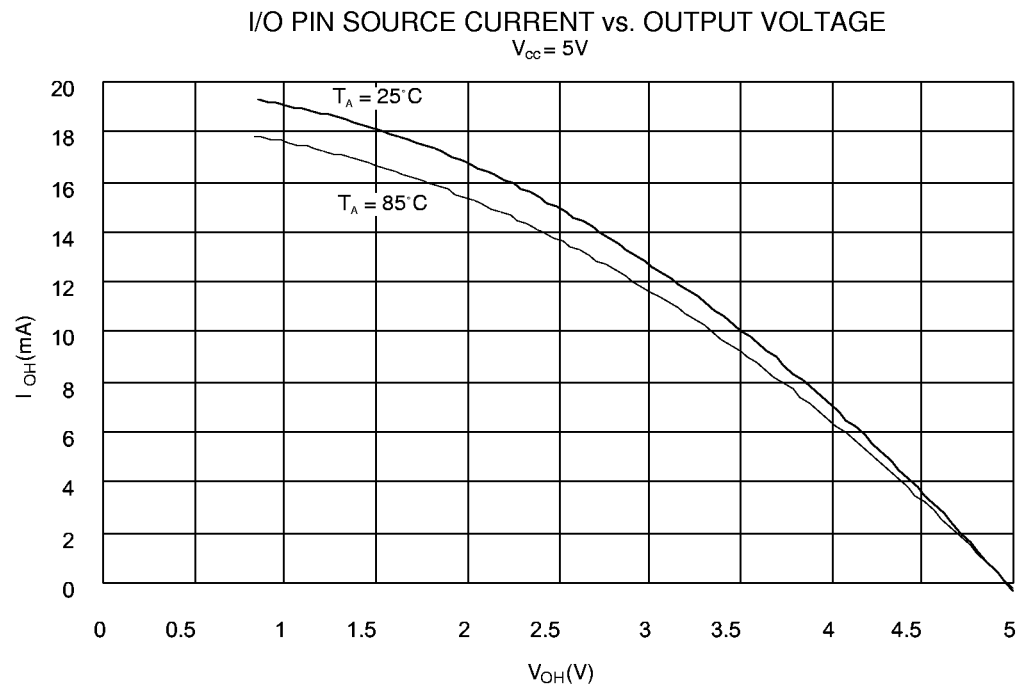
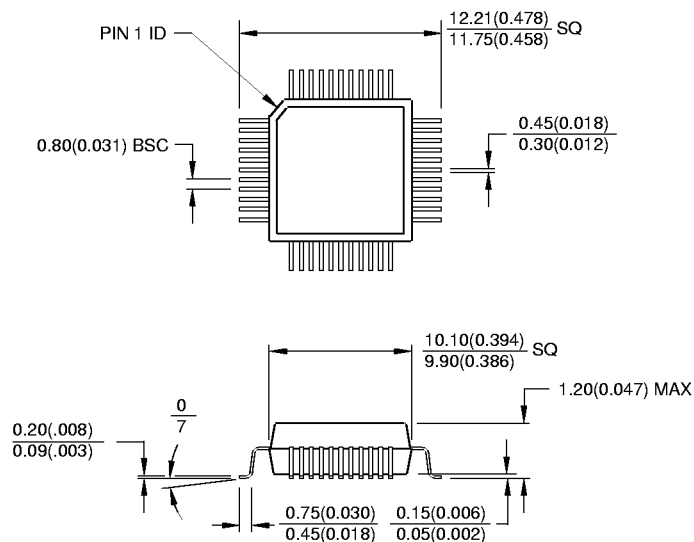


Figure 83. I/O Pin Source Current vs. Output Voltage



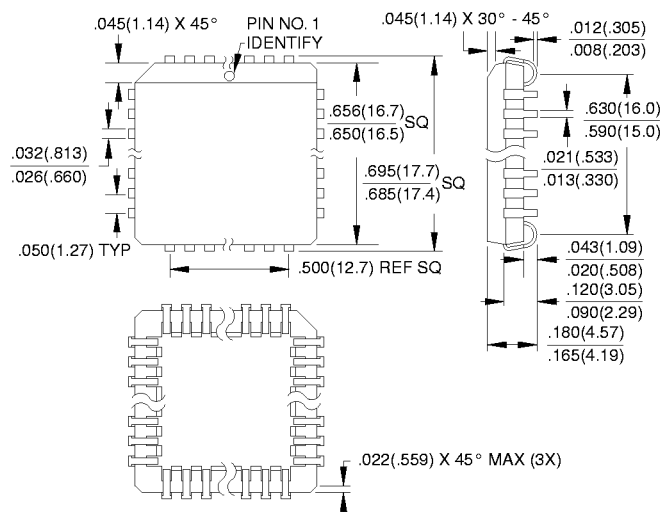
Packaging Information

44A, 44-lead, Thin (1.0 mm) Plastic Gull Wing Quad Flat Package (TQFP)
Dimensions in Millimeters and (Inches)*



*Controlling dimension: millimeters

44J, 44-lead, Plastic J-leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)



40P6, 40-lead, 0.600" Wide,
Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-011 AC

