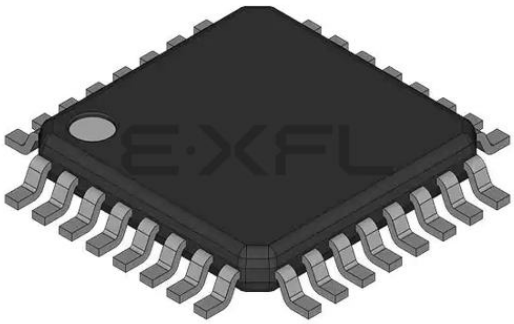


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

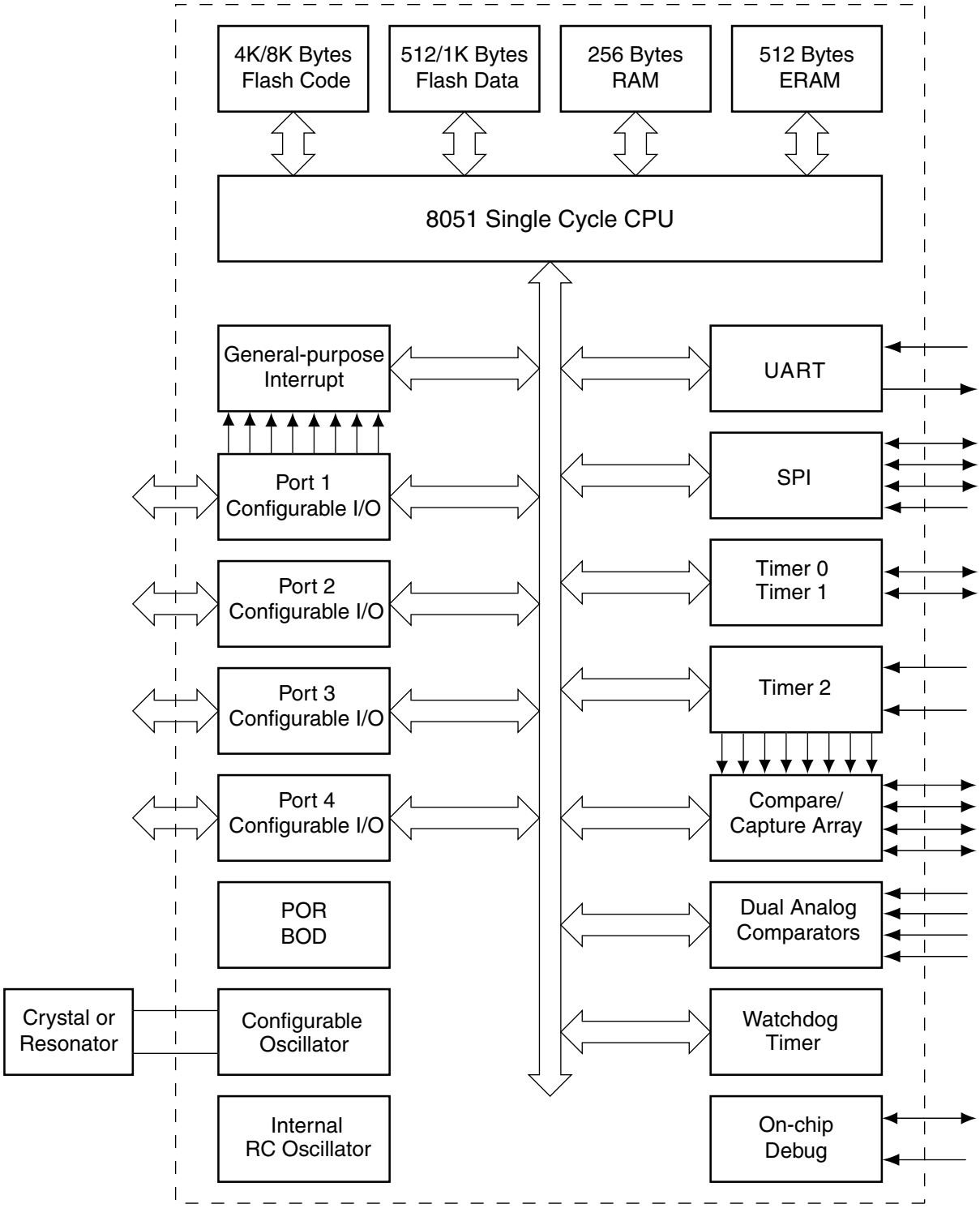
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	20MHz
Connectivity	SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	30
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-TQFP
Supplier Device Package	32-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/atmel/at89lp428-20au

2.1 Block Diagram

Figure 2-1. AT89LP428/828 Block Diagram



4. Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 4-1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect. User software should not write to these unlisted locations, since they may be used in future products to invoke new features.

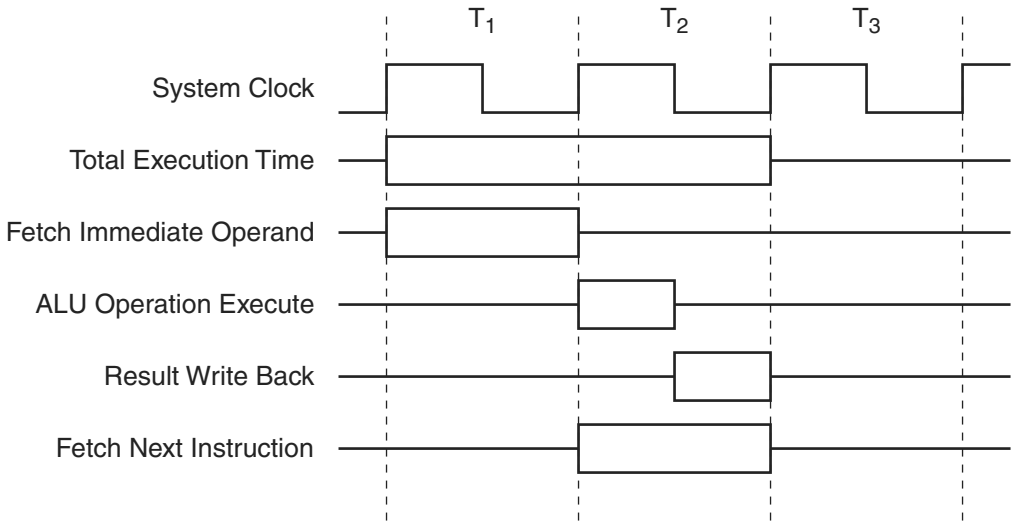
Table 4-1. AT89LP428/828 SFR Map and Reset Values

	8	9	A	B	C	D	E	F	
0F8H									0FFH
0F0H	B 0000 0000								0F7H
0E8H	SPSR 000x x000	SPCR 0000 0000	SPDR xxxx xxxx						0EFH
0E0H	ACC 0000 0000								0E7H
0D8H									0DFH
0D0H	PSW 0000 0000	T2CCA 0000 0000	T2CCL 0000 0000	T2CCH 0000 0000	T2CCC 0000 0000	T2CCF 0000 0000			0D7H
0C8H	T2CON 0000 0000	T2MOD 0000 0000	RCAP2L 0000 000	RCAP2H 0000 0000	TL2 0000 000	TH2 0000 0000			0CFH
0C0H	P4 xx11 1111		P1M0(2)	P1M1 0000 0000	P2M0(2)	P2M1 0000 0000	P3M0(2)	P3M1 0000 0000	0C7H
0B8H	IP 0000 0000	SADEN 0000 0000					P4M0(2)	P4M1 xx00 0000	0BFH
0B0H	P3 1111 1111				IE2 xxxx x000	IP2 xxxx x000	IP2H xxxx x000	IPH 0000 0000	0B7H
0A8H	IE 0000 0000	SADDR 0000 0000						AREF 0000 0000	0AFH
0A0H	P2 1111 1111		DPCF 0000 00x0				WDTRST (write-only)	WDTCON 0000 x000	0A7H
98H	SCON 0000 0000	SBUF xxxx xxxx	GPMOD 0000 0000	GPLS 0000 0000	GPIEN 0000 0000	GPIF 0000 0000		ACSRB 1100 0000	9FH
90H	P1 1111 1111	TCONB 0010 0100	RL0 0000 0000	RL1 0000 0000	RH0 0000 0000	RH1 0000 0000	MEMCON 0000 00xx	ACSRA 0000 0000	97H
88H	TCON 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000		CLKREG 0000 x000	8FH
80H		SP 0000 0111	DP0L 0000 0000	DP0H 0000 0000	DP1L 0000 0000	DP1H 0000 0000	PAGE xxxx xxx0	PCON 0000 0000	87H
	0	1	2	3	4	5	6	7	

Notes: 1. All SFRs in the left-most column are bit-addressable.

2. Reset value is 1111 1111B when Tristate-port Fuse is enabled and 0000 0000B when disabled.

Figure 5-3. Two-cycle ALU Operation (Example: ADD A, #data)



5.1 Enhanced Dual Data Pointers

The AT89LP428/828 provides two 16-bit data pointers: DPTR0 formed by the register pair DPOL and DPOH (82H an 83H), and DPTR1 formed by the register pair DP1L and DP1H (84H and 85H). The data pointers are used by several instructions to access the program or data memories. The Data Pointer Configuration Register (DPCF) controls operation of the dual data pointers (Table 5-4). The DPS bit in DPCF selects which data pointer is currently referenced by instructions including the DPTR operand. Each data pointer may be accessed at its respective SFR addresses regardless of the DPS value. The AT89LP428/828 provides two methods for fast context switching of the data pointers:

- Bit 2 of DPCF is hard-wired as a logic 0. The DPS bit may be toggled (to switch data pointers) simply by incrementing the DPCF register, without altering other bits in the register unintentionally. This is the preferred method when only a single data pointer will be used at one time.

```
EX:    INC  DPCF   ; Toggle DPS
```

- In some cases, both data pointers must be used simultaneously. To prevent frequent toggling of DPS, the AT89LP428/828 supports a prefix notation for selecting the opposite data pointer per instruction. All DPTR instructions, with the exception of JMP @A+DPTR, when prefixed with an 0A5H opcode will use the inverse value of DPS ($\overline{DPS}$) to select the data pointer. Some assemblers may support this operation by using the /DPTR operand. For example, the following code performs a block copy within EDATA:

```
       MOV  DPCF, #00H     ; DPS = 0
       MOV  DPTR, #SRC     ; load source address to dptr0
       MOV  /DPTR, #DST    ; load destination address to dptr1
       MOV  R7, #BLKSIZE   ; number of bytes to copy
COPY:  MOVX A, @DPTR       ; read source (dptr0)
       INC  DPTR           ; next src (dptr0+1)
       MOVX @/DPTR, A      ; write destination (dptr1)
       INC  /DPTR          ; next dst (dptr1+1)
       DJNZ R7, COPY
```

Table 6-2. CLKREG – Clock Control Register

CLKREG = 8FH — Reset Value = 0000 0000B

Not Bit Addressable

	TPS3	TPS2	TPS1	TPS0	CDV2	CDV1	CDV0	COE
Bit	7	6	5	4	3	2	1	0

Symbol	Function
TPS [3 - 0]	Timer Prescaler. The Timer Prescaler selects the time base for Timer 0, Timer 1, Timer 2 and the Watchdog Timer. The prescaler is implemented as a 4-bit binary down counter. When the counter reaches zero it is reloaded with the value stored in the TPS bits to give a division ratio between 1 and 16. By default the timers will count every clock cycle (TPS = 0000B). To configure the timers to count at a standard 8051 rate of once every 12 clock cycles, TPS should be set to 1011B.
CDV [2 - 0]	System Clock Division. Determines the frequency of the system clock relative to the oscillator clock source. **CDIV2 CDIV1 CDIV0 System Clock Frequency** 0 0 0 $f_{OSC}/1$ 0 0 1 $f_{OSC}/2$ 0 1 0 $f_{OSC}/4$ 0 1 1 $f_{OSC}/8$ 1 0 0 $f_{OSC}/16$ 1 0 1 $f_{OSC}/32$ 1 1 0 reserved 1 1 1 reserved
COE	Clock Out Enable. Set COE to output the system clock divided by 2 on XTAL2 (P4.1). The internal RC oscillator or external clock source must be selected in order to use this feature and P4.1 must be configured as an output.

7. Reset

During reset, all I/O Registers are set to their initial values, the port pins are tristated, and the program starts execution from the Reset Vector, 0000H. The AT89LP428/828 has five sources of reset: power-on reset, brown-out reset, external reset, watchdog reset, and software reset.

7.1 Power-on Reset

A Power-on Reset (POR) is generated by an on-chip detection circuit. The detection level V_{POR} is nominally 1.4V. The POR is activated whenever V_{CC} is below the detection level. The POR circuit can be used to trigger the start-up reset or to detect a supply voltage failure in devices without a brown-out detector. The POR circuit ensures that the device is reset from power-on. A power-on sequence is shown in Figure 7-1 on page 24. When V_{CC} reaches the Power-on Reset threshold voltage V_{POR}, an initialization sequence lasting t_{POR} is started. When the initialization sequence completes, the start-up timer determines how long the device is kept in POR after V_{CC} rise. The POR signal is activated again, without any delay, when V_{CC} falls below the POR threshold level. A Power-on Reset (i.e. a cold reset) will set the POF flag in PCON. The internally generated reset can be extended beyond the power-on period by holding the $\overline{RST}$ pin low longer than the time-out.

The Timer 0 and Timer 1 Interrupts are generated by TF0 and TF1, which are set by a rollover in their respective Timer/Counter registers (except for Timer 0 in Mode 3). When a timer interrupt is generated, the on-chip hardware clears the flag that generated it when the service routine is vectored to. The Timer 2 Interrupt is generated by a logic OR of bits TF2 and EXF2 in register T2CON. Neither of these flags is cleared by hardware when the CPU vectors to the service routine. The service routine normally must determine whether TF2 or EXF2 generated the interrupt and that bit must be cleared by software.

The Serial Port Interrupt is generated by the logic OR of RI and TI in SCON. Neither of these flags is cleared by hardware when the CPU vectors to the service routine. The service routine normally must determine whether RI or TI generated the interrupt and that bit must be cleared by software. The Serial Peripheral Interface Interrupt is generated by the logic OR of SPIF, MODF and TXE in SPSR. None of these flags is cleared by hardware when the CPU vectors to the service routine. The service routine normally must determine which bit generated the interrupt and that bit must be cleared by software.

A logic OR of all eight flags in the GPIF register causes the GPI. None of these flags is cleared by hardware when the service routine is vectored to. The service routine must determine which bit generated the interrupt and that bit must be cleared in software. If the interrupt was level activated, then the external requesting source must de-assert the interrupt before the flag may be cleared by software.

The CFA and CFB bits in ACSRA and ACSRB respectively generate the Comparator Interrupt. The service routine must normally determine whether CFA or CFB generated the interrupt, and the bit must be cleared by software.

A logic OR of the four least significant bits in the T2CCF register causes the Compare/Capture Array Interrupt. None of these flags is cleared by hardware when the service routine is vectored to. The service routine must determine which bit generated the interrupt and that bit must be cleared in software.

All of the bits that generate interrupts can be set or cleared by software, with the same result as though they had been set or cleared by hardware. That is, interrupts can be generated and pending interrupts can be canceled in software.

Table 9-1. Interrupt Vector Addresses

Interrupt	Source	Vector Address
System Reset	RST or POR or BOD	0000H
External Interrupt 0	IE0	0003H
Timer 0 Overflow	TF0	000BH
External Interrupt 1	IE1	0013H
Timer 1 Overflow	TF1	001BH
Serial Port Interrupt	RI or TI	0023H
Timer 2 Interrupt	TF2 or EXF2	002BH
Analog Comparator Interrupt	CFA or CFB	0033H
General-purpose Interrupt	$GPIF_{7-0}$	003BH
Compare/Capture Array Interrupt	$T2CCF_{3-0}$	0043H
Serial Peripheral Interface Interrupt	SPIF or MODF or TXE	004BH

Table 10-3. Port Configuration Registers

Port	Port Data	Port Configuration
1	P1 (90H)	P1M0 (C2H), P1M1 (C3H)
2	P2 (A0H)	P2M0 (C4H), P2M1 (C5H)
3	P3 (B0H)	P3M0 (C6H), P3M1 (C7H)
4	P4 (C0H)	P4M0 (BEH), P4M1 (BFH)

10.1.1 Quasi-bidirectional Output

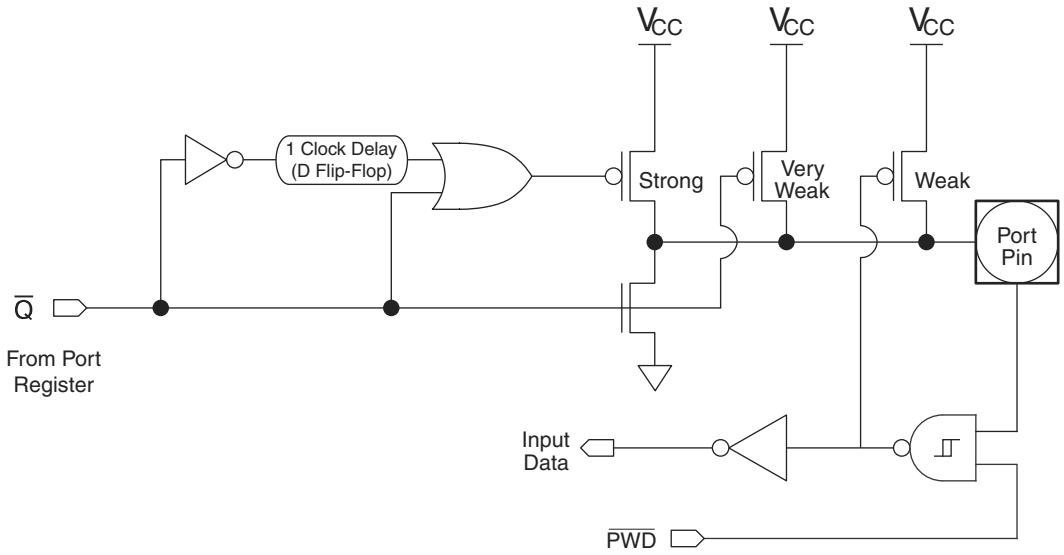
Port pins in quasi-bidirectional output mode function similar to standard 8051 port pins. A Quasi-bidirectional port can be used both as an input and output without the need to reconfigure the port. This is possible because when the port outputs a logic high, it is weakly driven, allowing an external device to pull the pin low. When the pin is driven low, it is driven strongly and able to sink a large current. There are three pull-up transistors in the quasi-bidirectional output that serve different purposes.

One of these pull-ups, called the “very weak” pull-up, is turned on whenever the port latch for the pin contains a logic “1”. This very weak pull-up sources a very small current that will pull the pin high if it is left floating.

A second pull-up, called the “weak” pull-up, is turned on when the port latch for the pin contains a logic “1” and the pin itself is also at a logic “1” level. This pull-up provides the primary source current for a quasi-bidirectional pin that is outputting a “1”. If this pin is pulled low by an external device, this weak pull-up turns off, and only the very weak pull-up remains on. In order to pull the pin low under these conditions, the external device has to sink enough current to overpower the weak pull-up and pull the port pin below its input threshold voltage.

The third pull-up is referred to as the “strong” pull-up. This pull-up is used to speed up low-to-high transitions on a quasi-bidirectional port pin when the port latch changes from a logic “0” to a logic “1”. When this occurs, the strong pull-up turns on for two CPU clocks quickly pulling the port pin high. The quasi-bidirectional port configuration is shown in Figure 10-1.

Figure 10-1. Quasi-bidirectional Output



10.3 Port Read-Modify-Write

A read from a port will read either the state of the pins or the state of the port register depending on which instruction is used. Simple read instructions will always access the port pins directly. Read-modify-write instructions, which read a value, possibly modify it, and then write it back, will always access the port register. This includes bit write instructions such as CLR or SETB as they actually read the entire port, modify a single bit, then write the data back to the entire port. See Table 10-4 for a complete list of Read-modify-write instructions which may access the ports.

Table 10-4. Port Read-Modify-Write Instructions

Mnemonic	Instruction	Example
ANL	Logical AND	ANL P1, A
ORL	Logical OR	ORL P1, A
XRL	Logical EX-OR	XRL P1, A
JBC	Jump if bit set and clear bit	JBC P3.0, LABEL
CPL	Complement bit	CPL P3.1
INC	Increment	INC P1
DEC	Decrement	DEC P3
DJNZ	Decrement and jump if not zero	DJNZ P3, LABEL
MOV PX.Y, C	Move carry to bit Y of Port X	MOV P1.0, C
CLR PX.Y	Clear bit Y of Port X	CLR P1.1
SETB PX.Y	Set bit Y of Port X	SETB P3.2

10.4 Port Alternate Functions

Most general-purpose digital I/O pins of the AT89LP428/828 share functionality with the various I/Os needed for the peripheral units. Table 10-6 lists the alternate functions of the port pins. Alternate functions are connected to the pins in a logic AND fashion. In order to enable the alternate function on a port pin, that pin must have a “1” in its corresponding port register bit, otherwise the input/output will always be “0”. However, alternate functions may be temporarily forced to “0” by clearing the associated port bit, provided that the pin is not in input-only mode. Furthermore, each pin must be configured for the correct input/output mode as required by its peripheral before it may be used as such. Table 10-5 shows how to configure a generic pin for use with an alternate function.

Table 10-5. Alternate Function Configurations for Pin y of Port x

PxM0.y	PxM1.y	Px.y	I/O Mode
0	0	1	Bidirectional (internal pull-up)
0	1	1	Output
1	0	X	Input
1	1	1	Bidirectional (external pull-up)

12. Enhanced Timer 2

The AT89LP428/828 includes a 16-bit Timer/Counter 2 with the following features:

- 16-bit timer/counter with one 16-bit reload/capture register
- One external reload/capture input
- Up/Down counting mode with external direction control
- UART baud rate generation
- Output-pin toggle on timer overflow
- Dual slope symmetric operating modes

Timer 2 is a 16-bit Timer/Counter that can operate as either a timer or an event counter. The type of operation is selected by bit C/$\overline{T2}$ in the SFR T2CON. Timer 2 has three operating modes: capture, auto-reload (up or down counting), and baud rate generator. The modes are selected by bits in T2CON and T2MOD, as shown in Table 12-3. Timer 2 also serves as the time base for the Compare/Capture Array (see “Compare/Capture Array” on page 61).

Timer 2 consists of two 8-bit registers, TH2 and TL2. In the Timer function, the register is incremented every clock cycle. Since a clock cycle consists of one oscillator period, the count rate is equal to the oscillator frequency. The timer rate can be prescaled by a value between 1 and 16 using the Timer Prescaler (see Table 6-2 on page 23).

In the Counter function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T2. In this function, the external input is sampled every clock cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during the cycle following the one in which the transition was detected. Since two clock cycles are required to recognize a 1-to-0 transition, the maximum count rate is 1/2 of the oscillator frequency. To ensure that a given level is sampled at least once before it changes, the level should be held for at least one full clock cycle.

Table 12-1. Timer 2 Operating Modes

RCLK + TCLK	CP/$\overline{RL2}$	DCEN	T2OE	TR2	Mode
0	0	0	0	1	16-bit Auto-reload
0	0	1	0	1	16-bit Auto-reload Up-down
0	1	X	0	1	16-bit Capture
1	X	X	X	1	Baud Rate Generator
X	X	X	1	1	Frequency Generator
X	X	X	X	0	(Off)

The following definitions for Timer 2 are used in the subsequent paragraphs:

Table 12-2. Timer 2 Definitions

Symbol	Definition
MIN	0000H
MAX	FFFFH
BOTTOM	16-bit value of {RCAP2H,RCAP2L} (standard modes)
TOP	16-bit value of {RCAP2H,RCAP2L} (enhanced modes)

Table 12-4. T2MOD – Timer 2 Mode Control Register

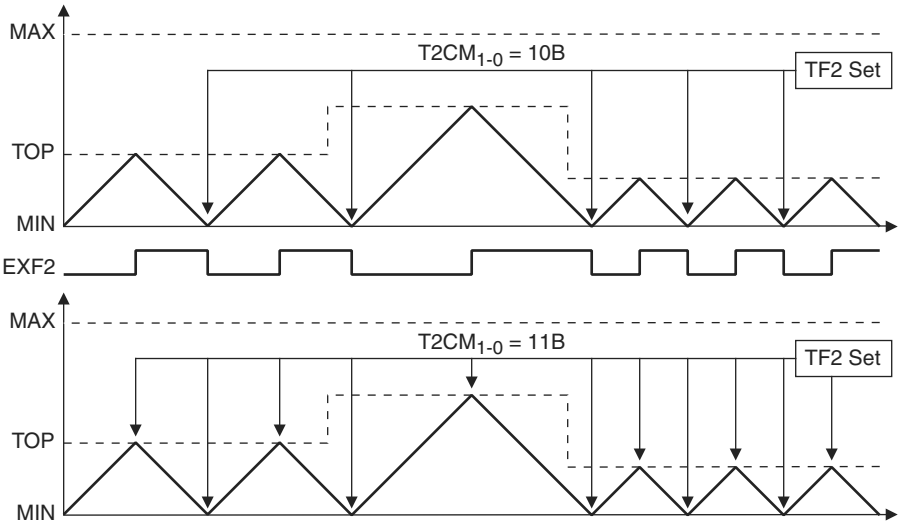
T2MOD Address = 0C9H — Reset Value = 0000 0000B

Not Bit Addressable

	PHSD	PHS2	PHS1	PHS0	T2CM1	T2CM0	T2OE	DCEN
Bit	7	6	5	4	3	2	1	0

Symbol	Function
PHSD	CCA Phase Direction. For phase modes with 3 or 4 channels, PHSD determines the direction that the channels are cycled through. PHSD also determines the initial phase relationship for 2 phase modes. PHSD Direction 0 A →B →A →B or A →B →C →A →B →C or A →B →C →D →A →B →C →D 1 B →A →B →A or C →B →A →C →B →A or D →C →B →A →D →C →B →A
PHS [2 - 0]	CCA Phase Mode. PWM channels may be grouped by 2, 3 or 4 such that only one channel in a group produces a pulse in any one period. The PHS [2 - 0] bits may only be written when the timer is not active, i.e. TR2 = 0. **PHS2 PHS1 PHS0 Phase Mode** 0 0 0 Disabled, all channels active 0 0 1 2-phase output on channels A & B 0 1 0 3-phase output on channels A, B & C 0 1 1 4-phase output on channels A, B, C & D 1 0 0 Dual 2-phase output on channels A & B and C & D 1 0 1 reserved 1 1 0 reserved 1 1 1 reserved
T2CM [1 - 0]	Timer 2 Count Mode. **T2CM1 T2CM0** Count Mode 0 0 Standard Timer 2 (up count: BOTTOM →MAX) 0 1 Clear on RCAP compare (up count: MIN →TOP) 1 0 Dual-slope with single update (up-down count: MIN →TOP →MIN) 1 1 Dual-slope with double update (up-down count: MIN →TOP →MIN)
T2OE	Timer 2 Output Enable. When T2OE = 1 and C/$\overline{T}$2 = 0, the T2 pin will toggle after every Timer 2 overflow.
DCEN	Timer 2 Down Count Enable. When Timer 2 operates in Auto-reload mode and EXEN2 = 1, setting DCEN = 1 will cause Timer 2 to count up or down depending on the state of T2EX.

Figure 12-6. Timer 2 Waveform: Dual Slope Modes



12.4 Baud Rate Generator

Timer 2 is selected as the baud rate generator by setting TCLK and/or RCLK in T2CON (Table 12-3 on page 53). Note that the baud rates for transmit and receive can be different if Timer 2 is used for the receiver or transmitter and Timer 1 is used for the other function. Setting RCLK and/or TCLK puts Timer 2 into its baud rate generator mode, as shown in Figure 12-7.

The baud rate generator mode is similar to the auto-reload mode, in that a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software.

The baud rates in UART modes 1 and 3 are determined by Timer 2's overflow rate according to the following equation.

$$\text{Modes 1 and 3 Baud Rates} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

The Timer can be configured for either timer or counter operation. In most applications, it is configured for timer operation ($C/\overline{T2} = 0$). The baud rate formulas are given below

.

$$\text{T2CM} = 00\text{B} \qquad \frac{\text{Modes 1, 3}}{\text{Baud Rate}} = \frac{\text{Oscillator Frequency}}{16 \times (\text{TPS} + 1) \times [65536 - (\text{RCAP2H,RCAP2L})]}$$

$$\text{T2CM} = 01\text{B} \qquad \frac{\text{Modes 1, 3}}{\text{Baud Rate}} = \frac{\text{Oscillator Frequency}}{16 \times (\text{TPS} + 1) \times [(\text{RCAP2H,RCAP2L}) + 1]}$$

where (RCAP2H, RCAP2L) is the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

Table 13-5. T2CCF – Timer/Counter 2 Compare/Capture Flags

T2CCF Address = 0D5H — Reset Value = XXXX 0000B

Not Bit Addressable

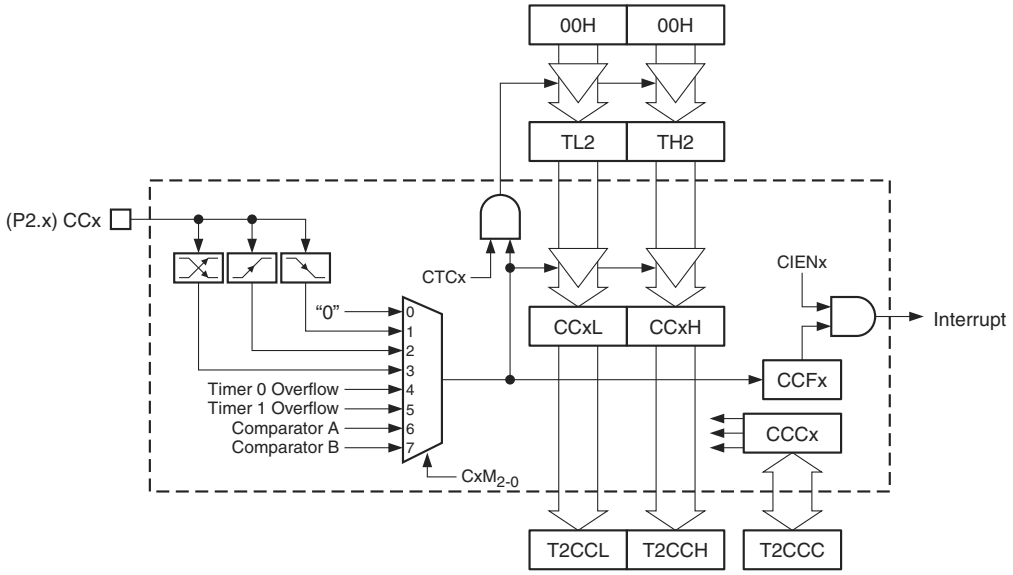
	–	–	–	–	CCFD	CCFC	CCFB	CCFA
Bit	7	6	5	4	3	2	1	0

Symbol	Function
CCFD	Channel D Compare/Capture Interrupt Flag. Set by a compare/capture event on channel D. Must be cleared by software. CCFD will generate an interrupt when CIEND = 1 and ECC = 1.
CCFC	Channel C Compare/Capture Interrupt Flag. Set by a compare/capture event on channel C. Must be cleared by software. CCFC will generate an interrupt when CIENC = 1 and ECC = 1.
CCFB	Channel B Compare/Capture Interrupt Flag. Set by a compare/capture event on channel B. Must be cleared by software. CCFB will generate an interrupt when CIENB = 1 and ECC = 1.
CCFA	Channel A Compare/Capture Interrupt Flag. Set by a compare/capture event on channel A. Must be cleared by software. CCFA will generate an interrupt when CIENA = 1 and ECC = 1.

13.2 Input Capture Mode

The Compare/Capture Array provides a variety of capture modes suitable for time-stamping events or performing measurements of pulse width, frequency, slope, etc. The CCA channels are configured for capture mode by clearing the CCM*x* bit in the associated CCC*x* register to 0. Each time a capture event occurs, the contents of Timer 2 (TH2 and TL2) are transferred to the 16-bit data register of the corresponding channel, and the channel's interrupt flag CCF*x* is set in T2CCF. Optionally, the capture event may also clear Timer 2 to 0000H by setting the CTC*x* bit in CCC*x*. The capture event is defined by the C*x*M$_{2-0}$ bits in CCC*x* and may be either externally or internally generated. A diagram of a CCA channel in capture mode is shown in Figure 13-2.

Figure 13-2. CCA Capture Mode Diagram



13.3.1 Waveform Generation

Each CCA channel has an associated external compare output pin: CCA (P2.0), CCB (P2.1), CCC (P2.2) and CCD (P2.3). The C*x*$M_{2\text{-}0}$ bits in CCC*x* determine what action is taken when a compare event occurs. The output pin may be set to 1, cleared to 0 or toggled. Output actions take place even if the interrupt is disabled; however, the associated I/O pin must be set to the desired output mode before the compare event occurs. The state of the compare outputs are initialized to 1 by reset.

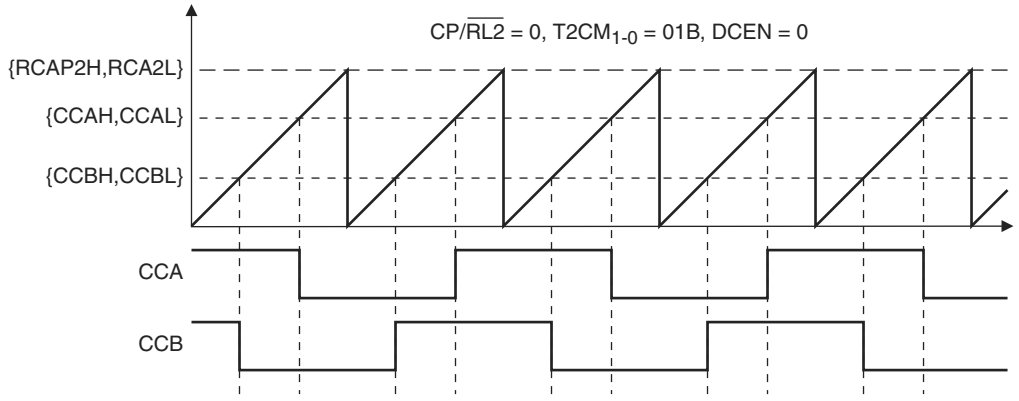
Multiple compare events per channel can occur within a single time period, provided that the software has time to update the compare value before the timer reaches the next compare point. In this case other interrupts should be disabled or the CCA interrupt given a higher priority in order to ensure that the interrupt is serviced in time.

A wide range of waveform generation configurations are possible using the various operating modes of Timer 2 and the CCA. Some example configurations are detailed below. Pulse width modulation is a special case of output compare. See “Pulse Width Modulation Mode” on page 68 for more details of PWM operation.

13.3.1.1 Normal Mode

The simplest waveform mode is when CP/$\overline{RL2}$ = 0 and T2CM$\overline{1\text{-}0}$ = 01B. In this mode the frequency of the output is determined by the TOP value stored in RCAP2L and RCAP2H and output edges occur at fractions of the timer period. Figure 13-4 shows an example of outputting two waveforms of the same frequency but different phase by using the toggle on match action. More complex waveforms are achieved by changing the TOP value and the compare values more frequently.

Figure 13-4. Normal Mode Waveform Example



13.3.1.2 Clear-Timer-on-Compare Mode

Clear-Timer-on-Compare (CTC) mode occurs when the CTC*x* bit of a compare channel is set to one. CTC mode works best when Timer 2 is in capture mode (CP/$\overline{RL2}$ = 1) to allow the full range of compare values. In CTC mode, the compare value defines the interval between output events because the timer is cleared after every compare match. Figure 13-5 shows an example waveform using the toggle on match action in CTC mode.

Table 15-2. GPLS – General-purpose Interrupt Level Select Register

GPLS = 9BH — Reset Value = 0000 0000B

Not Bit Addressable

	GPLS7	GPLS6	GPLS5	GPLS4	GPLS3	GPLS2	GPLS1	GPLS0
Bit	7	6	5	4	3	2	1	0

GPMOD.x 0 = detect low level or negative edge on P1.x

1 = detect high level or positive edge on P1.x

Table 15-3. GPIEN – General-purpose Interrupt Enable Register

GPIEN = 9CH — Reset Value = 0000 0000B

Not Bit Addressable

	GPIEN7	GPIEN6	GPIEN5	GPIEN4	GPIEN3	GPIEN2	GPIEN1	GPIEN0
Bit	7	6	5	4	3	2	1	0

GPIEN.x 0 = interrupt for P1.x disabled

1 = interrupt for P1.x enabled

Table 15-4. GPIF – General-purpose Interrupt Flag Register

GPIF = 9DH — Reset Value = 0000 0000B

Not Bit Addressable

	GPIF7	GPIF6	GPIF5	GPIF4	GPIF3	GPIF2	GPIF1	GPIF0
Bit	7	6	5	4	3	2	1	0

GPIF.x 0 = interrupt on P1.x inactive

1 = interrupt on P1.x active. Must be cleared by software.

interrupted by a data byte. An address byte, however, interrupts all slaves. Each slave can examine the received byte and see if it is being addressed. The addressed slave clears its SM2 bit and prepares to receive the data bytes that follows. The slaves that are not addressed set their SM2 bits and ignore the data bytes.

The SM2 bit can be used to check the validity of the stop bit in Mode 1. In a Mode 1 reception, if SM2 = 1, the receive interrupt is not activated unless a valid stop bit is received.

Table 16-1. SCON – Serial Port Control Register

SCON Address = 98H — Reset Value = 0000 0000B

Bit Addressable

Bit	7	6	5	4	3	2	1	0
	SM0/FE	SM1	SM2	REN	TB8	RB8	T1	RI

(SMOD0 = 0/1)[1]

Symbol	Function
FE	Framing error bit. This bit is set by the receiver when an invalid stop bit is detected. The FE bit is not cleared by valid frames and must be cleared by software. The SMOD0 bit must be set to enable access to the FE bit. FE will be set regardless of the state of SMOD0.
SM0	Serial Port Mode Bit 0, (SMOD0 must = 0 to access bit SM0)
SM1	Serial Port Mode Bit 1 **SM0** **SM1** **Mode** **Description** **Baud Rate**[2] 0 0 0 shift register $f_{osc}/2$ or $f_{osc}/4$ or Timer 1 0 1 1 8-bit UART variable (Timer 1 or Timer 2) 1 0 2 9-bit UART $f_{osc}/32$ or $f_{osc}/16$ 1 1 3 9-bit UART variable (Timer 1 or Timer 2)
SM2	Enables the Automatic Address Recognition feature in Modes 2 or 3. If SM2 = 1 then RI will not be set unless the received 9th data bit (RB8) is 1, indicating an address, and the received byte is a Given or Broadcast Address. In Mode 1, if SM2 = 1 then RI will not be activated unless a valid stop bit was received, and the received byte is a Given or Broadcast Address. In Mode 0, SM2 determines the idle state of the shift clock such that the clock is the inverse of SM2, i.e. when SM2 = 0 the clock idles high and when SM2 = 1 the clock idles low.
REN	Enables serial reception. Set by software to enable reception. Clear by software to disable reception.
TB8	The 9th data bit that will be transmitted in Modes 2 and 3. Set or clear by software as desired. In Mode 0, setting TB8 enables Timer 1 as the shift clock generator.
RB8	In Modes 2 and 3, the 9th data bit that was received. In Mode 1, if SM2 = 0, RB8 is the stop bit that was received. In Mode 0, RB8 is not used.
TI	Transmit interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or at the beginning of the stop bit in the other modes, in any serial transmission. Must be cleared by software.
RI	Receive interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or halfway through the stop bit time in the other modes, in any serial reception (except see SM2). Must be cleared by software.

Notes: 1. SMOD0 is located at PCON.6.

2. f_{osc} = oscillator frequency. The baud rate depends on SMOD1 (PCON.7).

Reception is initiated by the condition REN = 1 and R1 = 0. At the next clock cycle, the RX Control unit writes the bits 11111110 to the receive shift register and activates RECEIVE in the next clock phase. RECEIVE enables Shift Clock to alternate output function line of P3.1. As data bits come in from the right, “1”s shift out to the left. When the “0” that was initially loaded into the right-most position arrives at the left-most position in the shift register, it flags the RX Control block to do one last shift and load SBUF. Then RECEIVE is cleared and RI is set.

The relationship between the shift clock and data is determined by the combination of the SM2 and SMOD1 bits as listed in Table 16-5 and shown in Figure 16-2. The SM2 bit determines the idle state of the clock when not currently transmitting/receiving. The SMOD1 bit determines if the output data is stable for both edges of the clock, or just one.

Table 16-5. Mode 0 Clock and Data Modes

SM2	SMOD1	Clock Idle	Data Changed	Data Sampled
0	0	High	While clock is high	Positive edge of clock
0	1	High	Negative edge of clock	Positive edge of clock
1	0	Low	While clock is low	Negative edge of clock
1	1	Low	Negative edge of clock	Positive edge of clock

17.3 Pin Configuration

When the SPI is enabled (SPE = 1), the data direction of the MOSI, MISO, SCK, and SS pins is automatically overridden according to the MSTR bit as shown in Table 17-1. The user doesn't need to reconfigure the pins when switching from master to slave or vice-versa. For more details on port configuration, refer to "Port Configuration" on page 35.

Table 17-1. SPI Pin Configuration and Behavior when SPE = 1

Pin	Mode	Master (MSTR = 1)	Slave (MSTR = 0)
SCK	Quasi-bidirectional	Output	Input (Internal Pull-up)
	Push-pull Output	Output	Input (Tristate)
	Input-only	No output (Tristated)	Input (Tristate)
	Open-drain Output	Output	Input (External Pull-up)
MOSI	Quasi-bidirectional	Output(1)	Input (Internal Pull-up)
	Push-pull Output	Output(2)	Input (Tristate)
	Input-only	No output (Tristated)	Input (Tristate)
	Open-drain Output	Output(1)	Input (External Pull-up)
MISO	Quasi-bidirectional	Input (Internal Pull-up)	Output ($\overline{SS}$ = 0) Internal Pull-up ($\overline{SS}$ = 1 or DISSO = 1)
	Push-pull Output	Input (Tristate)	Output ($\overline{SS}$ = 0) Tristated ($\overline{SS}$ = 1 or DISSO = 1)
	Input-only	Input (Tristate)	No output (Tristated)
	Open-drain Output	Input (External Pull-up)	Output ($\overline{SS}$ = 0) External Pull-up ($\overline{SS}$ = 1 or DISSO = 1)

Notes: 1. In these modes MOSI is active only during transfers. MOSI will be pulled high between transfers to allow other masters to control the line.

2. In Push-pull mode MOSI is active only during transfers, otherwise it is tristated to prevent line contention. A weak external pull-up may be required to prevent MOSI from floating.

Table 18-2. ACSRB – Analog Comparator B Control and Status Register

ACSRB = 9FH — Reset Value = 1100 0000B

Not Bit Addressable

	CSB1	CSB0	CONB	CFB	CENB	CMB2	CMB1	CMB0
Bit	7	6	5	4	3	2	1	0

Symbol	Function
CSB [1 - 0]	Comparator B Positive Input Channel Select[1] **CSB1** **CSB0** **B+ Channel** 0 0 AIN0 (P2.4) 0 1 AIN1 (P2.5) 1 0 AIN2 (P2.6) 1 1 AIN3 (P2.7)
CONB	Comparator B Input Connect. When CONB = 1, the analog input pins are connected to the comparator. When CONB = 0 the analog input pins are disconnected from the comparator. CONB must be cleared to 0 before changing CSB [1 - 0] or RFB [1 - 0].
CFB	Comparator B Interrupt Flag. Set when the comparator output meets the conditions specified by the CMB [2 - 0] bits and CENB is set. The flag must be cleared by software. The interrupt may be enabled/disabled by setting/clearing bit 6 of IE.
CENB	Comparator B Enable. Set this bit to enable the comparator. Clearing this bit will force the comparator output low and prevent further events from setting CFB. When CENB = 1, the analog input pins, P2.4 - P2.7, have their digital inputs disabled if they are configured in input-only mode.
CMB [2 - 0]	Comparator B Interrupt Mode **CMB2** **CMB1** **CMB0** **Interrupt Mode** 0 0 0 Negative (Low) level 0 0 1 Positive edge 0 1 0 Toggle with debouncing[2] 0 1 1 Positive edge with debouncing[2] 1 0 0 Negative edge 1 0 1 Toggle 1 1 0 Negative edge with debouncing[2] 1 1 1 Positive (High) level

Notes: 1. CONB must be cleared to 0 before changing CSB [1 - 0].

2. Debouncing modes require the use of Timer 1 to generate the sampling delay.

Table 18-3. AREF – Analog Comparator Reference Control Register

AREF = AFH — Reset Value = 0000 0000B

Not Bit Addressable

	CBC1	CBC0	RFB1	RFB0	CAC1	CAC0	RFA1	RFA0
Bit	7	6	5	4	3	2	1	0

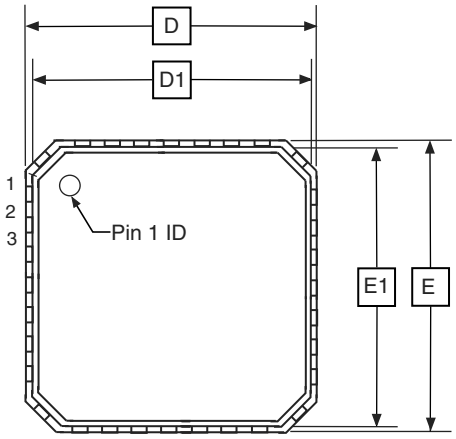
Symbol	Function		
CSC [1 - 0]	Comparator B Clock Select		
	CBC1	**CBC0**	**Clock Source**
	0	0	System Clock
	0	0	Timer 0 Overflow
	0	1	Timer 1 Overflow
	0	1	Timer 2 Overflow
RFB [1 - 0]	Comparator B Negative Input Channel Select(1)		
	CRF1	**RFB0**	**B-channel**
	0	0	AIN2 (P2.6)
	0	0	Internal $V_{AREF-\Delta}$ (~1.2V)
	0	1	Internal V_{AREF} (~1.3V)
	0	1	Internal $V_{AREF+\Delta}$ (~1.4V)
CAC [1 - 0]	Comparator A Clock Select		
	CAC1	**CAC0**	**Clock Source**
	0	0	System Clock
	0	0	Timer 0 Overflow
	0	1	Timer 1 Overflow
	0	1	Timer 2 Overflow
RFB [1 - 0]	Comparator A Negative Input Channel Select(2)		
	RFA1	**RFA0**	**A-channel**
	0	0	AIN1 (P2.5)
	0	0	Internal $V_{AREF-\Delta}$ (~1.2V)
	0	1	Internal V_{AREF} (~1.3V)
	0	1	Internal $V_{AREF+\Delta}$ (~1.4V)

Notes: 1. CONB (ACSRB.5) must be cleared to 0 before changing RFB [1 - 0].
2. CONA (ACSRA.5) must be cleared to 0 before changing RFA [1 - 0].

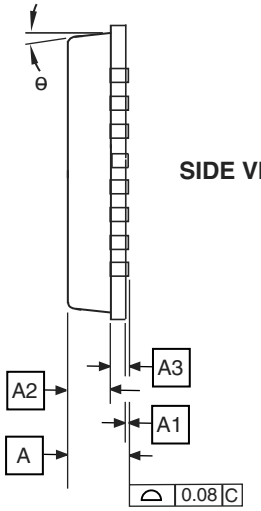
Table 21-1. Special Function Register Cross Reference (Continued)

PSW	D0H	
RCAP2H	CBH	Section 12.1 on page 53
RCAP2L	CAH	Section 12.1 on page 53
RH0	94H	Table 11-1 on page 41
RH1	95H	Table 11-1 on page 41
RL0	92H	Table 11-1 on page 41
RL1	93H	Table 11-1 on page 41
SADDR	A9H	Section 16.7 on page 90
SADEN	B9H	Section 16.7 on page 90
SBUF	99H	Section 16.3 on page 81
SCON	98H	Table 16-1 on page 78
SP	81H	
SPCR	E9H	Table 17-3 on page 97
SPDR	EAH	Table 17-2 on page 97
SPSR	E8H	Table 17-4 on page 98
T2CCA	D1H	Table 13-1 on page 63
T2CCC	D4H	Table 13-4 on page 64
T2CCF	D5H	Table 13-5 on page 65
T2CCH	D3H	Table 13-2 on page 63
T2CCL	D2H	Table 13-3 on page 63
T2CON	C8H	Table 12-3 on page 53
T2MOD	C9H	Table 12-4 on page 54
TCON	88H	Table 11-2 on page 45
TCONB	91H	Table 11-4 on page 47
TH0	8CH	Table 11-1 on page 41
TH1	8DH	Table 11-1 on page 41
TH2	CDH	Section 12.1 on page 53
TL0	8AH	Table 11-1 on page 41
TL1	8BH	Table 11-1 on page 41
TL2	CCH	Section 12.1 on page 53
TMOD	89H	Table 11-3 on page 46
WDTCON	**A7H**	Table 19-2 on page 106
WDTRST	**A6H**	Table 19-3 on page 106

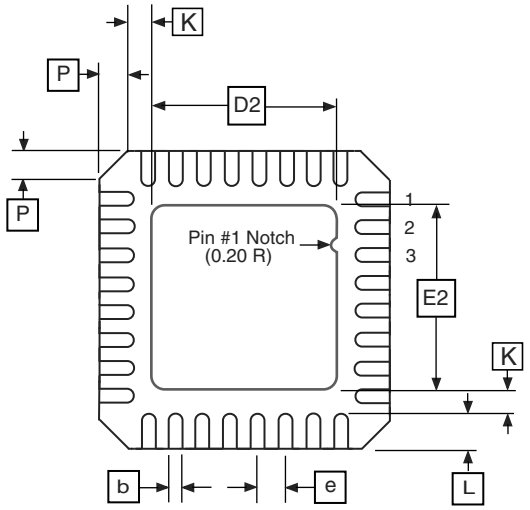
26.4 32M1-A – MLF



TOP VIEW



SIDE VIEW



BOTTOM VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	–	0.02	0.05	
A2	–	0.65	1.00	
A3		0.20 REF		
b	0.18	0.23	0.30	
D	4.90	5.00	5.10	
D1	4.70	4.75	4.80	
D2	2.95	3.10	3.25	
E	4.90	5.00	5.10	
E1	4.70	4.75	4.80	
E2	2.95	3.10	3.25	
e		0.50 BSC		
L	0.30	0.40	0.50	
P	–	–	0.60	
θ	–	–	12^{o}	
K	0.20	–	–	

Note: JEDEC Standard MO-220, Fig. 2 (Anvil Singulation), VHHD-2.

5/25/06

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**32M1-A**, 32-pad, 5 x 5 x 1.0 mm Body, Lead Pitch 0.50 mm, 3.10 mm Exposed Pad, Micro Lead Frame Package (MLF)	32M1-A	E