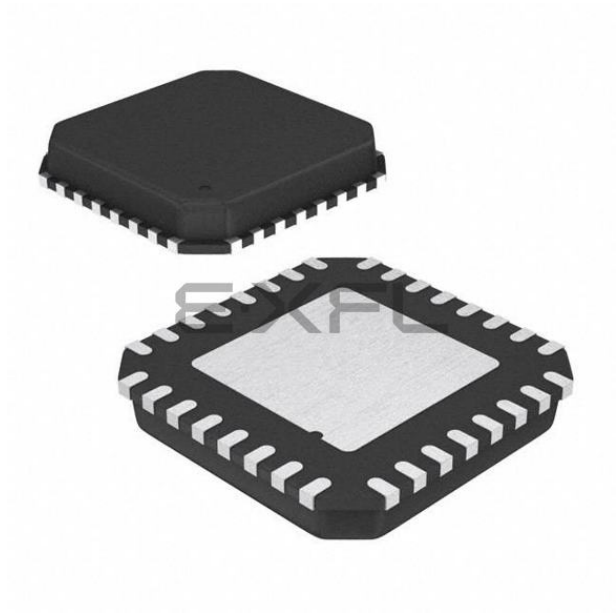

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Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	20MHz
Connectivity	SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	30
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-VQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at89lp428-20mh

2. Overview

The AT89LP428/828 is a low-power, high-performance CMOS 8-bit microcontroller with 4K/8K bytes of In-System Programmable Flash program memory and 512/1024 bytes of Flash data memory. The device is manufactured using Atmel®'s high-density nonvolatile memory technology and is compatible with the industry-standard MCS51 instruction set. The AT89LP428/828 is built around an enhanced CPU core that can fetch a single byte from memory every clock cycle. In the classic 8051 architecture, each fetch requires 6 clock cycles, forcing instructions to execute in 12, 24 or 48 clock cycles. In the AT89LP428/828 CPU, instructions need only 1 to 4 clock cycles providing 6 to 12 times more throughput than the standard 8051. Seventy percent of instructions need only as many clock cycles as they have bytes to execute, and most of the remaining instructions require only one additional clock. The enhanced CPU core is capable of 20 MIPS throughput whereas the classic 8051 CPU can deliver only 4 MIPS at the same current consumption. Conversely, at the same throughput as the classic 8051, the new CPU core runs at a much lower speed and thereby greatly reducing power consumption and EMI.

The AT89LP428/828 provides the following standard features: 4K/8K bytes of In-System Programmable Flash program memory, 512/1024 bytes of Flash data memory, 768 bytes of RAM, up to 30 I/O lines, three 16-bit timer/counters, up to six PWM outputs, a programmable watchdog timer, two analog comparators, a full-duplex serial port, a serial peripheral interface, an internal RC oscillator, on-chip crystal oscillator, and a four-level, ten-vector interrupt system. A block diagram is shown in Figure 2-1 on page 6.

Timer 0 and Timer 1 in the AT89LP428/828 are enhanced with two new modes. Mode 0 can be configured as a variable 9- to 16-bit timer/counter and Mode 1 can be configured as a 16-bit auto-reload timer/counter. In addition, the timer/counters may independently drive an 8-bit precision pulse width modulation output.

Timer 2 on the AT89LP428/828 serves as a 16-bit time base for a 4-channel Compare/Capture Array with up to four multi-phasic, variable precision PWM outputs.

The enhanced UART of the AT89LP428/828 includes Framing Error Detection and Automatic Address Recognition. In addition, enhancements to Mode 0 allow hardware accelerated emulation of half-duplex SPI or 2-wire interfaces.

The I/O ports of the AT89LP428/828 can be independently configured in one of four operating modes. In quasi-bidirectional mode, the ports operate as in the classic 8051. In input-only mode, the ports are tristated. Push-pull output mode provides full CMOS drivers and open-drain mode provides just a pull-down. In addition, all 8 pins of Port 1 can be configured to generate an interrupt using the General-purpose Interrupt (GPI) interface.

4. Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 4-1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect. User software should not write to these unlisted locations, since they may be used in future products to invoke new features.

Table 4-1. AT89LP428/828 SFR Map and Reset Values

	8	9	A	B	C	D	E	F	
0F8H									0FFH
0F0H	B 0000 0000								0F7H
0E8H	SPSR 000x x000	SPCR 0000 0000	SPDR xxxx xxxx						0EFH
0E0H	ACC 0000 0000								0E7H
0D8H									0DFH
0D0H	PSW 0000 0000	T2CCA 0000 0000	T2CCL 0000 0000	T2CCH 0000 0000	T2CCC 0000 0000	T2CCF 0000 0000			0D7H
0C8H	T2CON 0000 0000	T2MOD 0000 0000	RCAP2L 0000 000	RCAP2H 0000 0000	TL2 0000 000	TH2 0000 0000			0CFH
0C0H	P4 xx11 1111		P1M0(2)	P1M1 0000 0000	P2M0(2)	P2M1 0000 0000	P3M0(2)	P3M1 0000 0000	0C7H
0B8H	IP 0000 0000	SADEN 0000 0000					P4M0(2)	P4M1 xx00 0000	0BFH
0B0H	P3 1111 1111				IE2 xxxx x000	IP2 xxxx x000	IP2H xxxx x000	IPH 0000 0000	0B7H
0A8H	IE 0000 0000	SADDR 0000 0000						AREF 0000 0000	0AFH
0A0H	P2 1111 1111		DPCF 0000 00x0				WDTRST (write-only)	WDTCON 0000 x000	0A7H
98H	SCON 0000 0000	SBUF xxxx xxxx	GPMOD 0000 0000	GPLS 0000 0000	GPIEN 0000 0000	GPIF 0000 0000		ACSRB 1100 0000	9FH
90H	P1 1111 1111	TCONB 0010 0100	RL0 0000 0000	RL1 0000 0000	RH0 0000 0000	RH1 0000 0000	MEMCON 0000 00xx	ACSRA 0000 0000	97H
88H	TCON 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000		CLKREG 0000 x000	8FH
80H		SP 0000 0111	DP0L 0000 0000	DP0H 0000 0000	DP1L 0000 0000	DP1H 0000 0000	PAGE xxxx xxx0	PCON 0000 0000	87H
	0	1	2	3	4	5	6	7	

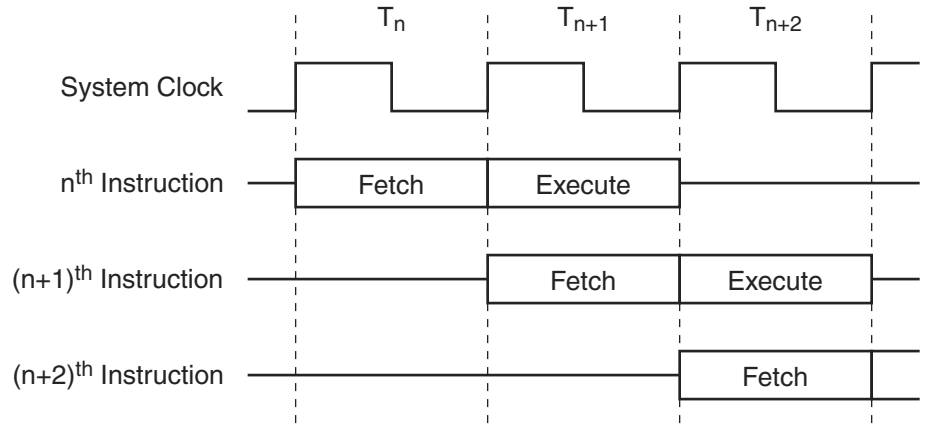
Notes: 1. All SFRs in the left-most column are bit-addressable.

2. Reset value is 1111 1111B when Tristate-port Fuse is enabled and 0000 0000B when disabled.

5. Enhanced CPU

The AT89LP428/828 uses an enhanced 8051 CPU that runs at 6 to 12 times the speed of standard 8051 devices (or 3 to 6 times the speed of X2 8051 devices). The increase in performance is due to two factors. First, the CPU fetches one instruction byte from the code memory every clock cycle. Second, the CPU uses a simple two-stage pipeline to fetch and execute instructions in parallel. This basic pipelining concept allows the CPU to obtain up to 1 MIPS per MHz. A simple example is shown in Figure 5-1.

Figure 5-1. Parallel Instruction Fetches and Executions



The MCS-51 instruction set allows for instructions of variable length from 1 to 3 bytes. In a single-clock-per-byte-fetch system this means each instruction takes at least as many clocks as it has bytes to execute. The majority of instructions in the AT89LP428/828 follow this rule: the instruction execution time in clock cycles equals the number of bytes per instruction with a few exceptions. Branches and Calls require an additional cycle to compute the target address and some other complex instructions require multiple cycles. See “Instruction Set Summary” on page 107 for more detailed information on individual instructions. Figures 5-2 and 5-3 show examples of 1- and 2-byte instructions.

Figure 5-2. Single-cycle ALU Operation (Example: INC R0)

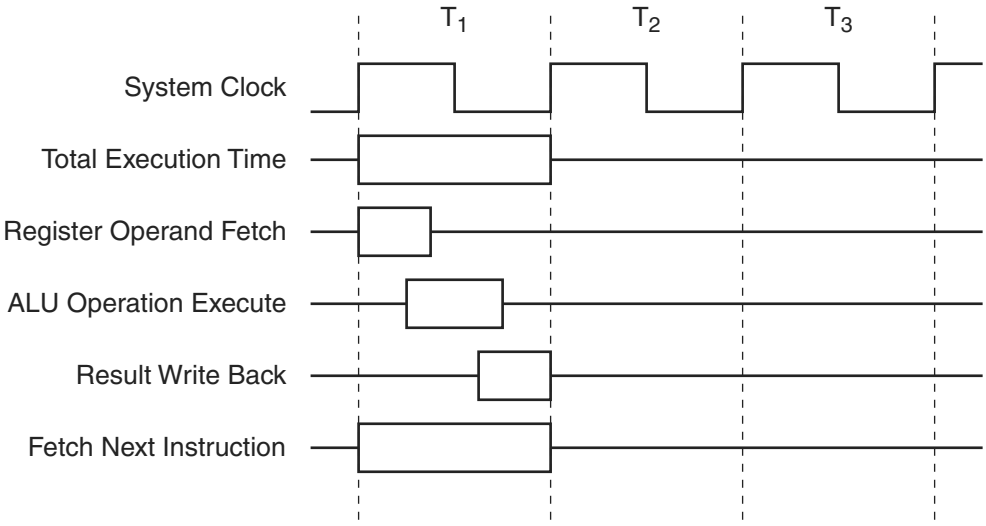


Table 9-6. IP2 – Interrupt Priority 2 Register

IP = B5H — Reset Value = 0xxx x000B

No Bit Addressable

	IP2D	–	–	–	–	PSP	PCC	PGP
Bit	7	6	5	4	3	2	1	0

Symbol	Function
IP2D	Interrupt Priority 2 Disable. Set IP2D to 1 to disable all interrupts with priority level two. Clear to 0 to enable all interrupts with priority level two when EA = 1.
PSP	Serial Peripheral Interface Interrupt Priority Low
PCC	Compare/Capture Array Interrupt Priority Low
PGP	General-purpose Interrupt 0 Priority Low

.

Table 9-7. IP2H – Interrupt Priority 2 High Register

IP2H = B6H — Reset Value = 0xxx x000B

Not Bit Addressable

	IP3D	–	–	–	–	PSPH	PCCH	PGPH
Bit	7	6	5	4	3	2	1	0

Symbol	Function
IP3D	Interrupt Priority 3 Disable. Set IP3D to 1 to disable all interrupts with priority level three. Clear to 0 to enable all interrupts with priority level three when EA = 1.
PSPH	Serial Peripheral Interface Interrupt Priority High
PCCH	Compare/Capture Array Interrupt Priority High
PGPH	General-purpose Interrupt 0 Priority High

10.1.2 Input-only Mode

The input only port configuration is shown in Figure 10-2. The output drivers are tristated. The input includes a Schmitt-triggered input for improved input noise rejection. The input circuitry of P3.2, P3.3, P3.6, P4.0 and P4.1 is not disabled during Power-down (see Figure 10-3) and therefore these pins should not be left floating during Power-down when configured in this mode.

Figure 10-2. Input Only

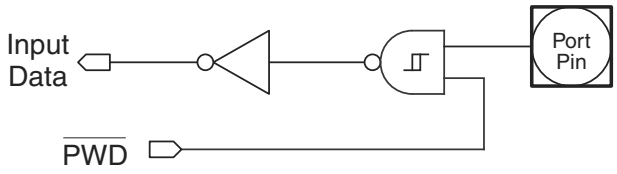
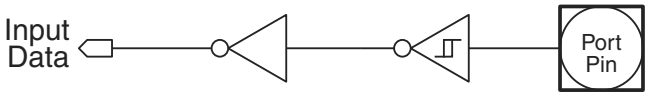


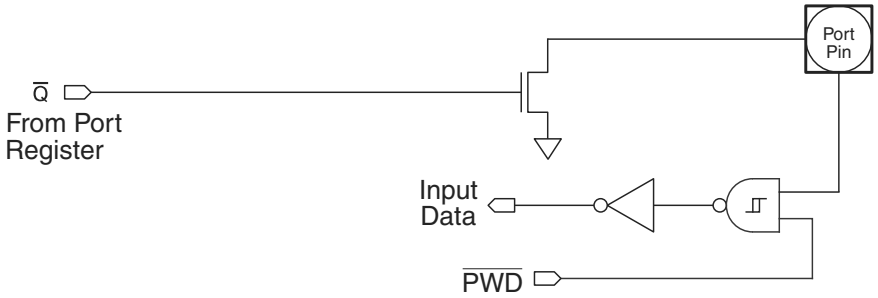
Figure 10-3. Input Circuit for P3.2, P3.3 and P3.6



10.1.3 Open-drain Output

The open-drain output configuration turns off all pull-ups and only drives the pull-down transistor of the port pin when the port latch contains a logic “0”. To be used as a logic output, a port configured in this manner must have an external pull-up, typically a resistor tied to V_{CC}. The pull-down for this mode is the same as for the quasi-bidirectional mode. The open-drain port configuration is shown in Figure 10-4. The input circuitry of P3.2, P3.3 and P3.6 is not disabled during Power-down (see Figure 10-3) and therefore these pins should not be left floating during Power-down when configured in this mode.

Figure 10-4. Open-drain Output



11. Enhanced Timer 0 and Timer 1 with PWM

The AT89LP428/828 has two 16-bit Timer/Counters, Timer 0 and Timer 1, with the following features:

- Two 16-bit timer/counters with 16-bit reload registers
- Two independent 8-bit precision PWM outputs with 8-bit prescalers
- UART or SPI baud rate generation using Timer 1
- Output pin toggle on timer overflow
- Split timer mode allows for three separate timers (two 8-bit, one 16-bit)
- Gated modes allow timers to run/halt based on an external input

Timer 0 and Timer 1 have similar modes of operation. As timers, they increase every clock cycle by default. Thus, the registers count clock cycles. Since a clock cycle consists of one oscillator period, the count rate is equal to the oscillator frequency. The timer rate can be prescaled by a value between 1 and 16 using the Timer Prescaler (see Table 6-2 on page 23). Both Timers share the same prescaler.

As counters, the timer registers are incremented in response to a 1-to-0 transition at the corresponding input pins, T0 or T1. The external input is sampled every clock cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during the cycle following the one in which the transition was detected. Since 2 clock cycles are required to recognize a 1-to-0 transition, the maximum count rate is 1/2 of the oscillator frequency. There are no restrictions on the duty cycle of the input signal, but it should be held for at least one full clock cycle to ensure that a given level is sampled at least once before it changes.

Furthermore, the Timer or Counter functions for Timer 0 and Timer 1 have four operating modes: variable width timer, 16-bit auto-reload timer, 8-bit auto-reload timer, and split timer. The control bits C/T in the Special Function Register TMOD select the Timer or Counter function. The bit pairs (M1, M0) in TMOD select the operating modes.

Table 11-1. Timer 0/1 Register Summary

Name	Address	Purpose	Bit-Addressable
TCON	88H	Control	Y
TMOD	89H	Mode	N
TL0	8AH	Timer 0 low-byte	N
TL1	8BH	Timer 1 low-byte	N
TH0	8CH	Timer 0 high-byte	N
TH1	8DH	Timer 1 high-byte	N
TCONB	91H	Mode	N
RL0	92H	Timer 0 reload low-byte	N
RL1	93H	Timer 1 reload low-byte	N
RH0	94H	Timer 0 reload high-byte	N
RH1	95H	Timer 1 reload high-byte	N

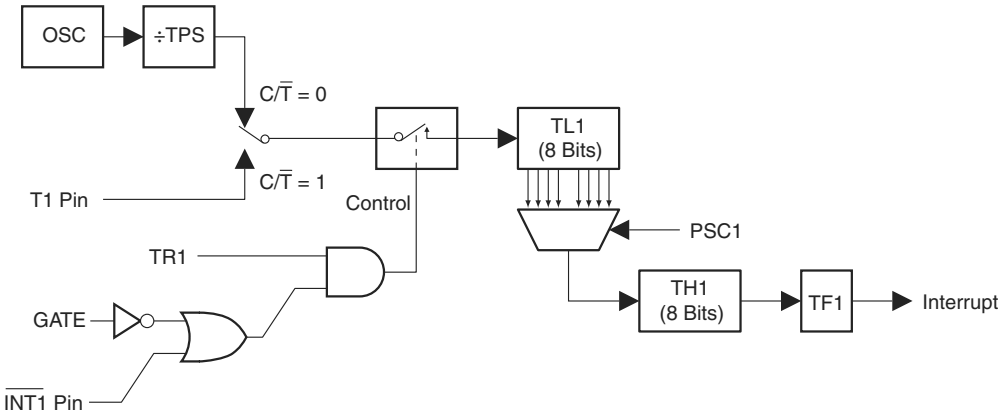
11.1 Mode 0 – Variable Width Timer/Counter

Both Timers in Mode 0 are 8-bit Counters with a variable prescaler. The prescaler may vary from 1 to 8 bits depending on the PSC bits in TCONB, giving the timer a range of 9 to 16 bits. By default the timer is configured as a 13-bit timer compatible to Mode 0 in the standard 8051. Figure 11-1 shows the Mode 0 operation as it applies to Timer 1 in 13-bit mode. As the count rolls over from all “1”s to all “0”s, it sets the Timer interrupt flag TF1. The counter input is enabled to the Timer when TR1 = 1 and either GATE = 0 or $\overline{INT1}$ = 1. Setting GATE = 1 allows the Timer to be controlled by external input $\overline{INT1}$, to facilitate pulse width measurements. TR1 is a control bit in the Special Function Register TCON. GATE is in TMOD. The 13-bit register consists of all 8 bits of TH1 and the lower 5 bits of TL1. The upper 3 bits of TL1 are indeterminate and should be ignored. Setting the run flag (TR1) does not clear the registers.

$$\text{Mode 0:} \qquad \text{Time-out Period} = \frac{256 \times 2^{PSC0+1}}{\text{Oscillator Frequency}} \times (TPS + 1)$$

Note: RH1/RL1 are not required by Timer 1 during Mode 0 and may be used as temporary storage registers.

Figure 11-1. Timer/Counter 1 Mode 0: Variable Width Counter



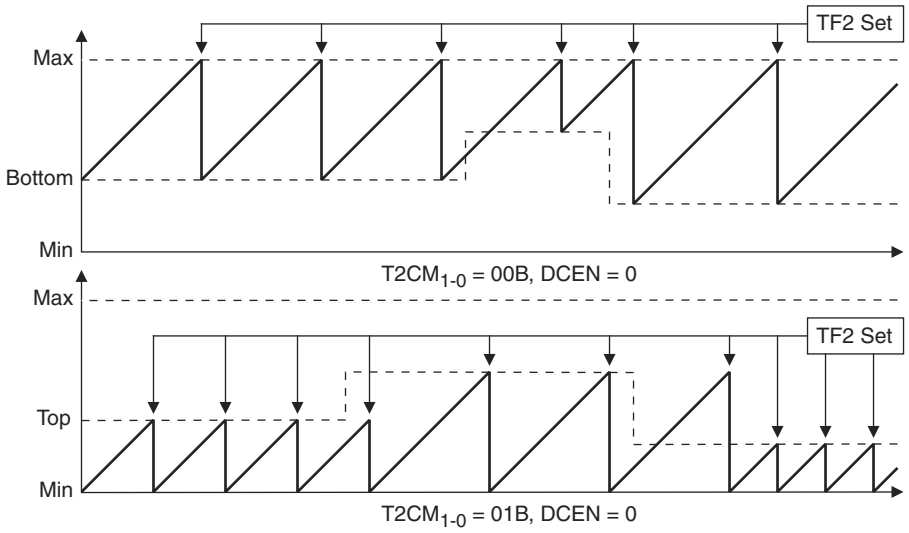
Mode 0 operation is the same for Timer 0 as for Timer 1, except that TR0, TF0 and $\overline{INT0}$ replace the corresponding Timer 1 signals in Figure 11-1. There are two different GATE bits, one for Timer 1 (TMOD.7) and one for Timer 0 (TMOD.3).

11.2 Mode 1 – 16-bit Auto-Reload Timer/Counter

In Mode 1 the Timers are configured for 16-bit auto-reload. The Timer register is run with all 16 bits. The 16-bit reload value is stored in the high and low reload registers (RH1/RL1). The clock is applied to the combined high and low timer registers (TH1/TL1). As clock pulses are received, the timer counts up: 0000H, 0001H, 0002H, etc. An overflow occurs on the FFFFH-to-0000H transition, upon which the timer register is reloaded with the value from RH1/RL1 and the overflow flag bit in TCON is set. See Figure 11-2. The reload registers default to 0000H, which gives the full 16-bit timer period compatible with the standard 8051. Mode 1 operation is the same for Timer/Counter 0.

$$\text{Mode 1:} \qquad \text{Time-out Period} = \frac{(65536 - \{RH0, RL0\})}{\text{Oscillator Frequency}} \times (TPS + 1)$$

Figure 12-3. Timer 2 Waveform: Auto-reload Mode (DCEN = 0)



12.3.2 Up or Down Counter

Setting DCEN = 1 enables Timer 2 to count up or down, as shown in Figure 12-4. In this mode, the T2EX pin controls the direction of the count (if EXEN2 = 1). A logic 1 at T2EX makes Timer 2 count up. When $T2CM_{1-0}$ = 00B, the timer will overflow at MAX and set the TF2 bit. This overflow also causes BOTTOM, the 16-bit value in RCAP2H and RCAP2L, to be reloaded into the timer registers, TH2 and TL2, respectively. A logic 0 at T2EX makes Timer 2 count down. The timer underflows when TH2 and TL2 equal BOTTOM, the 16-bit value stored in RCAP2H and RCAP2L. The underflow sets the TF2 bit and causes MAX to be reloaded into the timer registers. The EXF2 bit toggles whenever Timer 2 overflows or underflows and can be used as a 17th bit of resolution. In this operating mode, EXF2 does not flag an interrupt.

When T2EX = 1 and $T2CM_{1-0}$ = 01B, the timer will overflow at TOP and set the TF2 bit. This overflow also causes MIN to be reloaded into the timer registers. A logic 0 at T2EX makes Timer 2 count down. The timer underflows when TH2 and TL2 equal MIN. The underflow sets the TF2 bit and causes TOP to be reloaded into the timer registers. The behavior of Count Mode 0 versus Count Mode 0 when DCEN is enabled is shown in Figure 12-5. EXF2 is not toggle in this mode.

Figure 12-4. Timer 2 Diagram: Auto-reload Mode ($T2CM_{1-0}$ = 00B, DCEN = 1)

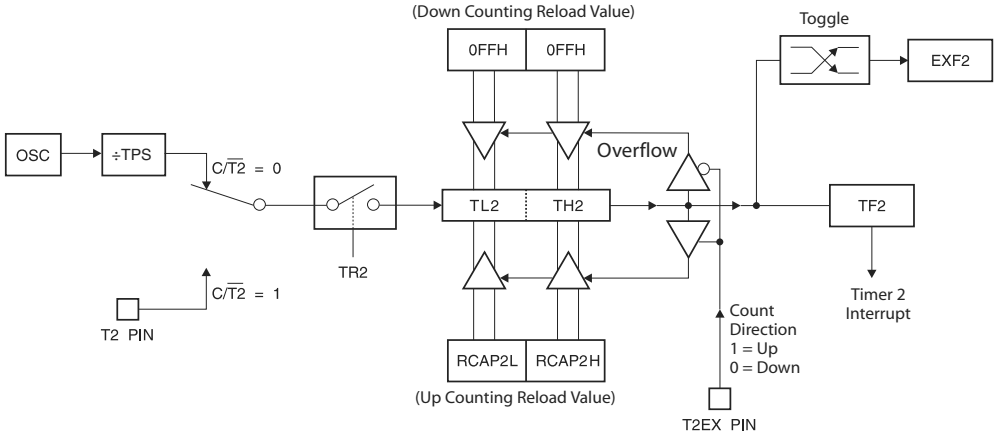


Table 13-1. T2CCA – Timer/Counter 2 Compare/Capture Address

T2CCA Address = 0D1H — Reset Value = xxxx xx00B

Not Bit Addressable

	–	–	–	–	–	–	T2CCA.1	T2CCA.0
Bit	7	6	5	4	3	2	1	0

Symbol	Function		
T2CCA [1 - 0]	Compare/Capture Address. Selects which CCA channel is currently accessible through the T2CCH, T2CCL and T2CCC registers. Only one channel may be accessed at a time.		
	T2CCA1	**T2CCA0**	**Channel**
	0	0	A – T2CCH, T2CCL and T2CCC access data and control for Channel A
	0	1	B – T2CCH, T2CCL and T2CCC access data and control for Channel B
	1	0	C – T2CCH, T2CCL and T2CCC access data and control for Channel C
	1	1	D – T2CCH, T2CCL and T2CCC access data and control for Channel D

Table 13-2. T2CCH – Timer/Counter 2 Compare/Capture Data High

T2CCH Address = 0D2H — Reset Value = 0000 0000B

Not Bit Addressable

	T2CCD.15	T2CCD.14	T2CCD.13	T2CCD.12	T2CCD.11	T2CCD.10	T2CCD.9	T2CCD.8
Bit	7	6	5	4	3	2	1	0

Symbol	Function
T2CCD [15 - 8]	Compare/Capture Data (High Byte). Reads from T2CCH will return the high byte from the CCA channel currently selected by T2CCA. The high byte of the selected CCA channel will be updated with the contents of T2CCH when T2CCL is written. When writing multiple channels with the same high byte, T2CCH need not be updated between writes to T2CCL.

Note: All writes/reads to/from T2CCH will access channel *X* as currently selected by T2CCA.The data registers for the remaining unselected channels are not accessible.

Table 13-3. T2CCL – Timer/Counter 2 Compare/Capture Data Low

T2CCC Address = 0D3H — Reset Value = 0000 0000B

Not Bit Addressable

	T2CCD.7	T2CCD.6	T2CCD.5	T2CCD.4	T2CCD.3	T2CCD.2	T2CCD.1	T2CCD.0
Bit	7	6	5	4	3	2	1	0

Symbol	Function
T2CCD [7 - 0]	Compare/Capture Data (Low Byte). Reads from T2CCL will return the low byte from the CCA channel currently selected by T2CCA. Writes to T2CCL will update the selected CCA channel with the 16-bit contents of T2CCH and T2CCL.

Note: All writes/reads to/from T2CCL will access channel *X* as currently selected by T2CCA.The data registers for the remaining unselected channels are not accessible.

Figure 15-1. GPI Block Diagram

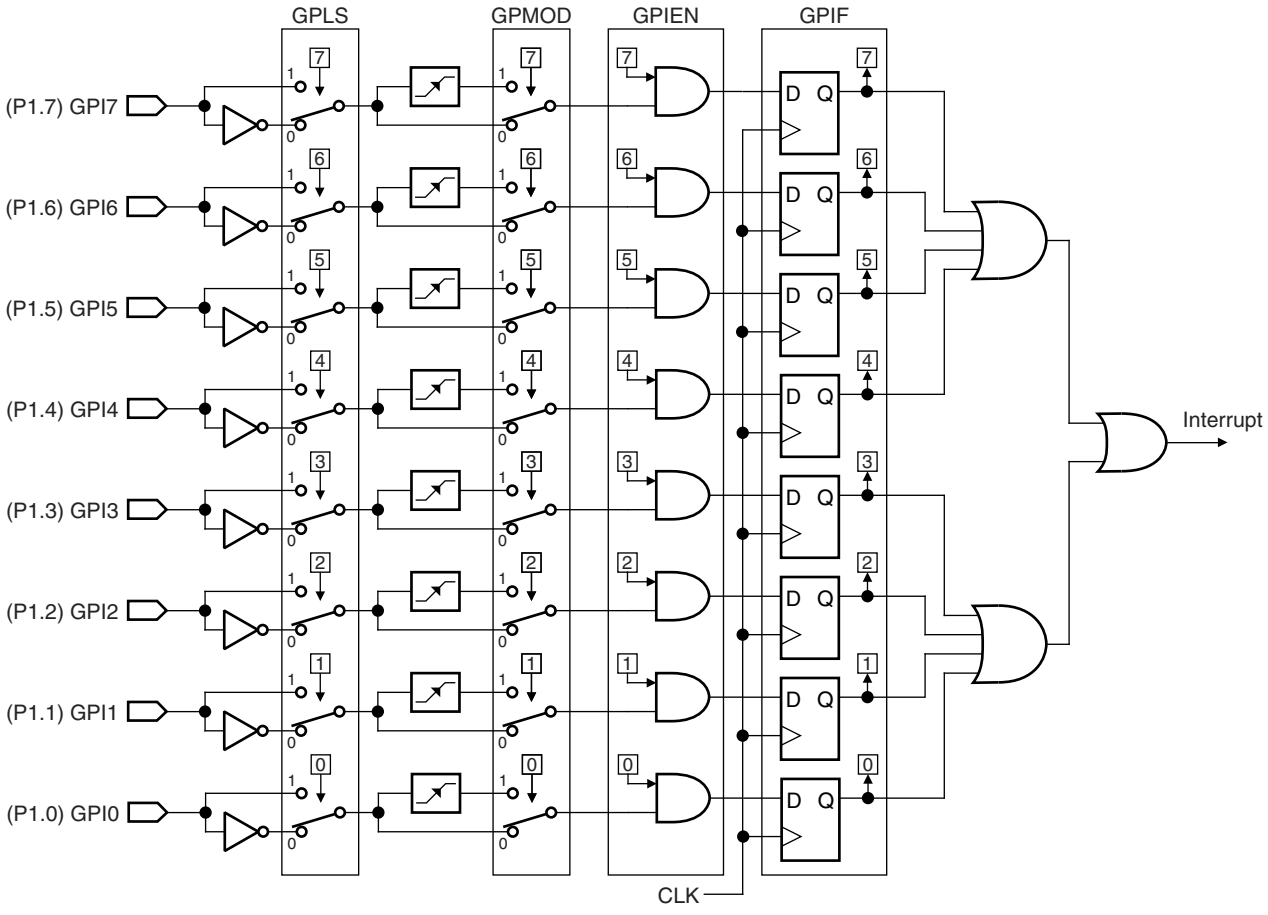


Table 15-1. GPMOD – General-purpose Interrupt Mode Register

GPMOD = 9AH — Reset Value = 0000 0000B

Not Bit Addressable

	GPMOD7	GPMOD6	GPMOD5	GPMOD4	GPMOD3	GPMOD2	GPMOD1	GPMOD0
Bit	7	6	5	4	3	2	1	0

GPMOD.x 0 = level-sensitive interrupt for P1.x

1 = edge-triggered interrupt for P1.x

In a more complex system, the following could be used to select slaves 1 and 2 while excluding slave 0:

Slave 0
SADDR = 1100 0000
SADEN = 1111 1001
Given = 1100 0XX0

Slave 1
SADDR = 1110 0000
SADEN = 1111 1010
Given = 1110 0X0X

Slave 2
SADDR = 1110 0000
SADEN = 1111 1100
Given = 1110 00XX

In the above example, the differentiation among the 3 slaves is in the lower 3 address bits. Slave 0 requires that bit 0 = 0 and it can be uniquely addressed by 1110 0110. Slave 1 requires that bit 1 = 0 and it can be uniquely addressed by 1110 and 0101. Slave 2 requires that bit 2 = 0 and its unique address is 1110 0011. To select Slaves 0 and 1 and exclude Slave 2, use address 1110 0100, since it is necessary to make bit 2 = 1 to exclude slave 2.

The Broadcast Address for each slave is created by taking the logic OR of SADDR and SADEN. Zeros in this result are treated as don't cares. In most cases, interpreting the don't cares as ones, the broadcast address will be FF hexadecimal.

Upon reset SADDR (SFR address 0A9H) and SADEN (SFR address 0B9H) are loaded with "0"s. This produces a given address of all "don't cares" as well as a Broadcast address of all "don't cares". This effectively disables the Automatic Addressing mode and allows the microcontroller to use standard 80C51-type UART drivers which do not make use of this feature.

17. Enhanced Serial Peripheral Interface

The Serial Peripheral Interface (SPI) allows high-speed synchronous data transfer between the AT89LP428/828 and peripheral devices or between multiple AT89LP428/828 devices, including multiple masters and slaves on a single bus. The SPI includes the following features:

- Full-duplex, 3-wire or 4-wire Synchronous Data Transfer
- Master or Slave Operation
- Maximum Bit Frequency = $f_{OSC}/4$
- LSB First or MSB First Data Transfer
- Four Programmable Bit Rates or Timer 1-based Baud Generation (Master Mode)
- End of Transmission Interrupt Flag
- Write Collision Flag Protection
- Double-buffered Receive and Transmit
- Transmit Buffer Empty Interrupt Flag
- Mode Fault (Master Collision) Detection and Interrupt
- Wake up from Idle Mode

A block diagram of the SPI is shown in Figure 17-1.

Table 18-3. AREF – Analog Comparator Reference Control Register

AREF = AFH — Reset Value = 0000 0000B

Not Bit Addressable

	CBC1	CBC0	RFB1	RFB0	CAC1	CAC0	RFA1	RFA0
Bit	7	6	5	4	3	2	1	0

Symbol	Function		
CSC [1 - 0]	Comparator B Clock Select		
	CBC1	**CBC0**	**Clock Source**
	0	0	System Clock
	0	0	Timer 0 Overflow
	0	1	Timer 1 Overflow
	0	1	Timer 2 Overflow
RFB [1 - 0]	Comparator B Negative Input Channel Select(1)		
	CRF1	**RFB0**	**B-channel**
	0	0	AIN2 (P2.6)
	0	0	Internal $V_{AREF-\Delta}$ (~1.2V)
	0	1	Internal V_{AREF} (~1.3V)
	0	1	Internal $V_{AREF+\Delta}$ (~1.4V)
CAC [1 - 0]	Comparator A Clock Select		
	CAC1	**CAC0**	**Clock Source**
	0	0	System Clock
	0	0	Timer 0 Overflow
	0	1	Timer 1 Overflow
	0	1	Timer 2 Overflow
RFB [1 - 0]	Comparator A Negative Input Channel Select(2)		
	RFA1	**RFA0**	**A-channel**
	0	0	AIN1 (P2.5)
	0	0	Internal $V_{AREF-\Delta}$ (~1.2V)
	0	1	Internal V_{AREF} (~1.3V)
	0	1	Internal $V_{AREF+\Delta}$ (~1.4V)

Notes: 1. CONB (ACSRB.5) must be cleared to 0 before changing RFB [1 - 0].
2. CONA (ACSRA.5) must be cleared to 0 before changing RFA [1 - 0].

20. Instruction Set Summary

The AT89LP428/828 is fully binary compatible with the MCS-51 instruction set. The difference between the AT89LP428/828 and the standard 8051 is the number of cycles required to execute an instruction. Instructions in the AT89LP428/828 may take 1, 2, 3, 4 or 5 clock cycles to complete. The execution times of most instructions may be computed using Table 20-1 on page 107.

Table 20-1. Instruction Execution Times and Exceptions

Generic Instruction Types	Cycle Count Formula
Most arithmetic, logical, bit and transfer instructions	# bytes
Branches and Calls	# bytes + 1
Single Byte Indirect (i.e. ADD A, @Ri, etc.)	2
RET, RETI	4
MOVC	3
MOVX	2/4[2]
MUL	2
DIV	4
INC DPTR	2

		Clock Cycles		
Arithmetic	**Bytes**	**8051**	**AT89LP**	**Hex Code**
ADD A, Rn	1	12	1	28 - 2F
ADD A, direct	2	12	2	25
ADD A, @Ri	1	12	2	26 - 27
ADD A, #data	2	12	2	24
ADDC A, Rn	1	12	1	38 - 3F
ADDC A, direct	2	12	2	35
ADDC A, @Ri	1	12	2	36 - 37
ADDC A, #data	2	12	2	34
SUBB A, Rn	1	12	1	98 - 9F
SUBB A, direct	2	12	2	95
SUBB A, @Ri	1	12	2	96 - 97
SUBB A, #data	2	12	2	94
INC Rn	1	12	1	08 - 0F
INC direct	2	12	2	05
INC @Ri	1	12	2	06 - 07
INC A	2	12	2	04
DEC Rn	1	12	1	18 - 1F
DEC direct	2	12	2	15
DEC @Ri	1	12	2	16 - 17
DEC A	2	12	2	14
INC DPTR	1	24	2	A3
INC /DPTR[1]	2	–	3	A5 A3

22. On-chip Debug System

The AT89LP428/828 On-chip Debug (OCD) System uses a 2-wire serial interface to control program flow; read, modify, and write the system state; and program the nonvolatile memory. The OCD System has the following features:

- Complete program flow control
- Read-modify-write access to all internal SFRs and data memories
- Four hardware program address breakpoints
- Unlimited program software breakpoints using BREAK instruction
- Break on change in program memory flow
- Break on stack overflow/underflow
- Break on Watchdog overflow
- Break on reset
- Non-intrusive operation
- Programming of nonvolatile memory

22.1 Physical Interface

The On-chip Debug System uses a 2-wire synchronous serial interface to establish communication between the target device and the controlling emulator system. The OCD interface is controlled by two User Fuses. OCD is enabled by clearing the OCD $\overline{\text{Enable}}$ Fuse. The OCD device connections are shown in Figure 22-1. When OCD is enabled, the $\overline{\text{RST}}$ port pin is configured as an input for the Debug Clock (DCL). Either the XTAL1, XTAL2 or P3.7 pin is configured as a bi-directional data line for the Debug Data (DDA) depending on the clock source selected. If the Internal RC Oscillator is selected, XTAL1 is configured as DDA (A). If the External Clock is selected, XTAL2 is configured as DDA (B). If the Crystal Oscillator is selected, P3.7 is configured as DDA (C). When OCD is enabled, the type of interface used depends on the OCD Interface Select User Fuse. This fuse selects between a normal Two-wire Interface (TWI) and a fast Two-wire Interface (FTWI). It is the duty of the user to program this fuse to the correct setting for their debug system at the same time they enable OCD (see “User Configuration Fuses” on page 121).

When designing a system where On-chip Debug will be used, the following observations must be considered for correct operation:

- P3.6/$\overline{\text{RST}}$ cannot be connected directly to V_{CC} and any external capacitors connected to $\overline{\text{RST}}$ must be removed.
- All external reset sources must be removed.
- If P3.7 needs to be debugged in-system using the crystal oscillator, the external clock option should be selected. The quartz crystal and any capacitors on XTAL1 or XTAL2 must be removed and an external clock signal must be driven on XTAL1. Some emulator systems may provide a user-configurable clock for this purpose.

23. Programming the Flash Memory

The Atmel AT89LP428/828 microcontroller features 4K/8K bytes of on-chip In-System Programmable Flash program memory and 512/1024 bytes of nonvolatile Flash data memory. In-System Programming allows programming and reprogramming of the microcontroller positioned inside the end system. Using a simple 4-wire SPI interface, the programmer communicates serially with the AT89LP428/828 microcontroller, reprogramming all nonvolatile memories on the chip. In-System Programming eliminates the need for physical removal of the chips from the system. This will save time and money, both during development in the lab, and when updating the software or parameters in the field. The programming interface of the AT89LP428/828 includes the following features:

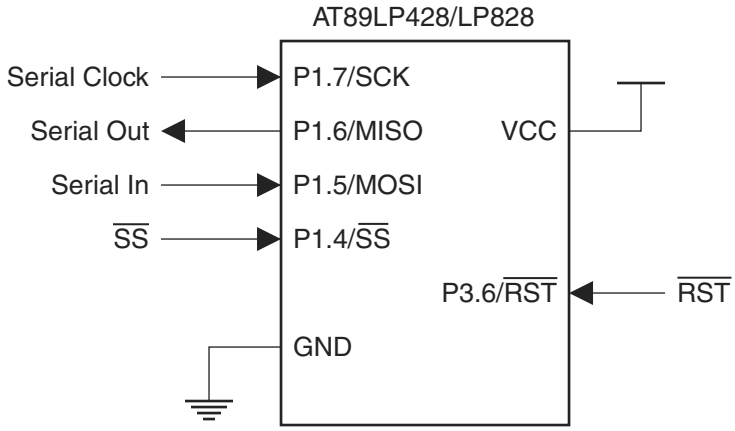
- 4-wire SPI Programming Interface
- Active-low Reset Entry into Programming
- Slave Select Allows Multiple Devices on Same Interface
- User Signature Array
- Flexible Page Programming
- Row Erase Capability
- Page Write with Auto-Erase Commands
- Programming Status Register

For more detailed information on In-System Programming, refer to the Application Note entitled “AT89LP In-System Programming Specification”.

23.1 Physical Interface

Flash Programming utilizes the Serial Peripheral Interface (SPI) pins of an AT89LP428/828 microcontroller. The SPI is a full-duplex synchronous serial interface consisting of four wires: Serial Clock (SCK), Master-in/Slave-out (MISO), Master-out/Slave-in (MOSI), and an active-low Slave Select ($\overline{SS}$). When programming an AT89LP428/828 device, the programmer always operates as the SPI master, and the target system always operates as the SPI slave. To enter or remain in Programming mode the device’s reset line ($\overline{RST}$) must be held active (low). With the addition of VCC and GND, an AT89LP428/828 microcontroller can be programmed with a minimum of seven connections as shown in Figure 23-1.

Figure 23-1. In-System Programming Device Connections



24. Electrical Characteristics

24.1 Absolute Maximum Ratings*

Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-0.7V to +5.5V
Maximum Operating Voltage	5.5V
DC Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

24.2 DC Characteristics

T_A = -40°C to 85°C, V_{CC} = 2.4V to 5.5V (unless otherwise noted)

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low-voltage		-0.5	0.3 V_{CC}	V
V_{IH}	Input High-voltage		0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low-voltage(1)	I_{OL} = 8 mA, V_{CC} = 5V ±10%		0.4	V
		I_{OL} = 4 mA		0.4	
V_{OH}	Output High-voltage With Weak Pull-ups Enabled	I_{OH} = -100 µA, V_{CC} = 5V ±10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
V_{OH1}	Output High-voltage With Strong Pull-ups Enabled	I_{OH} = -20 mA, V_{CC} = 5V ±10%	0.75 V_{CC}		
		I_{OH} = -8 mA, V_{CC} = 5V ±10%	0.9 V_{CC}		
		I_{OH} = -6 mA	0.75 V_{CC}		
		I_{OH} = -2 mA	0.9 V_{CC}		
I_{IL}	Logic 0 Input Current	V_{IN} = 0.45V		-100	µA
I_{TL}	Logic 1 to 0 Transition Current	V_{IN} = 2.7V, V_{CC} = 5V ±10%		-300	µA
I_{LI}	Input Leakage Current	0 < V_{IN} < V_{CC}		±10	µA
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I_{CC}	Power Supply Current	Active Mode, 12 MHz, V_{CC} = 5V/3V		10/6	mA
		Idle Mode, 12 MHz, V_{CC} = 5V/3V		5/3	mA
	Power-down Mode(2)	V_{CC} = 5V		5	µA
		V_{CC} = 3V		2	µA

Notes: 1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 10 mA
Maximum total I_{OL} for all output pins: 15 mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

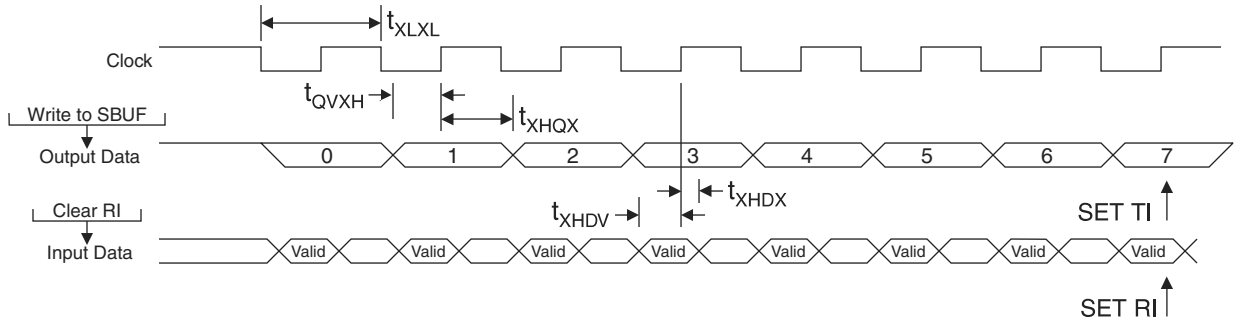
2. Minimum V_{CC} for Power-down is 2V.

24.8 Serial Port Timing: Shift Register Mode

The values in this table are valid for V_{CC} = 2.4V to 5.5V and Load Capacitance = 80 pF.

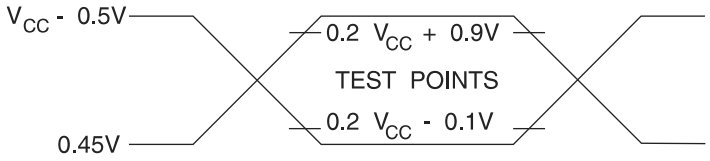
Symbol	Parameter	Variable Oscillator		Units
		Min	Max	
t_{XLXL}	Serial Port Clock Cycle Time	$2t_{CLCL}$ -15		µs
t_{QVXH}	Output Data Setup to Clock Rising Edge	t_{CLCL} -15		ns
t_{XHQX}	Output Data Hold after Clock Rising Edge	t_{CLCL} -15		ns
t_{XHDX}	Input Data Hold after Clock Rising Edge	0		ns
t_{XHDV}	Input Data Valid to Clock Rising Edge	15		ns

Figure 24-15. Shift Register Mode Timing Waveform



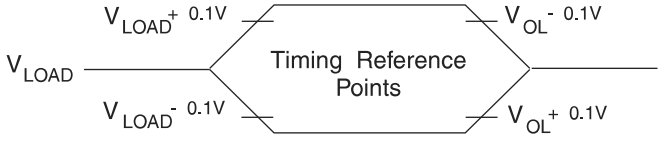
24.9 Test Conditions

24.9.1 AC Testing Input/Output Waveform(1)



Note: 1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic “1” and 0.45V for a logic “0”. Timing measurements are made at V_{IH} min. for a logic “1” and V_{IL} max. for a logic “0”.

24.9.2 Float Waveform(1)



Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

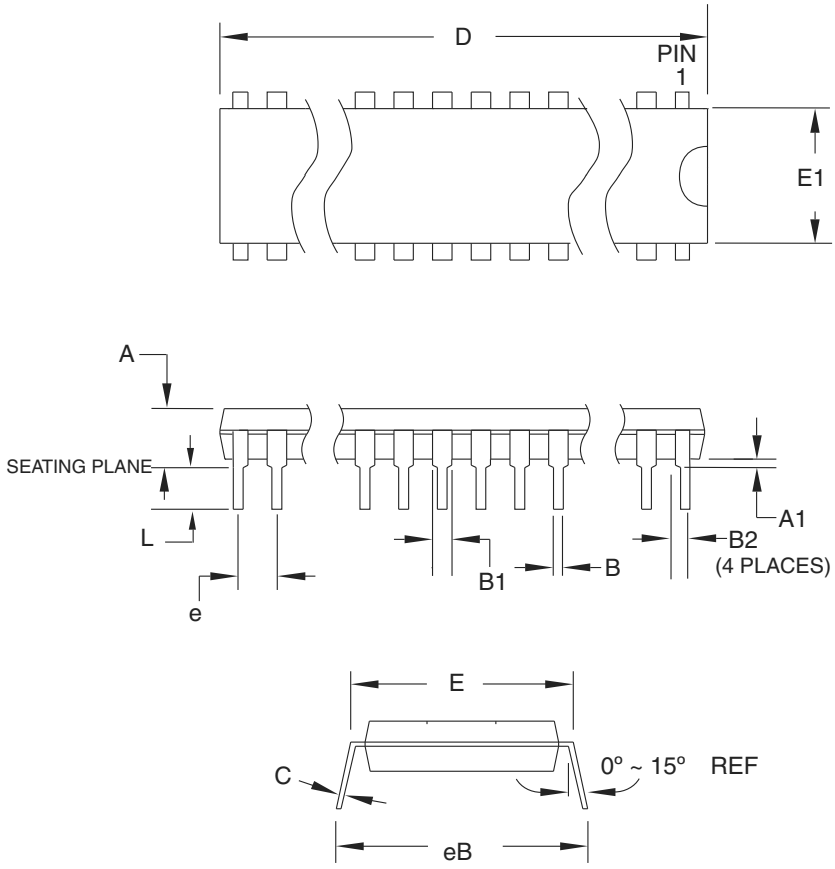
25. Ordering Information

25.1 Green Package (Pb/Halide-free)

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
20	2.4V to 5.5V	AT89LP428-20AU AT89LP428-20PU AT89LP428-20JU AT89LP428-20MU	32A 28P3 32J 32M1-A	Industrial (-40°C to 85°C)
		AT89LP828-20AU AT89LP828-20PU AT89LP828-20JU AT89LP828-20MU		
25	4.0V to 5.5V	AT89LP428-25AU AT89LP428-25PU AT89LP428-25JU AT89LP428-25MU	32A 28P3 32J 32M1-A	Industrial (-40°C to 85°C)
		AT89LP828-25AU AT89LP828-25PU AT89LP828-25JU AT89LP828-25MU		

Package Types	
32A	32-lead, Thin Plastic Quad Flat Package (TQFP)
28P3	28-lead, 0.300” Wide, Plastic Dual Inline Package (PDIP)
32J	32-lead, Plastic J-leaded Chip Carrier (PLCC)
32M1-A	32-pad, 5 x 5 x1.0 mm Body, Lead Pitch 0.5 mm, Micro Lead Frame Package (MLF)

26.2 28P3 – PDIP



COMMON DIMENSIONS
(Unit of Measure = mm)

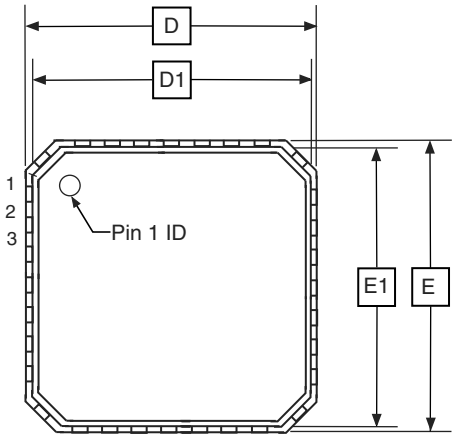
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	4.5724	
A1	0.254	–	–	
D	35.00	–	35.51	Note 1
E	7.366	–	8.382	
E1	7.112	–	7.518	Note 1
B	0.356	–	0.559	
B1	1.143	–	1.78	
B2	0.762	–	1.143	
L	2.921	–	3.81	
C	0.203	–	0.356	
eB	–	–	10.160	
e	2.540 TYP			

Note: 1. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

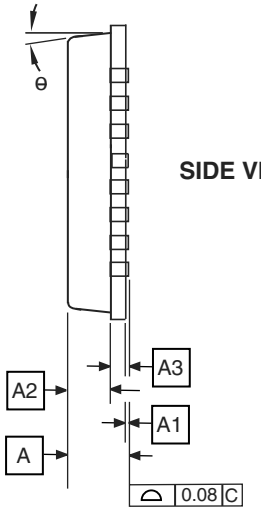
05/18/04

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**28P3**, 28-lead (0.300"/7.62 mm Wide) Plastic Dual Inline Package (PDIP)	28P3	C

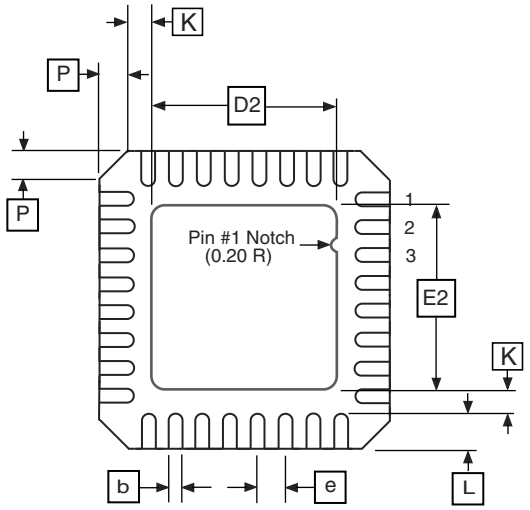
26.4 32M1-A – MLF



TOP VIEW



SIDE VIEW



BOTTOM VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	–	0.02	0.05	
A2	–	0.65	1.00	
A3		0.20 REF		
b	0.18	0.23	0.30	
D	4.90	5.00	5.10	
D1	4.70	4.75	4.80	
D2	2.95	3.10	3.25	
E	4.90	5.00	5.10	
E1	4.70	4.75	4.80	
E2	2.95	3.10	3.25	
e		0.50 BSC		
L	0.30	0.40	0.50	
P	–	–	0.60	
θ	–	–	12^{o}	
K	0.20	–	–	

Note: JEDEC Standard MO-220, Fig. 2 (Anvil Singulation), VHHD-2.

5/25/06

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**32M1-A**, 32-pad, 5 x 5 x 1.0 mm Body, Lead Pitch 0.50 mm, 3.10 mm Exposed Pad, Micro Lead Frame Package (MLF)	32M1-A	E