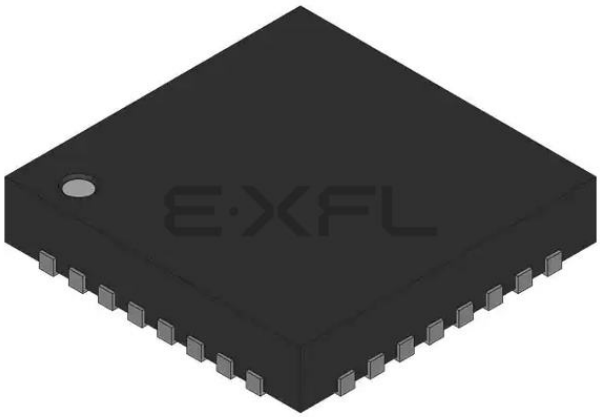

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Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	20MHz
Connectivity	SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	30
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-VQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/atmel/at89lp828-20mh

Table 1-1. AT89LP428/828 Pin Description (Continued)

Pin Number			Symbol	Type	Description
TQFP /MLF	PLCC	PDIP			
17	21	19	P1.1	I/O I I	P1.1: User-configurable I/O Port 1 bit 1. T2EX: Timer 2 External Capture/Reload Input. GPI1: General-purpose Interrupt input 1.
18	22	20	P1.2	I/O I	P1.2: User-configurable I/O Port 1 bit 2. GPI2: General-purpose Interrupt input 2.
19	23	N/A	P4.3	I/O	P4.3: User-configurable I/O Port 4 bit 3.
20	24	21	VCC	I	Supply Voltage.
21	25	N/A	P4.2	I/O	P4.2: User-configurable I/O Port 4 bit 2.
22	26	22	P1.3	I/O I	P1.3: User-configurable I/O Port 1 bit 3. GPI3: General-purpose Interrupt input 3.
23	27	23	P1.4	I/O I I	P1.4: User-configurable I/O Port 1 bit 4. $\overline{SS}$: SPI Slave-select. GPI6: General-purpose Interrupt input 4.
24	28	24	P1.5	I/O I/O I	P1.5: User-configurable I/O Port 1 bit 5. MOSI: SPI master-out/slave-in. When configured as master, this pin is an output. When configured as slave, this pin is an input. GPI5: General-purpose Interrupt input 5.
25	29	25	P1.6	I/O I/O I	P1.6: User-configurable I/O Port 1 bit 6. MISO: SPI master-in/slave-out. When configured as master, this pin is an input. When configured as slave, this pin is an output. GPI6: General-purpose Interrupt input 6.
26	30	26	P1.7	I/O I/O I	P1.7: User-configurable I/O Port 1 bit 7. SCK: SPI Clock. When configured as master, this pin is an output. When configured as slave, this pin is an input. GPI7: General-purpose Interrupt input 7.
27	31	27	P2.6	I/O I	P2.6: User-configurable I/O Port 2 bit 6. AIN2: Analog Input 2.
28	32	28	P2.7	I/O I	P2.7: User-configurable I/O Port 2 bit 7. AIN3: Analog Input 3.
29	1	1	P2.5	I/O I	P2.5: User-configurable I/O Port 2 bit 5. AIN1: Analog Input 1.
30	2	2	P2.4	I/O I	P2.4: User-configurable I/O Port 2 bit 5. AIN0: Analog Input 0.
31	3	3	P3.0	I/O I	P3.0: User-configurable I/O Port 3 bit 0. RXD: Serial Port Receiver Input.
32	4	4	P3.1	I/O O	P3.1: User-configurable I/O Port 3 bit 1. TXD: Serial Port Transmitter Output.

2.2.6 Serial Port

The baud rate of the UART in Mode 0 defaults to 1/4 the clock frequency, compared to 1/12 the clock frequency in the standard 8051. In should also be noted that when using Timer 1 to generate the baud rate in UART Modes 1 or 3, the timer counts at the clock frequency and not at 1/12 the clock frequency. To maintain the same baud rate in the AT89LP428/828 while running at the same frequency as a standard 8051, the time-out period must be 12 times longer. Mode 1 of Timer 1 supports 16-bit auto-reload to facilitate longer time-out periods for generating low baud rates. Timer 2 generated baud rates are twice as fast in the AT89LP428/828 than on standard 8051s when operating at the same frequency.

2.2.7 Watchdog Timer

The Watchdog Timer in AT89LP428/828 counts at a rate of once per clock cycle. This compares to once every 12 clocks in the standard 8051. A common prescaler is available to divide the time base for all timers and reduce the counting rate.

2.2.8 I/O Ports

The I/O ports of the AT89LP428/828 may be configured in four different modes. By default all the I/O ports revert to input-only (tristated) mode at power-up or reset. In the standard 8051, all ports are weakly pulled high during power-up or reset. To enable 8051-like ports, the ports must be put into quasi-bidirectional mode by clearing the P1M0, P2M0, P3M0 and P4M0 SFRs. The user can also configure the ports to start in quasi-bidirectional mode by disabling the Tristate-Port User Fuse. When this fuse is disabled, P1M0, P2M0, P3M0 and P4M0 will reset to 00H instead of FFH and the ports will be weakly pulled high.

3. Memory Organization

The AT89LP428/828 uses a Harvard Architecture with separate address spaces for program and data memory. The program memory has a regular linear address space with support for up to 64K bytes of directly addressable application code. The data memory has 256 bytes of internal RAM and 128 bytes of Special Function Register I/O space. The AT89LP428/828 does not support external data memory or external program memory; however, portions of the external data memory space are implemented on chip as Extra RAM and nonvolatile Flash data memory. The memory address spaces of the AT89LP428 and AT89LP828 are listed in Tables 3-1 and 3-2.

Table 3-1. AT89LP428 Memory Address Spaces

Name	Description	Range
DATA	Directly addressable internal RAM	00H - 7FH
IDATA	Indirectly addressable internal RAM and stack space	00H - FFH
SFR	Directly addressable I/O register space	80H - FFH
EDATA	On-chip Extra RAM	0000H - 01FFH
FDATA	On-chip nonvolatile Flash data memory	0200H - 03FFH
CODE	On-chip nonvolatile Flash program memory	0000H - 0FFFH
SIG	On-chip nonvolatile Flash signature array	0000H - 00FFH

3.3.2 FDATA

The Flash data memory is a portion of the external memory space implemented as an internal nonvolatile data memory. Flash data memory is enabled by setting the DMEN bit (MEMCON.3) to one. When IAP = 0 and DMEN = 1, the Flash data memory is mapped into the FDATA space, directly above the EDATA space near the bottom of the external memory address space. (Addresses 0200H–03FFH on AT89LP428 and 0200H–05FFH on AT89LP828. See Figure 3-3 on page 11). MOVX instructions to this address range will access the internal nonvolatile memory. FDATA is not accessible while DMEN = 0. FDATA can be accessed only by 16-bit (MOVX @DPTR) addresses. Addresses above the FDATA range are not implemented and should not be accessed. MOVX instructions to FDATA require a minimum of 4 clock cycles.

3.3.2.1 Write Protocol

The FDATA address space accesses an internal nonvolatile data memory. This address space can be read just like EDATA by issuing a MOVX A,@DPTR; however, writes to FDATA require a more complex protocol and take several milliseconds to complete. The AT89LP428/828 uses an *idle-while-write* architecture where the CPU is placed in an idle state while the write occurs. When the write completes, the CPU will continue executing with the instruction after the MOVX @DPTR,A instruction that started the write. All peripherals will continue to function during the write cycle; however, interrupts will not be serviced until the write completes.

To enable write access to the nonvolatile data memory, the MWEN bit (MEMCON.4) must be set to one. When MWEN = 1 and DMEN = 1, MOVX @DPTR,A may be used to write to FDATA. FDATA uses Flash memory with a page-based programming model. Flash data memory differs from traditional EEPROM data memory in the method of writing data. EEPROM generally can update a single byte with any value. Flash memory splits programming into write and erase operations. A Flash write can only program zeroes, i.e change ones into zeroes ($1 \rightarrow 0$). Any ones in the write data are ignored. A Flash erase sets an entire page of data to ones so that all bytes become FFH. Therefore after an erase, each byte in the page can be written once with any possible value. Bytes can be overwritten without an erase as long as only ones are changed into zeroes. However, if even a single bit needs updating from zero to one ($0 \rightarrow 1$); then the contents of the page must first be saved, the entire page must be erased and the zero bits in all bytes (old and new data combined) must be written. Avoiding unnecessary page erases greatly improves the endurance of the memory.

The AT89LP428/828 includes 8/16 data pages of 64 bytes each. One or more bytes in a page may be written at one time. The AT89LP428/828 includes a temporary page buffer of 64 bytes, so the maximum number of bytes written at one time is 64. The LDPG bit (MEMCON.5) allows multiple data bytes to be loaded to the temporary page buffer. While LDPG = 1, MOVX @DPTR,A instructions will load data to the page buffer, but will not start a write sequence. Note that a previously loaded byte must not be reloaded prior to the write sequence. To write the page into the memory, LDPG must first be cleared and then a MOVX @DPTR,A with the final data byte is issued. The address of the final MOVX determines which page will be written. If a MOVX @DPTR,A instruction is issued while LDPG = 0 without loading any previous bytes, only a single byte will be written. The page buffer is reset after each write operation. Figures 3-4 and 3-5 show the difference between byte writes and page writes.

9.1 Interrupt Response Time

The interrupt flags may be set by their hardware in any clock cycle. The interrupt controller polls the flags in the last clock cycle of the instruction in progress. If one of the flags was set in the preceding cycle, the polling cycle will find it and the interrupt system will generate an LCALL to the appropriate service routine as the next instruction, provided that the interrupt is not blocked by any of the following conditions: an interrupt of equal or higher priority level is already in progress; the instruction in progress is RETI or any write to the IE, IP, IPH, IE2, IP2 or IP2H registers; the CPU is currently forced into idle by an IAP or FDATA write. Each of these conditions will block the generation of the LCALL to the interrupt service routine. The second condition ensures that if the instruction in progress is RETI or any access to IE, IP, IPH, IE2, IP2 or IP2H, then at least one more instruction will be executed before any interrupt is vectored to. The polling cycle is repeated at the last cycle of each instruction, and the values polled are the values that were present at the previous clock cycle. If an active interrupt flag is not being serviced because of one of the above conditions and is no longer active when the blocking condition is removed, the denied interrupt will not be serviced. In other words, the fact that the interrupt flag was once active but not serviced is not remembered. Every polling cycle is new.

If a request is active and conditions are met for it to be acknowledged, a hardware subroutine call to the requested service routine will be the next instruction executed. The call itself takes four cycles. Thus, a minimum of five complete clock cycles elapsed between activation of an interrupt request and the beginning of execution of the first instruction of the service routine. A longer response time results if the request is blocked by one of the previously listed conditions. If an interrupt of equal or higher priority level is already in progress, the additional wait time depends on the nature of the other interrupt's service routine. If the instruction in progress is not in its final clock cycle, the additional wait time cannot be more than 4 cycles, since the longest are only 5 cycles long. If the instruction in progress is RETI or an access to IE or IP, the additional wait time cannot be more than 9 cycles (a maximum of four more cycles to complete the instruction in progress, plus a maximum of 5 cycles to complete the next instruction). Thus, in a single-interrupt system, the response time is always more than 5 clock cycles and less than 14 clock cycles. See Figure 9-1 and Figure 9-2.

Figure 9-1. Minimum Interrupt Response Time

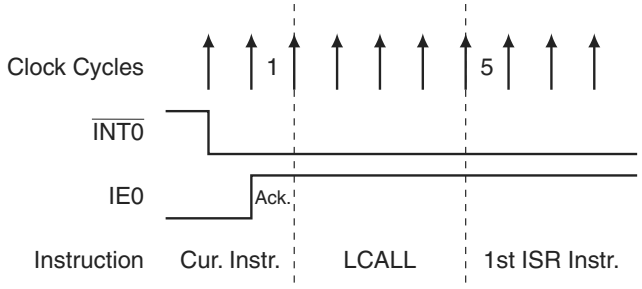


Figure 9-2. Maximum Interrupt Response Time

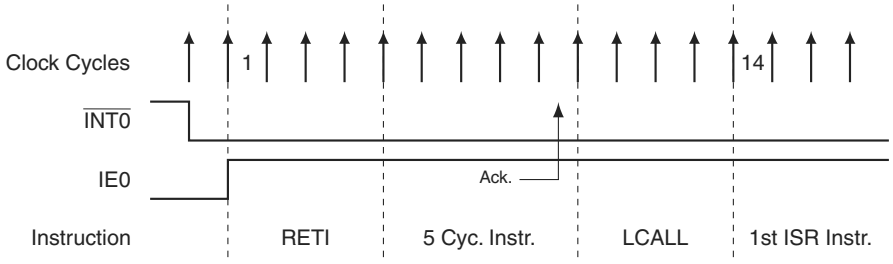


Table 9-4. IPH – Interrupt Priority High Register

IPH = B7H — Reset Value = 0000 0000B

Not Bit Addressable

	IP1D	PCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H
Bit	7	6	5	4	3	2	1	0

Symbol	Function
IP1D	Interrupt Priority 1 Disable. Set IP1D to 1 to disable all interrupts with priority level one. Clear to 0 to enable all interrupts with priority level one when EA = 1.
PCH	Comparator Interrupt Priority High
PT2H	Timer 2 Interrupt Priority High
PSH	Serial Port Interrupt Priority High
PT1H	Timer 1 Interrupt Priority High
PX1H	External Interrupt 1 Priority High
PT0H	Timer 0 Interrupt Priority High
PX0H	External Interrupt 0 Priority High

Table 9-5. IE2 – Interrupt Enable 2 Register

IE = B4H — Reset Value = xxxx x000B

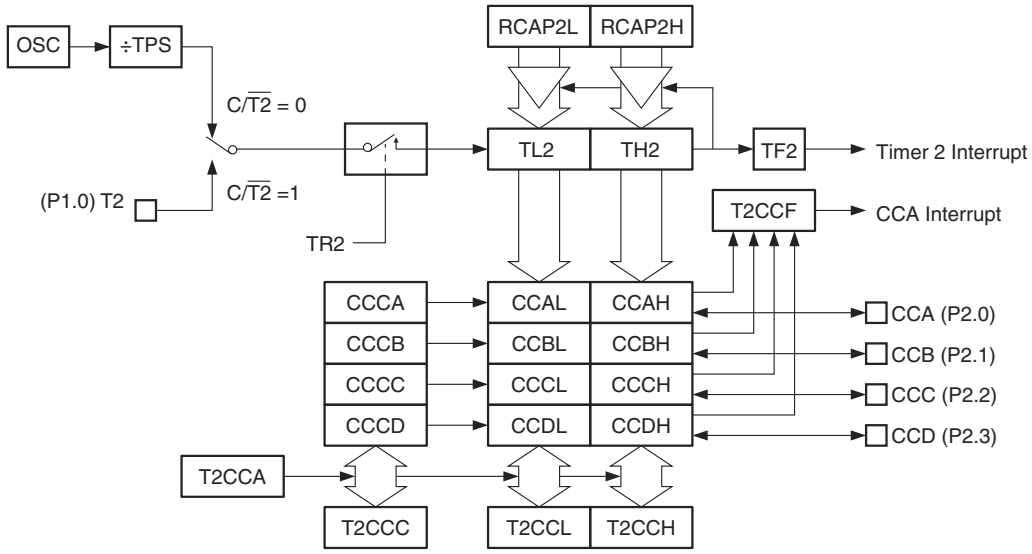
Not Bit Addressable

	–	–	–	–	–	ESP	ECC	EGP
Bit	7	6	5	4	3	2	1	0

Symbol	Function
ESP	Serial Peripheral Interface Interrupt Enable
ECC	Compare/Capture Array Interrupt Enable
EGP	General-purpose Interrupt Enable

Timer 2 must be running (TR2 = 1) in order to perform captures or compares with the CCA. However, when TR2 = 0 the external capture events will still set their associated flags and may be used as additional external interrupts.

Figure 13-1. Compare/Capture Array Block Diagram



13.1 CCA Registers

The Compare/Capture Array has five Special Function Registers: T2CCA, T2CCC, T2CCL, T2CCH and T2CCF. The T2CCF register contains the interrupt flags for each CCA channel. The CCA interrupt is a logic OR of the bits in T2CCF. The flags are set by hardware when a compare/capture event occurs on the relevant channel and must be cleared by software. The T2CCF bits will only generate an interrupt when the ECC bit (IE2.1) is set and the CIEN*x* bit in the associated channel's CCC*x* register is set.

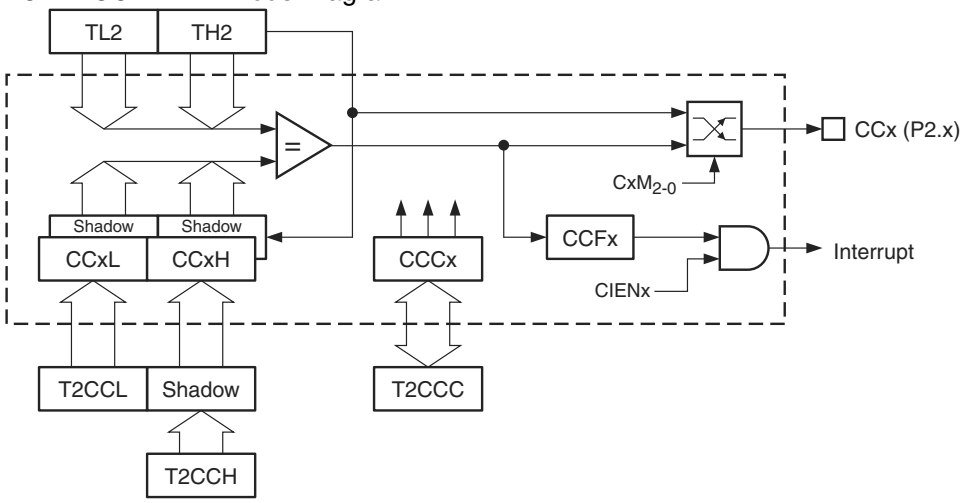
The T2CCC, T2CCL and T2CCH register locations are not true SFRs. These locations represent access points to the contents of the array. Writes/reads to/from the T2CCC, T2CCL and T2CCH locations will access the control, data low and data high bytes of the CCA channel currently selected by the index in T2CCA. Channels currently not indexed by T2CCA are not accessible.

When writing to T2CCH, the value is stored in a shadow register. When T2CCL is written, the 16-bit value formed by the contents of T2CCL and the T2CCH shadow is written into the array. Therefore, T2CCH must be written prior to writing T2CCL. All four channels use the same T2CCH shadow register. If the value of T2CCH remains constant for multiple writes, there is no need to update T2CCH between T2CCL writes. Every write to T2CCL will use the last value of T2CCH for the upper data byte. It is not possible to write to the data register of a channel configured for capture mode.

The configuration bits for each channel are stored in the CCC*x* registers accessible through T2CCC. See Table 13-4 on page 64 for a description of the CCC*x* register.

and precision is made by changing the TOP value of the timer. The CCA PWM always uses the greatest precision allowable for the selected output frequency, as compared to Timer 0 and 1 whose PWMs are fixed at 8-bit precision regardless of frequency.

Figure 13-7. CCA PWM Mode Diagram



13.4.1 Asymmetrical PWM

For Asymmetrical PWM, Timer 2 should be configured for Auto-reload mode and Count Mode 1 (CP/$\overline{RL2}$ = 0, DCEN = 0, T2CM$\overline{1\text{-}0}$ = 01B). Asymmetrical PWM uses single slope operation as shown in Figure 13-8. The timer counts up from BOTTOM to TOP and then restarts from BOTTOM. In non-inverting mode, the output CC*x* is set on the compare match between Timer 2 (TL2, TH2) and the channel data register (CC*x*L, CC*x*H), and cleared at BOTTOM. In inverting mode, the output CC*x* is cleared on the compare match between Timer 2 and the data register, and set at BOTTOM. The resulting asymmetrical output waveform is left-edge aligned.

The TOP value in RCAP2L and RCAP2H is double buffered such that the output frequency is only updated at the TOP to BOTTOM overflow. The channel data register (CC*x*L, CC*x*H) is also double-buffered such that the duty cycle is only updated at the TOP to BOTTOM overflow to prevent glitches. The output frequency and duty cycle for asymmetrical PWM are given by the following equations:

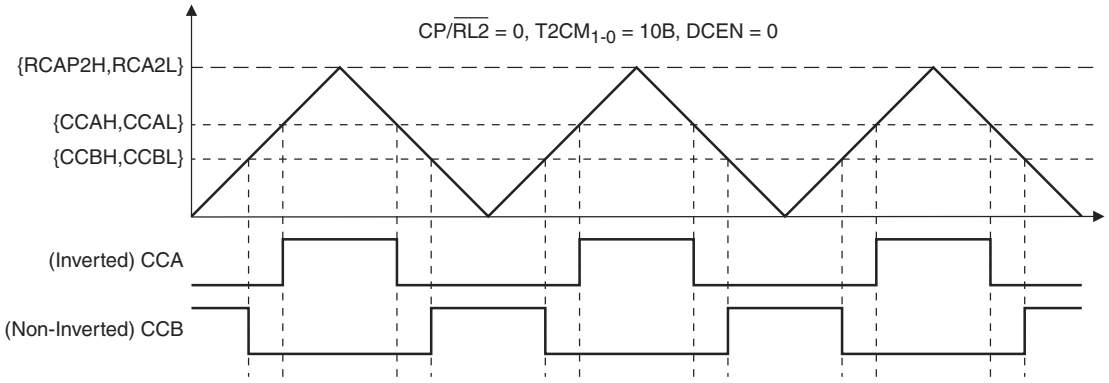
$$f_{OUT} = \frac{\text{Oscillator Frequency}}{\{\text{RCAP2H, RCAP2L}\} + 1} \times \frac{1}{\text{TPS} + 1}$$

$$\text{Inverting:} \qquad \text{Duty Cycle} = 100\% \times \frac{\{\text{CCxH, CCxL}\}}{\{\text{RCAP2H, RCAP2L}\} + 1}$$

$$\text{Non-Inverting:} \qquad \text{Duty Cycle} = 100\% \times \frac{\{\text{RCAP2H, RCAP2L}\} - \{\text{CCxH, CCxL}\} + 1}{\{\text{RCAP2H, RCAP2L}\} + 1}$$

The extreme compare values represent special cases when generating a PWM waveform. If the compare value is set equal to (or greater than) TOP, the output will remain low or high for non-inverting and inverting modes, respectively. If the compare value is set to BOTTOM (0000H), the output will remain high or low for non-inverting and inverting modes, respectively.

Figure 13-9. Non-overlapping Waveforms Using Symmetrical PWM



13.4.2.1 Phase and Frequency Correct PWM

When $T2CM_{1-0}$ = 10B, the Symmetrical PWM operates in phase and frequency correct mode. In this mode the compare value double buffer is only updated when the timer equals MIN (underflow). This guarantees that the resulting waveform is always symmetrical around the TOP value as shown in Figure 13-10 because the up and down count compare values are identical. The TF2 interrupt flag is only set at underflow.

13.4.2.2 Phase Correct PWM

When $T2CM_{1-0}$ = 11B, the Symmetrical PWM operates in phase correct mode. In this mode the compare value double buffer is updated when the timer equals MIN (underflow) and TOP (overflow). The resulting waveform may not be completely symmetrical around the TOP value as shown in Figure 13-11 because the up and down count compare values may not be identical. However, this allows the pulses to be weighted toward one edge or another. The TF2 interrupt flag is set at both underflow and overflow.

Figure 13-10. Phase and Frequency Correct Symmetrical (Center-Aligned) PWM

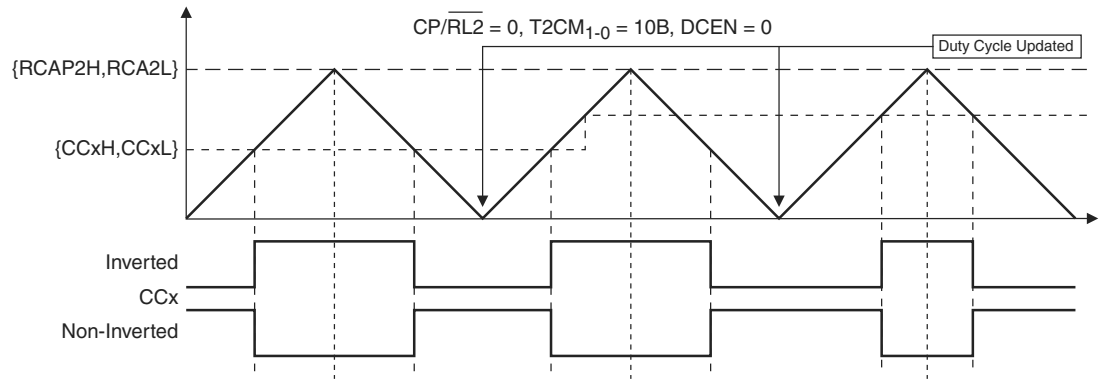


Figure 15-1. GPI Block Diagram

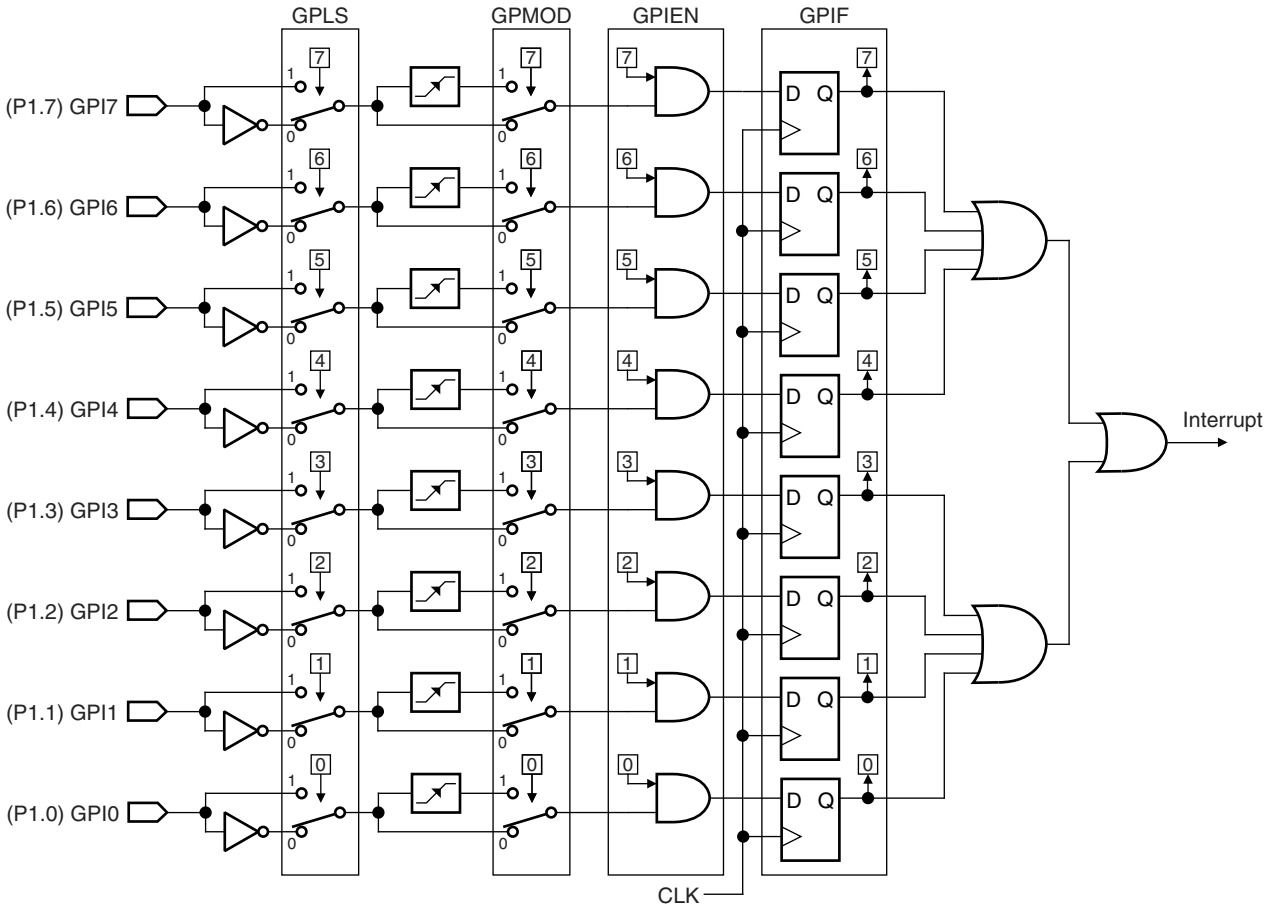


Table 15-1. GPMOD – General-purpose Interrupt Mode Register

GPMOD = 9AH — Reset Value = 0000 0000B

Not Bit Addressable

	GPMOD7	GPMOD6	GPMOD5	GPMOD4	GPMOD3	GPMOD2	GPMOD1	GPMOD0
Bit	7	6	5	4	3	2	1	0

GPMOD.x 0 = level-sensitive interrupt for P1.x

1 = edge-triggered interrupt for P1.x

interrupted by a data byte. An address byte, however, interrupts all slaves. Each slave can examine the received byte and see if it is being addressed. The addressed slave clears its SM2 bit and prepares to receive the data bytes that follows. The slaves that are not addressed set their SM2 bits and ignore the data bytes.

The SM2 bit can be used to check the validity of the stop bit in Mode 1. In a Mode 1 reception, if SM2 = 1, the receive interrupt is not activated unless a valid stop bit is received.

Table 16-1. SCON – Serial Port Control Register

SCON Address = 98H — Reset Value = 0000 0000B

Bit Addressable

Bit	7	6	5	4	3	2	1	0
	SM0/FE	SM1	SM2	REN	TB8	RB8	T1	RI

(SMOD0 = 0/1)[1]

Symbol	Function
FE	Framing error bit. This bit is set by the receiver when an invalid stop bit is detected. The FE bit is not cleared by valid frames and must be cleared by software. The SMOD0 bit must be set to enable access to the FE bit. FE will be set regardless of the state of SMOD0.
SM0	Serial Port Mode Bit 0, (SMOD0 must = 0 to access bit SM0)
SM1	Serial Port Mode Bit 1 **SM0** **SM1** **Mode** **Description** **Baud Rate**[2] 0 0 0 shift register $f_{osc}/2$ or $f_{osc}/4$ or Timer 1 0 1 1 8-bit UART variable (Timer 1 or Timer 2) 1 0 2 9-bit UART $f_{osc}/32$ or $f_{osc}/16$ 1 1 3 9-bit UART variable (Timer 1 or Timer 2)
SM2	Enables the Automatic Address Recognition feature in Modes 2 or 3. If SM2 = 1 then RI will not be set unless the received 9th data bit (RB8) is 1, indicating an address, and the received byte is a Given or Broadcast Address. In Mode 1, if SM2 = 1 then RI will not be activated unless a valid stop bit was received, and the received byte is a Given or Broadcast Address. In Mode 0, SM2 determines the idle state of the shift clock such that the clock is the inverse of SM2, i.e. when SM2 = 0 the clock idles high and when SM2 = 1 the clock idles low.
REN	Enables serial reception. Set by software to enable reception. Clear by software to disable reception.
TB8	The 9th data bit that will be transmitted in Modes 2 and 3. Set or clear by software as desired. In Mode 0, setting TB8 enables Timer 1 as the shift clock generator.
RB8	In Modes 2 and 3, the 9th data bit that was received. In Mode 1, if SM2 = 0, RB8 is the stop bit that was received. In Mode 0, RB8 is not used.
TI	Transmit interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or at the beginning of the stop bit in the other modes, in any serial transmission. Must be cleared by software.
RI	Receive interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or halfway through the stop bit time in the other modes, in any serial reception (except see SM2). Must be cleared by software.

Notes: 1. SMOD0 is located at PCON.6.

2. f_{osc} = oscillator frequency. The baud rate depends on SMOD1 (PCON.7).

Programmers can achieve very low baud rates with Timer 1 by configuring the Timer to run as a 16-bit auto-reload timer (high nibble of TMOD = 0001B). In this case, the baud rate is given by the following formula.

$$\text{Modes 1, 3 Baud Rate} = \frac{2^{\text{SMOD1}}}{32} \times \frac{\text{Oscillator Frequency}}{[65536 - (R\text{H1,RL1})]} \times \frac{1}{\text{TPS} + 1}$$

Table 16-2 lists commonly used baud rates and how they can be obtained from Timer 1.

Table 16-2. Commonly Used Baud Rates Generated by Timer 1 (TPS = 0000B)

Baud Rate	f_{osc} (MHz)	SMOD1	Timer 1		
			C/$\overline{T}$	Mode	Reload Value
Mode 0: 1 MHz	4	0	X	X	X
Mode 2: 750K	12	1	X	X	X
62.5K	12	1	0	2	F4H
38.4K	11.059	0	0	2	F7H
19.2K	11.059	1	0	2	DCH
9.6K	11.059	0	0	2	DCH
4.8K	11.059	0	0	2	B8H
2.4K	11.059	0	0	2	70H
1.2K	11.059	0	0	1	FEE0H
137.5	11.986	0	0	1	F55CH
110	6	0	0	1	F958H
110	12	0	0	1	F304H

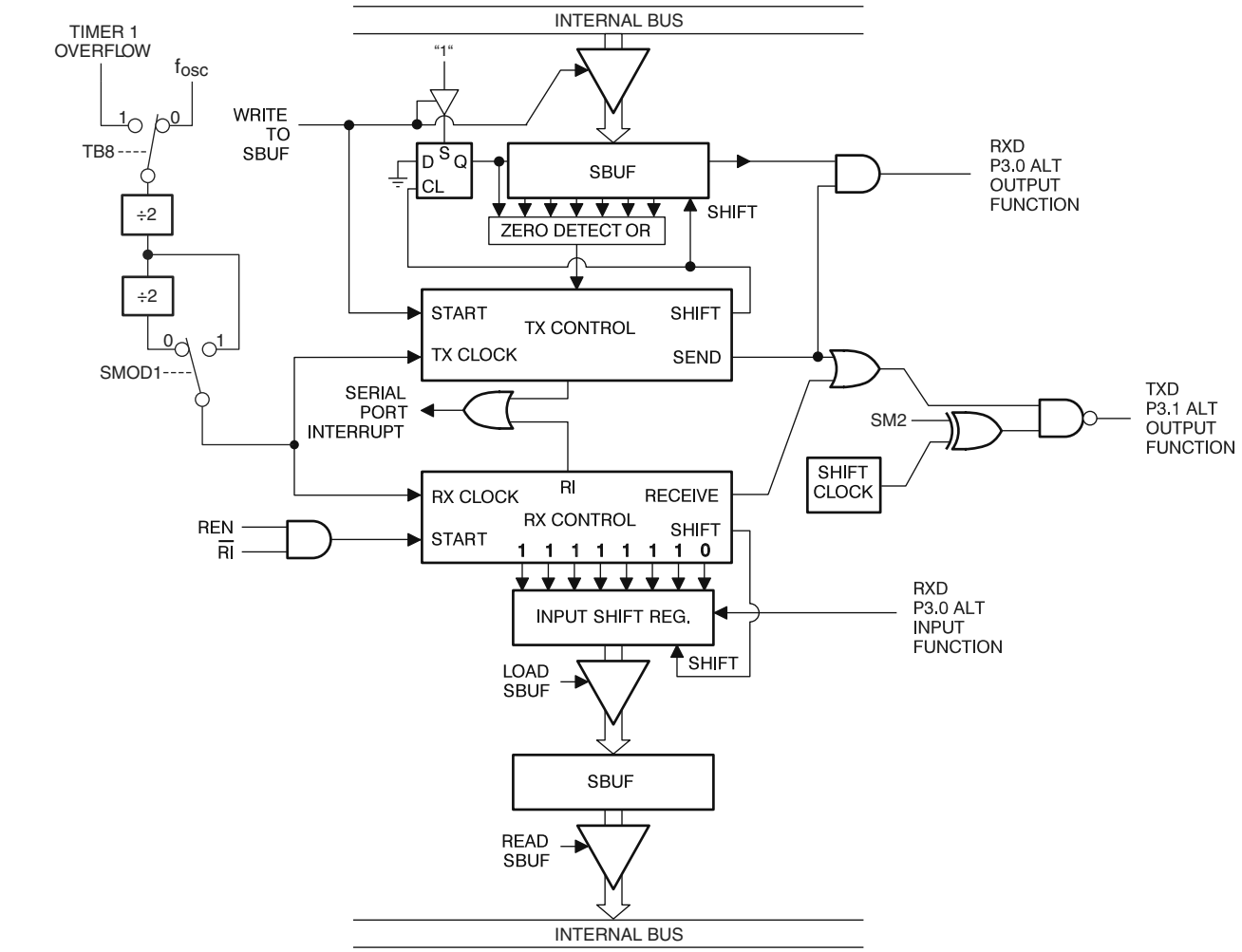
16.2.2 Using Timer 2 to Generate Baud Rates

Timer 2 is selected as the baud rate generator by setting TCLK and/or RCLK in T2CON. Under these conditions, the baud rates for transmit and receive can be simultaneously different by using Timer 1 for transmit and Timer 2 for receive, or vice versa. The baud rate generator mode is similar to the auto-reload mode, in that a rollover causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software. In this case, the baud rates in Modes 1 and 3 are determined by Timer 2's overflow rate according to the following equation:.

$$\text{Modes 1 and 3 Baud Rate} = \frac{1}{16} \times \frac{\text{Oscillator Frequency}}{[65536 - (\text{RCAP2H,RCAP2L})]} \times \frac{1}{\text{TPS} + 1}$$

Table 16-3 lists commonly used baud rates and how they can be obtained from Timer 2.

Figure 16-1. Serial Port Mode 0



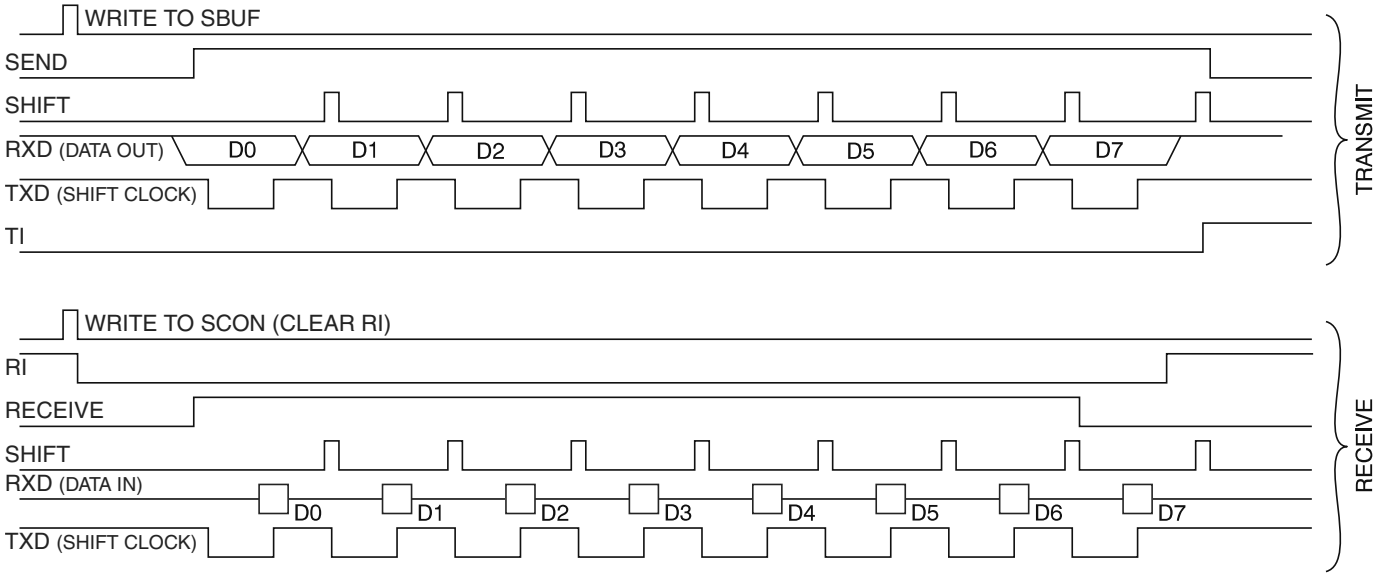


Table 20-1. Instruction Execution Times and Exceptions (Continued)

MUL AB	1	48	2	A4
DIV AB	1	48	4	84
DA A	1	12	1	D4
		Clock Cycles		
Logical	**Bytes**	**8051**	**AT89LP**	**Hex Code**
CLR A	1	12	1	E4
CPL A	1	12	1	F4
ANL A, Rn	1	12	1	58 - 5F
ANL A, direct	2	12	2	55
ANL A, @Ri	1	12	2	56 - 57
ANL A, #data	2	12	2	54
ANL direct, A	2	12	2	52
ANL direct, #data	3	24	3	53
ORL A, Rn	1	12	1	48 - 4F
ORL A, direct	2	12	2	45
ORL A, @Ri	1	12	2	46 - 47
ORL A, #data	2	12	2	44
ORL direct, A	2	12	2	42
ORL direct, #data	3	24	3	43
XRL A, Rn	1	12	1	68 - 6F
XRL A, direct	2	12	2	65
XRL A, @Ri	1	12	2	66 - 67
XRL A, #data	2	12	2	64
XRL direct, A	2	12	2	62
XRL direct, #data	3	24	3	63
RL A	1	12	1	23
RLC A	1	12	1	33
RR A	1	12	1	03
RRC A	1	12	1	13
SWAP A	1	12	1	C4
		Clock Cycles		
Data Transfer	**Bytes**	**8051**	**AT89LP**	**Hex Code**
MOV A, Rn	1	12	1	E8 - EF
MOV A, direct	2	12	2	E5
MOV A, @Ri	1	12	2	E6 - E7
MOV A, #data	2	12	2	74
MOV Rn, A	1	12	1	F8 - FF
MOV Rn, direct	2	24	2	A8 - AF
MOV Rn, #data	2	12	2	78 - 7F

21. Register Index

Table 21-1. Special Function Register Cross Reference

Name	Address	Description Index
ACC	E0H	
ACSRA	97H	Table 18-1 on page 102
ACSRB	9FH	Table 18-2 on page 103
AREF	AFH	Table 18-3 on page 104
B	F0H	
CLKREG	8FH	Table 6-2 on page 23
DPCF (AUXR1)	A2H	Table 5-4 on page 19
DPH0	83H	Section 5.1 on page 17
DPH1	85H	Section 5.1 on page 17
DPL0	82H	Section 5.1 on page 17
DPL1	83H	Section 5.1 on page 17
GPIEN	9CH	Table 15-3 on page 76
GPIF	9DH	Table 15-4 on page 76
GPLS	9BH	Table 15-2 on page 76
GPMOD	9AH	Table 15-1 on page 75
IE	A8H	Table 9-2 on page 32
IE2	B4H	Table 9-5 on page 33
IP	B8H	Table 9-3 on page 32
IP2	B5H	Table 9-6 on page 34
IPH	B7H	Table 9-4 on page 33
IP2H	B6H	Table 9-7 on page 34
MEMCON	96H	Table 3-4 on page 14
P1	90H	Table 10-3 on page 36
P1M0	C2H	Table 10-2 and Table 10-3 on page 36
P1M1	C3H	Table 10-2 and Table 10-3 on page 36
P2	A0H	Table 10-3 on page 36
P2M0	C4H	Table 10-2 and Table 10-3 on page 36
P2M1	C5H	Table 10-2 and Table 10-3 on page 36
P3	B0H	Table 10-3 on page 36
P3M0	C6H	Table 10-2 and Table 10-3 on page 36
P3M1	C7H	Table 10-2 and Table 10-3 on page 36
P4	C0H	Table 10-3 on page 36
P4M0	BEH	Table 10-2 and Table 10-3 on page 36
P4M1	BFH	Table 10-2 and Table 10-3 on page 36
PAGE	86H	Table 3-3 on page 11
PCON	87H	Table 8-1 on page 29

Table 21-1. Special Function Register Cross Reference (Continued)

PSW	D0H	
RCAP2H	CBH	Section 12.1 on page 53
RCAP2L	CAH	Section 12.1 on page 53
RH0	94H	Table 11-1 on page 41
RH1	95H	Table 11-1 on page 41
RL0	92H	Table 11-1 on page 41
RL1	93H	Table 11-1 on page 41
SADDR	A9H	Section 16.7 on page 90
SADEN	B9H	Section 16.7 on page 90
SBUF	99H	Section 16.3 on page 81
SCON	98H	Table 16-1 on page 78
SP	81H	
SPCR	E9H	Table 17-3 on page 97
SPDR	EAH	Table 17-2 on page 97
SPSR	E8H	Table 17-4 on page 98
T2CCA	D1H	Table 13-1 on page 63
T2CCC	D4H	Table 13-4 on page 64
T2CCF	D5H	Table 13-5 on page 65
T2CCH	D3H	Table 13-2 on page 63
T2CCL	D2H	Table 13-3 on page 63
T2CON	C8H	Table 12-3 on page 53
T2MOD	C9H	Table 12-4 on page 54
TCON	88H	Table 11-2 on page 45
TCONB	91H	Table 11-4 on page 47
TH0	8CH	Table 11-1 on page 41
TH1	8DH	Table 11-1 on page 41
TH2	CDH	Section 12.1 on page 53
TL0	8AH	Table 11-1 on page 41
TL1	8BH	Table 11-1 on page 41
TL2	CCH	Section 12.1 on page 53
TMOD	89H	Table 11-3 on page 46
WDTCON	**A7H**	Table 19-2 on page 106
WDTRST	**A6H**	Table 19-3 on page 106

data byte. After each data byte has been transmitted, the byte address is incremented to point to the next data byte. This allows a page command to linearly sweep the bytes within a page. If the byte address is incremented past the last byte in the page, the byte address will roll over to the first byte in the same page. While loading bytes into the page buffer, overwriting previously loaded bytes will result in data corruption.

For a summary of available commands, see Table 23-3 on page 119.

Figure 23-3. Command Sequence Flow Chart

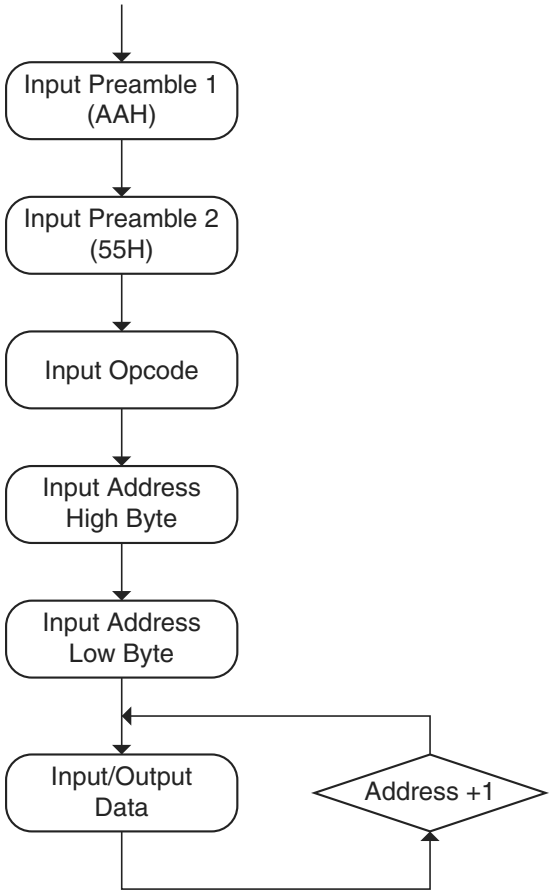
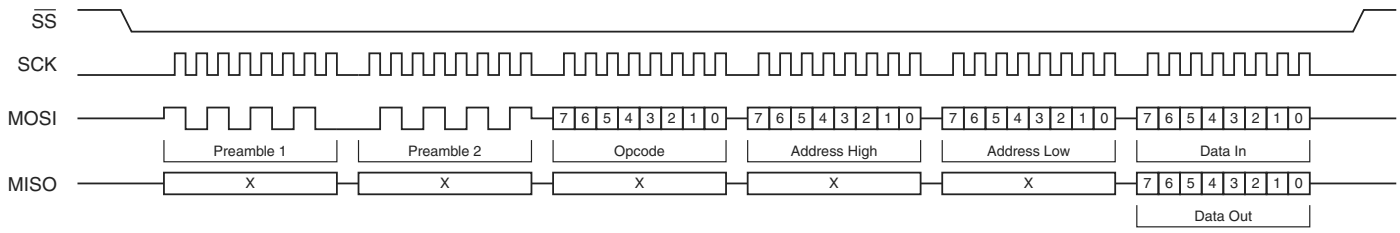


Figure 23-4. ISP Command Packet



24. Electrical Characteristics

24.1 Absolute Maximum Ratings*

Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-0.7V to +5.5V
Maximum Operating Voltage	5.5V
DC Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

24.2 DC Characteristics

T_A = -40°C to 85°C, V_{CC} = 2.4V to 5.5V (unless otherwise noted)

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low-voltage		-0.5	0.3 V_{CC}	V
V_{IH}	Input High-voltage		0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low-voltage(1)	I_{OL} = 8 mA, V_{CC} = 5V ±10%		0.4	V
		I_{OL} = 4 mA		0.4	
V_{OH}	Output High-voltage With Weak Pull-ups Enabled	I_{OH} = -100 µA, V_{CC} = 5V ±10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
V_{OH1}	Output High-voltage With Strong Pull-ups Enabled	I_{OH} = -20 mA, V_{CC} = 5V ±10%	0.75 V_{CC}		
		I_{OH} = -8 mA, V_{CC} = 5V ±10%	0.9 V_{CC}		
		I_{OH} = -6 mA	0.75 V_{CC}		
		I_{OH} = -2 mA	0.9 V_{CC}		
I_{IL}	Logic 0 Input Current	V_{IN} = 0.45V		-100	µA
I_{TL}	Logic 1 to 0 Transition Current	V_{IN} = 2.7V, V_{CC} = 5V ±10%		-300	µA
I_{LI}	Input Leakage Current	0 < V_{IN} < V_{CC}		±10	µA
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I_{CC}	Power Supply Current	Active Mode, 12 MHz, V_{CC} = 5V/3V		10/6	mA
		Idle Mode, 12 MHz, V_{CC} = 5V/3V		5/3	mA
	Power-down Mode(2)	V_{CC} = 5V		5	µA
		V_{CC} = 3V		2	µA

Notes: 1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 10 mA
Maximum total I_{OL} for all output pins: 15 mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

2. Minimum V_{CC} for Power-down is 2V.

24.3.4 Quasi-Bidirectional Input

Figure 24-7. Quasi-bidirectional Input Transition Current at 5V

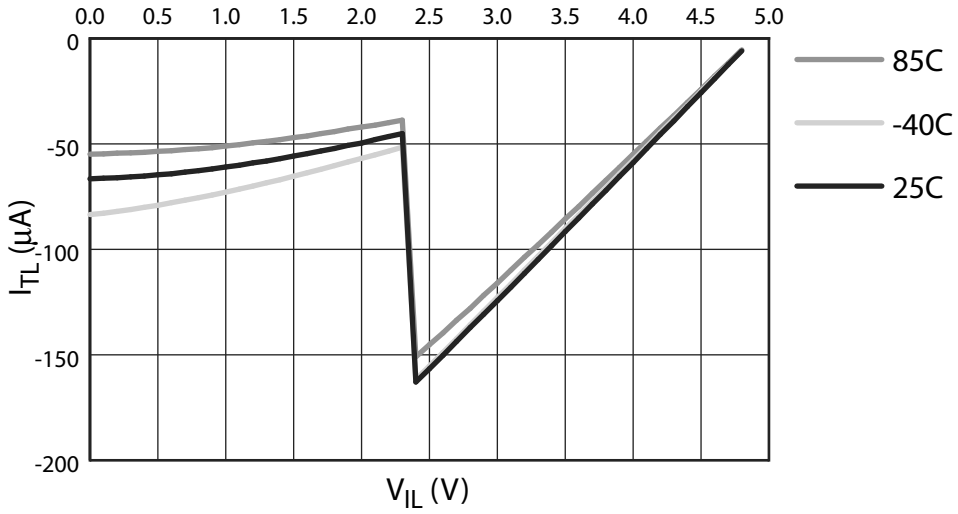
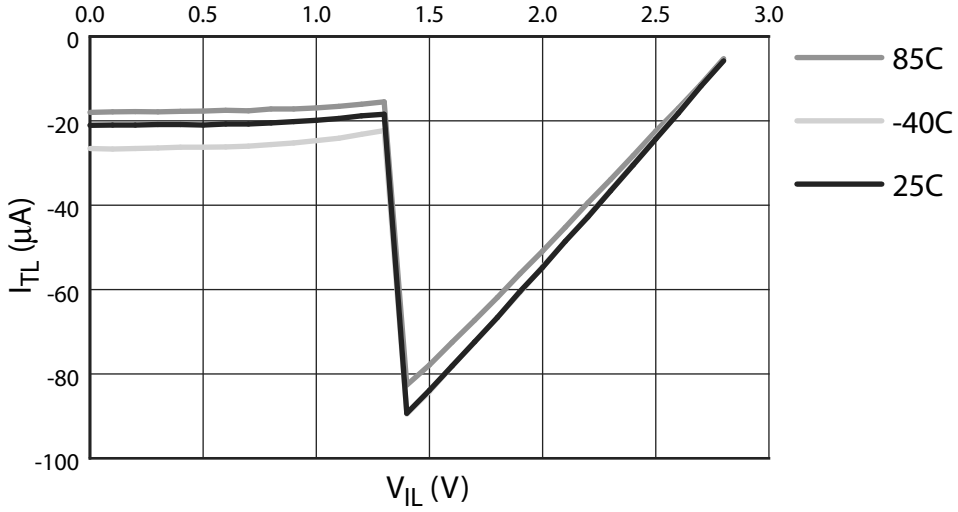
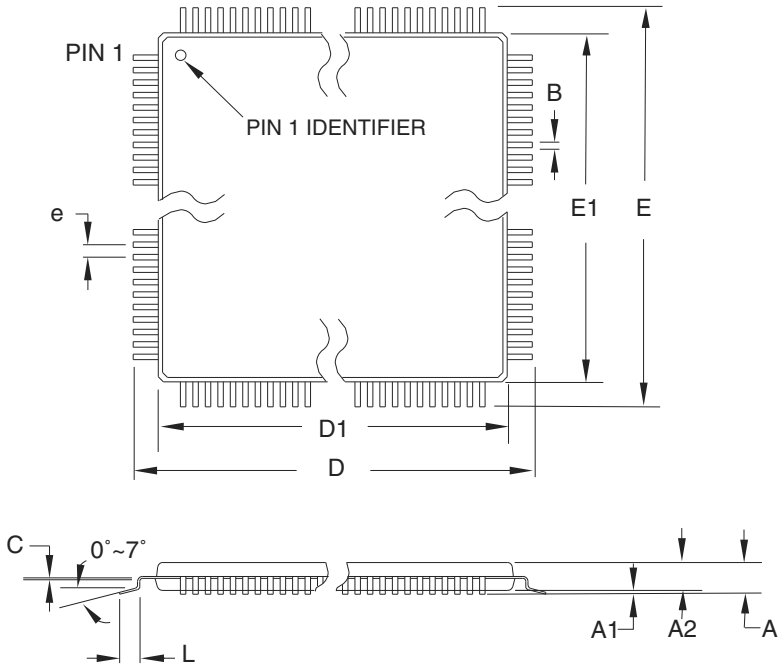


Figure 24-8. Quasi-bidirectional Input Transition Current at 3V



26. Packaging Information

26.1 32A – TQFP



COMMON DIMENSIONS
(Unit of Measure = mm)

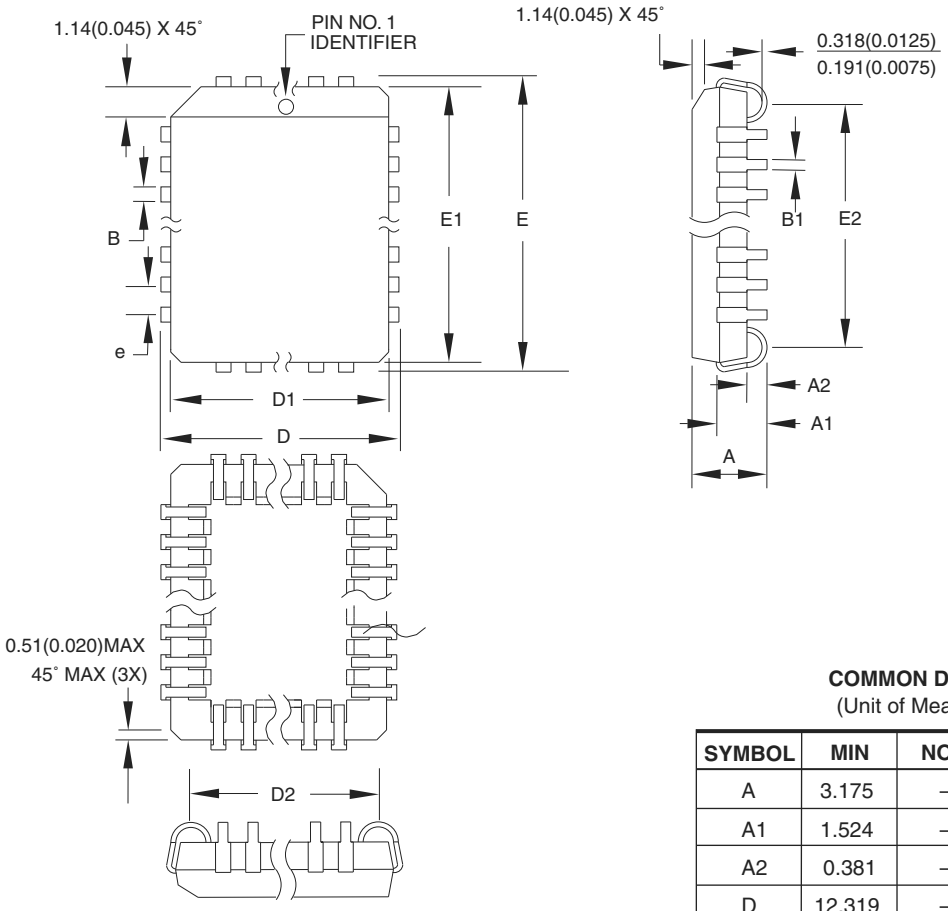
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	8.75	9.00	9.25	
D1	6.90	7.00	7.10	Note 2
E	8.75	9.00	9.25	
E1	6.90	7.00	7.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

Notes:
1. This package conforms to JEDEC reference MS-026, Variation ABA.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10 mm maximum.

10/5/2001

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**32A,** 32-lead, 7 x 7 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	32A	B

26.3 32J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	3.175	–	3.556	
A1	1.524	–	2.413	
A2	0.381	–	–	
D	12.319	–	12.573	
D1	11.354	–	11.506	Note 2
D2	9.906	–	10.922	
E	14.859	–	15.113	
E1	13.894	–	14.046	Note 2
E2	12.471	–	13.487	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes:
1. This package conforms to JEDEC reference MS-016, Variation AE.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**32J**, 32-lead, Plastic J-leaded Chip Carrier (PLCC)	32J	B