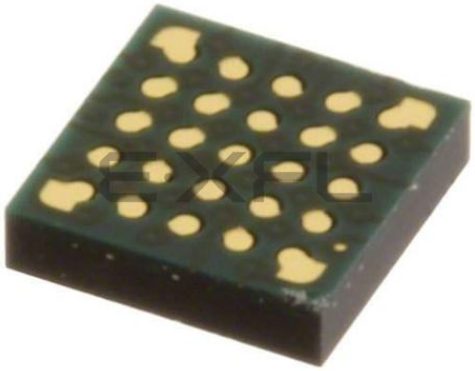


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	14
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 13x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	25-WFLGA
Supplier Device Package	25-LGA (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10e8eala-u0

<R> **Notes 1.** Current flowing to V_{DD}.

2. When high-speed on-chip oscillator and high-speed system clock are stopped.

3. Current flowing only to the real-time clock (RTC) (excluding the operating current of the low-speed on-chip ocsillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and I_{RTC}, when the real-time clock operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added. I_{DD2} subsystem clock operation includes the operational current of the real-time clock.

4. Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip ocsillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and I_{IT}, when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added.

5. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2}, or I_{DD3} and I_{WDT} when the watchdog timer is in operation.

6. Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{ADC}, I_{AVREF}, I_{ADREF} when the A/D converter operates in an operation mode or the HALT mode.

7. Current flowing to the AV_{DD}.

8. Current flowing from the reference voltage source of A/D converter.

9. Operation current flowing to the internal reference voltage.

10. Current flowing to the AV_{REFP}.

11. Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{LVD} when the LVD circuit is in operation.

12. Current flowing only during data flash rewrite.

13. Current flowing only during self programming.

Remarks 1. f_{IL}: Low-speed on-chip oscillator clock frequency

2. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

3. f_{CLK}: CPU/peripheral hardware clock frequency

4. Temperature condition of the TYP. value is T_A = 25°C

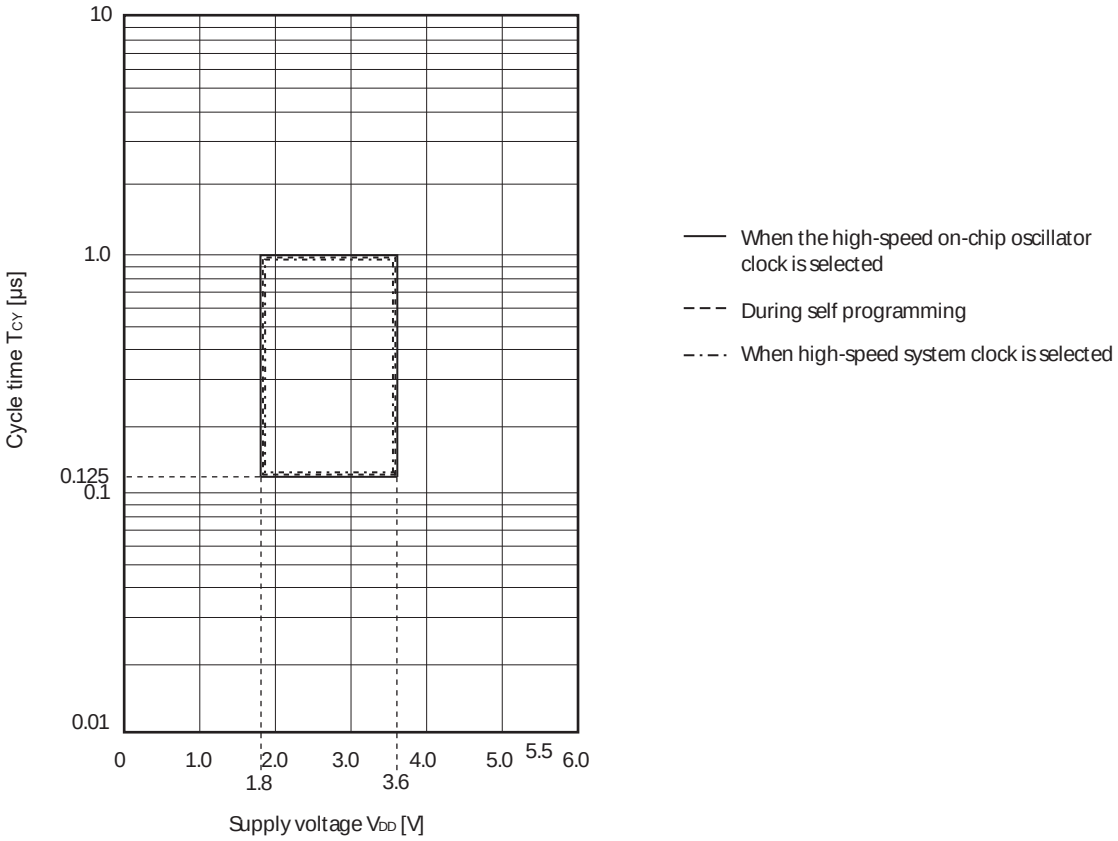
2.4 AC Characteristics

(T_A = –40 to +85°C, $AV_{DD} \le V_{DD} \le 3.6$ V, 1.6 V ≤ $EV_{DD0} \le V_{DD} \le 3.6$ V, $V_{SS} = EV_{SS0}$ = 0 V)

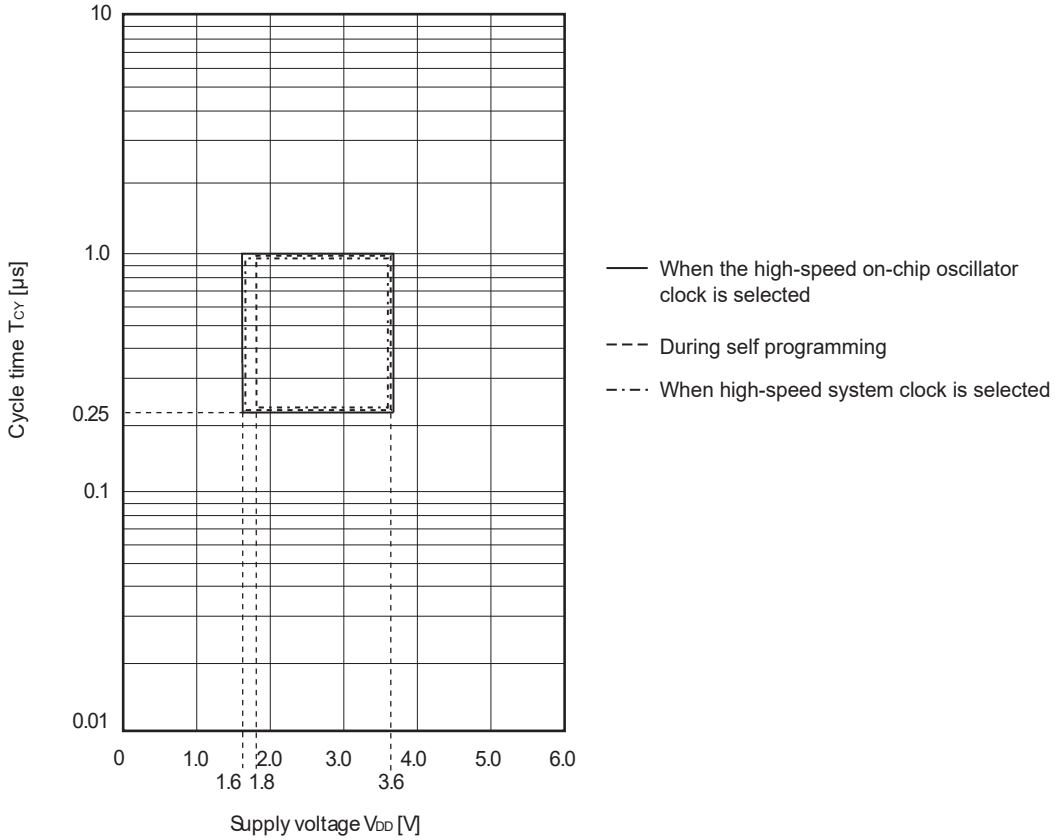
Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{MAIN}) operation	HS (high-speed main) mode	2.7 V ≤ V_{DD} ≤ 3.6 V	0.03125		1	μs
				2.4 V ≤ V_{DD} < 2.7 V	0.0625		1	μs
			LS (low-speed main) mode	1.8 V ≤ V_{DD} ≤ 3.6 V	0.125		1	μs
			LV (low-voltage main) mode	1.6 V ≤ V_{DD} ≤ 3.6 V	0.25		1	μs
		Subsystem clock (f_{SUB}) operation		1.8 V ≤ V_{DD} ≤ 3.6 V	28.5	30.5	31.3	μs
		In the self programming mode	HS (high-speed main) mode	2.7 V ≤ V_{DD} ≤ 3.6 V	0.03125		1	μs
				2.4 V ≤ V_{DD} < 2.7 V	0.0625		1	μs
			LS (low-speed main) mode	1.8 V ≤ V_{DD} ≤ 3.6 V	0.125		1	μs
			LV (low-voltage main) mode	1.6 V ≤ V_{DD} ≤ 3.6 V	0.25		1	μs
External system clock frequency	f_{EX}	2.7 V ≤ V_{DD} ≤ 3.6 V			1.0		20.0	MHz
		2.4 V ≤ V_{DD} < 2.7 V			1.0		16.0	MHz
		1.8 V ≤ V_{DD} < 2.4 V			1.0		8.0	MHz
		1.6 V ≤ V_{DD} < 1.8 V			1.0		4.0	MHz
	f_{EXS}				32		35	kHz
External system clock input high-level width, low-level width	t_{EXH}, t_{EXL}	2.7 V ≤ V_{DD} ≤ 3.6 V			24			ns
		2.4 V ≤ V_{DD} < 2.7 V			30			ns
		1.8 V ≤ V_{DD} < 2.4 V			60			ns
		1.6 V ≤ V_{DD} < 1.8 V			120			ns
	t_{EXHS}, t_{EXLS}				13.7			μs
TI00, TI01, TI03 to TI07 input high-level width, low-level width	t_{TIH}, t_{TIL}				1/f_{MCK}+10			ns[Note]
TO00, TO01, TO03 to TO07 output frequency	f_{TO}	HS (high-speed main) mode		2.7 V ≤ EV_{DD0} ≤ 3.6 V			8	MHz
				1.8 V ≤ EV_{DD0} < 2.7 V			4	MHz
				1.6 V ≤ EV_{DD0} < 1.8 V			2	MHz
		LS (low-speed main) mode		1.8 V ≤ EV_{DD0} ≤ 3.6 V			4	MHz
				1.6 V ≤ EV_{DD0} < 1.8 V			2	MHz
		LV (low-voltage main) mode		1.6 V ≤ EV_{DD0} ≤ 3.6 V			2	MHz
PCLBUZ0, PCLBUZ1 output frequency	f_{PCL}	HS (high-speed main) mode		2.7 V ≤ EV_{DD0} ≤ 3.6 V			8	MHz
				1.8 V ≤ EV_{DD0} < 2.7 V			4	MHz
				1.6 V ≤ EV_{DD0} < 1.8 V			2	MHz
		LS (low-speed main) mode		1.8 V ≤ EV_{DD0} ≤ 3.6 V			4	MHz
				1.6 V ≤ EV_{DD0} < 1.8 V			2	MHz
		LV (low-voltage main) mode		1.8 V ≤ EV_{DD0} ≤ 3.6 V			4	MHz
				1.6 V ≤ EV_{DD0} < 1.8 V			2	MHz
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}	INTP0		1.6 V ≤ V_{DD} ≤ 3.6 V	1			μs
		INTP1 to INTP11		1.6 V ≤ EV_{DD0} ≤ 3.6 V	1			μs
Key interrupt input high-level width, low-level width	t_{KR}	KR0 to KR9		1.8 V ≤ EV_{DD0} ≤ 3.6 V, 1.8 V ≤ AV_{DD0} ≤ 3.6 V	250			ns
				1.6 V ≤ EV_{DD0} < 1.8 V, 1.6 V ≤ AV_{DD0} < 1.8 V	1			μs
$\overline{RESET}$ low-level width	t_{RSL}				10			μs

(**Note** and **Remark** are listed on the next page.)

<R> T_{CY} vs V_{DD} (LS (low-speed main) mode)



<R> T_{CY} vs V_{DD} (LV (low-voltage main) mode)



(3) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions		HS[Note 1]		LS[Note 2]		LV[Note 3]		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY2}	2.7 V ≤ EV_{DD0} ≤ 3.6 V	t_{KCY1} ≥ 4/f_{CLK}	125		500		1000		ns
		2.4 V ≤ EV_{DD0} ≤ 3.6 V	t_{KCY1} ≥ 4/f_{CLK}	250		500		1000		ns
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	t_{KCY1} ≥ 4/f_{CLK}	500		500		1000		ns
		1.7 V ≤ EV_{DD0} ≤ 3.6 V	t_{KCY1} ≥ 4/f_{CLK}	1000		1000		1000		ns
		1.6 V ≤ EV_{DD0} ≤ 3.6 V	t_{KCY1} ≥ 4/f_{CLK}	–		1000		1000		ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	2.7 V ≤ EV_{DD0} ≤ 3.6 V		t_{KCY2}/2 –18		t_{KCY2}/2 –50		t_{KCY2}/2 –50		ns
		2.4 V ≤ EV_{DD0} ≤ 3.6 V		t_{KCY2}/2 –38		t_{KCY2}/2 –50		t_{KCY2}/2 –50		ns
		1.8 V ≤ EV_{DD0} ≤ 3.6 V		t_{KCY2}/2 –50		t_{KCY2}/2 –50		t_{KCY2}/2 –50		ns
		1.7 V ≤ EV_{DD0} ≤ 3.6 V		t_{KCY2}/2 –100		t_{KCY2}/2 –100		t_{KCY2}/2 –100		ns
		1.6 V ≤ EV_{DD0} ≤ 3.6 V		–		t_{KCY2}/2 –100		t_{KCY2}/2 –100		ns
SIp setup time (to SCKp↑)[Note 4]	t_{SIK2}	2.7 V ≤ EV_{DD0} ≤ 3.6 V		44		110		110		ns
		2.4 V ≤ EV_{DD0} ≤ 3.6 V		75		110		110		ns
		1.8 V ≤ EV_{DD0} ≤ 3.6 V		110		110		110		ns
		1.7 V ≤ EV_{DD0} ≤ 3.6 V		220		220		220		ns
		1.6 V ≤ EV_{DD0} ≤ 3.6 V		–		220		220		ns
SIp hold time (from SCKp↑)[Note 4]	t_{KSI2}	1.7 V ≤ EV_{DD} ≤ 3.6 V		19		19		19		ns
		1.6 V ≤ EV_{DD} ≤ 3.6 V		–		19		19		ns
Delay time from SCKp↓ to SOp output[Note 5]	t_{KSO2}	1.7 V ≤ EV_{DD} ≤ 3.6 V	C = 30 pF[Note 6]		25		25		25	ns
		1.6 V ≤ EV_{DD} ≤ 3.6 V	C = 30 pF[Note 6]		–		25		25	ns

Notes 1. HS is condition of HS (high-speed main) mode.

2. LS is condition of LS (low-speed main) mode.

3. LV is condition of LV (low-voltage main) mode.

4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time or SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

5. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

6. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark p: CSI number (p = 00, 01, 10, 11, 20, 21), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 1)

Notes 1. HS is condition of HS (high-speed main) mode.

2. LS is condition of LS (low-speed main) mode.

3. LV is condition of LV (low-voltage main) mode.

4. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

5. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time or SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

6. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

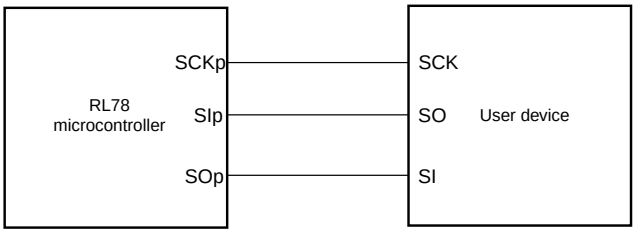
7. C is the load capacitance of the SOp output lines.

Caution Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

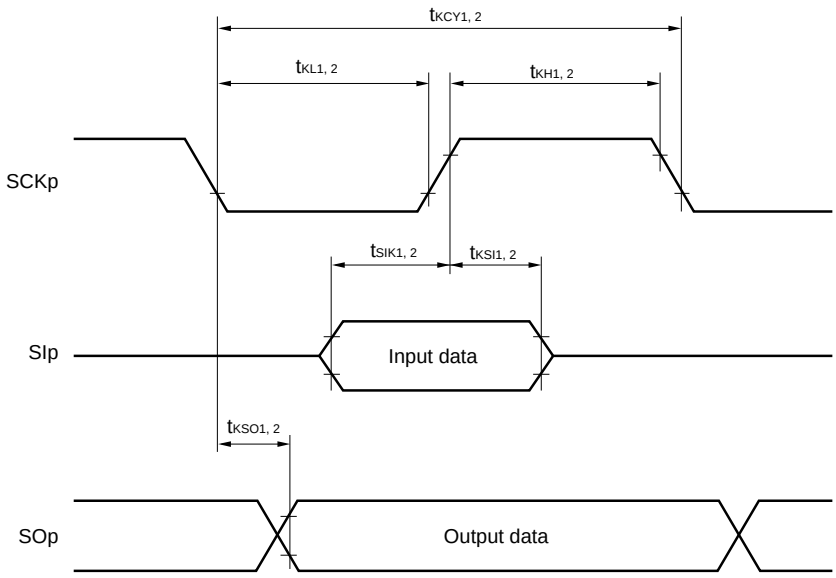
Remarks 1. p: CSI number (p = 00, 01, 10, 11, 20, 21), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),
g: PIM number (g = 0, 1)

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

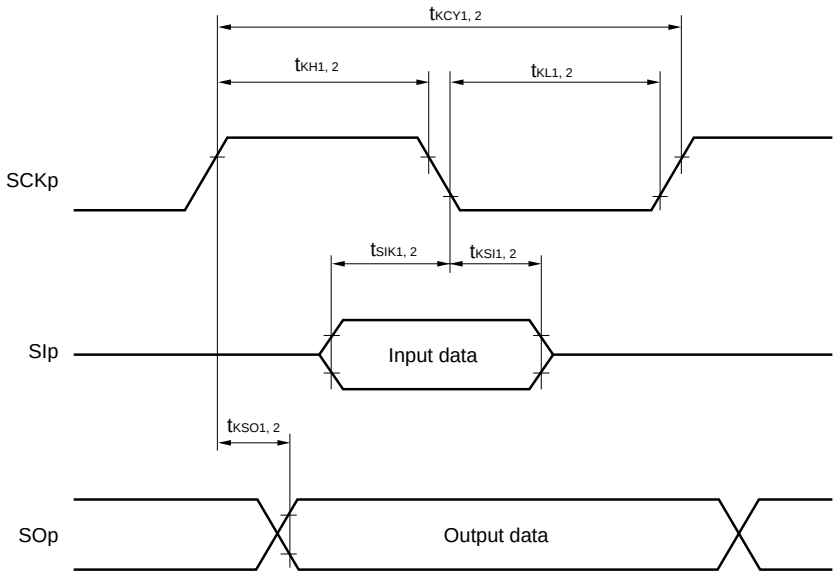
CSI mode connection diagram (during communication at same potential)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remarks 1. p: CSI number (p = 00, 01, 10, 11, 20, 21)

2. m: Unit number, n: Channel number (mn = 00 to 03, 10, 11)

(7) Communication at different potential (2.5 V) (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)

(T_A = –40 to +85°C, 2.7 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions		HS[Note 1]		LS[Note 2]		LV[Note 3]		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ	t_{KCY1} ≥ 2/f_{CLK}	300		1150		1150		ns
SCKp high-level width	t_{KH1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		t_{KCY1}/2 – 120		t_{KCY1}/2 – 120		t_{KCY1}/2 – 120		ns
SCKp low-level width	t_{KL1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		t_{KCY1}/2 – 10		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		ns
SIp setup time (to SCKp↑)[Note 4]	t_{SIK1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		121		479		479		ns
SIp hold time (from SCKp↑)[Note 4]	t_{KSI1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		10		10		10		ns
Delay time from SCKp↓ to SOp output[Note 4]	t_{KSO1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ			130		130		130	ns
SIp setup time (to SCKp↓)[Note 5]	t_{SIK1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		33		110		110		ns
SIp hold time (from SCKp↓)[Note 5]	t_{KSI1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		10		10		10		ns
Delay time from SCKp↑ to SOp output[Note 5]	t_{KSO1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ			10		10		10	ns

Notes 1. HS is condition of HS (high-speed main) mode.
2. LS is condition of LS (low-speed main) mode.
3. LV is condition of LV (low-voltage main) mode.
4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
5. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (When 25- to 48-pin products)/EV_{DD} tolerance (When 64-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

<R>

Remarks 1. R_b[Ω]: Communication line (SCKp, SOp) pull-up resistance, C_b[F]: Communication line (SCKp, SOp) load capacitance, V_b[V]: Communication line voltage
2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 1)

(8) Communication at different potential (1.8V, 2.5 V) (CSI mode) (master mode, SCKp... internal clock output) (1/2)

(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions		HS[Note 1]		LS[Note 2]		LV[Note 3]		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	t_{KCY1} ≥ 4/f_{CLK}	500		1150		1150		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[Note 4], C_b = 30 pF, R_b = 5.5 kΩ	t_{KCY1} ≥ 4/f_{CLK}	1150		1150		1150		ns
SCKp high-level width	t_{KH1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		t_{KCY1}/2 – 170		t_{KCY1}/2 – 170		t_{KCY1}/2 – 170		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[Note 4], C_b = 30 pF, R_b = 5.5 kΩ		t_{KCY1}/2 – 458		t_{KCY1}/2 – 458		t_{KCY1}/2 – 458		ns
SCKp low-level width	t_{KL1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		t_{KCY1}/2 – 18		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[Note 4], C_b = 30 pF, R_b = 5.5 kΩ		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		ns

Notes 1. HS is condition of HS (high-speed main) mode.

2. LS is condition of LS (low-speed main) mode.

3. LV is condition of LV (low-voltage main) mode.

4. Use it with $EV_{DD0} \geq V_b$.

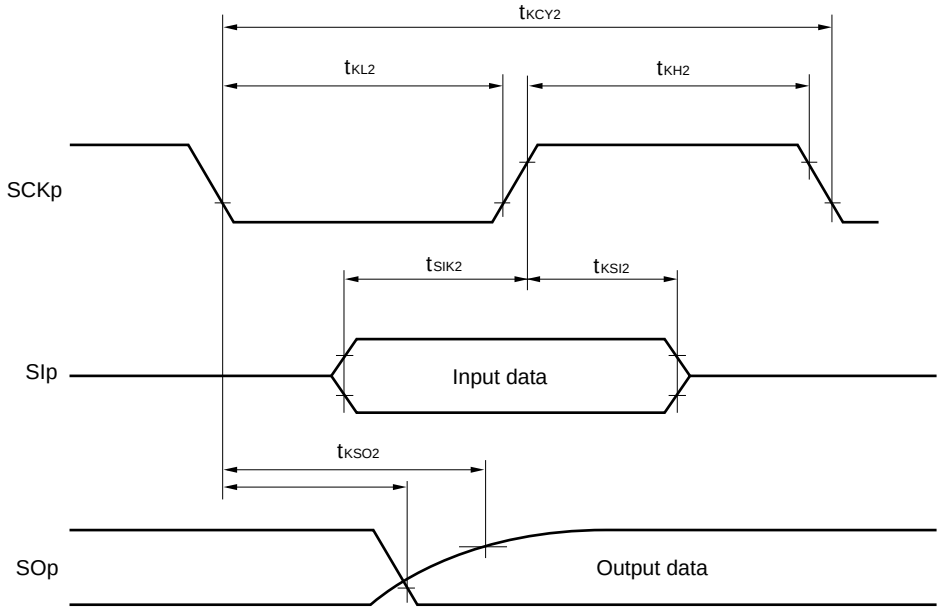
Caution **Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (When 25- to 48-pin products)/EV_{DD} tolerance (When 64-pin products)) mode for the SOp pin and SCKp** <R> **pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.**

Remarks 1. R_b[Ω]: Communication line (SCKp, SOp) pull-up resistance, C_b[F]: Communication line (SCKp, SOp) load capacitance, V_b[V]: Communication line voltage

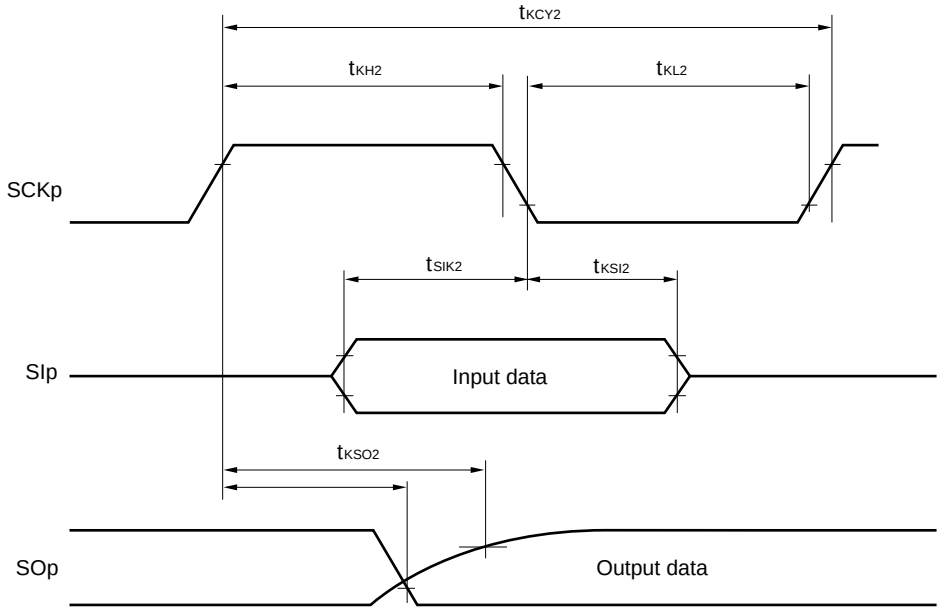
2. p: CSI number (p = 00, 10, 20), m: Unit number , n: Channel number (mn = 00, 02, 10), g: PIM and POM number (g = 0, 1)

3. CSI01, CSI11, and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remarks 1. p: CSI number (p = 00, 10, 20), m: Unit number, n: Channel number (mn = 00, 02, 10), g: PIM and POM number (g = 0, 1)

2. CSI01, CSI11, and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

2.5.2 Serial interface IICA

(1) I^2C standard mode

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions	Standard Mode[Note 1]						Unit
			HS[Note 2]		LS[Note 3]		LV[Note 4]		
			MIN.	MAX.	MIN.	MIN.	MAX.	MIN.	
SCLA0 clock frequency	f_{SCL}	2.7 V ≤ EV_{DD0} ≤ 3.6 V	0	100	0	100	0	100	kHz
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	0	100	0	100	0	100	
		1.7 V ≤ EV_{DD0} ≤ 3.6 V	0	100	0	100	0	100	
		1.6 V ≤ EV_{DD0} ≤ 3.6 V	–		0	100	0	100	
Setup time of restart condition	$t_{SU:STA}$	2.7 V ≤ EV_{DD0} ≤ 3.6 V	4.7		4.7		4.7		μs
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	4.7		4.7		4.7		
		1.7 V ≤ EV_{DD0} ≤ 3.6 V	4.7		4.7		4.7		
		1.6 V ≤ EV_{DD0} ≤ 3.6 V	–		4.7		4.7		
Hold time[Note 5]	$t_{HD:STA}$	2.7 V ≤ EV_{DD0} ≤ 3.6 V	4.0		4.0		4.0		μs
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	4.0		4.0		4.0		
		1.7 V ≤ EV_{DD0} ≤ 3.6 V	4.0		4.0		4.0		
		1.6 V ≤ EV_{DD0} ≤ 3.6 V	–		4.0		4.0		
Hold time when SCLA0 = “L”	t_{LOW}	2.7 V ≤ EV_{DD0} ≤ 3.6 V	4.7		4.7		4.7		μs
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	4.7		4.7		4.7		
		1.7 V ≤ EV_{DD0} ≤ 3.6 V	4.7		4.7		4.7		
		1.6 V ≤ EV_{DD0} ≤ 3.6 V	–		4.7		4.7		
Hold time when SCLA0 = “H”	t_{HIGH}	2.7 V ≤ EV_{DD0} ≤ 3.6 V	4.0		4.0		4.0		μs
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	4.0		4.0		4.0		
		1.7 V ≤ EV_{DD0} ≤ 3.6 V	4.0		4.0		4.0		
		1.6 V ≤ EV_{DD0} ≤ 3.6 V	–		4.0		4.0		
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ EV_{DD0} ≤ 3.6 V	250		250		250		ns
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	250		250		250		
		1.7 V ≤ EV_{DD0} ≤ 3.6 V	250		250		250		
		1.6 V ≤ EV_{DD0} ≤ 3.6 V	–		250		250		
Data hold time (transmission)[Note 6]	$t_{HD:DAT}$	2.7 V ≤ EV_{DD0} ≤ 3.6 V	0	3.45	0	3.45	0	3.45	μs
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	0	3.45	0	3.45	0	3.45	
		1.7 V ≤ EV_{DD0} ≤ 3.6 V	0	3.45	0	3.45	0	3.45	
		1.6 V ≤ EV_{DD0} ≤ 3.6 V	–	–	0	3.45	0	3.45	
Setup time of stop condition	$t_{SU:STO}$	2.7 V ≤ EV_{DD0} ≤ 3.6 V	4.0		4.0		4.0		μs
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	4.0		4.0		4.0		
		1.7 V ≤ EV_{DD0} ≤ 3.6 V	4.0		4.0		4.0		
		1.6 V ≤ EV_{DD0} ≤ 3.6 V	–		4.0		4.0		
Bus-free time	t_{BUF}	2.7 V ≤ EV_{DD0} ≤ 3.6 V	4.7		4.7		4.7		μs
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	4.7		4.7		4.7		
		1.7 V ≤ EV_{DD0} ≤ 3.6 V	4.7		4.7		4.7		
		1.6 V ≤ EV_{DD0} ≤ 3.6 V	–		4.7		4.7		

(**Note** and **Remark** are listed on the next page.)

<R> **(5) When reference voltage (+) = AV_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) = AV_{SS} (ADREFM = 0), target for conversion: ANI16 to ANI30, interanal reference voltage, temperature sensor output voltage**

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD0} ≤ 3.6 V, 1.6 V ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V, AV_{SS} = 0 V, Reference voltage (+) = AV_{DD}, Reference voltage (–) = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}		2.4 V ≤ AV_{DD} ≤ 3.6 V	8		12	bit
			1.8 V ≤ AV_{DD} ≤ 3.6 V	8		10 Note 1	
			1.6 V ≤ AV_{DD} ≤ 3.6 V	8 Note 2			
Overall error Note 3	AINL	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±8.5	LSB
		10-bit resolution	1.8 V ≤ AV_{DD} ≤ 3.6 V			±6.0	
		8-bit resolution	1.6 V ≤ AV_{DD} ≤ 3.6 V			±3.5	
Conversion time	t_{CONV}	ADTYP = 0, 12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V	4.125			μs
		ADTYP = 0, 10-bit resolution Note 1	1.8 V ≤ AV_{DD} ≤ 3.6 V	9.5			
		ADTYP = 0, 8-bit resolution Note 2	1.6 V ≤ AV_{DD} ≤ 3.6 V	57.5			
		ADTYP = 1, 8-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V	3.3125			μs
			1.8 V ≤ AV_{DD} ≤ 3.6 V	7.875			
			1.6 V ≤ AV_{DD} ≤ 3.6 V	54.25			
Zero-scale error Note 3	E_{ZS}	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±8.0	LSB
		10-bit resolution	1.8 V ≤ AV_{DD} ≤ 3.6 V			±5.5	
		8-bit resolution	1.6 V ≤ AV_{DD} ≤ 3.6 V			±3.0	
Full-scale error Note 3	E_{FS}	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±8.0	LSB
		10-bit resolution	1.8 V ≤ AV_{DD} ≤ 3.6 V			±5.5	
		8-bit resolution	1.6 V ≤ AV_{DD} ≤ 3.6 V			±3.0	
Integral linearity error Note 3	ILE	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±3.5	LSB
		10-bit resolution	1.8 V ≤ AV_{DD} ≤ 3.6 V			±2.5	
		8-bit resolution	1.6 V ≤ AV_{DD} ≤ 3.6 V			±1.5	
Differential linearity error Note 3	DLE	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±2.5	LSB
		10-bit resolution	1.8 V ≤ AV_{DD} ≤ 3.6 V			±2.5	
		8-bit resolution	1.6 V ≤ AV_{DD} ≤ 3.6 V			±2.0	
Analog input voltage	V_{AIN}			0		AV_{DD} and EV_{DD0}	V
		Interanal reference voltage (2.4 V ≤ V_{DD} ≤ 3.6 V, HS (high-speed main) mode)		V_{BGR} Note 4			V
		Temperature sensor output voltage (2.4 V ≤ V_{DD} ≤ 3.6 V, HS (high-speed main) mode)		V_{TMPS25} Note 4			V

Notes 1. Cannot be used for lower 2 bit of ADCR register

2. Cannot be used for lower 4 bit of ADCR register

3. Excludes quantization error (±1/2 LSB).

4. See **2.6.2 Temperature sensor, internal reference voltage output characteristics**.

3.3.2 Supply current characteristics

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V) **(1/3)**

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current	I_{DD1} Note 1	Operating mode	HS (high-speed main) mode Note 5	f_{IH} = 32 MHz Note 3	Basic operation	V_{DD} = 3.0 V		2.1		mA
					Normal operation	V_{DD} = 3.0 V		4.6	7.5	mA
				f_{IH} = 24 MHz Note 3	Normal operation	V_{DD} = 3.0 V		3.7	5.8	mA
				f_{IH} = 16 MHz Note 3	Normal operation	V_{DD} = 3.0 V		2.7	4.2	mA
			HS (high-speed main) mode Note 5	f_{MX} = 20 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		3.0	4.9	mA
						Resonator connection		3.2	5.0	
				f_{MX} = 10 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		1.9	2.9	mA
						Resonator connection		1.9	2.9	
			Subsystem clock mode	f_{SUB} = 32.768 kHz Note 4 T_A = –40°C	Normal operation	Square wave input		4.1	4.9	μA
						Resonator connection		4.2	5.0	
				f_{SUB} = 32.768 kHz Note 4 T_A = +25°C	Normal operation	Square wave input		4.2	4.9	μA
						Resonator connection		4.3	5.0	
				f_{SUB} = 32.768 kHz Note 4 T_A = +50°C	Normal operation	Square wave input		4.3	5.5	μA
						Resonator connection		4.4	5.6	
				f_{SUB} = 32.768 kHz Note 4 T_A = +70°C	Normal operation	Square wave input		4.5	6.3	μA
						Resonator connection		4.6	6.4	
				f_{SUB} = 32.768 kHz Note 4 T_A = +85°C	Normal operation	Square wave input		4.8	7.7	μA
						Resonator connection		4.9	7.8	
				f_{SUB} = 32.768 kHz Note 4 T_A = +105°C	Normal operation	Square wave input		6.9	19.7	μA
						Resonator connection		7.0	19.8	

(**Notes** and **Remarks** are listed on the next page.)

Notes 1. Total current flowing into V_{DD} and EV_{DD0}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, on-chip pull-up/pull-down resistors, and data flash rewriting.

2. When high-speed on-chip oscillator and subsystem clock are stopped.

3. When high-speed system clock and subsystem clock are stopped.

4. When high-speed on-chip oscillator and high-speed system clock are stopped. When setting ultra-low power consumption oscillation (AMPHS1 = 1). Not including the current flowing into the RTC, 12-bit interval timer and watchdog timer

5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: V_{DD} = 2.7 V to 3.6 V@1 MHz to 32 MHz
V_{DD} = 2.4 V to 3.6 V@1 MHz to 16 MHz

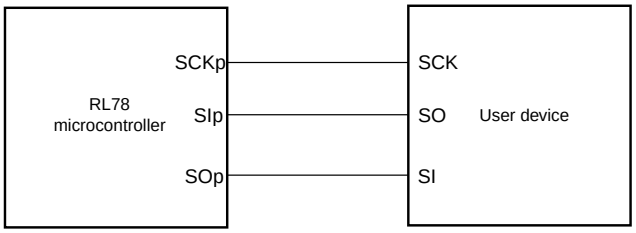
Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH}: High-speed on-chip oscillator clock frequency

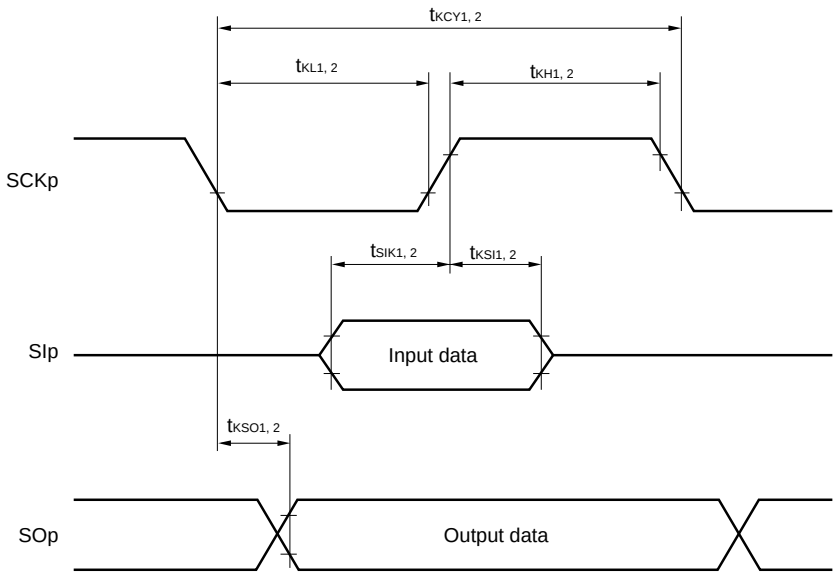
3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

4. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

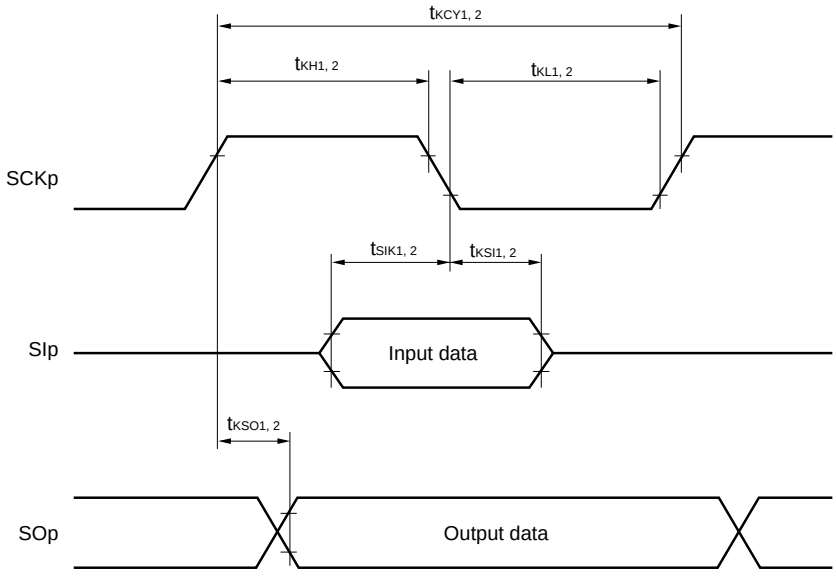
CSI mode connection diagram (during communication at same potential)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



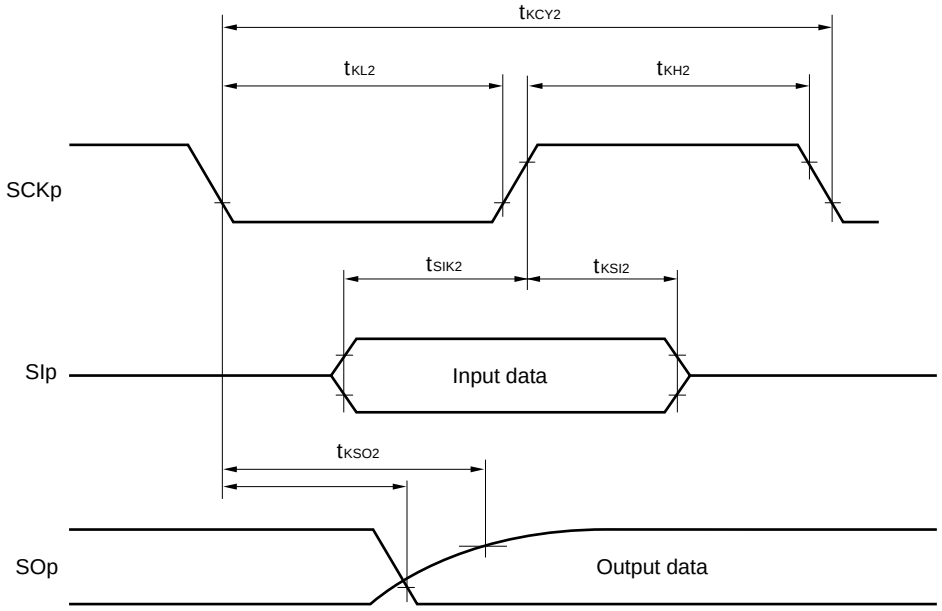
CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



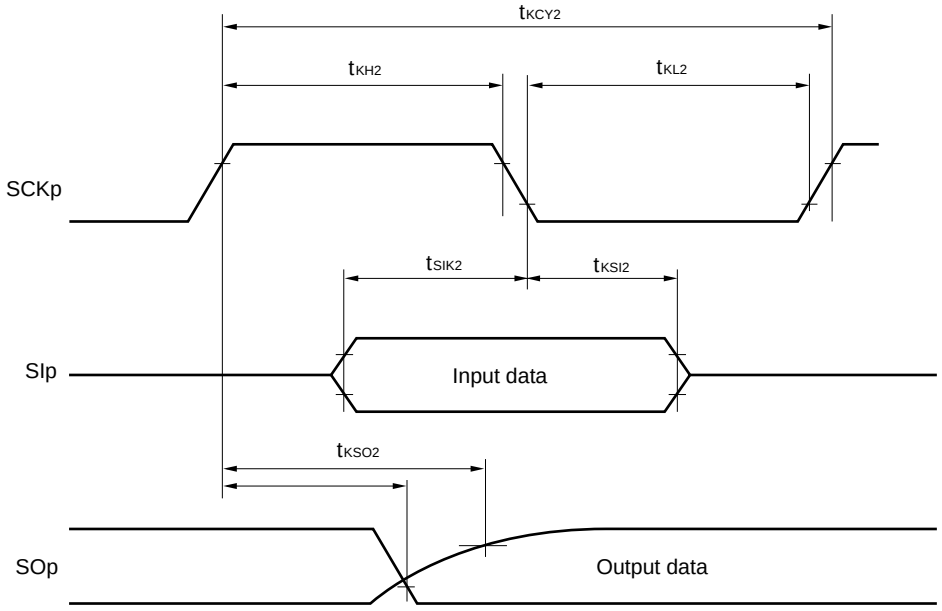
Remarks 1. p: CSI number (p = 00, 01, 10, 11, 20, 21)

2. m: Unit number, n: Channel number (mn = 00 to 03, 10, 11)

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remarks 1. p: CSI number (p = 00, 10, 20), m: Unit number, n: Channel number (mn = 00, 02, 10), g: PIM and POM number (g = 0, 1)

2. CSI01, CSI11, and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

(8) Communication at different potential (1.8 V, 2.5 V) (simplified I^2C mode) (1/2)

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCLr clock frequency	f_{SCL}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ		400 Note 1	kHz
		2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ		100 Note 1	kHz
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 100 pF, R_b = 5.5 kΩ		100 Note 1	kHz
Hold time when SCLr = “L”	t_{LOW}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	1200		ns
		2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	4600		ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 100 pF, R_b = 5.5 kΩ	4650		ns
Hold time when SCLr = “H”	t_{HIGH}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	500		ns
		2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	2400		ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 100 pF, R_b = 5.5 kΩ	1830		ns

(**Notes**, **Caution** and **Remarks** are listed on the next page.)

<R> **(3) When reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = AV_{REFM}/ANI1 (ADREFM = 1), target for conversion: ANI16 to ANI30, interanal reference voltage, temperature sensor output voltage**

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, 2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V, AV_{SS} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (–) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}		2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V	8		12	bit
Overall error[Note 1]	AINL	12-bit resolution	2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±7.0	LSB
Conversion time	t_{CONV}	ADTYP = 0, 12-bit resolution	2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V	4.125			μs
Zero-scale error[Note 1]	E_{ZS}	12-bit resolution	2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±5.0	LSB
Full-scale error[Note 1]	E_{FS}	12-bit resolution	2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±5.0	LSB
Integral linearity error[Note 1]	ILE	12-bit resolution	2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±3.0	LSB
Differential linearity error[Note 1]	DLE	12-bit resolution	2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±2.0	LSB
Analog input voltage	V_{AIN}			0.		AV_{REFP} and EV_{DD0}	V
		Interanal reference voltage (2.4 V ≤ V_{DD} ≤ 3.6 V, HS (high-speed main) mode)		V_{BGR}[Note 2]			V
		Temperature sensor output voltage (2.4 V ≤ V_{DD} ≤ 3.6 V, HS (high-speed main) mode)		V_{TMPS25}[Note 2]			V

Notes 1. Excludes quantization error (±1/2 LSB).

2. See **3.6.2 Temperature sensor, internal reference voltage output characteristics**.

<R> **(4) When reference voltage (+) = AV_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) = AV_{SS} (ADREFM = 0), target for conversion: ANI16 to ANI30, interanal reference voltage, temperature sensor output voltage**

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD0} ≤ V_{DD0} ≤ 3.6 V, 2.4 V ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V, AV_{SS} = 0 V, Reference voltage (+) = AV_{DD}, Reference voltage (–) = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}		2.4 V ≤ AV_{DD} ≤ 3.6 V	8		12	bit
Overall error[Note 1]	AINL	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±8.5	LSB
Conversion time	t_{CONV}	ADTYP = 0, 12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V	4.125			μs
Zero-scale error[Note 1]	E_{ZS}	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±8.0	LSB
Full-scale error[Note 1]	E_{FS}	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±8.0	LSB
Integral linearity error[Note 1]	ILE	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±3.5	LSB
Differential linearity error[Note 1]	DLE	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±2.5	LSB
Analog input voltage	V_{AIN}			0		AV_{DD} and EV_{DD0}	V
		Interanal reference voltage (2.4 V ≤ V_{DD} ≤ 3.6 V, HS (high-speed main) mode)		V_{BGR}[Note 2]			V
		Temperature sensor output voltage (2.4 V ≤ V_{DD} ≤ 3.6 V, HS (high-speed main) mode)		V_{TMPS25}[Note 2]			V

Notes 1. Excludes quantization error (±1/2 LSB).

2. See **3.6.2 Temperature sensor, internal reference voltage output characteristics**.

<R> **(5) When reference voltage (+) = Internal reference voltage (1.45 V) (ADREFP1 = 1, ADREFP0 = 0), reference voltage (–) = AV_{SS} (ADREFM = 0), target for conversion: ANI0 to ANI12, ANI16 to ANI30**

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 3.6 V, 2.4 V ≤ EV_{DD} ≤ V_{DD}, 2.4 V ≤ AV_{DD} ≤ V_{DD}, V_{SS} = EV_{SS0} = 0 V, AV_{SS} = 0 V, Reference voltage (+) = Internal reference voltage, Reference voltage (–) = AV_{SS} = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}			8		bit
Conversion time	t_{CONV}	8-bit resolution	16.0			μs
Zero-scale error[Note]	E_{ZS}	8-bit resolution			±4.0	LSB
Integral linearity error[Note]	ILE	8-bit resolution			±2.0	LSB
Differential linearity error[Note]	DLE	8-bit resolution			±2.5	LSB
Reference voltage (+)	$AV_{REF(+)}$	= Internal reference voltage (V_{BGR})	1.38	1.45	1.50	V
Analog input voltage	V_{AIN}		0		V_{BGR}	V

Note Excludes quantization error (±1/2 LSB).

3.6.2 Temperature sensor, internal reference voltage output characteristics

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V, HS (high-speed main) mode)

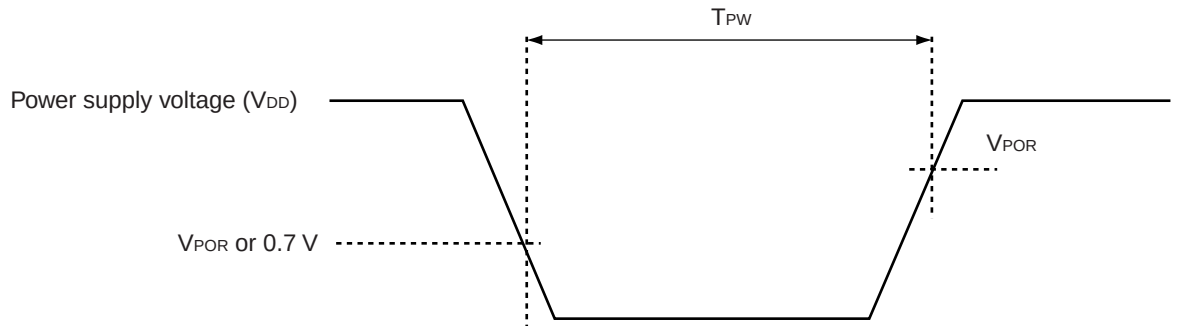
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V_{TMPS25}	Setting ADS register = 80H, T_A = +25°C		1.05		V
Internal reference voltage	V_{BGR}	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	F_{VTMPS}	Temperature sensor output voltage that depends on the temperature		–3.6		mV/°C
Operation stabilization wait time	t_{AMP}		10			μs

3.6.3 POR circuit characteristics

(T_A = –40 to +105°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POR}	Power supply rise time	1.45	1.51	1.57	V
	V_{PDR}	Power supply fall time	1.44	1.50	1.56	V
Minimum pulse width[Note]	T_{PW}		300			μs

Note This is the time required for the POR circuit to execute a reset when V_{DD} falls below V_{PDR}. When the microcontroller enters STOP mode or if the main system clock (f_{MAIN}) has been stopped by setting bit 0 (HIOSTOP) and bit 7 (MSTOP) of the clock operation status control register (CSC), this is the time required for the POR circuit to execute a reset before V_{DD} rises to V_{POR} after having fallen below 0.7 V.



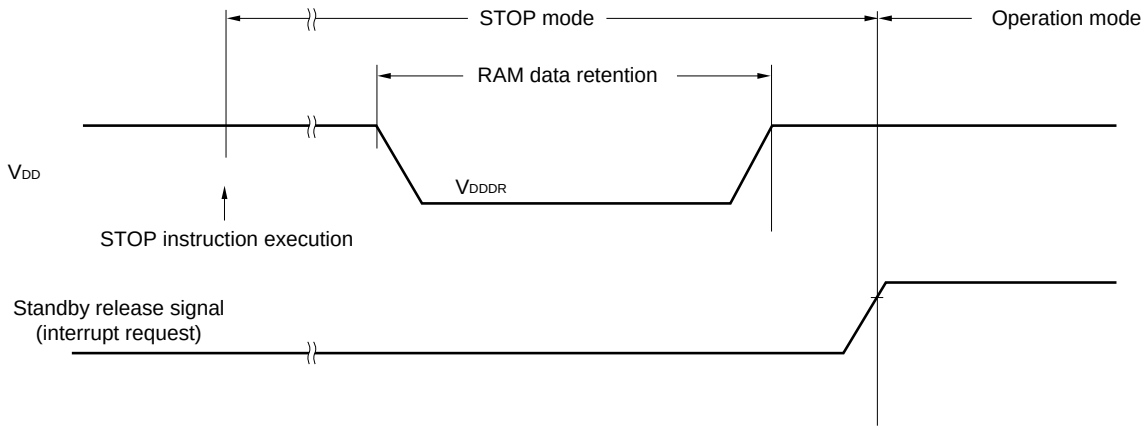
<R> 3.7 RAM Data Retention Characteristics

<R> **(T_A = –40 to +105°C, V_{SS} = 0 V)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.44[Note]		3.6	V

<R> **Note** This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.

<R>



3.8 Flash Memory Programming Characteristics

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CPU/peripheral hardware clock frequency	f_{CLK}	2.4 V ≤ V_{DD} ≤ 3.6 V	1		32	MHz
Number of code flash rewrites[Notes 1, 2, 3]	C_{erwr}	Retained for 20 years T_A = 85°C	1,000			Times
Number of data flash rewrites[Notes 1, 2, 3]		Retained for 1 years T_A = 25°C		1,000,000		
		Retained for 5 years T_A = 85°C	100,000			
		Retained for 20 years T_A = 85°C	10,000			

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite.
The retaining years are until next rewrite after the rewrite.

2. When using flash memory programmer and Renesas Electronics self programming library

3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

<R> **4.** This temperature is the average value at which data are retained.