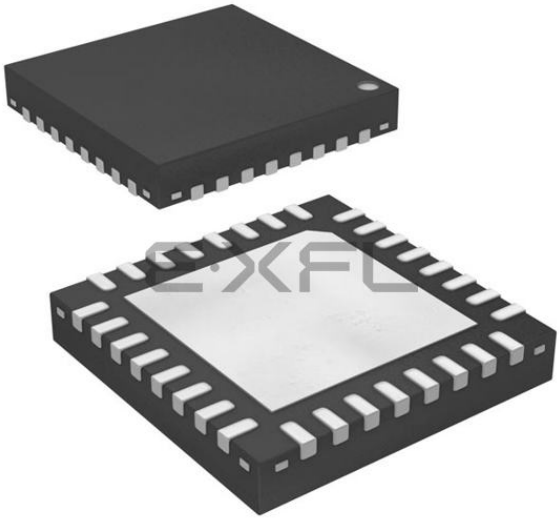
Renesas Electronics America Inc - R5F10EBAANA#U0 Datasheet



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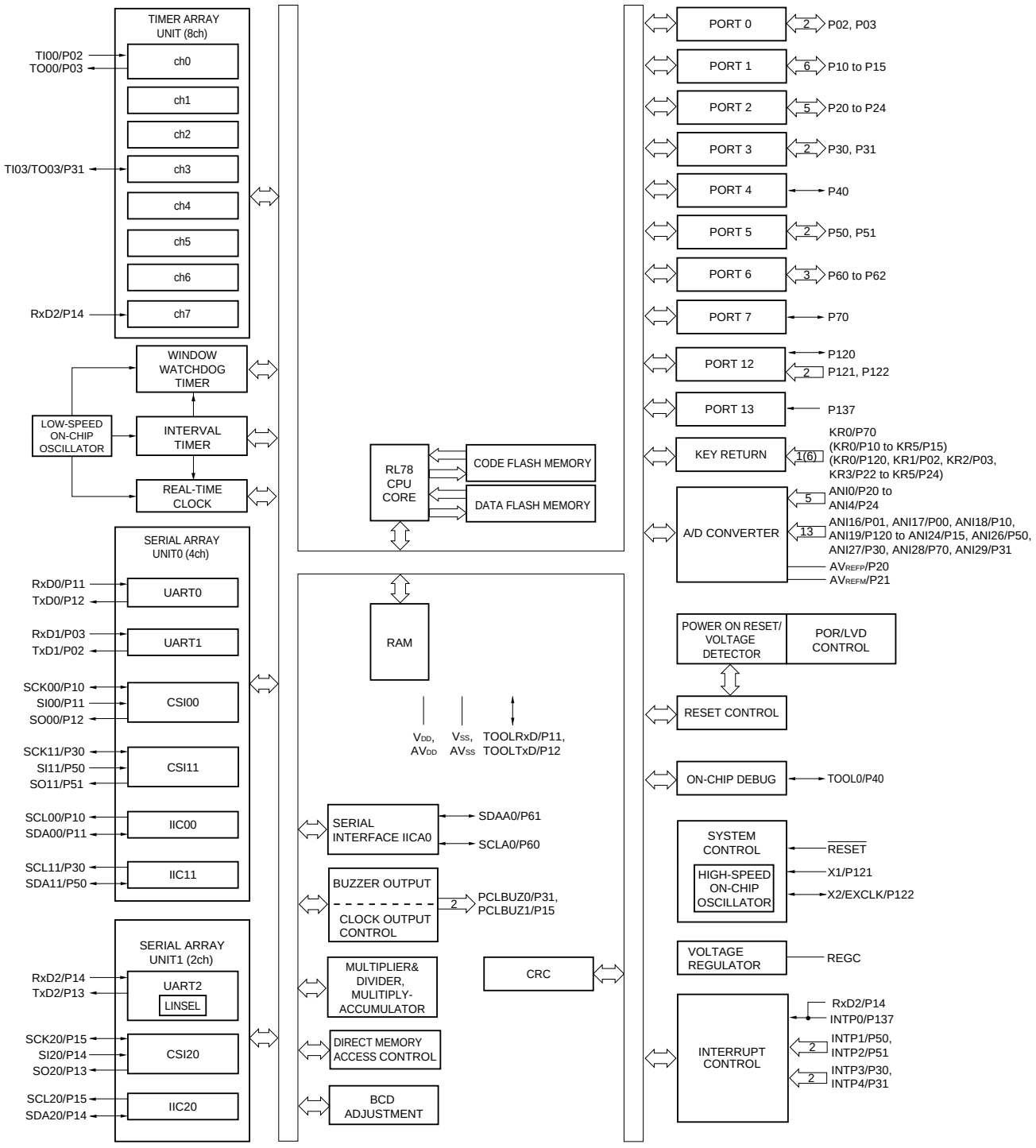
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

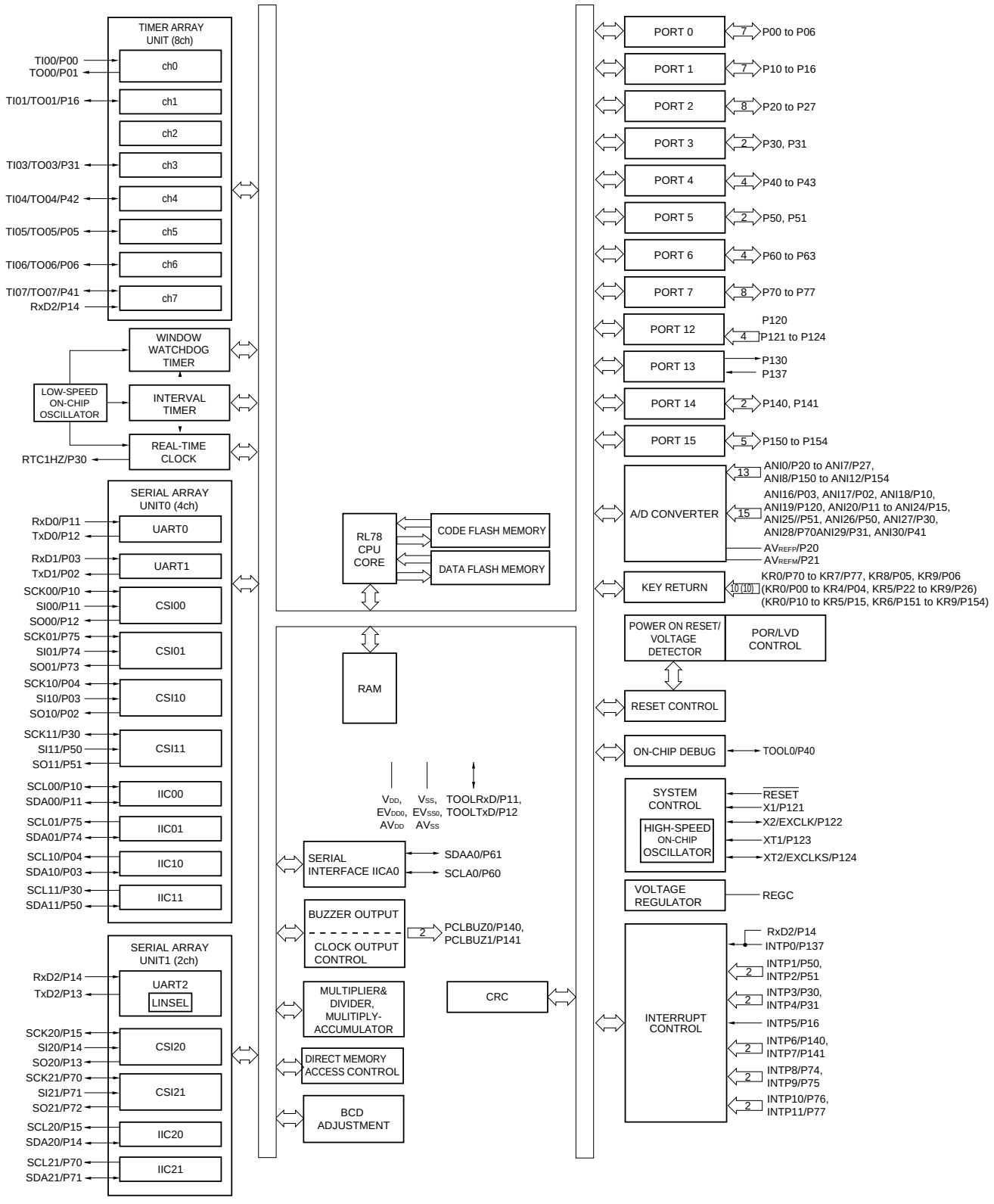
Details	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	20
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 18x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-WFQFN Exposed Pad
Supplier Device Package	32-HWQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10ebaana-u0

<R> 1.5.2 32-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.5.4 64-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

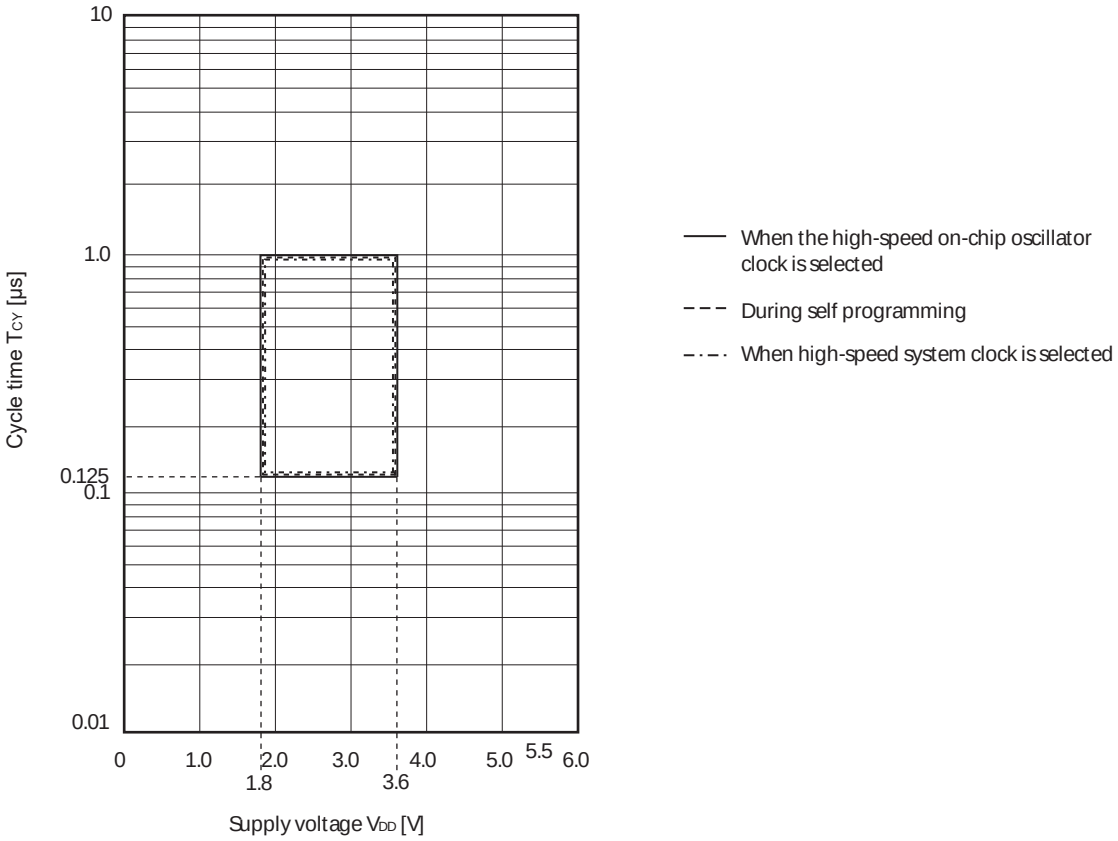
2.3.2 Supply current characteristics

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V) **(1/3)**

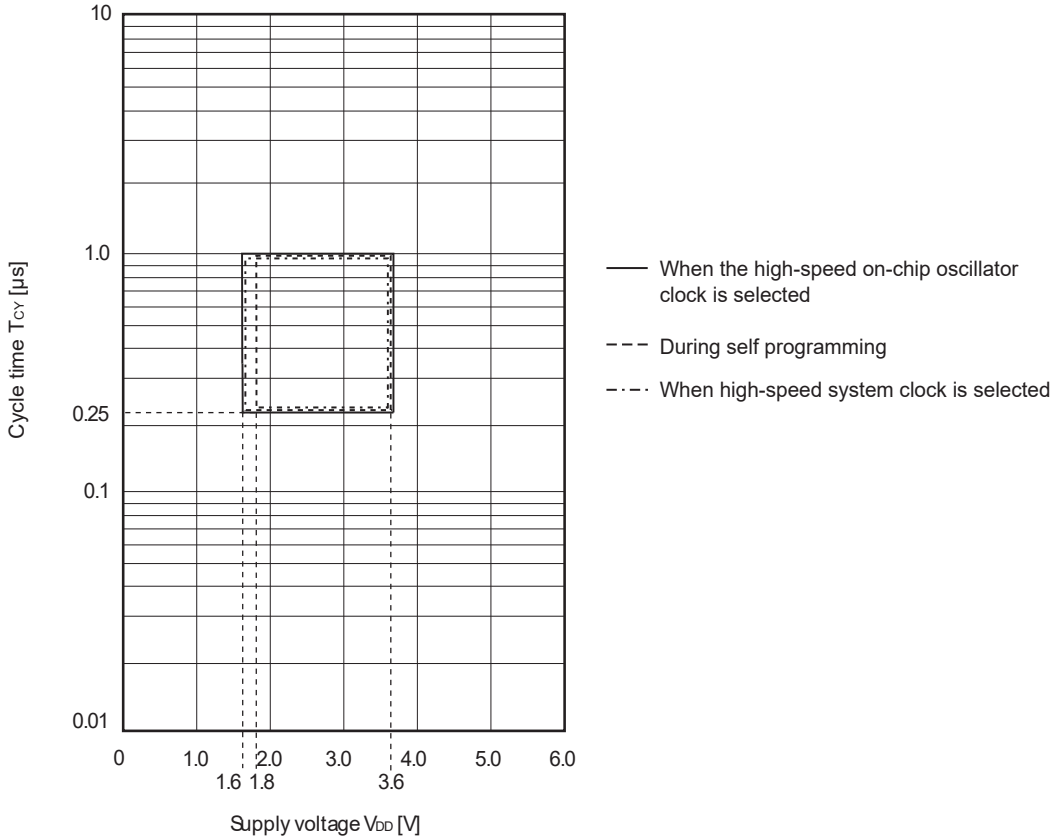
Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current[Note 1]	I_{DD1}	Operating mode	HS (high-speed main) mode[Note 5]	f_{IH} = 32 MHz[Note 3]	Basic operation	V_{DD} = 3.0 V		2.1		mA
					Normal operation	V_{DD} = 3.0 V		4.6	7.0	mA
				f_{IH} = 24 MHz[Note 3]	Normal operation	V_{DD} = 3.0 V		3.7	5.5	mA
				f_{IH} = 16 MHz[Note 3]	Normal operation	V_{DD} = 3.0 V		2.7	4.0	mA
			LS (low-speed main) mode[Note 5]	f_{IH} = 8 MHz[Note 3]	Normal operation	V_{DD} = 3.0 V		1.2	1.8	mA
						V_{DD} = 2.0 V		1.2	1.8	
			LV (Low-voltage main) mode[Note 5]	f_{IH} = 4 MHz[Note 3]	Normal operation	V_{DD} = 3.0 V		1.2	1.7	mA
						V_{DD} = 2.0 V		1.2	1.7	
			HS (high-speed main) mode[Note 5]	f_{MX} = 20 MHz[Note 2], V_{DD} = 3.0 V	Normal operation	Square wave input		3.0	4.6	mA
						Resonator connection		3.2	4.8	
				f_{MX} = 10 MHz[Note 2], V_{DD} = 3.0 V	Normal operation	Square wave input		1.9	2.7	mA
						Resonator connection		1.9	2.7	
			LS (low-speed main) mode[Note 5]	f_{MX} = 8 MHz[Note 2], V_{DD} = 3.0 V	Normal operation	Square wave input		1.1	1.7	mA
						Resonator connection		1.1	1.7	
				f_{MX} = 8 MHz[Note 2], V_{DD} = 2.0 V	Normal operation	Square wave input		1.1	1.7	mA
						Resonator connection		1.1	1.7	
			Subsystem clock mode	f_{SUB} = 32.768 kHz[Note 4] T_A = –40°C	Normal operation	Square wave input		4.1	4.9	μA
						Resonator connection		4.2	5.0	
				f_{SUB} = 32.768 kHz[Note 4] T_A = +25°C	Normal operation	Square wave input		4.2	4.9	μA
						Resonator connection		4.3	5.0	
				f_{SUB} = 32.768 kHz[Note 4] T_A = +50°C	Normal operation	Square wave input		4.3	5.5	μA
						Resonator connection		4.4	5.6	
				f_{SUB} = 32.768 kHz[Note 4] T_A = +70°C	Normal operation	Square wave input		4.5	6.3	μA
						Resonator connection		4.6	6.4	
				f_{SUB} = 32.768 kHz[Note 4] T_A = +85°C	Normal operation	Square wave input		4.8	7.7	μA
						Resonator connection		4.9	7.8	

(**Notes** and **Remarks** are listed on the next page.)

<R> T_{CY} vs V_{DD} (LS (low-speed main) mode)



<R> T_{CY} vs V_{DD} (LV (low-voltage main) mode)



(5) During communication at same potential (simplified I^2C mode) (2/2)

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions	HS[Note 1]		LS[Note 2]		LV[Note 3]		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data hold time (transmission)	$t_{HD:DAT}$	2.7 V ≤ EV_{DD0} ≤ 3.6 V, C_b = 50 pF, R_b = 2.7 kΩ	0	305	0	305	0	305	ns
		1.8 V ≤ EV_{DD0} ≤ 3.6 V, C_b = 100 pF, R_b = 3 kΩ	0	355	0	355	0	355	ns
		1.8 V ≤ EV_{DD0} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	0	405	0	405	0	405	ns
		1.7 V ≤ EV_{DD0} ≤ 1.8 V, C_b = 100 pF, R_b = 5 kΩ	0	405	0	405	0	405	ns
		1.6 V ≤ EV_{DD0} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	–	–	0	405	0	405	ns

Notes 1. HS is condition of HS (high-speed main) mode.

2. LS is condition of LS (low-speed main) mode.

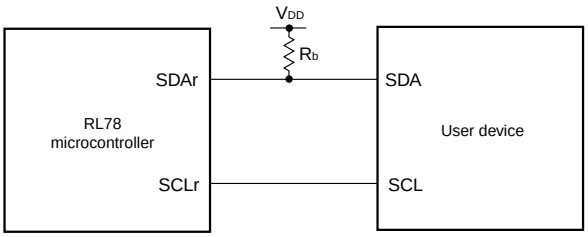
3. LV is condition of LV (low-voltage main) mode.

4. The value must also be f_{CLK}/4 or lower.

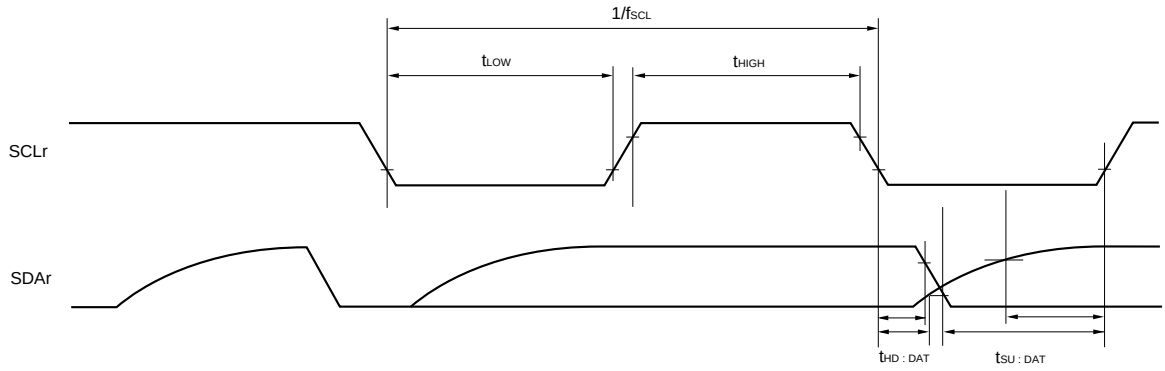
5. Set the f_{MCK} value to keep the hold time of SCLr = “L” and SCLr = “H”.

Caution Select the normal input buffer and the N-ch open drain output (V_{DD} tolerance (When 25- to 48-pin products)/EV_{DD} tolerance (When 64-pin products)) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).

Simplified I^2C mode mode connection diagram (during communication at same potential)



Simplified I^2C mode serial transfer timing (during communication at same potential)

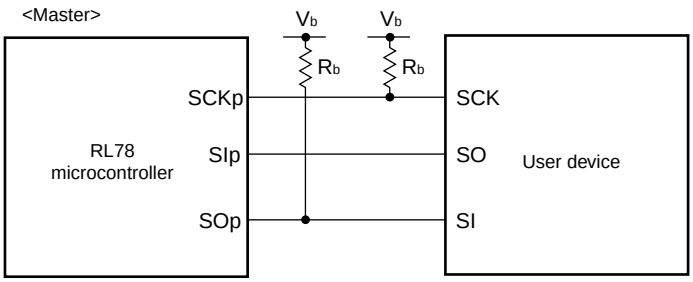


Remarks 1. R_b[Ω]: Communication line (SDAr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance

2. r: IIC number (r = 00, 01, 10, 11, 20, 21), g: PIM number (g = 0, 1), h: POM number (h = 0, 1)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number, mn = 00 to 03, 10, 11)

CSI mode connection diagram (during communication at different potential)

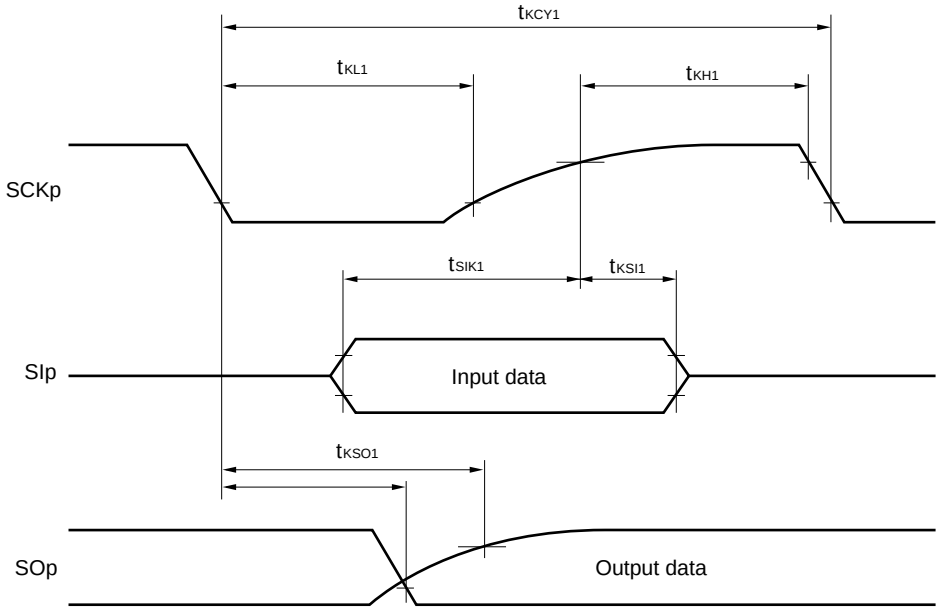


Remarks 1. R_b[Ω]: Communication line (SCKp, SOp) pull-up resistance, C_b[F]: Communication line (SCKp, SOp) load capacitance, V_b[V]: Communication line voltage

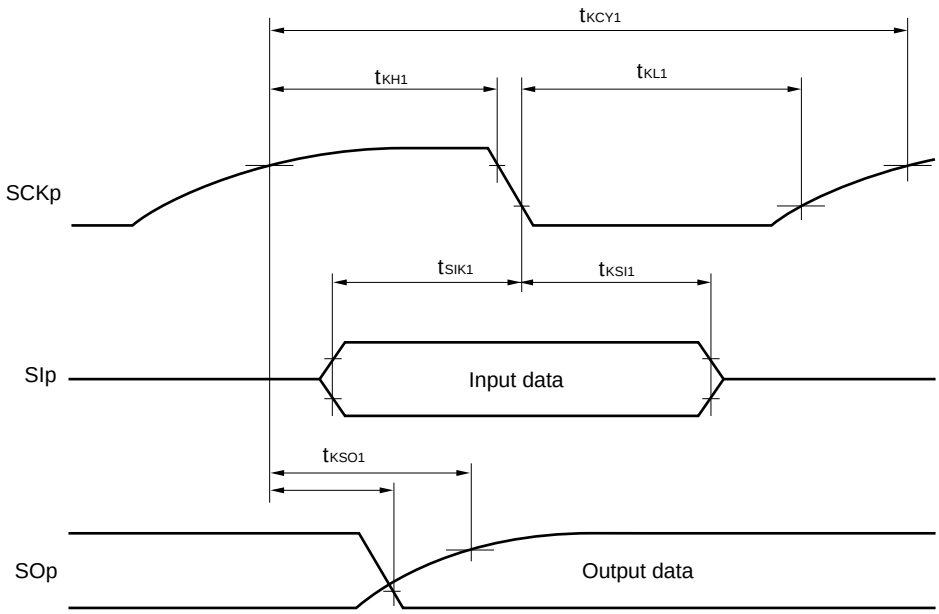
2. p: CSI number (p = 00, 10, 20), m: Unit number , n: Channel number (mn = 00, 02, 10), g: PIM and POM number (g = 0, 1)

3. CSI01, CSI11, and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remarks 1. p: CSI number (p = 00, 10, 20), m: Unit number, n: Channel number (m = 00, 02, 10), g: PIM and POM number (g = 0, 1)

2. CSI01, CSI11, and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

(2) I^2C fast mode, fast mode plus

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions	Fast Mode[Note 7]						Fast Mode Plus[Note 8]		Unit
			HS[Note 2]		LS[Note 3]		LV[Note 4]		HS[Note 2]		
			MIN.	MAX.	MIN.	MIN.	MAX.	MIN.	MAX.	MIN.	
SCLA0 clock frequency	f_{SCL}	2.7 V ≤ EV_{DD0} ≤ 3.6 V	0	400	0	400	0	400	0	1000	kHz
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	0	400	0	400	0	400	–		
Setup time of restart condition	$t_{SU:STA}$	2.7 V ≤ EV_{DD0} ≤ 3.6 V	0.6		0.6		0.6		0.26		μs
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	0.6		0.6		0.6		–		
Hold time[Note 5]	$t_{HD:STA}$	2.7 V ≤ EV_{DD0} ≤ 3.6 V	0.6		0.6		0.6		0.26		μs
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	0.6		0.6		0.6		–		
Hold time when SCLA0 = “L”	t_{LOW}	2.7 V ≤ EV_{DD0} ≤ 3.6 V	1.3		1.3		1.3		0.5		μs
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	1.3		1.3		1.3		–		
Hold time when SCLA0 = “H”	t_{HIGH}	2.7 V ≤ EV_{DD0} ≤ 3.6 V	0.6		0.6		0.6		0.26		μs
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	0.6		0.6		0.6		–		
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ EV_{DD0} ≤ 3.6 V	100		100		100		50		ns
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	100		100		100		–		
Data hold time (transmission)[Note 6]	$t_{HD:DAT}$	2.7 V ≤ EV_{DD0} ≤ 3.6 V	0	0.9	0	0.9	0	0.9	0	450	μs
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	0	0.9	0	0.9	0	0.9	–		
Setup time of stop condition	$t_{SU:STO}$	2.7 V ≤ EV_{DD0} ≤ 3.6 V	0.6		0.6		0.6		0.26		μs
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	0.6		0.6		0.6		–		
Bus-free time	t_{BUF}	2.7 V ≤ EV_{DD0} ≤ 3.6 V	1.3		1.3		1.3		0.5		μs
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	1.3		1.3		1.3		–		

Notes 1. In normal mode, use it with f_{CLK} ≥ 1 MHz, 1.6 V ≤ EV_{DD} ≤ 3.6 V.

2. HS is condition of HS (high-speed main) mode.

3. LS is condition of LS (low-speed main) mode.

4. LV is condition of LV (low-voltage main) mode.

5. The first clock pulse is generated after this period when the start/restart condition is detected.

6. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

7. In fast mode, use it with f_{CLK} ≥ 3.5 MHz, 1.8 V ≤ EV_{DD} ≤ 3.6 V.

8. In fast mode plus, use it with f_{CLK} ≥ 10 MHz, 2.7 V ≤ EV_{DD} ≤ 3.6 V.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C_b = 400 pF, R_b = 2.7 kΩ

Fast mode: C_b = 320 pF, R_b = 1.1 kΩ

Fast mode plus: C_b = 120 pF, R_b = 1.1 kΩ

<R> **(4) When reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = AV_{REFM}/ANI1 (ADREFM = 1), target for conversion: ANI16 to ANI30, interanal reference voltage, temperature sensor output voltage**

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, 1.6 V ≤ AV_{REFP} ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V, AV_{SS} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (–) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}		2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V	8		12	bit
			1.8 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V	8		10 Note 1	
			1.6 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V	8 Note 2			
Overall error Note 3	AINL	12-bit resolution	2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±7.0	LSB
		10-bit resolution	1.8 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±5.5	
		8-bit resolution	1.6 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±3.0	
Conversion time	t_{CONV}	ADTYP = 0, 12-bit resolution	2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V	4.125			μs
		ADTYP = 0, 10-bit resolution Note 1	1.8 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V	9.5			
		ADTYP = 0, 8-bit resolution Note 2	1.6 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V	57.5			
		ADTYP = 1, 8-bit resolution	2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V	3.3125			
			1.8 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V	7.875			
			1.6 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V	54.25			
Zero-scale error Note 3	E_{ZS}	12-bit resolution	2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±5.0	LSB
		10-bit resolution	1.8 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±5.0	
		8-bit resolution	1.6 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±2.5	
Full-scale error Note 3	E_{FS}	12-bit resolution	2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±5.0	LSB
		10-bit resolution	1.8 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±5.0	
		8-bit resolution	1.6 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±2.5	
Integral linearity error Note 3	ILE	12-bit resolution	2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±3.0	LSB
		10-bit resolution	1.8 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±2.0	
		8-bit resolution	1.6 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±1.5	
Differential linearity error Note 3	DLE	12-bit resolution	2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±2.0	LSB
		10-bit resolution	1.8 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±2.0	
		8-bit resolution	1.6 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±1.5	
Analog input voltage	V_{AIN}			0		AV_{REFP} and EV_{DD0}	V
		Interanal reference voltage (2.4 V ≤ V_{DD} ≤ 3.6 V, HS (high-speed main) mode)		V_{BGR} Note 4			V
		Temperature sensor output voltage (2.4 V ≤ V_{DD} ≤ 3.6 V, HS (high-speed main) mode)		V_{TMPS25} Note 4			V

Notes 1. Cannot be used for lower 2 bit of ADCR register

2. Cannot be used for lower 4 bit of ADCR register

3. Excludes quantization error (±1/2 LSB).

4. See **2.6.2 Temperature sensor, internal reference voltage output characteristics**.

<R> **(6) When reference voltage (+) = Internal reference voltage (1.45 V) (ADREFP1 = 1, ADREFP0 = 0), reference voltage (–) = AV_{SS} (ADREFM = 0), target ANI pin: ANI0 to ANI12, ANI16 to ANI30**

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} ≤ 3.6 V, 1.6 V ≤ EV_{DD} ≤ V_{DD}, 1.6 V ≤ AV_{DD} ≤ V_{DD}, V_{SS} = EV_{SS0} = 0 V, AV_{SS} = 0 V, Reference voltage (+) = Internal reference voltage, Reference voltage (–) = AV_{SS} = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}			8		bit
Conversion time	t_{CONV}	8-bit resolution	16			μs
Zero-scale error[Note]	E_{ZS}	8-bit resolution			±4.0	LSB
Integral linearity error[Note]	ILE	8-bit resolution			±2.0	LSB
Differential linearity error[Note]	DLE	8-bit resolution			±2.5	LSB
Reference voltage (+)	$AV_{REF(+)}$	= Internal reference voltage (V_{BGR})	1.38	1.45	1.5	V
Analog input voltage	V_{AIN}		0		V_{BGR}	V

Note Excludes quantization error (±1/2 LSB).

2.6.2 Temperature sensor, internal reference voltage output characteristics

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V, HS (high-speed main) mode)

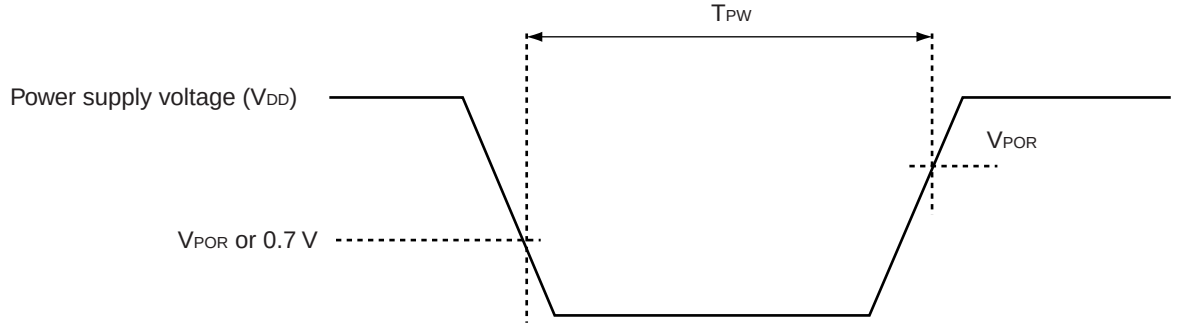
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V_{TMPS25}	Setting ADS register = 80H, T_A = +25°C		1.05		V
Internal reference voltage	V_{BGR}	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	F_{VTMPS}	Temperature sensor output voltage that depends on the temperature		–3.6		mV/°C
Operation stabilization wait time	t_{AMP}		10			μs

2.6.3 POR circuit characteristics

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POR}	Power supply rise time	1.47	1.51	1.55	V
	V_{PDR}	Power supply fall time	1.46	1.50	1.54	V
Minimum pulse width[Note]	T_{PW}		300			μs

Note This is the time required for the POR circuit to execute a reset when V_{DD} falls below V_{PDR}. When the microcontroller enters STOP mode or if the main system clock (f_{MAIN}) has been stopped by setting bit 0 (HIOSTOP) and bit 7 (MSTOP) of the clock operation status control register (CSC), this is the time required for the POR circuit to execute a reset before V_{DD} rises to V_{POR} after having fallen below 0.7 V.



3.3 DC Characteristics

3.3.1 Pin characteristics

<R> **(T_A = –40 to +105°C, 2.4 V ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V, 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)** **(1/5)**

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high[Note 1]	I_{OH1}	Per pin for P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P130, P140, P141	2.4 V ≤ EV_{DD0} ≤ 3.6 V			–3.0[Note 2]	mA
		Total of P00 to P04, P40 to P43, P120, P130, P140, P141 (When duty ≤ 70%[Note 3])	2.7 V ≤ EV_{DD0} ≤ 3.6 V			–10.0	mA
			2.4 V ≤ EV_{DD0} < 2.7 V			–5.0	mA
		Total of P05, P06, P10 to P16, P30, P31, P50, P51, P70 to P77, (When duty ≤ 70%[Note 3])	2.7 V ≤ EV_{DD0} ≤ 3.6 V			–19.0	mA
			2.4 V ≤ EV_{DD0} < 2.7 V			–10.0	mA
		Total of all pins (When duty ≤ 70%[Note 3])	2.4 V ≤ EV_{DD0} ≤ 3.6 V			–29.0	mA
	I_{OH2}	Per pin for P20 to P27, P150 to P154	2.4 V ≤ AV_{DD} ≤ 3.6 V			–0.1[Note 2]	mA
		Total of all pins (When duty ≤ 70%[Note 3])	2.4 V ≤ AV_{DD} ≤ 3.6 V			–1.3	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from the EV_{DD0}, V_{DD} pins to an output pin.

2. However, do not exceed the total current value.

3. Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OH} = –10.0 mA
Total output current of pins = (–10.0 × 0.7)/(80 × 0.01) ≅ –8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Caution P00, P02 to P04, P10 to P15, P43, P50, P71, and P74 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCKp cycle time	t_{KCY1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V	t_{KCY1} ≥ 4/f_{CLK}	250			ns
		2.4 V ≤ EV_{DD0} ≤ 3.6 V	t_{KCY1} ≥ 4/f_{CLK}	500			ns
SCKp high-/low-level width	t_{KH1}, t_{KL1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V		t_{KCY1}/2 – 36			ns
		2.4 V ≤ EV_{DD0} ≤ 3.6 V		t_{KCY1}/2 – 76			ns
SIp setup time (to SCKp↑)[Note 1]	t_{SIK1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V		66			ns
		2.4 V ≤ EV_{DD0} ≤ 3.6 V		113			ns
SIp hold time (from SCKp↑)[Note 1]	t_{KSI1}			38			ns
Delay time from SCKp↓ to SOp output[Note 2]	t_{KSO1}	C = 30 p[Note 3]				50	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time or SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark p: CSI number (p = 00, 01, 10, 11, 20, 21), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 1)

(5) Communication at different potential (1.8 V, 2.5 V) (UART mode) (dedicated baud rate generator output) (1/2)

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Transfer rate[Note 1]		Reception	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V				f_{MCK}/12	bps
				Theoretical value of the maximum transfer rate f_{CLK} = 32 MHz, f_{MCK} = f_{CLK}			2.6	Mbps
			2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V				f_{MCK}/12	bps
				Theoretical value of the maximum transfer rate f_{CLK} = 32 MHz, f_{MCK} = f_{CLK}			2.6[Note 2]	Mbps

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps.

2. The following conditions are required for low-voltage interface when EV_{DD0} < V_{DD}.
2.4 V ≤ EV_{DD0} < 2.7 V : MAX. 1.3 Mbps

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (When 25- to 48-pin products)/EV_{DD} tolerance (When 64-pin products)) mode for the TxDq pin by using <R> **port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.**

Remarks 1. V_b[V]: Communication line voltage

2. q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10, 11)

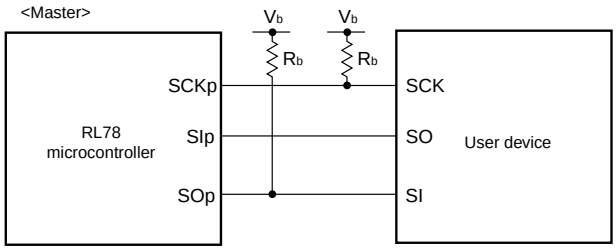
(6) Communication at different potential (1.8 V, 2.5 V) (CSI mode) (master mode, SCKp... internal clock output) (2/2)
(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SIp setup time (to SCKp↑)Note 1	t_{SIK1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	354			ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	958			ns
SIp hold time (from SCKp↑)Note 1	t_{KSI1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	38			ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	38			ns
Delay time from SCKp↓ to SOp outputNote 1	t_{KSO1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ			390	ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ			966	ns
SIp setup time (to SCKp↓)Note 2	t_{SIK1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	88			ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	220			ns
SIp hold time (from SCKp↓)Note 2	t_{KSI1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	38			ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	38			ns
Delay time from SCKp↑ to SOp outputNote 2	t_{KSO1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ			50	ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ			50	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (When 25- to 48-pin products)/EV_{DD} tolerance (When 64-pin products)) mode for the SOp pin and SCKp <R> **pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.**

CSI mode connection diagram (during communication at different potential)



Remarks 1. R_b[Ω]: Communication line (SCKp, SOp) pull-up resistance, C_b[F]: Communication line (SCKp, SOp) load capacitance, V_b[V]: Communication line voltage
2. p: CSI number (p = 00, 10, 20), m: Unit number , n: Channel number (mn = 00, 02, 10), g: PIM and POM number (g = 0, 1)
3. CSI01, CSI11, and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

(8) Communication at different potential (1.8 V, 2.5 V) (simplified I^2C mode) (1/2)

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCLr clock frequency	f_{SCL}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ		400 Note 1	kHz
		2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ		100 Note 1	kHz
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 100 pF, R_b = 5.5 kΩ		100 Note 1	kHz
Hold time when SCLr = “L”	t_{LOW}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	1200		ns
		2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	4600		ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 100 pF, R_b = 5.5 kΩ	4650		ns
Hold time when SCLr = “H”	t_{HIGH}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	500		ns
		2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	2400		ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 100 pF, R_b = 5.5 kΩ	1830		ns

(**Notes**, **Caution** and **Remarks** are listed on the next page.)

3.6 Analog Characteristics

3.6.1 A/D converter characteristics

Division of A/D Converter Characteristics

Reference voltag / Input channel	Reference voltage (+) = AV_{REFP} Reference voltage (–) = AV_{REFM}	Reference voltage (+) = AV_{DD} Reference voltage (–) = AV_{SS}	Reference voltage (+) = Internal refrence voltage Reference voltage (–) = AV_{SS}
High-accuracy channel; ANI0 to ANI12 (input buffer power supply: AV_{DD})	See **3.6.1 (1)**	See **3.6.1 (2)**	See **3.6.1 (5)**
Standard channel; ANI16 to ANI30 (input buffer power supply: V_{DD} or EV_{DD0})	See **3.6.1 (3)**	See **3.6.1 (4)**	
Temperature sensor, internal reference voltage output	See **3.6.1 (3)**	See **3.6.1 (4)**	–

<R> **(1) When reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = AV_{REFM}/ANI1 (ADREFM = 1), target for conversion: ANI2 to ANI12**

(T_A = –40 to +105°C, 2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V, AV_{SS} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (–) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}		2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V	8.		12.	bit
Overall error[Note]	AINL	12-bit resolution	2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±6.0	LSB
Conversion time	t_{CONV}	ADTYP = 0, 12-bit resolution	2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V	3.375			μs
Zero-scale error[Note]	E_{ZS}	12-bit resolution	2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±4.5	LSB
Full-scale error[Note]	E_{FS}	12-bit resolution	2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±4.5	LSB
Integral linearity error[Note]	ILE	12-bit resolution	2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±2.0	LSB
Differential linearity error[Note]	DLE	12-bit resolution	2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±1.5	LSB
Analog input voltage	V_{AIN}			0		AV_{REFP}	V

Note Excludes quantization error (±1/2 LSB).

<R> **(2) When reference voltage (+) = AV_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) = AV_{SS} (ADREFM = 0), target for conversion: ANI0 to ANI12**

(T_A = –40 to +105°C, 2.4 V ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V, AV_{SS} = 0 V, Reference voltage (+) = AV_{DD}, Reference voltage (–) = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}		2.4 V ≤ AV_{DD} ≤ 3.6 V	8		12	bit
Overall error[Note]	AINL	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±7.5	LSB
Conversion time	t_{CONV}	ADTYP = 0, 12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V	3.375			μs
Zero-scale error[Note]	E_{ZS}	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±6.0	LSB
Full-scale error[Note]	E_{FS}	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±6.0	LSB
Integral linearity error[Note]	ILE	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±3.0	LSB
Differential linearity error[Note]	DLE	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±2.0	LSB
Analog input voltage	V_{AIN}			0		AV_{DD}	V

Note Excludes quantization error (±1/2 LSB).

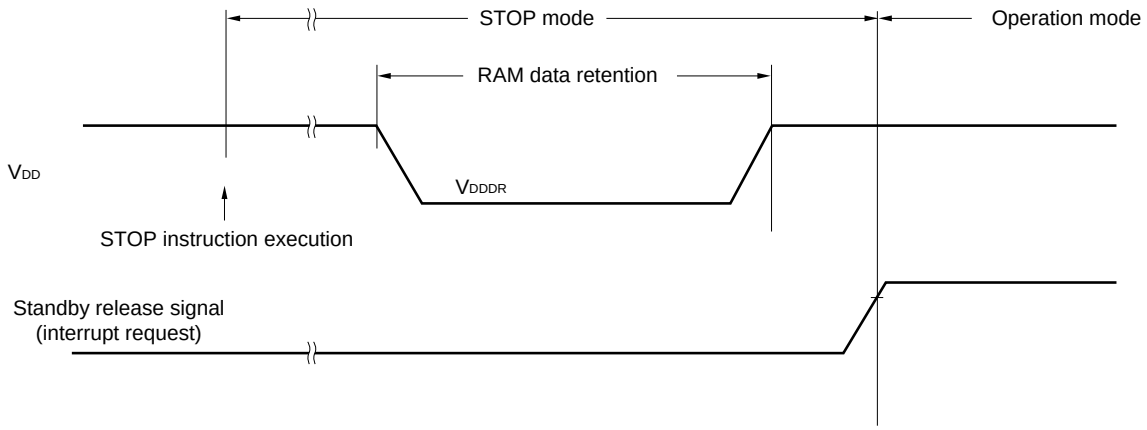
<R> 3.7 RAM Data Retention Characteristics

<R> **(T_A = –40 to +105°C, V_{SS} = 0 V)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.44[Note]		3.6	V

<R> **Note** This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.

<R>



3.8 Flash Memory Programming Characteristics

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CPU/peripheral hardware clock frequency	f_{CLK}	2.4 V ≤ V_{DD} ≤ 3.6 V	1		32	MHz
Number of code flash rewrites[Notes 1, 2, 3]	C_{erwr}	Retained for 20 years T_A = 85°C	1,000			Times
Number of data flash rewrites[Notes 1, 2, 3]		Retained for 1 years T_A = 25°C		1,000,000		
		Retained for 5 years T_A = 85°C	100,000			
		Retained for 20 years T_A = 85°C	10,000			

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite.
The retaining years are until next rewrite after the rewrite.

2. When using flash memory programmer and Renesas Electronics self programming library

3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

<R> **4.** This temperature is the average value at which data are retained.

4. PACKAGE DRAWINGS

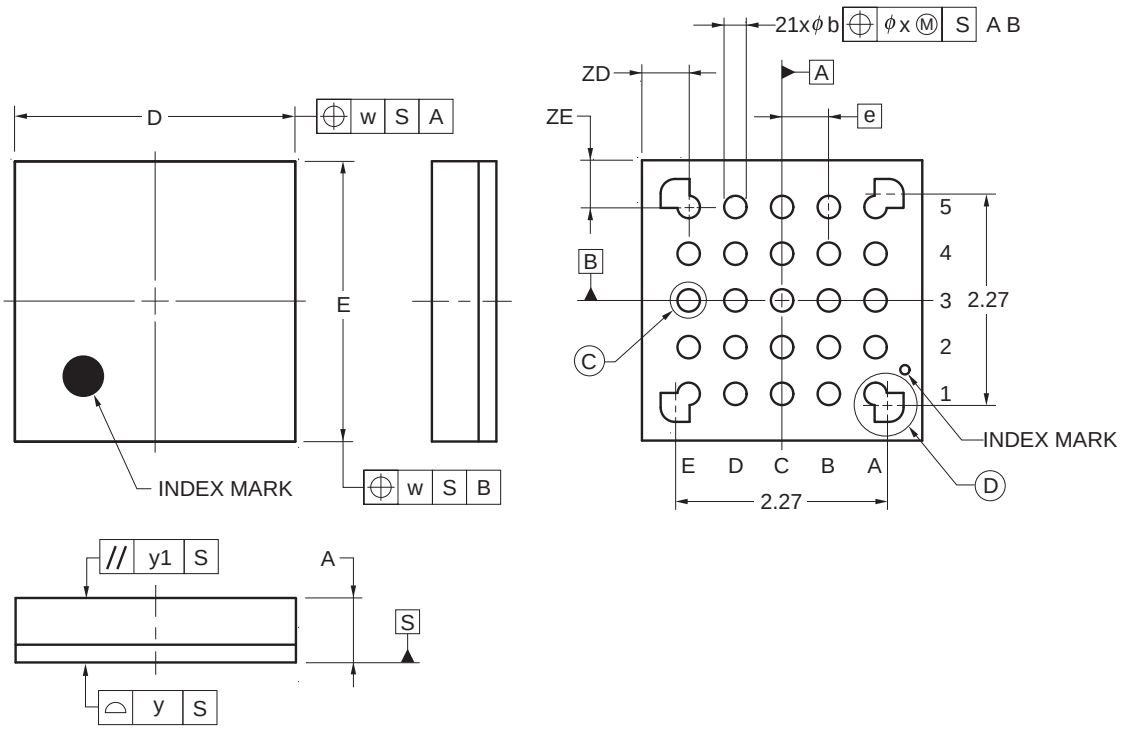
4.1 25-pin products

R5F10E8AALA, R5F10E8CALA, R5F10E8DALA, R5F10E8EALA

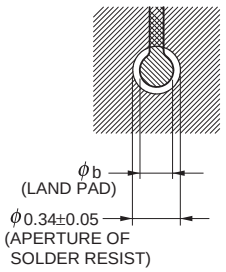
<R>

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-WFLGA25-3x3-0.50	PWLG0025KA-A	P25FC-50-2N2-3	0.01

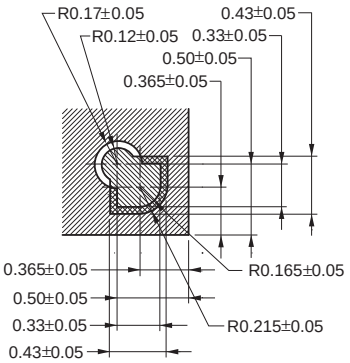
Unit: mm



DETAIL OF Ⓒ PART



DETAIL OF Ⓓ PART



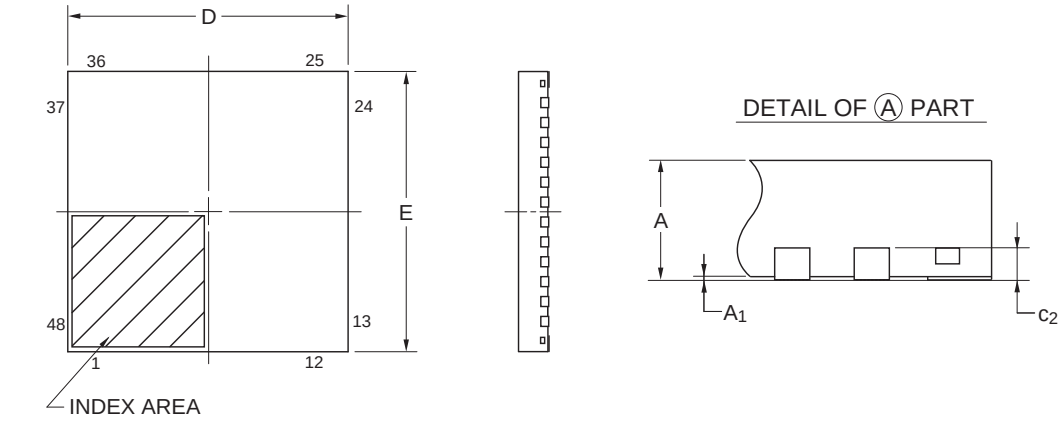
ITEM	DIMENSIONS
D	3.00±0.10
E	3.00±0.10
w	0.20
e	0.50
A	0.69±0.07
b	0.24±0.05
x	0.05
y	0.08
y1	0.20
ZD	0.50
ZE	0.50

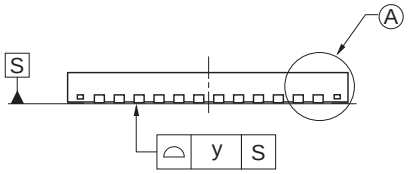
R5F10EGAANA, R5F10EGCANA, R5F10EGDANA, R5F10EGEANA
R5F10EGAGNA, R5F10EGCGNA, R5F10EGDGNA, R5F10EGEGNA

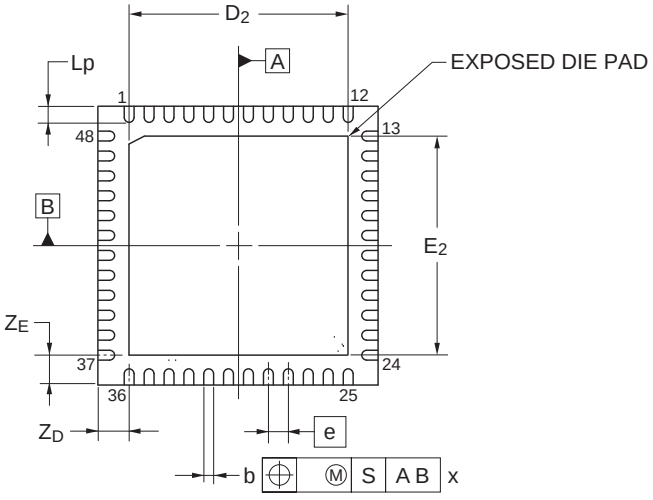
<R>

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-HWQFN48-7x7-0.50	PWQN0048KB-A	48PJN-A P48K8-50-5B4-7	0.13

Unit: mm







Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	6.95	7.00	7.05
E	6.95	7.00	7.05
A	—	—	0.80
A_1	0.00	—	—
b	0.18	0.25	0.30
e	—	0.50	—
Lp	0.30	0.40	0.50
x	—	—	0.05
y	—	—	0.05
Z_D	—	0.75	—
Z_E	—	0.75	—
c_2	0.15	0.20	0.25
D_2	—	5.50	—
E_2	—	5.50	—