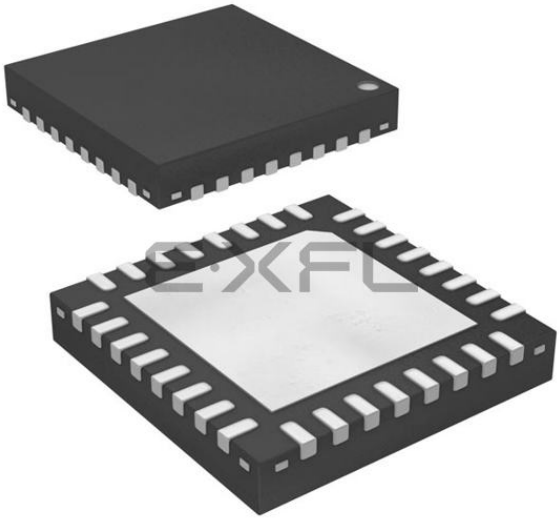
Renesas Electronics America Inc - R5F10EBCANA#U0 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	20
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 18x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-WFQFN Exposed Pad
Supplier Device Package	32-HWQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10ebcana-u0

<R> **Table 1-1. List of Ordering Part Numbers**

Pin count	Package	Fields of Application[Note]	Ordering Part Number
25 pins	25-pin plastic WFLGA (3 × 3 mm, 0.5 mm pitch)	A	R5F10E8AALA#U0, R5F10E8CALA#U0, R5F10E8DALA#U0, R5F10E8EALA#U0, R5F10E8AALA#W0, R5F10E8CALA#W0, R5F10E8DALA#W0, R5F10E8EALA#W0
		G	R5F10E8AGLA#U0, R5F10E8CGLA#U0, R5F10E8DGLA#U0, R5F10E8EGLA#U0, R5F10E8AGLA#W0, R5F10E8CGLA#W0, R5F10E8DGLA#W0, R5F10E8EGLA#W0
32 pins	32-pin plastic HWQFN (5 × 5 mm, 0.5 mm pitch)	A	R5F10EBAANA#U0, R5F10EBCANA#U0, R5F10EBDANA#U0, R5F10EBEANA#U0, R5F10EBAANA#W0, R5F10EBCANA#W0, R5F10EBDANA#W0, R5F10EBEANA#W0
		G	R5F10EBAGNA#U0, R5F10EBCGNA#U0, R5F10EBDGNA#U0, R5F10EBEGNA#U0, R5F10EBAGNA#W0, R5F10EBCGNA#W0, R5F10EBDGNA#W0, R5F10EBEGNA#W0
48 pins	48-pin plastic LFQFP (7 × 7 mm, 0.5 mm pitch)	A	R5F10EGAAFB#V0, R5F10EGCAFB#V0, R5F10EGDAFB#V0, R5F10EGEAFB#V0, R5F10EGAAFB#X0, R5F10EGCAFB#X0, R5F10EGDAFB#X0, R5F10EGEAFB#X0
		G	R5F10EBAGNA#V0, R5F10EBCGNA#V0, R5F10EBDGNA#V0, R5F10EBEGNA#V0, R5F10EBAGNA#X0, R5F10EBCGNA#X0, R5F10EBDGNA#X0, R5F10EBEGNA#X0
	48-pin plastic HWQFN (7 × 7 mm, 0.5 mm pitch)	A	R5F10EGAANA#U0, R5F10EGCANA#U0, R5F10EGDANA#U0, R5F10EGEANA#U0, R5F10EGAANA#W0, R5F10EGCANA#W0, R5F10EGDANA#W0, R5F10EGEANA#W0
		G	R5F10EGAGNA#U0, R5F10EGCGNA#U0, R5F10EGDGNA#U0, R5F10EGEGNA#U0, R5F10EGAGNA#W0, R5F10EGCGNA#W0, R5F10EGDGNA#W0, R5F10EGEGNA#W0
64 pins	64-pin plastic LFQFP (10 × 10 mm, 0.5 mm pitch)	A	R5F10ELCAFB#V0, R5F10ELDAFB#V0, R5F10ELEAFB#V0, R5F10ELCAFB#X0, R5F10ELDAFB#X0, R5F10ELEAFB#X0
		G	R5F10ELCGFB#V0, R5F10ELDGFB#V0, R5F10ELEGFB#V0, R5F10ELCGFB#X0, R5F10ELDGFB#X0, R5F10ELEGFB#X0
	64-pin plastic VFBGA (4 × 4 mm, 0.4 mm pitch)	A	R5F10ELCABG#U0, R5F10ELDABG#U0, R5F10ELEABG#U0, R5F10ELCABG#W0, R5F10ELDABG#W0, R5F10ELEABG#W0
		G	R5F10ELCGBG#U0, R5F10ELDGBG#U0, R5F10ELEGBG#U0, R5F10ELCGBG#W0, R5F10ELDGBG#W0, R5F10ELEGBG#W0

<R> **Note** For the fields of application, see **Figure 1-1 Part Number, Memory Size, and Package of RL78/G1A**.

Caution The part number above is valid as of when this manual was issued. For the latest part number, see the web page of the target product on the Renesas Electronics website.

1.3 Pin Configuration (Top View)

1.3.1 25-pin products

- 25-pin plastic WFLGA (3 × 3 mm, 0.50 mm pitch)

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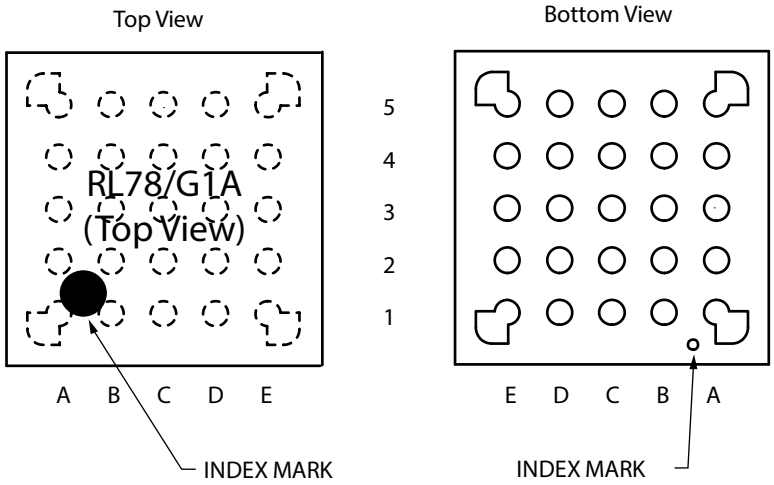

	A	B	C	D	E	
5	P40/TOOL0	$\overline{\text{RESET}}$	P03/ANI16/ RxD1/TO00/ (KR1)	P23/ANI3/ (KR3)	AV_{SS}	5
4	P122/X2/ EXCLK	P137/INTP0	P02/ANI17/ TxD1/TI00/ (KR0)	P22/ANI2/ (KR2)	AV_{DD}	4
3	P121/X1	V_{DD}	P21/ANI1/ AV_{REFM}	P11/ANI20/ SI00/SDA00/ RxD0/ TOOLRxD	P10/ANI18/ SCK00/SCL00	3
2	REGC	V_{SS}	P30/ANI27/ SCK11/SCL11/ INTP3	P51/ANI25/ SO11/INTP2	P50/ANI26/ SI11/SDA11 INTP1	2
1	P60/SCLA0	P61/SDAA0	P31/ANI29/TI03/ TO03/PCLBUZ0 /INTP4	P12/ANI21/ SO00/TxD0/ TOOLTxD	P20/ANI0/ AV_{REFP}	1
	A	B	C	D	E	

Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification**.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

- 64-pin plastic VFBGA (4 × 4 mm, 0.4 mm pitch)

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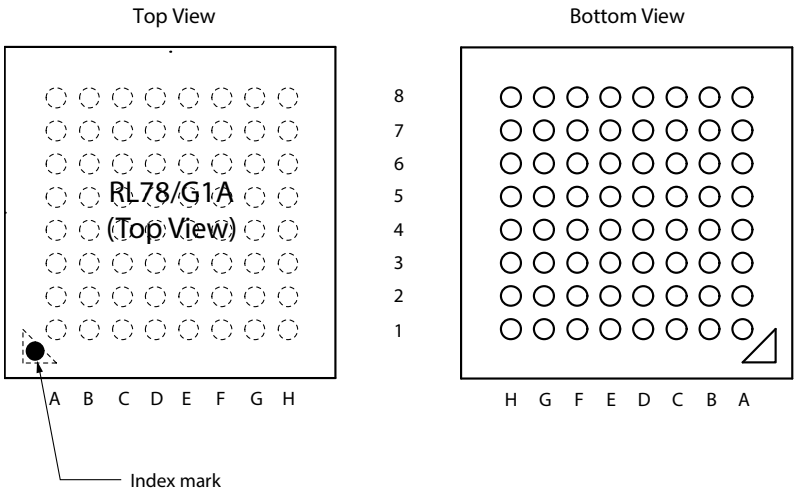


Pin No.	Name	Pin No.	Name	Pin No.	Name	Pin No.	Name
A1	P05/TI05/TO05/KR8	C1	P51/ANI25/SO11 /INTP2	E1	P153/ANI11/(KR8)	G1	AV_{DD}
A2	P30/ANI27/SCK11 /SCL11/INTP3 /RTC1HZ	C2	P71/SI21/SDA21/KR1	E2	P154/ANI12/(KR9)	G2	P25/ANI5/(KR8)
A3	P70/ANI28/SCK21 /SCL21/KR0	C3	P74/SI01/SDA01 /INTP8/KR4	E3	P10/ANI18/SCK00 /SCL00/(KR0)	G3	P24/ANI4/(KR7)
A4	P75/SCK01/SCL01 /INTP9/KR5	C4	P16/TI01/TO01/INTP5	E4	P11/ANI20/SI00 /SDA00/RxD0 /TOOLRxD/(KR1)	G4	P22/ANI2/(KR5)
A5	P77/INTP11/KR7	C5	P15/ANI24/SCK20 /SCL20/(KR5)	E5	P03/ANI16/SI10 /SDA10/RxD1/(KR3)	G5	P130
A6	P61/SDAA0	C6	P63	E6	P41/ANI30/TI07/TO07	G6	P02/ANI17/SO10/TxD1 /(KR2)
A7	P60/SCLA0	C7	V_{SS}	E7	$\overline{RESET}$	G7	P00/TI00/(KR0)
A8	EV_{DD0}	C8	P121/X1	E8	P137/INTP0	G8	P124/XT2/EXCLKS
B1	P50/ANI26 /SI11 /SDA11/INTP1	D1	P13/ANI22/SO20 /TxD2/(KR3)	F1	P150/ANI8	H1	AV_{SS}
B2	P72/SO21/KR2	D2	P06/TI06/TO06/KR9	F2	P151/ANI9/(KR6)	H2	P27/ANI7
B3	P73/SO01/KR3	D3	P12/ANI21/SO00 /TxD0/TOOLTxD/(KR2)	F3	P152/ANI10/(KR7)	H3	P26/ANI6/(KR9)
B4	P76/INTP10/KR6	D4	P14/ANI23/SI20/ SDA20/RxD2/(KR4)	F4	$P21/ANI1/AV_{REFM}$	H4	P23/ANI3/(KR6)
B5	P31/ANI29/TI03/TO03 /INTP4	D5	P42/TI04/TO04	F5	P04/SCK10/SCL10 /(KR4)	H5	$P20/ANI0/AV_{REFP}$
B6	P62	D6	P40/TOOL0	F6	P43	H6	P141/PCLBUZ1/INTP7
B7	V_{DD}	D7	REGC	F7	P01/TO00/(KR1)	H7	P140/PCLBUZ0/INTP6
B8	EV_{SS0}	D8	P122/X2/EXCLK	F8	P123/XT1	H8	P120/ANI19

Cautions 1. Make EV_{SS0} pin the same potential as V_{SS} pin.

2. Make V_{DD} pin the potential that is higher than EV_{DD0} pin.

3. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification.**

2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD} and EV_{DD0} pins and connect the V_{SS} and EV_{SS0} pins to separate ground lines.

3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

Absolute Maximum Ratings (T_A = 25°C) (2/2)

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	I_{OH1}	Per pin	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P130, P140, P141	–40	mA
		Total of all pins –170 mA	P00 to P04, P40 to P43, P120, P130, P140, P141	–70	mA
			P05, P06, P10 to P16, P30, P31, P50, P51, P70 to P77,	–100	mA
	I_{OH2}	Per pin	P20 to P27, P150 to P154	–0.1	mA
		Total of all pins		–1.3	mA
Output current, low	I_{OL1}	Per pin	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P60 to P63, P70 to P77, P120, P130, P140, P141	40	mA
		Total of all pins 170 mA	P00 to P04, P40 to P43, P120, P130, P140, P141	70	mA
			P05, P06, P10 to P16, P30, P31, P50, P51, P60 to P63, P70 to P77	100	mA
	I_{OL2}	Per pin	P20 to P27, P150 to P154	0.4	mA
		Total of all pins		6.4	mA
Operating ambient temperature	T_A	In normal operation mode		–40 to +85	°C
		In flash memory programming mode			
Storage temperature	T_{stg}			–65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.2 Oscillator Characteristics

2.2.1 X1, XT1 oscillator characteristics

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f_X)Note	Ceramic resonator/crystal resonator	2.7 V ≤ V_{DD} ≤ 3.6 V	1.0		20.0	MHz
		2.4 V ≤ V_{DD} < 2.7 V	1.0		16.0	MHz
		1.8 V ≤ V_{DD} < 2.4 V	1.0		8.0	MHz
		1.6 V ≤ V_{DD} < 1.8 V	1.0		4.0	MHz
XT1 clock oscillation frequency (f_X)Note	Crystal resonator		32	32.768	35	kHz

Note Indicates only permissible oscillator frequency ranges. See AC Characteristics for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

<R> **Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.**

2.2.2 On-chip oscillator characteristics

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequencyNotes 1, 2	f_{IH}			1		32	MHz
High-speed on-chip oscillator clock frequency accuracy		–20 to +85 °C	1.8 V ≤ V_{DD} ≤ 3.6 V	–1.0		+1.0	%
			1.6 V ≤ V_{DD} < 1.8 V	–5.0		+5.0	%
		–40 to –20 °C	1.8 V ≤ V_{DD} ≤ 3.6 V	–1.5		+1.5	%
			1.6 V ≤ V_{DD} < 1.8 V	–5.5		+5.5	%
Low-speed on-chip oscillator clock frequency	f_{IL}				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				–15		+15	%

Notes 1. High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H/010C2H) and bits 0 to 2 of HOCODIV register.

2. This indicates the oscillator characteristics only. See AC Characteristics for instruction execution time.

(T_A = –40 to +85°C, 1.6 V ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V) **(3/5)**

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P140, P141	Normal input buffer	0.8EV_{DD0}		EV_{DD0}	V
	V_{IH2}	P01, P03, P04, P10, P11, P13 to P16, P43	TTL input buffer 3.3 V ≤ EV_{DD0} ≤ 3.6 V	2.0		EV_{DD0}	V
			TTL input buffer 1.6 V ≤ EV_{DD0} < 3.3 V	1.5		EV_{DD0}	V
	V_{IH3}	P20 to P27, P150 to P154		0.7AV_{DD}		AV_{DD}	V
	V_{IH4}	P60 to P63		0.7EV_{DD0}		6.0	V
	V_{IH5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0.8V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P140, P141	Normal input buffer	0		0.2EV_{DD0}	V
	V_{IL2}	P01, P03, P04, P10, P11, P13 to P16, P43	TTL input buffer 3.3 V ≤ EV_{DD0} ≤ 3.6 V	0		0.5	V
			TTL input buffer 1.6 V ≤ EV_{DD0} < 3.3 V	0		0.32	V
	V_{IL3}	P20 to P27, P150 to P154		0		0.3AV_{DD}	V
	V_{IL4}	P60 to P63		0		0.3EV_{DD0}	V
	V_{IL5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0		0.2V_{DD}	V

Caution The maximum value of V_{IH} of pins P00, P02 to P04, P10 to P15, P43, P50, P71, and P74 is EV_{DD0}, even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

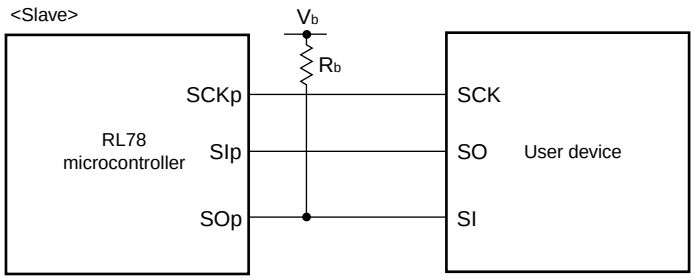
2.3.2 Supply current characteristics

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V) **(1/3)**

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current[Note 1]	I_{DD1}	Operating mode	HS (high-speed main) mode[Note 5]	f_{IH} = 32 MHz[Note 3]	Basic operation	V_{DD} = 3.0 V		2.1		mA
					Normal operation	V_{DD} = 3.0 V		4.6	7.0	mA
				f_{IH} = 24 MHz[Note 3]	Normal operation	V_{DD} = 3.0 V		3.7	5.5	mA
				f_{IH} = 16 MHz[Note 3]	Normal operation	V_{DD} = 3.0 V		2.7	4.0	mA
			LS (low-speed main) mode[Note 5]	f_{IH} = 8 MHz[Note 3]	Normal operation	V_{DD} = 3.0 V		1.2	1.8	mA
						V_{DD} = 2.0 V		1.2	1.8	
			LV (Low-voltage main) mode[Note 5]	f_{IH} = 4 MHz[Note 3]	Normal operation	V_{DD} = 3.0 V		1.2	1.7	mA
						V_{DD} = 2.0 V		1.2	1.7	
			HS (high-speed main) mode[Note 5]	f_{MX} = 20 MHz[Note 2], V_{DD} = 3.0 V	Normal operation	Square wave input		3.0	4.6	mA
						Resonator connection		3.2	4.8	
				f_{MX} = 10 MHz[Note 2], V_{DD} = 3.0 V	Normal operation	Square wave input		1.9	2.7	mA
						Resonator connection		1.9	2.7	
			LS (low-speed main) mode[Note 5]	f_{MX} = 8 MHz[Note 2], V_{DD} = 3.0 V	Normal operation	Square wave input		1.1	1.7	mA
						Resonator connection		1.1	1.7	
				f_{MX} = 8 MHz[Note 2], V_{DD} = 2.0 V	Normal operation	Square wave input		1.1	1.7	mA
						Resonator connection		1.1	1.7	
			Subsystem clock mode	f_{SUB} = 32.768 kHz[Note 4] T_A = –40°C	Normal operation	Square wave input		4.1	4.9	μA
						Resonator connection		4.2	5.0	
				f_{SUB} = 32.768 kHz[Note 4] T_A = +25°C	Normal operation	Square wave input		4.2	4.9	μA
						Resonator connection		4.3	5.0	
				f_{SUB} = 32.768 kHz[Note 4] T_A = +50°C	Normal operation	Square wave input		4.3	5.5	μA
						Resonator connection		4.4	5.6	
				f_{SUB} = 32.768 kHz[Note 4] T_A = +70°C	Normal operation	Square wave input		4.5	6.3	μA
						Resonator connection		4.6	6.4	
				f_{SUB} = 32.768 kHz[Note 4] T_A = +85°C	Normal operation	Square wave input		4.8	7.7	μA
						Resonator connection		4.9	7.8	

(**Notes** and **Remarks** are listed on the next page.)

CSI mode connection diagram (during communication at different potential)



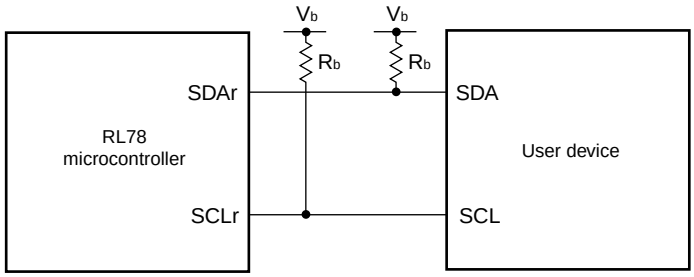
Remarks 1. R_b[Ω]: Communication line (SOp) pull-up resistance, C_b[F]: Communication line (SOp) load capacitance, V_b[V]: Communication line voltage

2. p: CSI number (p = 00, 10, 20), m: Unit number (m = 0, 1), n: Channel number (n = 00, 02, 10), g: PIM and POM number (g = 0, 1)

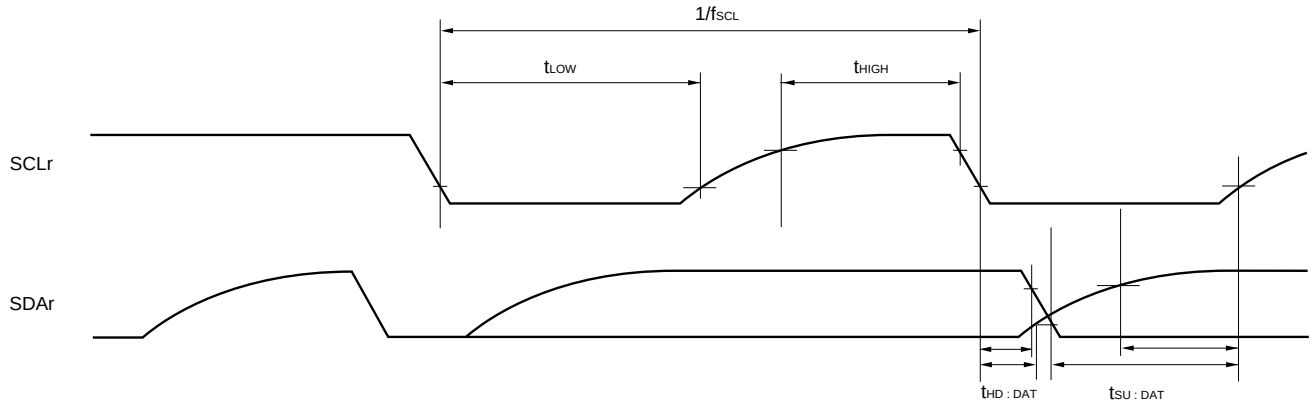
3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 02, 10))

4. CSI01, CSI11, and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

Simplified I²C mode connection diagram (during communication at different potential)



Simplified I²C mode serial transfer timing (during communication at different potential)



Remarks 1. R_b[Ω]: Communication line (SDAr, SCLr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance, V_b[V]: Communication line voltage

2. r: IIC number (r = 00, 10, 20), g: PIM, POM number (g = 0, 1)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 02, 10)

4. IIC01, IIC11, and IIC21 cannot communicate at different potential. Use IIC00, IIC10, or IIC20 for communication at different potential.

2.5.2 Serial interface IICA

(1) I^2C standard mode

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions	Standard Mode[Note 1]						Unit
			HS[Note 2]		LS[Note 3]		LV[Note 4]		
			MIN.	MAX.	MIN.	MIN.	MAX.	MIN.	
SCLA0 clock frequency	f_{SCL}	2.7 V ≤ EV_{DD0} ≤ 3.6 V	0	100	0	100	0	100	kHz
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	0	100	0	100	0	100	
		1.7 V ≤ EV_{DD0} ≤ 3.6 V	0	100	0	100	0	100	
		1.6 V ≤ EV_{DD0} ≤ 3.6 V	–		0	100	0	100	
Setup time of restart condition	$t_{SU:STA}$	2.7 V ≤ EV_{DD0} ≤ 3.6 V	4.7		4.7		4.7		μs
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	4.7		4.7		4.7		
		1.7 V ≤ EV_{DD0} ≤ 3.6 V	4.7		4.7		4.7		
		1.6 V ≤ EV_{DD0} ≤ 3.6 V	–		4.7		4.7		
Hold time[Note 5]	$t_{HD:STA}$	2.7 V ≤ EV_{DD0} ≤ 3.6 V	4.0		4.0		4.0		μs
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	4.0		4.0		4.0		
		1.7 V ≤ EV_{DD0} ≤ 3.6 V	4.0		4.0		4.0		
		1.6 V ≤ EV_{DD0} ≤ 3.6 V	–		4.0		4.0		
Hold time when SCLA0 = “L”	t_{LOW}	2.7 V ≤ EV_{DD0} ≤ 3.6 V	4.7		4.7		4.7		μs
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	4.7		4.7		4.7		
		1.7 V ≤ EV_{DD0} ≤ 3.6 V	4.7		4.7		4.7		
		1.6 V ≤ EV_{DD0} ≤ 3.6 V	–		4.7		4.7		
Hold time when SCLA0 = “H”	t_{HIGH}	2.7 V ≤ EV_{DD0} ≤ 3.6 V	4.0		4.0		4.0		μs
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	4.0		4.0		4.0		
		1.7 V ≤ EV_{DD0} ≤ 3.6 V	4.0		4.0		4.0		
		1.6 V ≤ EV_{DD0} ≤ 3.6 V	–		4.0		4.0		
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ EV_{DD0} ≤ 3.6 V	250		250		250		ns
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	250		250		250		
		1.7 V ≤ EV_{DD0} ≤ 3.6 V	250		250		250		
		1.6 V ≤ EV_{DD0} ≤ 3.6 V	–		250		250		
Data hold time (transmission)[Note 6]	$t_{HD:DAT}$	2.7 V ≤ EV_{DD0} ≤ 3.6 V	0	3.45	0	3.45	0	3.45	μs
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	0	3.45	0	3.45	0	3.45	
		1.7 V ≤ EV_{DD0} ≤ 3.6 V	0	3.45	0	3.45	0	3.45	
		1.6 V ≤ EV_{DD0} ≤ 3.6 V	–	–	0	3.45	0	3.45	
Setup time of stop condition	$t_{SU:STO}$	2.7 V ≤ EV_{DD0} ≤ 3.6 V	4.0		4.0		4.0		μs
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	4.0		4.0		4.0		
		1.7 V ≤ EV_{DD0} ≤ 3.6 V	4.0		4.0		4.0		
		1.6 V ≤ EV_{DD0} ≤ 3.6 V	–		4.0		4.0		
Bus-free time	t_{BUF}	2.7 V ≤ EV_{DD0} ≤ 3.6 V	4.7		4.7		4.7		μs
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	4.7		4.7		4.7		
		1.7 V ≤ EV_{DD0} ≤ 3.6 V	4.7		4.7		4.7		
		1.6 V ≤ EV_{DD0} ≤ 3.6 V	–		4.7		4.7		

(**Note** and **Remark** are listed on the next page.)

(2) I^2C fast mode, fast mode plus

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions	Fast Mode[Note 7]						Fast Mode Plus[Note 8]		Unit
			HS[Note 2]		LS[Note 3]		LV[Note 4]		HS[Note 2]		
			MIN.	MAX.	MIN.	MIN.	MAX.	MIN.	MAX.	MIN.	
SCLA0 clock frequency	f_{SCL}	2.7 V ≤ EV_{DD0} ≤ 3.6 V	0	400	0	400	0	400	0	1000	kHz
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	0	400	0	400	0	400	–		
Setup time of restart condition	$t_{SU:STA}$	2.7 V ≤ EV_{DD0} ≤ 3.6 V	0.6		0.6		0.6		0.26		μs
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	0.6		0.6		0.6		–		
Hold time[Note 5]	$t_{HD:STA}$	2.7 V ≤ EV_{DD0} ≤ 3.6 V	0.6		0.6		0.6		0.26		μs
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	0.6		0.6		0.6		–		
Hold time when SCLA0 = “L”	t_{LOW}	2.7 V ≤ EV_{DD0} ≤ 3.6 V	1.3		1.3		1.3		0.5		μs
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	1.3		1.3		1.3		–		
Hold time when SCLA0 = “H”	t_{HIGH}	2.7 V ≤ EV_{DD0} ≤ 3.6 V	0.6		0.6		0.6		0.26		μs
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	0.6		0.6		0.6		–		
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ EV_{DD0} ≤ 3.6 V	100		100		100		50		ns
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	100		100		100		–		
Data hold time (transmission)[Note 6]	$t_{HD:DAT}$	2.7 V ≤ EV_{DD0} ≤ 3.6 V	0	0.9	0	0.9	0	0.9	0	450	μs
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	0	0.9	0	0.9	0	0.9	–		
Setup time of stop condition	$t_{SU:STO}$	2.7 V ≤ EV_{DD0} ≤ 3.6 V	0.6		0.6		0.6		0.26		μs
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	0.6		0.6		0.6		–		
Bus-free time	t_{BUF}	2.7 V ≤ EV_{DD0} ≤ 3.6 V	1.3		1.3		1.3		0.5		μs
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	1.3		1.3		1.3		–		

Notes 1. In normal mode, use it with f_{CLK} ≥ 1 MHz, 1.6 V ≤ EV_{DD} ≤ 3.6 V.

2. HS is condition of HS (high-speed main) mode.

3. LS is condition of LS (low-speed main) mode.

4. LV is condition of LV (low-voltage main) mode.

5. The first clock pulse is generated after this period when the start/restart condition is detected.

6. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

7. In fast mode, use it with f_{CLK} ≥ 3.5 MHz, 1.8 V ≤ EV_{DD} ≤ 3.6 V.

8. In fast mode plus, use it with f_{CLK} ≥ 10 MHz, 2.7 V ≤ EV_{DD} ≤ 3.6 V.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C_b = 400 pF, R_b = 2.7 kΩ

Fast mode: C_b = 320 pF, R_b = 1.1 kΩ

Fast mode plus: C_b = 120 pF, R_b = 1.1 kΩ

2.6.4 LVD circuit characteristics

LVD Detection Voltage of Reset Mode and Interrupt Mode

(T_A = –40 to +85°C, $V_{PDR} \le V_{DD} \le 3.6$ V, V_{SS} = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V_{LVD2}	Power supply rise time	3.07	3.13	3.19	V
			Power supply fall time	3.00	3.06	3.12	V
		V_{LVD3}	Power supply rise time	2.96	3.02	3.08	V
			Power supply fall time	2.90	2.96	3.02	V
		V_{LVD4}	Power supply rise time	2.86	2.92	2.97	V
			Power supply fall time	2.80	2.86	2.91	V
		V_{LVD5}	Power supply rise time	2.76	2.81	2.87	V
			Power supply fall time	2.70	2.75	2.81	V
		V_{LVD6}	Power supply rise time	2.66	2.71	2.76	V
			Power supply fall time	2.60	2.65	2.70	V
		V_{LVD7}	Power supply rise time	2.56	2.61	2.66	V
			Power supply fall time	2.50	2.55	2.60	V
		V_{LVD8}	Power supply rise time	2.45	2.50	2.55	V
			Power supply fall time	2.40	2.45	2.50	V
		V_{LVD9}	Power supply rise time	2.05	2.09	2.13	V
			Power supply fall time	2.00	2.04	2.08	V
		V_{LVD10}	Power supply rise time	1.94	1.98	2.02	V
			Power supply fall time	1.90	1.94	1.98	V
		V_{LVD11}	Power supply rise time	1.84	1.88	1.91	V
			Power supply fall time	1.80	1.84	1.87	V
		V_{LVD12}	Power supply rise time	1.74	1.77	1.81	V
			Power supply fall time	1.70	1.73	1.77	V
		V_{LVD13}	Power supply rise time	1.64	1.67	1.70	V
			Power supply fall time	1.60	1.63	1.66	V
Minimum pulse width		t_{LW}		300			μs
Detection delay time						300	μs

Caution Set the detection voltage (V_{LVD}) to be within the operating voltage range. The operating voltage range depends on the setting of the user option byte (000C2H/010C2H). The following shows the operating voltage range.

HS (high-speed main) mode: V_{DD} = 2.7 to 3.6 V@1 MHz to 32 MHz

V_{DD} = 2.4 to 3.6 V@1 MHz to 16 MHz

LS (low-speed main) mode: V_{DD} = 1.8 to 3.6 V@1 MHz to 8 MHz

LV (low-voltage main) mode: V_{DD} = 1.6 to 3.6 V@1 MHz to 4 MHz

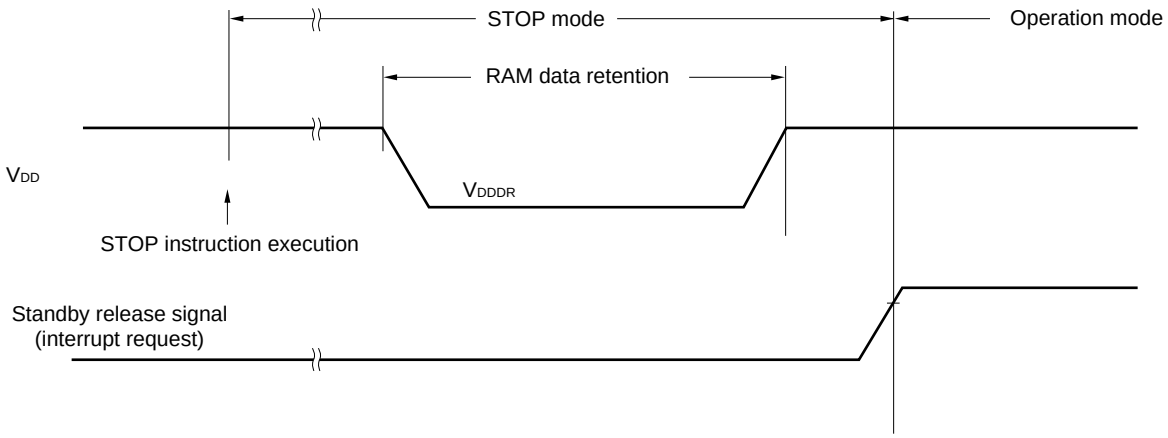
<R> 2.7 RAM Data Retention Characteristics

<R> **(T_A = –40 to +85°C, V_{SS} = 0 V)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.46 Note		3.6	V

<R> **Note** This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.

<R>



<R> 2.8 Flash Memory Programming Characteristics

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CPU/peripheral hardware clock frequency	f_{CLK}	1.8 V ≤ V_{DD} ≤ 3.6 V	1		32	MHz
Number of code flash rewrites Notes 1, 2	C_{erwr}	Retained for 20 years T_A = 85°C Note 3	1,000			Times
Number of data flash rewrites Notes 1, 2		Retained for 1 years T_A = 25°C Note 3		1,000,000		
		Retained for 5 years T_A = 85°C Note 3	100,000			
		Retained for 20 years T_A = 85°C Note 3	10,000			

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite.
The retaining years are until next rewrite after the rewrite.

2. When using flash memory programmer and Renesas Electronics self programming library

3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

3.2 Oscillator Characteristics

3.2.1 X1, XT1 oscillator characteristics

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f_X)Note	Ceramic resonator/crystal resonator	2.7 V ≤ V_{DD} ≤ 3.6 V	1.0		20.0	MHz
		2.4 V ≤ V_{DD} < 2.7 V	1.0		16.0	
XT1 clock oscillation frequency (f_X)Note	Crystal resonator		32	32.768	35	kHz

Note Indicates only permissible oscillator frequency ranges. See AC Characteristics for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

<R> **Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.**

3.2.2 On-chip oscillator characteristics

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator oscillation frequencyNotes 1, 2	f_{IH}			1		32	MHz
High-speed on-chip oscillator oscillation frequency accuracy		+85 to +105 °C	2.4 V ≤ V_{DD} ≤ 3.6 V	–2		+2	%
		–20 to +85 °C	2.4 V ≤ V_{DD} ≤ 3.6 V	–1		+1	%
		–40 to –20 °C	2.4 V ≤ V_{DD} ≤ 3.6 V	–1.5		+1.5	%
Low-speed on-chip oscillator oscillation frequency	f_{IL}				15		kHz
Low-speed on-chip oscillator oscillation frequency accuracy				–15		+15	%

Notes 1. High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H/010C2H) and bits 0 to 2 of HOCODIV register.

2. This indicates the oscillator characteristics only. See AC Characteristics for instruction execution time.

<R> **Notes 1.** Current flowing to V_{DD}.

2. When high-speed on-chip oscillator and high-speed system clock are stopped.

3. Current flowing only to the real-time clock (RTC) (excluding the operating current of the low-speed on-chip ocsillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and I_{RTC}, when the real-time clock operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added. I_{DD2} subsystem clock operation includes the operational current of the real-time clock.

4. Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip ocsillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and I_{IT}, when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added.

5. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2}, or I_{DD3} and I_{WDT} when the watchdog timer is in operation.

6. Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{ADC}, I_{AVREF}, I_{ADREF} when the A/D converter operates in an operation mode or the HALT mode.

7. Current flowing to the AV_{DD}.

8. Current flowing from the reference voltage source of A/D converter.

9. Operation current flowing to the internal reference voltage.

10. Current flowing to the AV_{REFP}.

11. Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{LVD} when the LVD circuit is in operation.

12. Current flowing only during data flash rewrite.

13. Current flowing only during self programming.

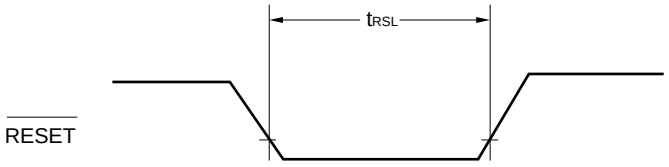
Remarks 1. f_{IL}: Low-speed on-chip oscillator clock frequency

2. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

3. f_{CLK}: CPU/peripheral hardware clock frequency

4. Temperature condition of the TYP. value is T_A = 25°C

$\overline{\text{RESET}}$ Input Timing



(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCKp cycle time	t_{KCY1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V	t_{KCY1} ≥ 4/f_{CLK}	250			ns
		2.4 V ≤ EV_{DD0} ≤ 3.6 V	t_{KCY1} ≥ 4/f_{CLK}	500			ns
SCKp high-/low-level width	t_{KH1}, t_{KL1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V		t_{KCY1}/2 – 36			ns
		2.4 V ≤ EV_{DD0} ≤ 3.6 V		t_{KCY1}/2 – 76			ns
SIp setup time (to SCKp↑)[Note 1]	t_{SIK1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V		66			ns
		2.4 V ≤ EV_{DD0} ≤ 3.6 V		113			ns
SIp hold time (from SCKp↑)[Note 1]	t_{KSI1}			38			ns
Delay time from SCKp↓ to SOp output[Note 2]	t_{KSO1}	C = 30 p[Note 3]				50	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time or SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark p: CSI number (p = 00, 01, 10, 11, 20, 21), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 1)

(4) During communication at same potential (simplified I^2C mode)

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCLr clock frequency	f_{SCL}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, C_b = 50 pF, R_b = 2.7 kΩ		400 Note 1	kHz
		2.4 V ≤ EV_{DD0} ≤ 3.6 V, C_b = 100 pF, R_b = 3 kΩ		100 Note 1	kHz
Hold time when SCLr = “L”	t_{LOW}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, C_b = 50 pF, R_b = 2.7 kΩ	1200		ns
		2.4 V ≤ EV_{DD0} ≤ 3.6 V, C_b = 100 pF, R_b = 3 kΩ	4600		ns
Hold time when SCLr = “H”	t_{HIGH}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, C_b = 50 pF, R_b = 2.7 kΩ	1200		ns
		2.4 V ≤ EV_{DD0} ≤ 3.6 V, C_b = 100 pF, R_b = 3 kΩ	4600		ns
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ EV_{DD0} ≤ 3.6 V, C_b = 50 pF, R_b = 2.7 kΩ	1/f_{MCK} + 220 Note 2		ns
		2.4 V ≤ EV_{DD} ≤ 3.6 V, C_b = 100 pF, R_b = 3 kΩ	1/f_{MCK} + 580 Note 2		ns
Data hold time (transmission)	$t_{HD:DAT}$	2.7 V ≤ EV_{DD0} ≤ 3.6 V, C_b = 50 pF, R_b = 2.7 kΩ	0	770	ns
		2.4 V ≤ EV_{DD0} ≤ 3.6 V, C_b = 100 pF, R_b = 3 kΩ	0	1420	ns

Notes 1. The value must also be f_{CLK}/4 or lower.

2. Set the f_{MCK} value to keep the hold time of SCLr = “L” and SCLr = “H”.

Caution Select the normal input buffer and the N-ch open drain output (V_{DD} tolerance (When 25- to 48-pin products)/EV_{DD} tolerance (When 64-pin products)) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).

(5) Communication at different potential (1.8 V, 2.5 V) (UART mode) (dedicated baud rate generator output) (1/2)

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Transfer rate[Note 1]		Reception	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V				f_{MCK}/12	bps
				Theoretical value of the maximum transfer rate f_{CLK} = 32 MHz, f_{MCK} = f_{CLK}			2.6	Mbps
			2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V				f_{MCK}/12	bps
				Theoretical value of the maximum transfer rate f_{CLK} = 32 MHz, f_{MCK} = f_{CLK}			2.6[Note 2]	Mbps

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps.

2. The following conditions are required for low-voltage interface when EV_{DD0} < V_{DD}.
2.4 V ≤ EV_{DD0} < 2.7 V : MAX. 1.3 Mbps

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (When 25- to 48-pin products)/EV_{DD} tolerance (When 64-pin products)) mode for the TxDq pin by using <R> **port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.**

Remarks 1. V_b[V]: Communication line voltage

2. q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10, 11)

(5) Communication at different potential (1.8 V, 2.5 V) (UART mode) (dedicated baud rate generator output) (2/2)

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Transfer rate		Transmission	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V				**Note 1**	bps
				Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 2.7 kΩ, V_b = 2.3 V			1.2 Note 2	Mbps
			2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V				**Note 3**	bps
				Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 5.5 kΩ, V_b = 1.6 V			0.43 Note 4	Mbps

Notes 1. The smaller maximum transfer rate derived by using f_{MCK}/12 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ EV_{DD0} ≤ 3.6 V and 2.3 V ≤ V_b ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

2. This value as an example is calculated when the conditions described in the “Conditions” column are met. See **Note 1** above to calculate the maximum transfer rate under conditions of the customer.

3. The smaller maximum transfer rate derived by using f_{MCK}/12 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.4 V ≤ EV_{DD0} < 3.3 V and 1.6 V ≤ V_b ≤ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

4. This value as an example is calculated when the conditions described in the “Conditions” column are met. See **Note 3** above to calculate the maximum transfer rate under conditions of the customer.

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (When 25- to 48-pin products)/EV_{DD} tolerance (When 64-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

<R>