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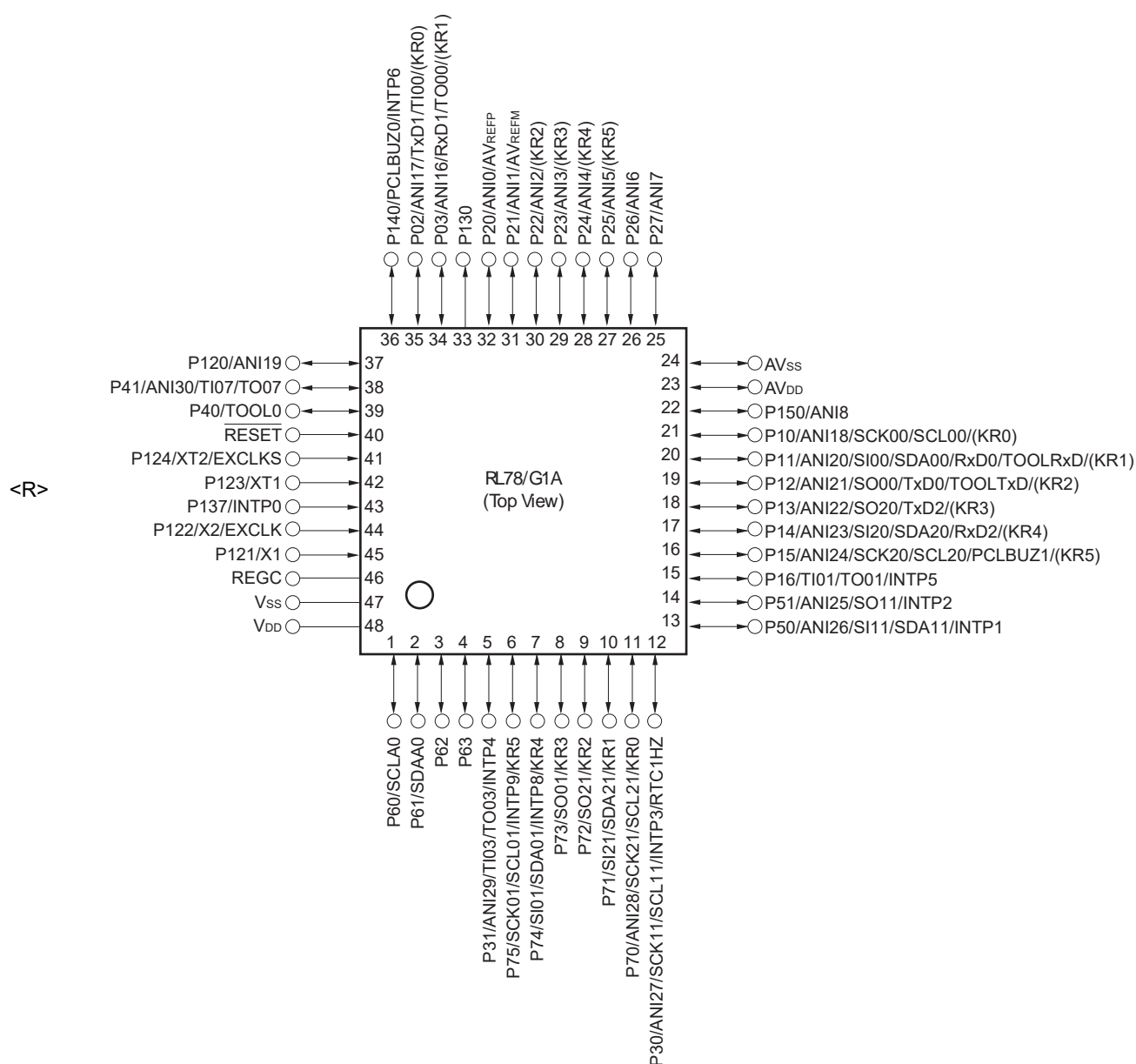
"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I ² C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	32
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LFQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10egaafb-v0

- 48-pin plastic HWQFN (7 × 7 mm, 0.5 mm pitch)



Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μ F).

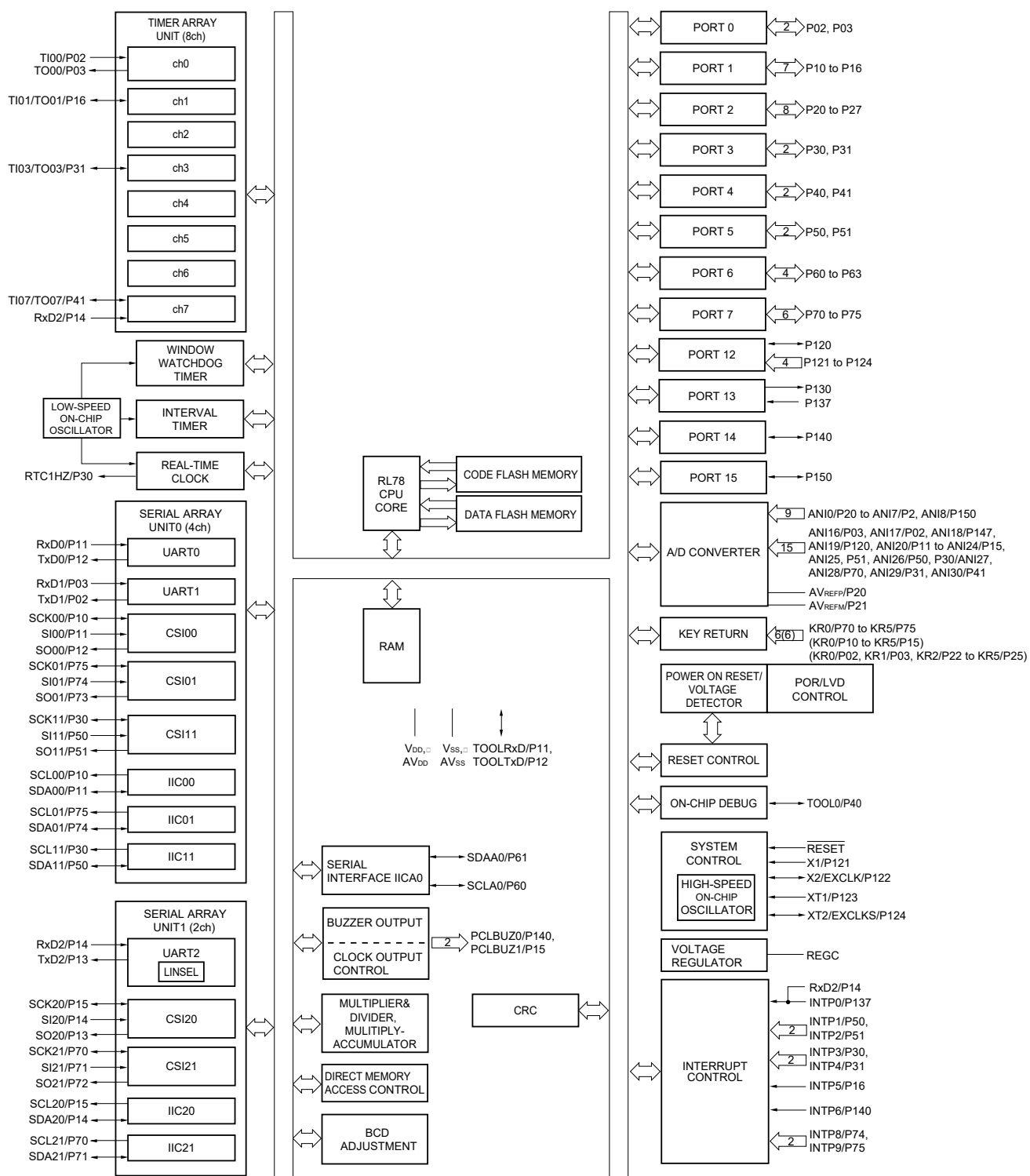
Remarks 1. For pin identification, see 1.4 Pin Identification.

- Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.4 Pin Identification

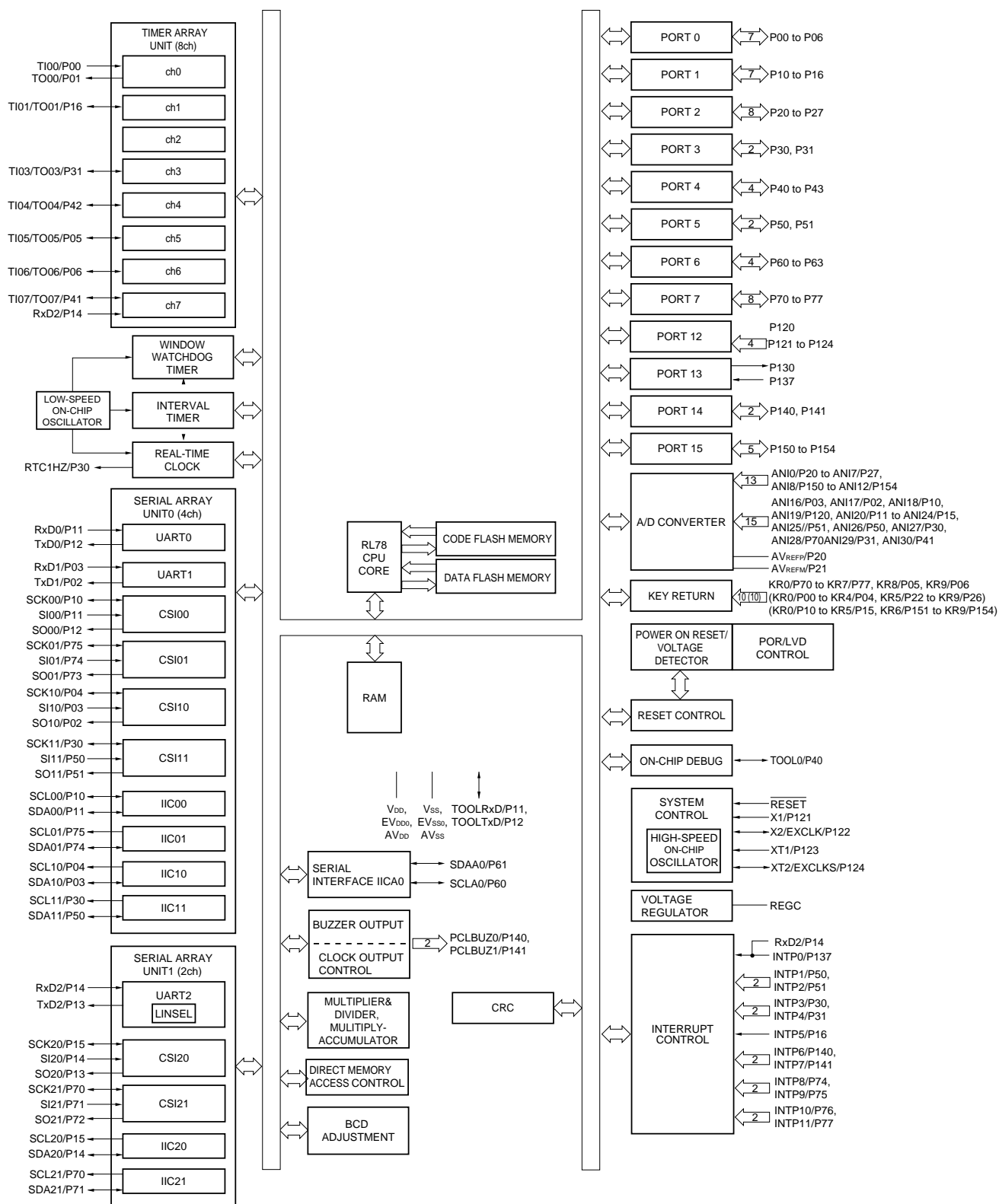
ANI0 to ANI12,		PCLBUZ0, PCLBUZ1:	Programmable clock output/buzzer output
ANI16 to ANI30:	Analog input		
AVDD:	Analog power supply	REGC:	Regulator capacitance
AVSS:	Analog ground	RESET:	Reset
AVREFM:	A/D converter reference potential (– side) input	RTC1HZ:	Real-time clock correction clock (1 Hz) output
AVREFP:	A/D converter reference potential (+ side) input	RxD0 to RxD2:	Receive data
EVDD0:	Power supply for port	SCK00, SCK01, SCK10,	
EVSS0:	Ground for port	SCK11, SCK20, SCK21:	Serial clock input/output
EXCLK:	External clock input (main system clock)	SCLA0, SCL00, SCL01,	
		SCL10, SCL11, SCL20,	
EXCLKS:	External clock input (subsystem clock)	SCL21:	Serial clock output
		SDAA0, SDA00, SDA01,	
INTP0 to INTP11:	Interrupt Request from External	SDA10, SDA11, SDA20,	
		SDA21:	Serial data input/output
KR0 to KR9:	Key return	SI00, SI01, SI10, SI11,	
P00 to P06:	Port 0	SI20, SI21:	Serial data input
P10 to P16:	Port 1	SO00, SO01, SO10,	
P20 to P27:	Port 2	SO11, SO20, SO21:	Serial data output
P30, P31:	Port 3	TI00, TI01, TI03 to TI07:	Timer input
P40 to P43:	Port 4	TO00, TO01,	
P50, P51:	Port 5	TO03 to TO07:	Timer output
P60 to P63:	Port 6	TOOL0:	Data input/output for tool
P70 to P77:	Port 7	TOOLRxD, TOOLTxD:	Data input/output for external device
P120 to P124:	Port 12	TxD0 to TxD2:	Transmit data
P130, P137:	Port 13	VDD:	Power supply
P140, P141:	Port 14	VSS:	Ground
P150 to P154:	Port 15	X1, X2:	Crystal oscillator (main system clock)
		XT1, XT2:	Crystal oscillator (subsystem clock)

<R> 1.5.3 48-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.5.4 64-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

2.1 Absolute Maximum Ratings

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$) (1/2)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V_{DD}		-0.5 to $+6.5$	V
	EV_{DD0}		-0.5 to $+6.5$	V
	AV_{DD}		-0.5 to $+4.6$	V
	AV_{REFP}		-0.3 to $AV_{DD} + 0.3$ ^{Note 3}	V
	EV_{SS0}		-0.5 to $+0.3$	V
	AV_{SS}		-0.5 to $+0.3$	V
	AV_{REFM}		-0.3 to $AV_{DD} + 0.3$ ^{Note 3} and $AV_{REFM} \leq AV_{REFP}$	V
REGC pin input voltage	V_{IREGC}	REGC	-0.3 to $+2.8$ and -0.3 to $V_{DD} + 0.3$ ^{Note 1}	V
Input voltage	V_{I1}	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P140, P141	-0.3 to $EV_{DD0} + 0.3$ and -0.3 to $V_{DD} + 0.3$ ^{Note 2}	V
	V_{I2}	P60 to P63 (N-ch open-drain)	-0.3 to $+6.5$	V
	V_{I3}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$	-0.3 to $V_{DD} + 0.3$ ^{Note 2}	V
	V_{I4}	P20 to P27, P150 to P154	-0.3 to $AV_{DD} + 0.3$ ^{Note 2}	V
Output voltage	V_{O1}	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P60 to P63, P70 to P77, P120, P130, P140, P141	-0.3 to $EV_{DD0} + 0.3$ ^{Note 2}	V
	V_{O2}	P20 to P27, P150 to P154	-0.3 to $AV_{DD} + 0.3$ ^{Note 2}	V
Analog input voltage	V_{AI1}	ANI16 to ANI30	-0.3 to $EV_{DD0} + 0.3$ and -0.3 to $AV_{REF(+)} + 0.3$ ^{Notes 2, 4}	V
	V_{AI2}	ANI0 to ANI12	-0.3 to $AV_{DD} + 0.3$ and -0.3 to $AV_{REF(+)} + 0.3$ ^{Notes 2, 4}	V

Notes 1. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

2. Must be 6.5 V or lower.

3. Must be 4.6 V or lower.

4. Do not exceed $AV_{REF(+)} + 0.3$ V in case of A/D conversion target pin.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remarks 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2. $AV_{REF(+)}$: + side reference voltage of the A/D converter.

3. V_{SS} : Reference voltage

2.2 Oscillator Characteristics

2.2.1 X1, XT1 oscillator characteristics

(T_A = -40 to +85°C, 1.6 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f _x) ^{Note}	Ceramic resonator/crystal resonator	2.7 V ≤ V _{DD} ≤ 3.6 V	1.0		20.0	MHz
		2.4 V ≤ V _{DD} < 2.7 V	1.0		16.0	MHz
		1.8 V ≤ V _{DD} < 2.4 V	1.0		8.0	MHz
		1.6 V ≤ V _{DD} < 1.8 V	1.0		4.0	MHz
XT1 clock oscillation frequency (f _x) ^{Note}	Crystal resonator		32	32.768	35	kHz

Note Indicates only permissible oscillator frequency ranges. See AC Characteristics for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

<R> **Caution** Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

2.2.2 On-chip oscillator characteristics

(T_A = -40 to +85°C, 1.6 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency ^{Notes 1, 2}	f _{IH}			1		32	MHz
High-speed on-chip oscillator clock frequency accuracy		-20 to +85 °C	1.8 V ≤ V _{DD} ≤ 3.6 V	-1.0		+1.0	%
			1.6 V ≤ V _{DD} < 1.8 V	-5.0		+5.0	%
		-40 to -20 °C	1.8 V ≤ V _{DD} ≤ 3.6 V	-1.5		+1.5	%
			1.6 V ≤ V _{DD} < 1.8 V	-5.5		+5.5	%
Low-speed on-chip oscillator clock frequency	f _{IL}				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				-15		+15	%

Notes 1. High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H/010C2H) and bits 0 to 2 of HOCODIV register.

2. This indicates the oscillator characteristics only. See AC Characteristics for instruction execution time.

- Notes**
1. Total current flowing into V_{DD} and EV_{DD0} , including the input leakage current flowing when the level of the input pin is fixed to V_{DD} , EV_{DD0} or V_{SS} , EV_{SS0} . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, on-chip pull-up/pull-down resistors, and data flash rewriting.
 2. When high-speed on-chip oscillator and subsystem clock are stopped.
 3. When high-speed system clock and subsystem clock are stopped.
 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When setting ultra-low power consumption oscillation ($AMP_{HS1} = 1$). Not including the current flowing into the RTC, 12-bit interval timer and watchdog timer
 5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
 HS (high-speed main) mode: $V_{DD} = 2.7\text{ V to }3.6\text{ V}@1\text{ MHz to }32\text{ MHz}$
 $V_{DD} = 2.4\text{ V to }3.6\text{ V}@1\text{ MHz to }16\text{ MHz}$
 LS (low-speed main) mode: $V_{DD} = 1.8\text{ V to }3.6\text{ V}@1\text{ MHz to }8\text{ MHz}$
 LV (Low-voltage main) mode: $V_{DD} = 1.6\text{ V to }3.6\text{ V}@1\text{ MHz to }4\text{ MHz}$

- Remarks**
1. f_{MX} : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 2. f_{IH} : High-speed on-chip oscillator clock frequency
 3. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)
 4. Except subsystem clock operation, temperature condition of the TYP. value is $T_A = 25^\circ\text{C}$

2.4 AC Characteristics

(T_A = -40 to +85°C, AV_{DD} ≤ V_{DD} ≤ 3.6 V, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T _{cy}	Main system clock (f _{MAIN}) operation	HS (high-speed main) mode	2.7 V ≤ V _{DD} ≤ 3.6 V	0.03125	1	μs
				2.4 V ≤ V _{DD} < 2.7 V	0.0625	1	μs
			LS (low-speed main) mode	1.8 V ≤ V _{DD} ≤ 3.6 V	0.125	1	μs
			LV (low-voltage main) mode	1.6 V ≤ V _{DD} ≤ 3.6 V	0.25	1	μs
		Subsystem clock (f _{SUB}) operation		1.8 V ≤ V _{DD} ≤ 3.6 V	28.5	30.5	31.3 μs
		In the self programming mode	HS (high-speed main) mode	2.7 V ≤ V _{DD} ≤ 3.6 V	0.03125	1	μs
				2.4 V ≤ V _{DD} < 2.7 V	0.0625	1	μs
			LS (low-speed main) mode	1.8 V ≤ V _{DD} ≤ 3.6 V	0.125	1	μs
			LV (low-voltage main) mode	1.6 V ≤ V _{DD} ≤ 3.6 V	0.25	1	μs
External system clock frequency	f _{EX}	2.7 V ≤ V _{DD} ≤ 3.6 V		1.0		20.0	MHz
		2.4 V ≤ V _{DD} < 2.7 V		1.0		16.0	MHz
		1.8 V ≤ V _{DD} < 2.4 V		1.0		8.0	MHz
		1.6 V ≤ V _{DD} < 1.8 V		1.0		4.0	MHz
	f _{EXS}			32		35	kHz
External system clock input high-level width, low-level width	t _{EXH} , t _{EXL}	2.7 V ≤ V _{DD} ≤ 3.6 V		24			ns
		2.4 V ≤ V _{DD} < 2.7 V		30			ns
		1.8 V ≤ V _{DD} < 2.4 V		60			ns
		1.6 V ≤ V _{DD} < 1.8 V		120			ns
	t _{EXHS} , t _{EXLS}			13.7			μs
TI00, TI01, TI03 to TI07 input high-level width, low-level width	t _{TIH} , t _{TIL}			1/f _{MCK} +10			ns ^{Note}
TO00, TO01, TO03 to TO07 output frequency	f _{TO}	HS (high-speed main) mode	2.7 V ≤ EV _{DD0} ≤ 3.6 V			8	MHz
			1.8 V ≤ EV _{DD0} < 2.7 V			4	MHz
			1.6 V ≤ EV _{DD0} < 1.8 V			2	MHz
		LS (low-speed main) mode	1.8 V ≤ EV _{DD0} ≤ 3.6 V			4	MHz
			1.6 V ≤ EV _{DD0} < 1.8 V			2	MHz
		LV (low-voltage main) mode	1.6 V ≤ EV _{DD0} ≤ 3.6 V			2	MHz
PCLBUZ0, PCLBUZ1 output frequency	f _{PCL}	HS (high-speed main) mode	2.7 V ≤ EV _{DD0} ≤ 3.6 V			8	MHz
			1.8 V ≤ EV _{DD0} < 2.7 V			4	MHz
			1.6 V ≤ EV _{DD0} < 1.8 V			2	MHz
		LS (low-speed main) mode	1.8 V ≤ EV _{DD0} ≤ 3.6 V			4	MHz
			1.6 V ≤ EV _{DD0} < 1.8 V			2	MHz
		LV (low-voltage main) mode	1.8 V ≤ EV _{DD0} ≤ 3.6 V			4	MHz
Interrupt input high-level width, low-level width	t _{INTH} , t _{INTL}	INTP0	1.6 V ≤ V _{DD} ≤ 3.6 V	1			μs
		INTP1 to INTP11	1.6 V ≤ EV _{DD0} ≤ 3.6 V	1			μs
Key interrupt input high-level width, low-level width	t _{KR}	KR0 to KR9	1.8 V ≤ EV _{DD0} ≤ 3.6 V, 1.8 V ≤ AV _{DD0} ≤ 3.6 V	250			ns
			1.6 V ≤ EV _{DD0} < 1.8 V, 1.6 V ≤ AV _{DD0} < 1.8 V	1			μs
RESET low-level width	t _{RSL}			10			μs

(Note and Remark are listed on the next page.)

- Notes**
1. HS is condition of HS (high-speed main) mode.
 2. LS is condition of LS (low-speed main) mode.
 3. LV is condition of LV (low-voltage main) mode.
 4. Transfer rate in the SNOOZE mode: MAX. 1 Mbps
 5. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time or SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 6. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 7. C is the load capacitance of the SOp output lines.

Caution Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- Remarks**
1. p: CSI number (p = 00, 01, 10, 11, 20, 21), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),
g: PIM number (g = 0, 1)
 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00 to 03, 10, 11))

(10) Communication at different potential (1.8 V, 2.5 V) (simplified I²C mode) (2/2)**(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)**

Parameter	Symbol	Conditions	HS ^{Note 1}		LS ^{Note 2}		LV ^{Note 3}		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data setup time (reception)	t _{SU:DAT}	2.7 V ≤ EV _{DD0} ≤ 3.6 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ	1/f _{MCK} + 135 ^{Note 6}		1/f _{MCK} + 190 ^{Note 6}		1/f _{MCK} + 190 ^{Note 6}		ns
		2.7 V ≤ EV _{DD0} ≤ 3.6 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	1/f _{MCK} + 190 ^{Note 6}		1/f _{MCK} + 190 ^{Note 6}		1/f _{MCK} + 190 ^{Note 6}		ns
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 5} , C _b = 100 pF, R _b = 5.5 kΩ	1/f _{MCK} + 190 ^{Note 6}		1/f _{MCK} + 190 ^{Note 6}		1/f _{MCK} + 190 ^{Note 6}		ns
Data hold time (transmission)	t _{HD:DAT}	2.7 V ≤ EV _{DD0} ≤ 3.6 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ	0	305	0	305	0	305	ns
		2.7 V ≤ EV _{DD0} ≤ 3.6 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	0	355	0	355	0	355	ns
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 5} , C _b = 100 pF, R _b = 5.5 kΩ	0	405	0	405	0	405	ns

Notes 1. HS is condition of HS (high-speed main) mode.**2.** LS is condition of LS (low-speed main) mode.**3.** LV is condition of LV (low-voltage main) mode.**4.** The value must also be f_{CLK}/4 or lower.**5.** Use it with EV_{DD0} ≥ V_b.**6.** Set the f_{MCK} value to keep the hold time of SCLr = “L” and SCLr = “H”.

Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance (When 25- to 48-pin products)/EV_{DD} tolerance (When 64-pin products)) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance (When 25- to 48-pin products)/EV_{DD} tolerance (When 64-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

<R>

(Remarks are listed on the next page.)

2.5.2 Serial interface IICA

(1) I²C standard mode(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions	Standard Mode ^{Note 1}						Unit
			HS ^{Note 2}		LS ^{Note 3}		LV ^{Note 4}		
			MIN.	MAX.	MIN.	MIN.	MAX.	MIN.	
SCLA0 clock frequency	f _{SCL}	2.7 V ≤ EV _{DD0} ≤ 3.6 V	0	100	0	100	0	100	kHz
		1.8 V ≤ EV _{DD0} ≤ 3.6 V	0	100	0	100	0	100	
		1.7 V ≤ EV _{DD0} ≤ 3.6 V	0	100	0	100	0	100	
		1.6 V ≤ EV _{DD0} ≤ 3.6 V	—		0	100	0	100	
Setup time of restart condition	t _{SU:STA}	2.7 V ≤ EV _{DD0} ≤ 3.6 V	4.7		4.7		4.7		μs
		1.8 V ≤ EV _{DD0} ≤ 3.6 V	4.7		4.7		4.7		
		1.7 V ≤ EV _{DD0} ≤ 3.6 V	4.7		4.7		4.7		
		1.6 V ≤ EV _{DD0} ≤ 3.6 V	—		4.7		4.7		
Hold time ^{Note 5}	t _{HD:STA}	2.7 V ≤ EV _{DD0} ≤ 3.6 V	4.0		4.0		4.0		μs
		1.8 V ≤ EV _{DD0} ≤ 3.6 V	4.0		4.0		4.0		
		1.7 V ≤ EV _{DD0} ≤ 3.6 V	4.0		4.0		4.0		
		1.6 V ≤ EV _{DD0} ≤ 3.6 V	—		4.0		4.0		
Hold time when SCLA0 = “L”	t _{LOW}	2.7 V ≤ EV _{DD0} ≤ 3.6 V	4.7		4.7		4.7		μs
		1.8 V ≤ EV _{DD0} ≤ 3.6 V	4.7		4.7		4.7		
		1.7 V ≤ EV _{DD0} ≤ 3.6 V	4.7		4.7		4.7		
		1.6 V ≤ EV _{DD0} ≤ 3.6 V	—		4.7		4.7		
Hold time when SCLA0 = “H”	t _{HIGH}	2.7 V ≤ EV _{DD0} ≤ 3.6 V	4.0		4.0		4.0		μs
		1.8 V ≤ EV _{DD0} ≤ 3.6 V	4.0		4.0		4.0		
		1.7 V ≤ EV _{DD0} ≤ 3.6 V	4.0		4.0		4.0		
		1.6 V ≤ EV _{DD0} ≤ 3.6 V	—		4.0		4.0		
Data setup time (reception)	t _{SU:DAT}	2.7 V ≤ EV _{DD0} ≤ 3.6 V	250		250		250		ns
		1.8 V ≤ EV _{DD0} ≤ 3.6 V	250		250		250		
		1.7 V ≤ EV _{DD0} ≤ 3.6 V	250		250		250		
		1.6 V ≤ EV _{DD0} ≤ 3.6 V	—		250		250		
Data hold time (transmission) ^{Note 6}	t _{HD:DAT}	2.7 V ≤ EV _{DD0} ≤ 3.6 V	0	3.45	0	3.45	0	3.45	μs
		1.8 V ≤ EV _{DD0} ≤ 3.6 V	0	3.45	0	3.45	0	3.45	
		1.7 V ≤ EV _{DD0} ≤ 3.6 V	0	3.45	0	3.45	0	3.45	
		1.6 V ≤ EV _{DD0} ≤ 3.6 V	—	—	0	3.45	0	3.45	
Setup time of stop condition	t _{SU:STO}	2.7 V ≤ EV _{DD0} ≤ 3.6 V	4.0		4.0		4.0		μs
		1.8 V ≤ EV _{DD0} ≤ 3.6 V	4.0		4.0		4.0		
		1.7 V ≤ EV _{DD0} ≤ 3.6 V	4.0		4.0		4.0		
		1.6 V ≤ EV _{DD0} ≤ 3.6 V	—		4.0		4.0		
Bus-free time	t _{BUF}	2.7 V ≤ EV _{DD0} ≤ 3.6 V	4.7		4.7		4.7		μs
		1.8 V ≤ EV _{DD0} ≤ 3.6 V	4.7		4.7		4.7		
		1.7 V ≤ EV _{DD0} ≤ 3.6 V	4.7		4.7		4.7		
		1.6 V ≤ EV _{DD0} ≤ 3.6 V	—		4.7		4.7		

(Note and Remark are listed on the next page.)

3.3 DC Characteristics

3.3.1 Pin characteristics

<R> ($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq AV_{DD} \leq V_{DD} \leq 3.6\text{ V}$, $2.4\text{ V} \leq EV_{DD0} \leq V_{DD} \leq 3.6\text{ V}$, $V_{SS} = EV_{SS0} = 0\text{ V}$) (1/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, high ^{Note 1}	I _{OH1}	Per pin for P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P130, P140, P141	$2.4\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$		$-3.0^{\text{Note 2}}$	mA
		Total of P00 to P04, P40 to P43, P120, P130, P140, P141 (When duty $\leq 70\%$ ^{Note 3})	$2.7\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$		-10.0	mA
			$2.4\text{ V} \leq EV_{DD0} < 2.7\text{ V}$		-5.0	mA
		Total of P05, P06, P10 to P16, P30, P31, P50, P51, P70 to P77, (When duty $\leq 70\%$ ^{Note 3})	$2.7\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$		-19.0	mA
			$2.4\text{ V} \leq EV_{DD0} < 2.7\text{ V}$		-10.0	mA
	I _{OH2}	Total of all pins (When duty $\leq 70\%$ ^{Note 3})	$2.4\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$		-29.0	mA
		Per pin for P20 to P27, P150 to P154	$2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$		$-0.1^{\text{Note 2}}$	mA
		Total of all pins (When duty $\leq 70\%$ ^{Note 3})	$2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$		-1.3	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from the EV_{DD0}, V_{DD} pins to an output pin.

2. However, do not exceed the total current value.

3. Specification under conditions where the duty factor $\leq 70\%$.

The output current value that has changed to the duty factor $> 70\%$ the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = $(I_{OH} \times 0.7)/(n \times 0.01)$

<Example> Where $n = 80\%$ and $I_{OH} = -10.0\text{ mA}$

$$\text{Total output current of pins} = (-10.0 \times 0.7)/(80 \times 0.01) \cong -8.7\text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Caution P00, P02 to P04, P10 to P15, P43, P50, P71, and P74 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

- <R> **Notes**
1. Current flowing to V_{DD} .
 2. When high-speed on-chip oscillator and high-speed system clock are stopped.
 3. Current flowing only to the real-time clock (RTC) (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2} , and I_{RTC} , when the real-time clock operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added. I_{DD2} subsystem clock operation includes the operational current of the real-time clock.
 4. Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2} , and I_{IT} , when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added.
 5. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontrollers is the sum of I_{DD1} , I_{DD2} , or I_{DD3} and I_{WDT} when the watchdog timer is in operation.
 6. Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{ADC} , I_{AVREF} , I_{ADREF} when the A/D converter operates in an operation mode or the HALT mode.
 7. Current flowing to the AV_{DD} .
 8. Current flowing from the reference voltage source of A/D converter.
 9. Operation current flowing to the internal reference voltage.
 10. Current flowing to the AV_{REFP} .
 11. Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of I_{DD1} , I_{DD2} or I_{DD3} and I_{LVD} when the LVD circuit is in operation.
 12. Current flowing only during data flash rewrite.
 13. Current flowing only during self programming.

- Remarks**
1. f_{IL} : Low-speed on-chip oscillator clock frequency
 2. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)
 3. f_{CLK} : CPU/peripheral hardware clock frequency
 4. Temperature condition of the TYP. value is $T_A = 25^{\circ}\text{C}$

3.4 AC Characteristics

(T_A = -40 to $+105^\circ\text{C}$, AV_{DD} ≤ V_{DD} ≤ 3.6 V, 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T _{CY}	Main system clock (f _{MAIN}) operation	HS (high-speed main) mode	2.7 V ≤ V _{DD} ≤ 3.6 V	0.03125	1	μs
				2.4 V ≤ V _{DD} < 2.7 V	0.0625	1	μs
		Subsystem clock (f _{SUB}) operation		2.4 V ≤ V _{DD} ≤ 3.6 V	28.5	30.5	31.3 μs
		In the self programming mode	HS (high-speed main) mode	2.7 V ≤ V _{DD} ≤ 3.6 V	0.03125	1	μs
				2.4 V ≤ V _{DD} < 2.7 V	0.0625	1	μs
External system clock frequency	f _{EX}	2.7 V ≤ V _{DD} ≤ 3.6 V		1.0		20.0	MHz
		2.4 V ≤ V _{DD} < 2.7 V		1.0		16.0	MHz
	f _{EXS}			32		35	kHz
External system clock input high-level width, low-level width	t _{EXH} , t _{EXL}	2.7 V ≤ V _{DD} ≤ 3.6 V		24			ns
		2.4 V ≤ V _{DD} < 2.7 V		30			ns
	t _{EXHS} , t _{EXLS}			13.7			μs
TI00, TI01, TI03 to TI07 input high-level width, low-level width	t _{TIH} , t _{TIL}			1/f _{MCK} +10			ns ^{Note}
TO00, TO01, TO03 to TO07 output frequency	f _{TO}	HS (high-speed main) mode		2.7 V ≤ EV _{DD0} ≤ 3.6 V		8	MHz
				2.4 V ≤ EV _{DD0} < 2.7 V		4	MHz
PCLBUZ0, PCLBUZ1 output frequency	f _{PCL}	HS (high-speed main) mode		2.7 V ≤ EV _{DD0} ≤ 3.6 V		8	MHz
				2.4 V ≤ EV _{DD0} < 2.7 V		4	MHz
Interrupt input high-level width, low-level width	t _{INTH} , t _{INTL}	INTP0	2.4 V ≤ V _{DD} ≤ 3.6 V	1			μs
		INTP1 to INTP11	2.4 V ≤ EV _{DD0} ≤ 3.6 V	1			μs
Key interrupt input high-level width, low-level width	t _{KR}	KR0 to KR9	2.4 V ≤ EV _{DD0} ≤ 3.6 V, 2.4 V ≤ AV _{DD0} ≤ 3.6 V	250			ns
RESET low-level width	t _{RSL}			10			μs

Note The following conditions are required for low-voltage interface when EV_{DD0} < V_{DD}.2.4 V ≤ EV_{DD0} < 2.7 V : MIN. 125 ns**Remark** f_{MCK}: Timer array unit operation clock frequency

(Operation clock to be set by the CKS0n bit of timer clock select register 0 (TPS0) and timer mode register 0n (TMR0n). n: Channel number (n = 0 to 7))

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)

(T_A = -40 to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq \text{V}_{\text{DD}} \leq 3.6\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCKp cycle time	t_{KCY1}	$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$ $t_{\text{KCY1}} \geq 4/f_{\text{CLK}}$	250			ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$ $t_{\text{KCY1}} \geq 4/f_{\text{CLK}}$	500			ns
SCKp high-/low-level width	$t_{\text{KH1}},$ t_{KL1}	$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$	$t_{\text{KCY1}}/2 - 36$			ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$	$t_{\text{KCY1}}/2 - 76$			ns
Slp setup time (to SCKp \uparrow) ^{Note 1}	t_{SIK1}	$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$	66			ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$	113			ns
Slp hold time (from SCKp \uparrow) ^{Note 1}	t_{KSI1}		38			ns
Delay time from SCKp \downarrow to SOp output ^{Note 2}	t_{KSO1}	$C = 30\text{ p}$ ^{Note 3}			50	ns

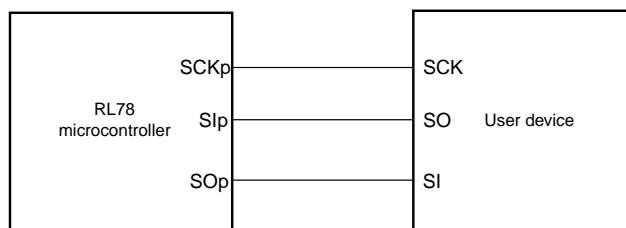
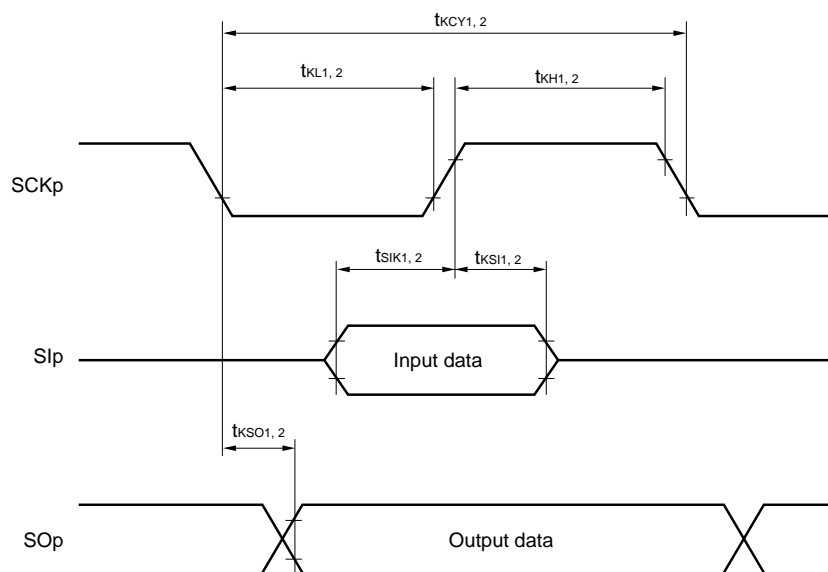
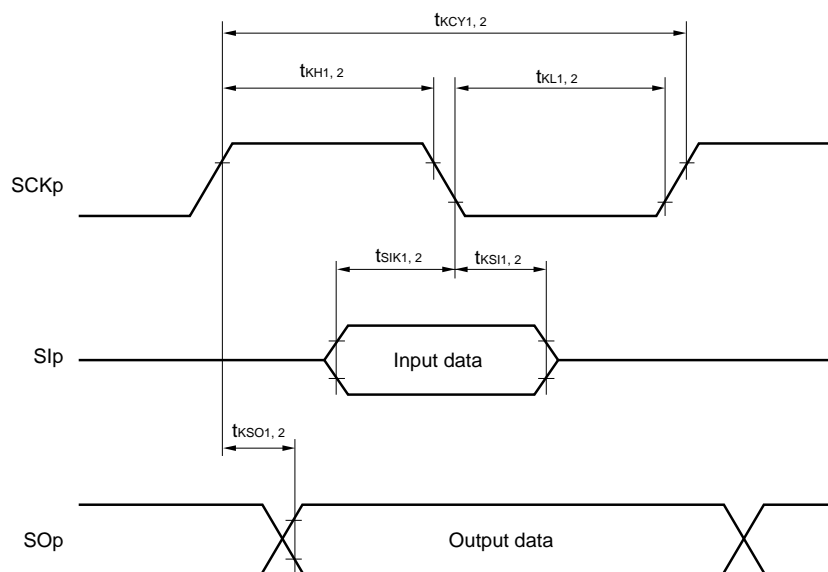
Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time or Slp hold time becomes “from SCKp \downarrow ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp \uparrow ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark p: CSI number (p = 00, 01, 10, 11, 20, 21), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 1)

CSI mode connection diagram (during communication at same potential)**CSI mode serial transfer timing (during communication at same potential)**(When $\text{DAPmn} = 0$ and $\text{CKPmn} = 0$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 1$.)**CSI mode serial transfer timing (during communication at same potential)**(When $\text{DAPmn} = 0$ and $\text{CKPmn} = 1$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 0$.)

- Remarks**
1. p: CSI number (p = 00, 01, 10, 11, 20, 21)
 2. m: Unit number, n: Channel number (mn = 00 to 03, 10, 11)

(5) Communication at different potential (1.8 V, 2.5 V) (UART mode) (dedicated baud rate generator output) (1/2)
($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq EV_{DD0} \leq V_{DD} \leq 3.6\text{ V}$, $V_{SS} = EV_{SS0} = 0\text{ V}$)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Transfer rate ^{Note 1}		Reception	$2.7\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$				$f_{MCK}/12$	bps
				Theoretical value of the maximum transfer rate $f_{CLK} = 32\text{ MHz}$, $f_{MCK} = f_{CLK}$			2.6	Mbps
			$2.4\text{ V} \leq EV_{DD0} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$				$f_{MCK}/12$	bps
				Theoretical value of the maximum transfer rate $f_{CLK} = 32\text{ MHz}$, $f_{MCK} = f_{CLK}$			2.6 ^{Note 2}	Mbps

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps.

2. The following conditions are required for low-voltage interface when $EV_{DD0} < V_{DD}$.

$2.4\text{ V} \leq EV_{DD0} < 2.7\text{ V}$: MAX. 1.3 Mbps

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (When 25- to 48-pin products)/ EV_{DD} tolerance (When 64-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

<R>

Remarks 1. $V_b[V]$: Communication line voltage

2. q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1)

3. f_{MCK} : Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

(7) Communication at different potential (1.8 V, 2.5 V) (CSI mode) (slave mode, SCKp... external clock input)

 $(T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq EV_{DD0} \leq V_{DD} \leq 3.6\text{ V}$, $V_{SS} = EV_{SS0} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCKp cycle time ^{Note 1}	t_{KCY2}	$2.7\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$	$24\text{ MHz} < f_{MCK}$	$40/f_{MCK}$		ns
			$20\text{ MHz} < f_{MCK} \leq 24\text{ MHz}$	$32/f_{MCK}$		ns
			$16\text{ MHz} < f_{MCK} \leq 20\text{ MHz}$	$28/f_{MCK}$		ns
			$8\text{ MHz} < f_{MCK} \leq 16\text{ MHz}$	$24/f_{MCK}$		ns
			$4\text{ MHz} < f_{MCK} \leq 8\text{ MHz}$	$16/f_{MCK}$		ns
			$f_{MCK} \leq 4\text{ MHz}$	$12/f_{MCK}$		ns
		$2.4\text{ V} \leq EV_{DD0} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$	$24\text{ MHz} < f_{MCK}$	$96/f_{MCK}$		ns
			$20\text{ MHz} < f_{MCK} \leq 24\text{ MHz}$	$72/f_{MCK}$		ns
			$16\text{ MHz} < f_{MCK} \leq 20\text{ MHz}$	$64/f_{MCK}$		ns
			$8\text{ MHz} < f_{MCK} \leq 16\text{ MHz}$	$52/f_{MCK}$		ns
			$4\text{ MHz} < f_{MCK} \leq 8\text{ MHz}$	$32/f_{MCK}$		ns
			$f_{MCK} \leq 4\text{ MHz}$	$20/f_{MCK}$		ns
SCKp high-/low-level width	t_{KH2} , t_{KL2}	$2.7\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$	$t_{KCY2}/2 - 36$			ns
		$2.4\text{ V} \leq EV_{DD0} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$	$t_{KCY2}/2 - 100$			ns
Slp setup time (to SCKp \uparrow) ^{Note 2}	t_{SIK2}	$2.7\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$	$1/f_{MCK} + 40$			ns
		$2.4\text{ V} \leq EV_{DD0} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$	$1/f_{MCK} + 60$			
Slp hold time (from SCKp \uparrow) ^{Note 2}	t_{KSI2}		$1/f_{MCK} + 62$			ns
Delay time from SCKp \downarrow to SOp output ^{Note 3}	t_{KSO2}	$2.7\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$			$2/f_{MCK} + 428$	ns
		$2.4\text{ V} \leq EV_{DD0} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$			$2/f_{MCK} + 1146$	ns

Notes 1. Transfer rate in the SNOOZE mode : MAX. 1 Mbps**2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time or Slp hold time becomes "from SCKp \downarrow " when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.**3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp \uparrow " when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the Slp pin and SCKp pin and the N-ch open drain output (V_{DD} tolerance (When 25- to 48-pin products)/ EV_{DD} tolerance (When 64-pin products)) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

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(Remarks are listed on the next page.)

(8) Communication at different potential (1.8 V, 2.5 V) (simplified I²C mode) (1/2)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq E_{VDD0} \leq V_{DD} \leq 3.6\text{ V}$, $V_{SS} = E_{VSS0} = 0\text{ V}$)**

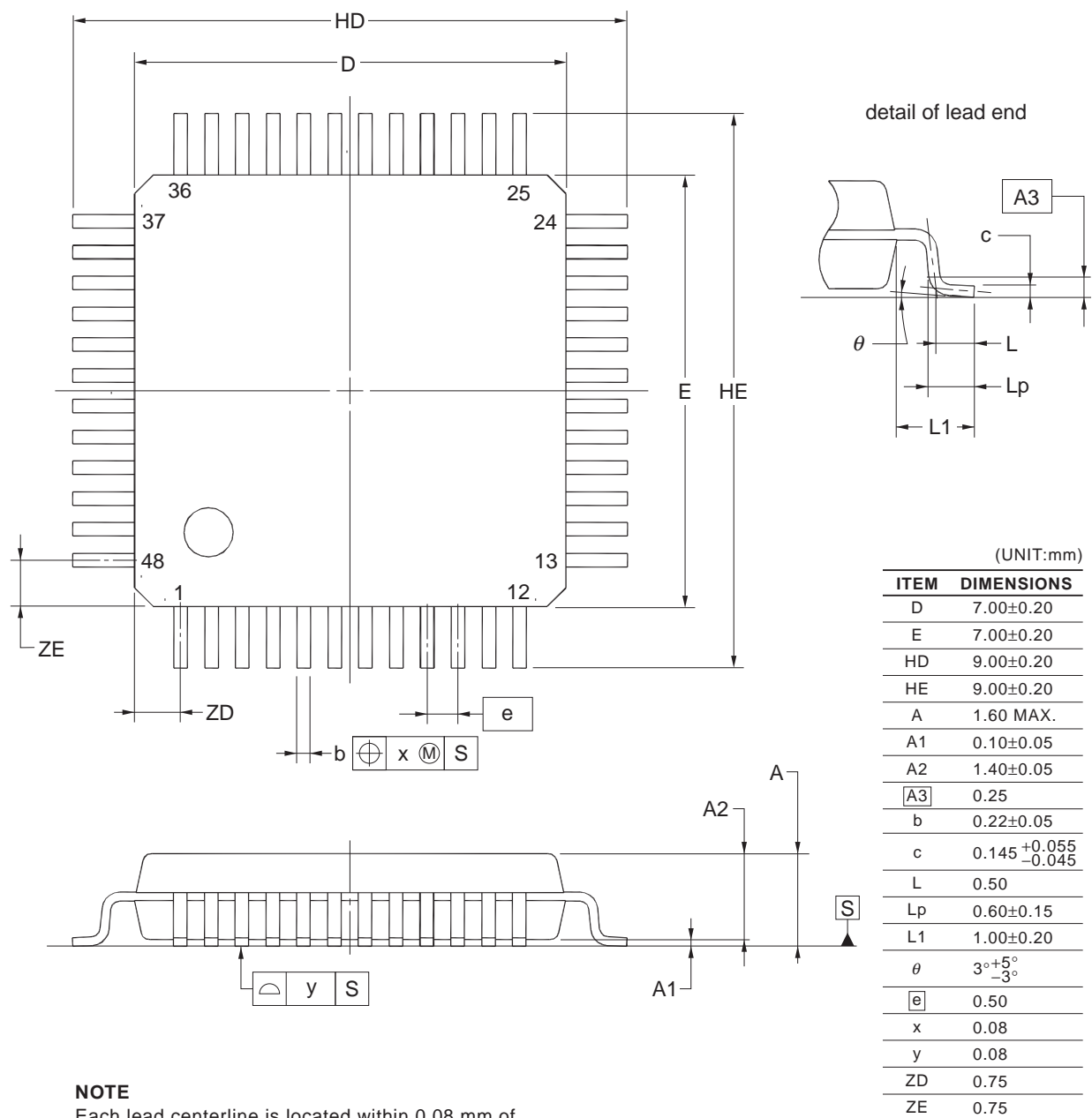
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCLr clock frequency	f_{SCL}	$2.7\text{ V} \leq E_{VDD0} \leq 3.6\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$		400 ^{Note 1}	kHz
		$2.7\text{ V} \leq E_{VDD0} \leq 3.6\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 2.7\text{ k}\Omega$		100 ^{Note 1}	kHz
		$2.4\text{ V} \leq E_{VDD0} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 5.5\text{ k}\Omega$		100 ^{Note 1}	kHz
Hold time when SCLr = "L"	t_{LOW}	$2.7\text{ V} \leq E_{VDD0} \leq 3.6\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	1200		ns
		$2.7\text{ V} \leq E_{VDD0} \leq 3.6\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	4600		ns
		$2.4\text{ V} \leq E_{VDD0} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 5.5\text{ k}\Omega$	4650		ns
Hold time when SCLr = "H"	t_{HIGH}	$2.7\text{ V} \leq E_{VDD0} \leq 3.6\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	500		ns
		$2.7\text{ V} \leq E_{VDD0} \leq 3.6\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	2400		ns
		$2.4\text{ V} \leq E_{VDD0} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 5.5\text{ k}\Omega$	1830		ns

(Notes, Caution and Remarks are listed on the next page.)

4.3 48-pin products

R5F10EGAAFB, R5F10EGCAFB, R5F10EGDAFB, R5F10EGEAFB
R5F10EGAGFB, R5F10EGCGFB, R5F10EGDGFB, R5F10EGEGFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP48-7x7-0.50	PLQP0048KF-A	P48GA-50-8EU-1	0.16

**NOTE**

Each lead centerline is located within 0.08 mm of its true position at maximum material condition.