Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	32
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LFQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10egdafb-v0

Absolute Maximum Ratings (T$_A$ = 25°C) (2/2)

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	I$_{OH1}$	Per pin	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P130, P140, P141	−40	mA
		Total of all pins −170 mA	P00 to P04, P40 to P43, P120, P130, P140, P141	−70	mA
			P05, P06, P10 to P16, P30, P31, P50, P51, P70 to P77,	−100	mA
	I$_{OH2}$	Per pin	P20 to P27, P150 to P154	−0.1	mA
		Total of all pins		−1.3	mA
Output current, low	I$_{OL1}$	Per pin	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P60 to P63, P70 to P77, P120, P130, P140, P141	40	mA
		Total of all pins 170 mA	P00 to P04, P40 to P43, P120, P130, P140, P141	70	mA
			P05, P06, P10 to P16, P30, P31, P50, P51, P60 to P63, P70 to P77	100	mA
	I$_{OL2}$	Per pin	P20 to P27, P150 to P154	0.4	mA
		Total of all pins		6.4	mA
Operating ambient temperature	T$_A$	In normal operation mode		−40 to +85	°C
		In flash memory programming mode			
Storage temperature	T$_{stg}$			−65 to +150	°C

Caution **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T$_A$ = −40 to +85°C, 1.6 V ≤ AV$_{DD}$ ≤ V$_{DD}$ ≤ 3.6 V, 1.6 V ≤ EV$_{DD0}$ ≤ V$_{DD}$ ≤ 3.6 V, V$_{SS}$ = EV$_{SS0}$ = 0 V) (2/5)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low[Note 1]	I$_{OL1}$	Per pin for P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P130, P140, P141				20.0[Note 2]	mA
		Per pin for P60 to P63				15.0[Note 2]	mA
		Total of P00 to P04, P40 to P43, P120, P130, P140, P141 (When duty ≤ 70%[Note 3])	2.7 V ≤ EV$_{DD0}$ ≤ 3.6 V			15.0	mA
			1.8 V ≤ EV$_{DD0}$ < 2.7 V			9.0	mA
			1.6 V ≤ EV$_{DD0}$ < 1.8 V			4.5	mA
		Total of P05, P06, P10 to P16, P30, P31, P50, P51, P60 to P63, P70 to P77 (When duty ≤ 70%[Note 3])	2.7 V ≤ EV$_{DD0}$ ≤ 3.6 V			35.0	mA
			1.8 V ≤ EV$_{DD0}$ < 2.7 V			20.0	mA
			1.6 V ≤ EV$_{DD0}$ < 1.8 V			10.0	mA
		Total of all pins (When duty ≤ 70%[Note 3])				50.0	mA
	I$_{OL2}$	Per pin for P20 to P27, P150 to P154				0.4[Note 2]	mA
		Total of all pins (When duty ≤ 70%[Note 3])	1.6 V ≤ AV$_{DD}$ ≤ 3.6 V			5.2	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the EV$_{SS0}$ and V$_{SS}$ pin.

2. However, do not exceed the total current value.

3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I$_{OL}$ × 0.7)/(n × 0.01)

<Example> Where n = 80% and I$_{OL}$ = 10.0 mA

Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≅ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Notes 1. Total current flowing into V_{DD} and EV_{DD0}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, on-chip pull-up/pull-down resistors, and data flash rewriting.

    2. When high-speed on-chip oscillator and subsystem clock are stopped.

    3. When high-speed system clock and subsystem clock are stopped.

    4. When high-speed on-chip oscillator and high-speed system clock are stopped. When setting ultra-low power consumption oscillation (AMPHS1 = 1). Not including the current flowing into the RTC, 12-bit interval timer and watchdog timer

    5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

        HS (high-speed main) mode: V_{DD} = 2.7 V to 3.6 V@1 MHz to 32 MHz

                                  V_{DD} = 2.4 V to 3.6 V@1 MHz to 16 MHz

        LS (low-speed main) mode: V_{DD} = 1.8 V to 3.6 V@1 MHz to 8 MHz

        LV (Low-voltage main) mode: V_{DD} = 1.6 V to 3.6 V@1 MHz to 4 MHz

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

    2. f_{IH}: High-speed on-chip oscillator clock frequency

    3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

    4. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

(8) Communication at different potential (1.8V, 2.5 V) (CSI mode) (master mode, SCKp... internal clock output) (1/2)

(T$_A$ = −40 to +85°C, 1.8 V ≤ EV$_{DD0}$ ≤ V$_{DD}$ ≤ 3.6 V, V$_{SS}$ = EV$_{SS0}$ = 0 V)

Parameter	Symbol	Conditions		HS[Note 1]		LS[Note 2]		LV[Note 3]		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t$_{KCY1}$	2.7 V ≤ EV$_{DD0}$ ≤ 3.6 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 30 pF, R$_b$ = 2.7 kΩ	t$_{KCY1}$ ≥ 4/f$_{CLK}$	500		1150		1150		ns
		1.8 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V[Note 4], C$_b$ = 30 pF, R$_b$ = 5.5 kΩ	t$_{KCY1}$ ≥ 4/f$_{CLK}$	1150		1150		1150		ns
SCKp high-level width	t$_{KH1}$	2.7 V ≤ EV$_{DD0}$ ≤ 3.6 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 30 pF, R$_b$ = 2.7 kΩ		t$_{KCY1}$/2 − 170		t$_{KCY1}$/2 − 170		t$_{KCY1}$/2 − 170		ns
		1.8 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V[Note 4], C$_b$ = 30 pF, R$_b$ = 5.5 kΩ		t$_{KCY1}$/2 − 458		t$_{KCY1}$/2 − 458		t$_{KCY1}$/2 − 458		ns
SCKp low-level width	t$_{KL1}$	2.7 V ≤ EV$_{DD0}$ ≤ 3.6 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 30 pF, R$_b$ = 2.7 kΩ		t$_{KCY1}$/2 − 18		t$_{KCY1}$/2 − 50		t$_{KCY1}$/2 − 50		ns
		1.8 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V[Note 4], C$_b$ = 30 pF, R$_b$ = 5.5 kΩ		t$_{KCY1}$/2 − 50		t$_{KCY1}$/2 − 50		t$_{KCY1}$/2 − 50		ns

Notes 1. HS is condition of HS (high-speed main) mode.

2. LS is condition of LS (low-speed main) mode.

3. LV is condition of LV (low-voltage main) mode.

4. Use it with EV$_{DD0}$ ≥ V$_b$.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V$_{DD}$ tolerance (When 25- to 48-pin products)/EV$_{DD}$ tolerance (When 64-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V$_{IH}$ and V$_{IL}$, see the DC characteristics with TTL input buffer selected.

<R>

Remarks 1. R$_b$[Ω]: Communication line (SCKp, SOp) pull-up resistance, C$_b$[F]: Communication line (SCKp, SOp) load capacitance, V$_b$[V]: Communication line voltage

2. p: CSI number (p = 00, 10, 20), m: Unit number , n: Channel number (mn = 00, 02, 10), g: PIM and POM number (g = 0, 1)

3. CSI01, CSI11, and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

Simplified I^{2}C mode connection diagram (during communication at different potential)
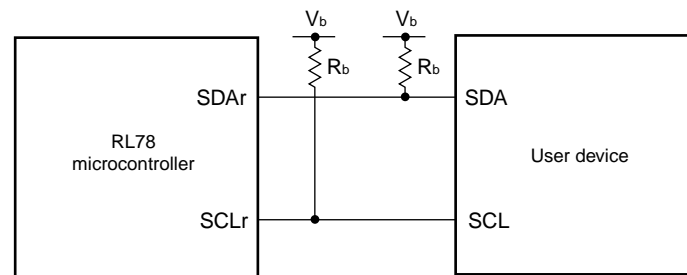
Simplified I^{2}C mode serial transfer timing (during communication at different potential)
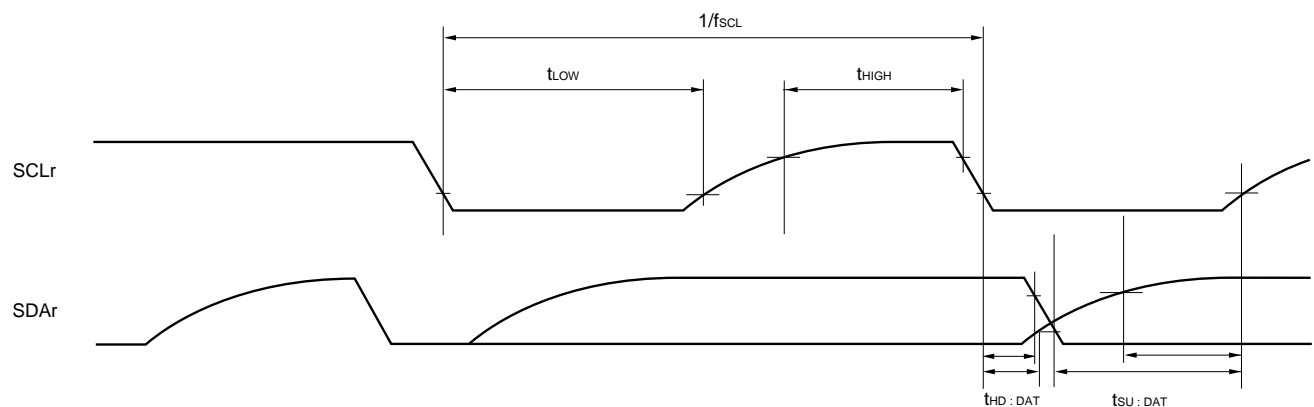
Remarks 1. R$_b$[Ω]: Communication line (SDAr, SCLr) pull-up resistance, C$_b$[F]: Communication line (SDAr, SCLr) load capacitance, V$_b$[V]: Communication line voltage

   2. r: IIC number (r = 00, 10, 20), g: PIM, POM number (g = 0, 1)

   3. f$_{MCK}$: Serial array unit operation clock frequency
   (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).   m: Unit number, n: Channel number (mn = 00, 02, 10)

   4. IIC01, IIC11, and IIC21 cannot communicate at different potential.   Use IIC00, IIC10, or IIC20 for communication at different potential.

(2) I²C fast mode, fast mode plus

(T_A = −40 to +85°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions	Fast Mode[7]						Fast Mode Plus[8]		Unit
			HS[2]		LS[3]		LV[4]		HS[2]		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	2.7 V ≤ EV_{DD0} ≤ 3.6 V	0	400	0	400	0	400	0	1000	kHz
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	0	400	0	400	0	400	–		
Setup time of restart condition	$t_{SU:STA}$	2.7 V ≤ EV_{DD0} ≤ 3.6 V	0.6		0.6		0.6		0.26		µs
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	0.6		0.6		0.6		–		
Hold time[5]	$t_{HD:STA}$	2.7 V ≤ EV_{DD0} ≤ 3.6 V	0.6		0.6		0.6		0.26		µs
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	0.6		0.6		0.6		–		
Hold time when SCLA0 = "L"	t_{LOW}	2.7 V ≤ EV_{DD0} ≤ 3.6 V	1.3		1.3		1.3		0.5		µs
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	1.3		1.3		1.3		–		
Hold time when SCLA0 = "H"	t_{HIGH}	2.7 V ≤ EV_{DD0} ≤ 3.6 V	0.6		0.6		0.6		0.26		µs
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	0.6		0.6		0.6		–		
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ EV_{DD0} ≤ 3.6 V	100		100		100		50		ns
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	100		100		100		–		
Data hold time (transmission)[6]	$t_{HD:DAT}$	2.7 V ≤ EV_{DD0} ≤ 3.6 V	0	0.9	0	0.9	0	0.9	0	450	µs
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	0	0.9	0	0.9	0	0.9	–		
Setup time of stop condition	$t_{SU:STO}$	2.7 V ≤ EV_{DD0} ≤ 3.6 V	0.6		0.6		0.6		0.26		µs
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	0.6		0.6		0.6		–		
Bus-free time	t_{BUF}	2.7 V ≤ EV_{DD0} ≤ 3.6 V	1.3		1.3		1.3		0.5		µs
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	1.3		1.3		1.3		–		

Notes 1. In normal mode, use it with f_{CLK} ≥ 1 MHz, 1.6 V ≤ EV_{DD} ≤ 3.6 V.

    2. HS is condition of HS (high-speed main) mode.

    3. LS is condition of LS (low-speed main) mode.

    4. LV is condition of LV (low-voltage main) mode.

    5. The first clock pulse is generated after this period when the start/restart condition is detected.

    6. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

    7. In fast mode, use it with f_{CLK} ≥ 3.5 MHz, 1.8 V ≤ EV_{DD} ≤ 3.6 V.

    8. In fast mode plus, use it with f_{CLK} ≥ 10 MHz, 2.7 V ≤ EV_{DD} ≤ 3.6 V.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

    Standard mode: C_b = 400 pF, R_b = 2.7 kΩ

    Fast mode: C_b = 320 pF, R_b = 1.1 kΩ

    Fast mode plus: C_b = 120 pF, R_b = 1.1 kΩ

2.6   Analog Characteristics

2.6.1   A/D converter characteristics

Division of A/D Converter Characteristics

Reference voltage / Input channel	Reference voltage (+) = AV$_{REFP}$ Reference voltage (−) = AV$_{REFM}$	Reference voltage (+) = AV$_{DD}$ Reference voltage (−) = AV$_{SS}$	Reference voltage (+) = Internal refrence voltage Reference voltage (−) = AV$_{SS}$
High-accuracy channel; ANI0 to ANI12 (input buffer power supply: AV$_{DD}$)	See **2.6.1 (1)** See **2.6.1 (2)**	See **2.6.1 (3)**	See **2.6.1 (6)**
Standard channel; ANI16 to ANI30 (input buffer power supply: V$_{DD}$ or EV$_{DD0}$)	See **2.6.1 (4)**	See **2.6.1 (5)**	
Temperature sensor, internal reference voltage output	See **2.6.1 (4)**	See **2.6.1 (5)**	–

<R>   **(1) When reference voltage (+) = AV$_{REFP}$/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = AV$_{REFM}$/ANI1 (ADREFM = 1), target for conversion: ANI2 to ANI12**

<R>   **(T$_A$ = –40 to +85°C, 2.4 V ≤ AV$_{REFP}$ ≤ AV$_{DD}$ ≤ V$_{DD}$ ≤ 3.6 V, V$_{SS}$ = 0 V, AV$_{SS}$ = 0 V, Reference voltage (+) = AV$_{REFP}$, Reference voltage (–) = AV$_{REFM}$ = 0 V, HALT mode)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	R$_{ES}$				12	bit
Overall error[Notes 1, 2, 3]	AINL	12-bit resolution		±1.7	±3.3	LSB
Conversion time	t$_{CONV}$	ADTYP = 0, 12-bit resolution	3.375			µs
Zero-scale error[Notes 1, 2, 3]	E$_{ZS}$	12-bit resolution		±1.3	±3.2	LSB
Full-scale error[Notes 1, 2, 3]	E$_{FS}$	12-bit resolution		±0.7	±2.9	LSB
Integral linearity error[Notes 1, 2, 3]	ILE	12-bit resolution		±1.0	±1.4	LSB
Differential linearity error[Notes 1, 2, 3]	DLE	12-bit resolution		±0.9	±1.2	LSB
Analog input voltage	V$_{AIN}$		0		AV$_{REFP}$	V

Notes 1. TYP. Value is the average value at AV$_{DD}$ = AV$_{REFP}$ = 3 V and T$_A$ = 25°C.   MAX. value is the average value ±3σ at normalized distribution.
   2. These values are the results of characteristic evaluation and are not checked for shipment.
   3. Excludes quantization error (±1/2 LSB).

Cautions 1. Route the wiring so that noise will not be superimposed on each power line and ground line, and insert a capacitor to suppress noise.
   In addition, separate the reference voltage line of AV$_{REFP}$ from the other power lines to keep it free from the influences of noise.
   2. During A/D conversion, keep a pulse, such as a digital signal, that abruptly changes its level from being input to or output from the pins adjacent to the converter pins and P20 to P27 and P150 to P154.

<R> **(3) When reference voltage (+) = AV$_{DD}$ (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) = AV$_{SS}$ (ADREFM = 0), target for conversion: ANI0 to ANI12**

(T_A = −40 to +85°C, 1.6 V ≤ AV$_{DD}$ ≤ V$_{DD}$ ≤ 3.6 V, V$_{SS}$ = 0 V, AV$_{SS}$ = 0 V, Reference voltage (+) = AV$_{DD}$, Reference voltage (–) = AV$_{SS}$ = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}		2.4 V ≤ AV$_{DD}$ ≤ 3.6 V	8		12	bit
			1.8 V ≤ AV$_{DD}$ ≤ 3.6 V	8		10[Note 1]	
			1.6 V ≤ AV$_{DD}$ ≤ 3.6 V		8[Note 2]		
Overall error[Note 3]	AINL	12-bit resolution	2.4 V ≤ AV$_{DD}$ ≤ 3.6 V			±7.5	LSB
		10-bit resolution	1.8 V ≤ AV$_{DD}$ ≤ 3.6 V			±5.5	
		8-bit resolution	1.6 V ≤ AV$_{DD}$ ≤ 3.6 V			±3.0	
Conversion time	t_{CONV}	ADTYP = 0, 12-bit resolution	2.4 V ≤ AV$_{DD}$ ≤ 3.6 V	3.375			μs
		ADTYP = 0, 10-bit resolution[Note 1]	1.8 V ≤ AV$_{DD}$ ≤ 3.6 V	6.75			
		ADTYP = 0, 8-bit resolution[Note 2]	1.6 V ≤ AV$_{DD}$ ≤ 3.6 V	13.5			
		ADTYP = 1, 8-bit resolution	2.4 V ≤ AV$_{DD}$ ≤ 3.6 V	2.5625			
			1.8 V ≤ AV$_{DD}$ ≤ 3.6 V	5.125			
			1.6 V ≤ AV$_{DD}$ ≤ 3.6 V	10.25			
Zero-scale error[Note 3]	E_{ZS}	12-bit resolution	2.4 V ≤ AV$_{DD}$ ≤ 3.6 V			±6.0	LSB
		10-bit resolution	1.8 V ≤ AV$_{DD}$ ≤ 3.6 V			±5.0	
		8-bit resolution	1.6 V ≤ AV$_{DD}$ ≤ 3.6 V			±2.5	
Full-scale error[Note 3]	E_{FS}	12-bit resolution	2.4 V ≤ AV$_{DD}$ ≤ 3.6 V			±6.0	LSB
		10-bit resolution	1.8 V ≤ AV$_{DD}$ ≤ 3.6 V			±5.0	
		8-bit resolution	1.6 V ≤ AV$_{DD}$ ≤ 3.6 V			±2.5	
Integral linearity error[Note 3]	ILE	12-bit resolution	2.4 V ≤ AV$_{DD}$ ≤ 3.6 V			±3.0	LSB
		10-bit resolution	1.8 V ≤ AV$_{DD}$ ≤ 3.6 V			±2.0	
		8-bit resolution	1.6 V ≤ AV$_{DD}$ ≤ 3.6 V			±1.5	
Differential linearity error[Note 3]	DLE	12-bit resolution	2.4 V ≤ AV$_{DD}$ ≤ 3.6 V			±2.0	LSB
		10-bit resolution	1.8 V ≤ AV$_{DD}$ ≤ 3.6 V			±2.0	
		8-bit resolution	1.6 V ≤ AV$_{DD}$ ≤ 3.6 V			±1.5	
<R> Analog input voltage	V_{AIN}			0		AV$_{DD}$	V

Notes **1.** Cannot be used for lower 2 bit of ADCR register

    2. Cannot be used for lower 4 bit of ADCR register

    3. Excludes quantization error (±1/2 LSB).

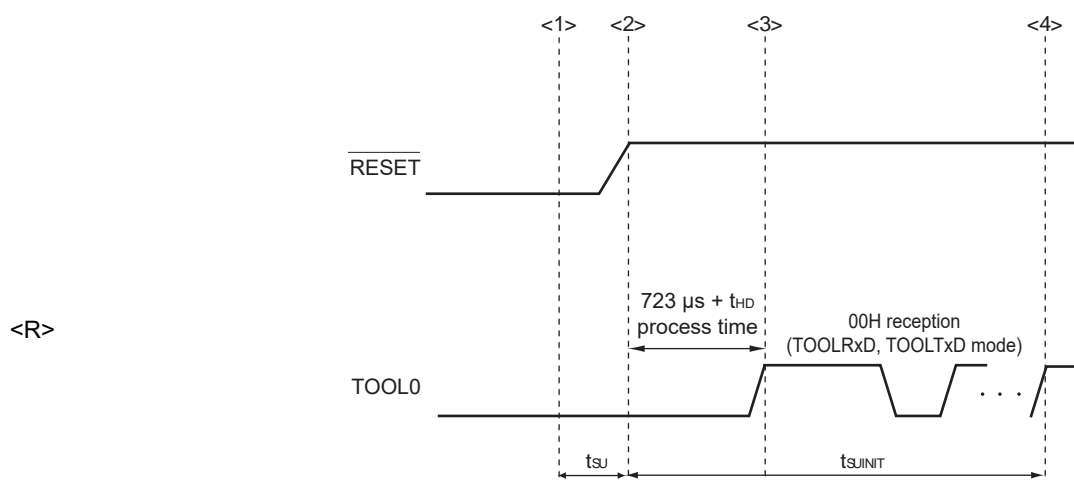## 2.9 Dedicated Flash Memory Programmer Communication (UART)

(T_A = −40 to +85°C, 1.8 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During flash memory programming	115.2 k		1 M	bps

2.10 Timing Specs for Switching Flash Memory Programming Modes

(T_A = −40 to +85°C, 1.8 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

	Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
	How long from when an external reset ends until the initial communication settings are specified	t_{SUINIT}	POR and LVD reset must end before the external reset ends.			100	ms
	How long from when the TOOL0 pin is placed at the low level until a external reset ends	t_{SU}	POR and LVD reset must end before the external reset ends.	10			μs
\<R\>	How long the TOOL0 pin must be kept at the low level after an external reset ends (except flash firmware processing time)	t_{HD}	POR and LVD reset must end before the external reset ends.	1			ms

\<R\>

<1> The low level is input to the TOOL0 pin.
<2> The pins reset ends (POR and LVD reset must end before the external reset ends.).
<3> The TOOL0 pin is set to the high level.
<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t_{SUINIT}: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the resets end.

      t_{SU}: How long from when the TOOL0 pin is placed at the low level until a external reset ends

\<R\> t_{HD}: How long to keep the TOOL0 pin at the low level from when the external resets end (except flash firmware processing time)

(T_A = –40 to +105°C, 2.4 V ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V, 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)   (4/5)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P130, P140, P141	2.7 V ≤ EV_{DD0} ≤ 3.6 V, I_{OH1} = –2.0 mA	EV_{DD0} – 0.6			V
			2.4 V ≤ EV_{DD0} ≤ 3.6 V, I_{OH1} = –1.5 mA	EV_{DD0} – 0.5			V
	V_{OH2}	P20 to P27, P150 to P154	2.4 V ≤ AV_{DD} ≤ 3.6 V, I_{OH2} = –100 μA	AV_{DD} – 0.5			V
Output voltage, low	V_{OL1}	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P130, P140, P141	2.7 V ≤ EV_{DD0} ≤ 3.6 V, I_{OL1} = 3.0 mA			0.6	V
			2.7 V ≤ EV_{DD0} ≤ 3.6 V, I_{OL1} = 1.5 mA			0.4	V
			2.4 V ≤ EV_{DD0} ≤ 3.6 V, I_{OL1} = 0.6 mA			0.4	V
	V_{OL2}	P20 to P27, P150 to P154	2.4 V ≤ AV_{DD} ≤ 3.6 V, I_{OL2} = 400 μA			0.4	V
	V_{OL3}	P60 to P63	2.7 V ≤ EV_{DD0} ≤ 3.6 V, I_{OL3} = 3.0 mA			0.4	V
			2.4 V ≤ EV_{DD0} ≤ 3.6 V, I_{OL3} = 2.0 mA			0.4	V

Caution **P00, P02 to P04, P10 to P15, P43, P50, P71, and P74 do not output high level in N-ch open-drain mode.**

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)
(T$_A$ = −40 to +105°C, 2.4 V ≤ EV$_{DD0}$ ≤ V$_{DD}$ ≤ 3.6 V, V$_{SS}$ = EV$_{SS0}$ = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCKp cycle time	t$_{KCY1}$	2.7 V ≤ EV$_{DD0}$ ≤ 3.6 V	t$_{KCY1}$ ≥ 4/f$_{CLK}$	250			ns
		2.4 V ≤ EV$_{DD0}$ ≤ 3.6 V	t$_{KCY1}$ ≥ 4/f$_{CLK}$	500			ns
SCKp high-/low-level width	t$_{KH1}$, t$_{KL1}$	2.7 V ≤ EV$_{DD0}$ ≤ 3.6 V		t$_{KCY1}$/2 − 36			ns
		2.4 V ≤ EV$_{DD0}$ ≤ 3.6 V		t$_{KCY1}$/2 − 76			ns
SIp setup time (to SCKp↑)[Note 1]	t$_{SIK1}$	2.7 V ≤ EV$_{DD0}$ ≤ 3.6 V		66			ns
		2.4 V ≤ EV$_{DD0}$ ≤ 3.6 V		113			ns
SIp hold time (from SCKp↑)[Note 1]	t$_{KSI1}$			38			ns
Delay time from SCKp↓ to SOp output[Note 2]	t$_{KSO1}$	C = 30 p[Note 3]				50	ns

Notes   **1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time or SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

     2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

     3. C is the load capacitance of the SCKp and SOp output lines.

Caution   **Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

Remark   p: CSI number (p = 00, 01, 10, 11, 20, 21), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),
        g: PIM and POM numbers (g = 0, 1)

(4) During communication at same potential (simplified I²C mode)

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCLr clock frequency	f_{SCL}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, C_b = 50 pF, R_b = 2.7 kΩ		400[Note 1]	kHz
		2.4 V ≤ EV_{DD0} ≤ 3.6 V, C_b = 100 pF, R_b = 3 kΩ		100[Note 1]	kHz
Hold time when SCLr = "L"	t_{LOW}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, C_b = 50 pF, R_b = 2.7 kΩ	1200		ns
		2.4 V ≤ EV_{DD0} ≤ 3.6 V, C_b = 100 pF, R_b = 3 kΩ	4600		ns
Hold time when SCLr = "H"	t_{HIGH}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, C_b = 50 pF, R_b = 2.7 kΩ	1200		ns
		2.4 V ≤ EV_{DD0} ≤ 3.6 V, C_b = 100 pF, R_b = 3 kΩ	4600		ns
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ EV_{DD0} ≤ 3.6 V, C_b = 50 pF, R_b = 2.7 kΩ	$1/f_{MCK}$ + 220[Note 2]		ns
		2.4 V ≤ EV_{DD} ≤ 3.6 V, C_b = 100 pF, R_b = 3 kΩ	$1/f_{MCK}$ + 580[Note 2]		ns
Data hold time (transmission)	$t_{HD:DAT}$	2.7 V ≤ EV_{DD0} ≤ 3.6 V, C_b = 50 pF, R_b = 2.7 kΩ	0	770	ns
		2.4 V ≤ EV_{DD0} ≤ 3.6 V, C_b = 100 pF, R_b = 3 kΩ	0	1420	ns

Notes 1. The value must also be f_{CLK}/4 or lower.

2. Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution **Select the normal input buffer and the N-ch open drain output (V_{DD} tolerance (When 25- to 48-pin products)/EV_{DD} tolerance (When 64-pin products)) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).**

Simplified I^{2}C mode mode connection diagram (during communication at same potential)
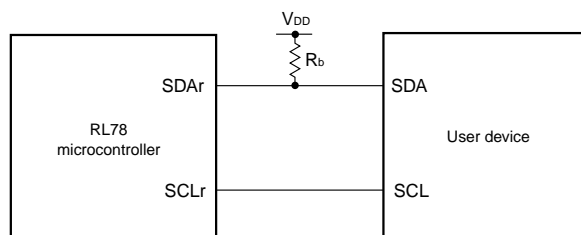
Simplified I^{2}C mode serial transfer timing (during communication at same potential)
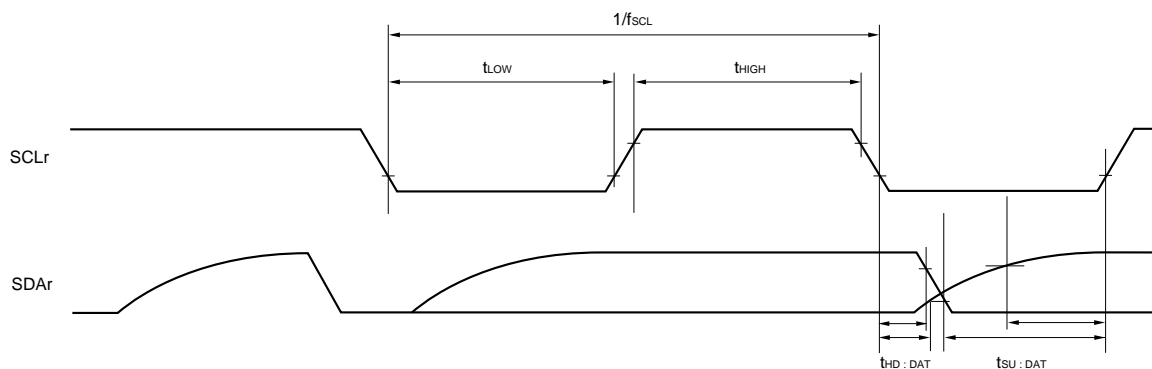
Remarks 1. R$_b$[Ω]: Communication line (SDAr) pull-up resistance, C$_b$[F]: Communication line (SDAr, SCLr) load capacitance

     2. r: IIC number (r = 00, 01, 10, 11, 20, 21), g: PIM number (g = 0, 1), h: POM number (h = 0, 1)

     3. f$_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number, mn = 00 to 03, 10, 11)

(7) Communication at different potential (1.8 V, 2.5 V) (CSI mode) (slave mode, SCKp... external clock input)
(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCKp cycle time[Note 1]	t_{KCY2}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V	24 MHz < f_{MCK}	40/f_{MCK}			ns
			20 MHz < f_{MCK} ≤ 24 MHz	32/f_{MCK}			ns
			16 MHz < f_{MCK} ≤ 20 MHz	28/f_{MCK}			ns
			8 MHz < f_{MCK} ≤ 16 MHz	24/f_{MCK}			ns
			4 MHz < f_{MCK} ≤ 8 MHz	16/f_{MCK}			ns
			f_{MCK} ≤ 4 MHz	12/f_{MCK}			ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V	24 MHz < f_{MCK}	96/f_{MCK}			ns
			20 MHz < f_{MCK} ≤ 24 MHz	72/f_{MCK}			ns
			16 MHz < f_{MCK} ≤ 20 MHz	64/f_{MCK}			ns
			8 MHz < f_{MCK} ≤ 16 MHz	52/f_{MCK}			ns
			4 MHz < f_{MCK} ≤ 8 MHz	32/f_{MCK}			ns
			f_{MCK} ≤ 4 MHz	20/f_{MCK}			ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V		t_{KCY2}/2 – 36			ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V		t_{KCY2}/2 – 100			ns
SIp setup time (to SCKp↑)[Note 2]	t_{SIK2}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V		1/f_{MCK} + 40			ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V		1/f_{MCK} + 60			ns
SIp hold time (from SCKp↑)[Note 2]	t_{KSI2}			1/f_{MCK} + 62			ns
Delay time from SCKp↓ to SOp output[Note 3]	t_{KSO2}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ				2/f_{MCK} + 428	ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ				2/f_{MCK} + 1146	ns

Notes 1. Transfer rate in the SNOOZE mode : MAX. 1 Mbps

   2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.   The SIp setup time or SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

   3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.   The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the SIp pin and SCKp pin and the N-ch open drain output (V_{DD} tolerance (When 25- to 48-pin products)/EV_{DD} tolerance (When 64-pin products)) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).   For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

<R>

(**Remarks** are listed on the next page.)

3.5.2 Serial interface IICA

(1) I²C standard mode, fast mode

(T$_A$ = −40 to +105°C, 2.4 V ≤ EV$_{DD0}$ ≤ V$_{DD}$ ≤ 3.6 V, V$_{SS}$ = EV$_{SS0}$ = 0 V)

Parameter	Symbol	Conditions		Standard Mode		Fast Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f$_{SCL}$	Fast mode: f$_{CLK}$ ≥ 3.5 MHz	2.4 V ≤ EV$_{DD0}$ ≤ 3.6 V			0	400	kHz
		Normal mode: f$_{CLK}$ ≥ 1 MHz	2.4 V ≤ EV$_{DD0}$ ≤ 3.6 V	0	100			kHz
Setup time of restart condition	t$_{SU:STA}$			4.7		0.6		μs
Hold time[Note 1]	t$_{HD:STA}$			4.0		0.6		μs
Hold time when SCLA0 = "L"	t$_{LOW}$			4.7		1.3		μs
Hold time when SCLA0 = "H"	t$_{HIGH}$			4.0		0.6		μs
Data setup time (reception)	t$_{SU:DAT}$			250		100		ns
Data hold time (transmission)[Note 2]	t$_{HD:DAT}$			0	3.45	0	0.9	μs
Setup time of stop condition	t$_{SU:STO}$			4.0		0.6		μs
Bus-free time	t$_{BUF}$			4.7		1.3		μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

   2. The maximum value (MAX.) of t$_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Remark The maximum value of C$_b$ (communication line capacitance) and the value of R$_b$ (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C$_b$ = 400 pF, R$_b$ = 2.7 kΩ

Fast mode: C$_b$ = 320 pF, R$_b$ = 1.1 kΩ

IICA serial transfer timing
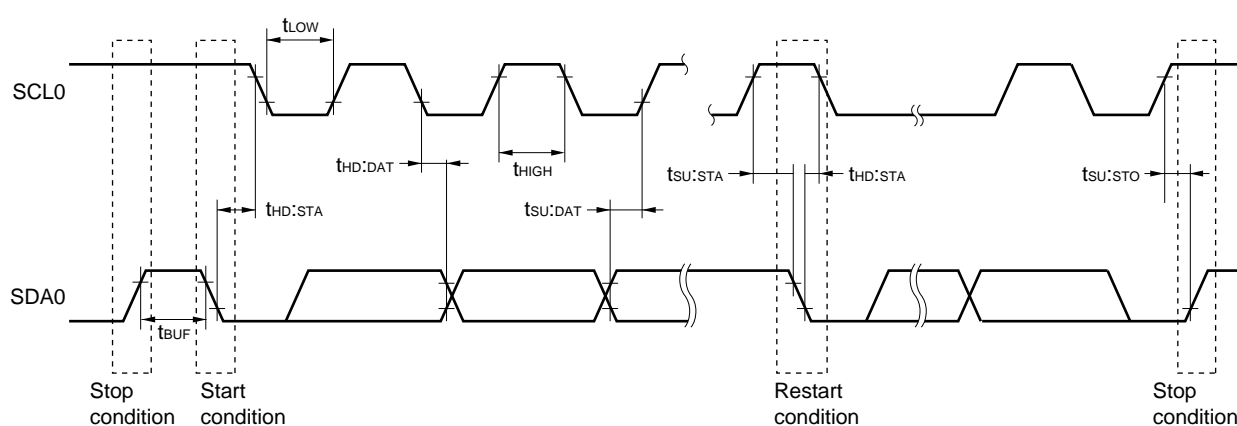
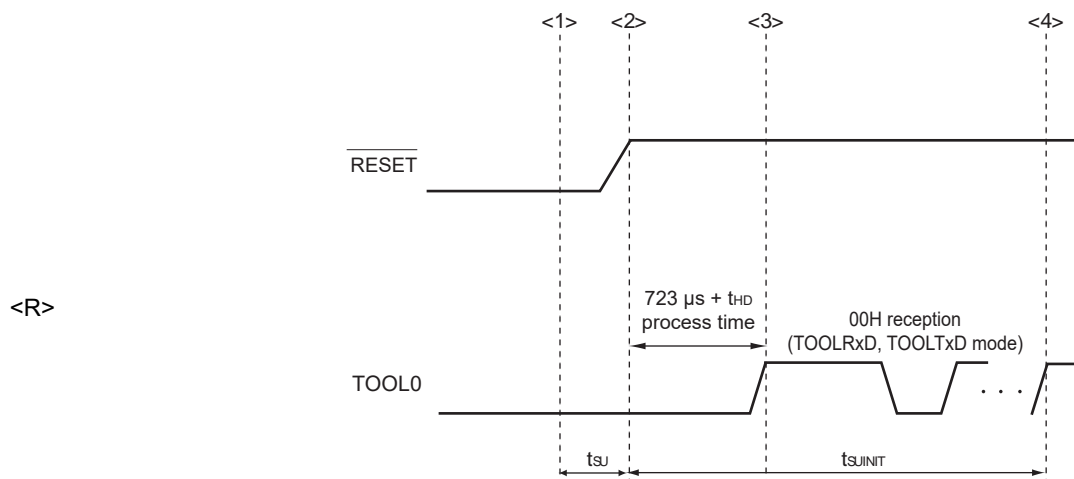## 3.9 Dedicated Flash Memory Programmer Communication (UART)

(T_A = −40 to +105°C, 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During flash memory programming	115.2 k		1 M	bps

3.10 Timing Specs for Switching Flash Memory Programming Modes

(T_A = −40 to +105°C, 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

	Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
	How long from when an external reset ends until the initial communication settings are specified	t_{SUINIT}	POR and LVD reset must end before the external reset ends.			100	ms
	How long from when the TOOL0 pin is placed at the low level until a external reset ends	t_{SU}	POR and LVD reset must end before the external reset ends.	10			μs
\<R\>	How long the TOOL0 pin must be kept at the low level after an external reset ends (except flash firmware processing time)	t_{HD}	POR and LVD reset must end before the external reset ends.	1			ms

\<R\>

<1> The low level is input to the TOOL0 pin.
<2> The pins reset ends (POR and LVD reset must end before the external reset ends.).
<3> The TOOL0 pin is set to the high level.
<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t_{SUINIT}: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the resets end.

       t_{SU}:   How long from when the TOOL0 pin is placed at the low level until a external reset ends

\<R\> t_{HD}:   How long to keep the TOOL0 pin at the low level from when the external resets end (except flash firmware processing time)
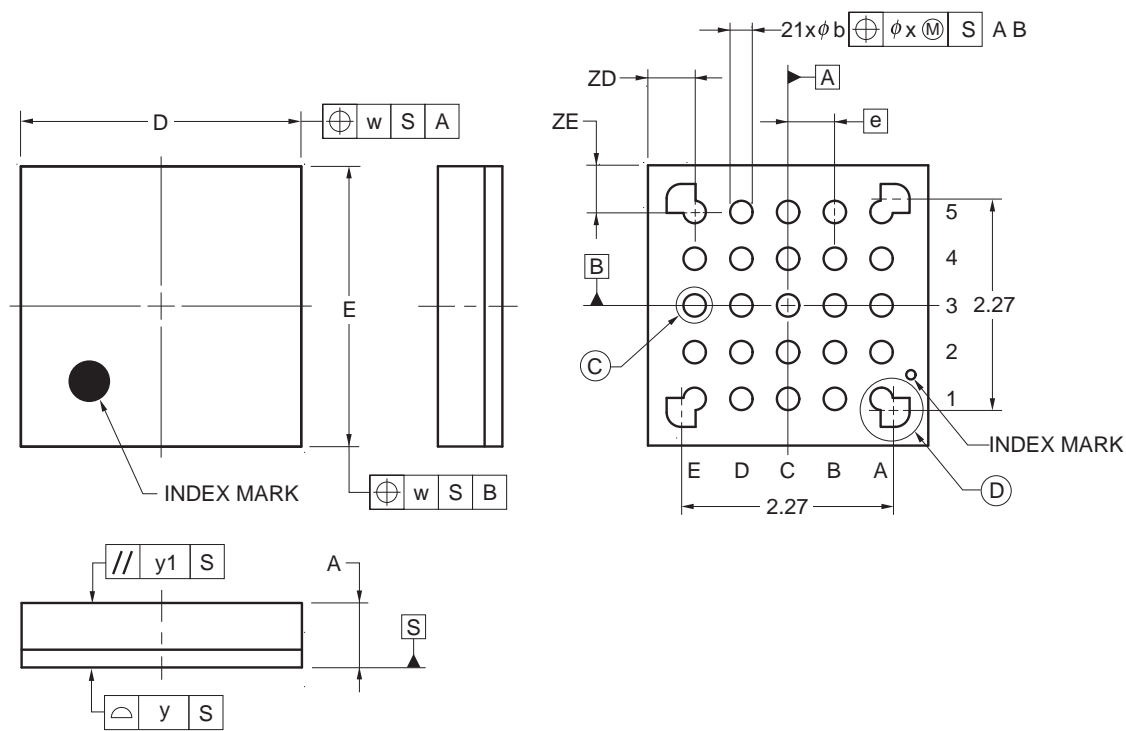
4. PACKAGE DRAWINGS

4.1 25-pin products

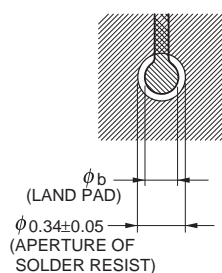R5F10E8AALA, R5F10E8CALA, R5F10E8DALA, R5F10E8EALA

<R>

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-WFLGA25-3x3-0.50	PWLG0025KA-A	P25FC-50-2N2-3	0.01

Unit: mm

DETAIL OF (C) PART

DETAIL OF (D) PART

φb
(LAND PAD)

φ0.34±0.05
(APERTURE OF
SOLDER RESIST)

R0.17±0.05   0.43±0.05
R0.12±0.05   0.33±0.05
0.50±0.05
0.365±0.05

0.365±0.05   R0.165±0.05
0.50±0.05
0.33±0.05   R0.215±0.05
0.43±0.05
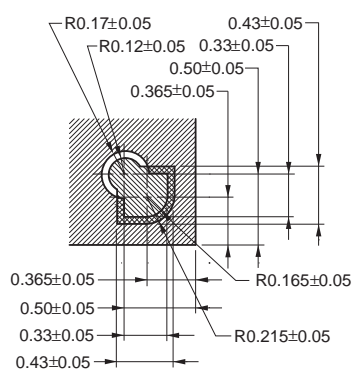
ITEM	DIMENSIONS
D	3.00±0.10
E	3.00±0.10
w	0.20
e	0.50
A	0.69±0.07
b	0.24±0.05
x	0.05
y	0.08
y1	0.20
ZD	0.50
ZE	0.50

R5F10EGAANA, R5F10EGCANA, R5F10EGDANA, R5F10EGEANA

R5F10EGAGNA, R5F10EGCGNA, R5F10EGDGNA, R5F10EGEGNA

<R>

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-HWQFN48-7x7-0.50	PWQN0048KB-A	48PJN-A P48K8-50-5B4-7	0.13

Unit: mm

DETAIL OF Ⓐ PART

INDEX AREA

EXPOSED DIE PAD

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	6.95	7.00	7.05
E	6.95	7.00	7.05
A	—	—	0.80
A₁	0.00	—	—
b	0.18	0.25	0.30
e	—	0.50	—
Lp	0.30	0.40	0.50
x	—	—	0.05
y	—	—	0.05
Z_D	—	0.75	—
Z_E	—	0.75	—
c₂	0.15	0.20	0.25
D₂	—	5.50	—
E₂	—	5.50	—

			Description
Rev.	**Date**	**Page**	**Summary**
0.01	Dec 26, 2011	-	First Edition issued
1.00	Sep 25, 2013	p.1	Modification of 1.1 Features
		p.4	Modification of Table 1-1. List of Ordering Part Numbers
		p.6	Modification of Remark 3 to 1.3.2 32-pin products.
		p.13	Modification of 1.5.2 32-pin products.
		p.14	Modification of 1.5.3 48-pin products.
		p.16	Modification of 1.6 Outline of Functions
		p.21	Modification of 2.2.1 X1, XT1 oscillator characteristics
		p.31, 32	Modification of Note 1 in 2.3.2 Supply current characteristics
		p.34, 35	Modification of Minimum Instruction Execution Time during Main System Clock Operation
		p.37	Modification of AC Timing Test Points in 2.5 Peripheral Functions Characteristics
		p.46 to 58	Modification of Caution to 2.5.1 Serial array unit.
		p.63 to 68	Modification of 2.6.1 A/D converter characteristics
		p.71	Modification of 2.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics
		p.71	Modification of 2.8 Flash Memory Programming Characteristics
		p.72	Modification of 2.10 Timing Specs for Switching Flash Memory Programming Modes
		p.73 to 117	Addition of 3 ELECTRICAL SPECIFICATIONS (G: INDUSTRIAL APPLICATIONS $T_A = -40$ to $+105°C$)
		p.118 to 123	Modification of 4. PACKAGE DRAWINGS
2.10	Nov 30, 2016	p.4	Modification of Table 1-1. List of Ordering Part Numbers
		p.5 to 10	Modification of the position of the index mark in 1.3.1 25-pin products to 1.3.4 64-pin products
		p.6	Modification of Remark 3
		p.13	Modification of 1.5.2 32-pin products
		p.14	Modification of 1.5.3 48-pin products
		p.16	Modification of description in 1.6 Outline of Functions
		p.21	Modification of 2.2.1 X1, XT1 oscillator characteristics
		p.31, 32	Modification of Note 1 in 2.3.2 Supply current characteristics
		p.34, 35	Modification of Minimum Instruction Execution Time during Main System Clock Operation
		p.36	Modification of AC Timing Test Points and TI/TO Timing
		p.38	Modification of AC Timing Test Points in 2.5 Peripheral Functions Characteristics
		p.48, 50 to 52, 55, 59	Modification of Caution in 2.5.1 Serial array unit
		p.64 to 69	Modification of conditions of 2.6.1 A/D converter characteristics
		p.72	Renamed to 2.7 RAM Data Retention Characteristics, and modification of note and figure
		p.72	Modification of 2.8 Flash Memory Programming Characteristics

NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.