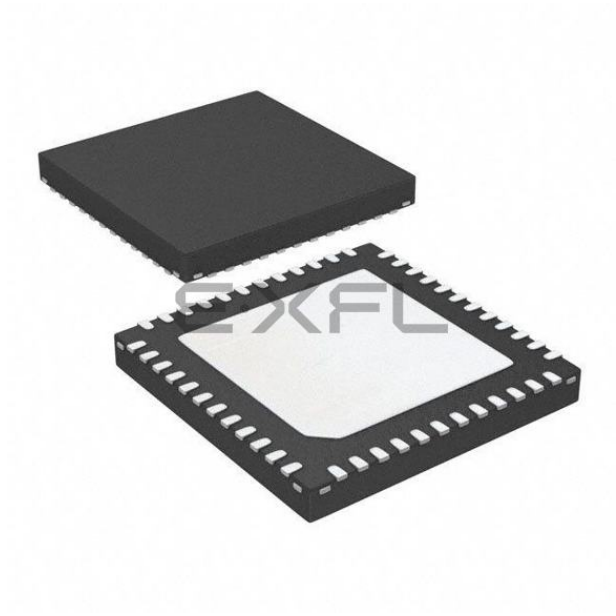


**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

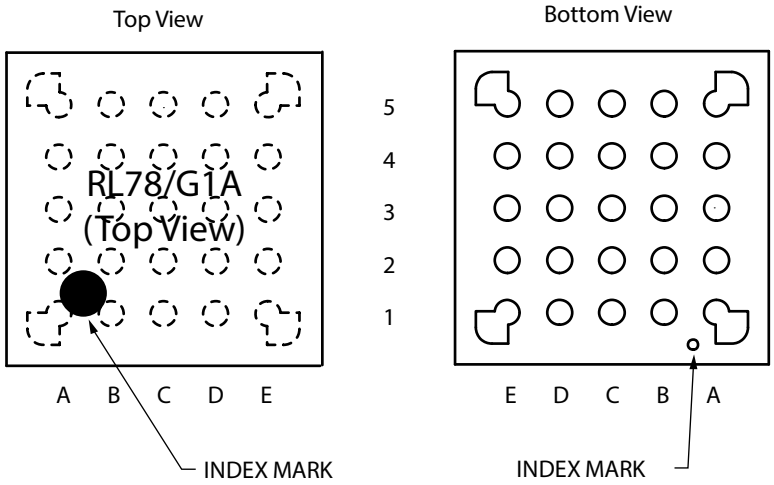
| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | RL78 |
| Core Size | 16-Bit |
| Speed | 32MHz |
| Connectivity | CSI, I²C, LINbus, UART/USART |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 32 |
| Program Memory Size | 48KB (48K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 3K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.6V ~ 3.6V |
| Data Converters | A/D 24x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-WFQFN Exposed Pad |
| Supplier Device Package | 48-HWQFN (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10egdana-u0 |

## 1.3 Pin Configuration (Top View)

### 1.3.1 25-pin products

- 25-pin plastic WFLGA (3 × 3 mm, 0.50 mm pitch)

<R>




| | A | B | C | D | E | |
|---|---|---|---|---|---|---|
| 5 | P40/TOOL0 | $\overline{\text{RESET}}$ | P03/ANI16/ RxD1/TO00/ (KR1) | P23/ANI3/ (KR3) | $AV_{SS}$ | 5 |
| 4 | P122/X2/ EXCLK | P137/INTP0 | P02/ANI17/ TxD1/TI00/ (KR0) | P22/ANI2/ (KR2) | $AV_{DD}$ | 4 |
| 3 | P121/X1 | $V_{DD}$ | P21/ANI1/ $AV_{REFM}$ | P11/ANI20/ SI00/SDA00/ RxD0/ TOOLRxD | P10/ANI18/ SCK00/SCL00 | 3 |
| 2 | REGC | $V_{SS}$ | P30/ANI27/ SCK11/SCL11/ INTP3 | P51/ANI25/ SO11/INTP2 | P50/ANI26/ SI11/SDA11 INTP1 | 2 |
| 1 | P60/SCLA0 | P61/SDAA0 | P31/ANI29/TI03/ TO03/PCLBUZ0 /INTP4 | P12/ANI21/ SO00/TxD0/ TOOLTxD | P20/ANI0/ $AV_{REFP}$ | 1 |
| | A | B | C | D | E | |

**Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).**

**Remarks 1.** For pin identification, see **1.4 Pin Identification**.

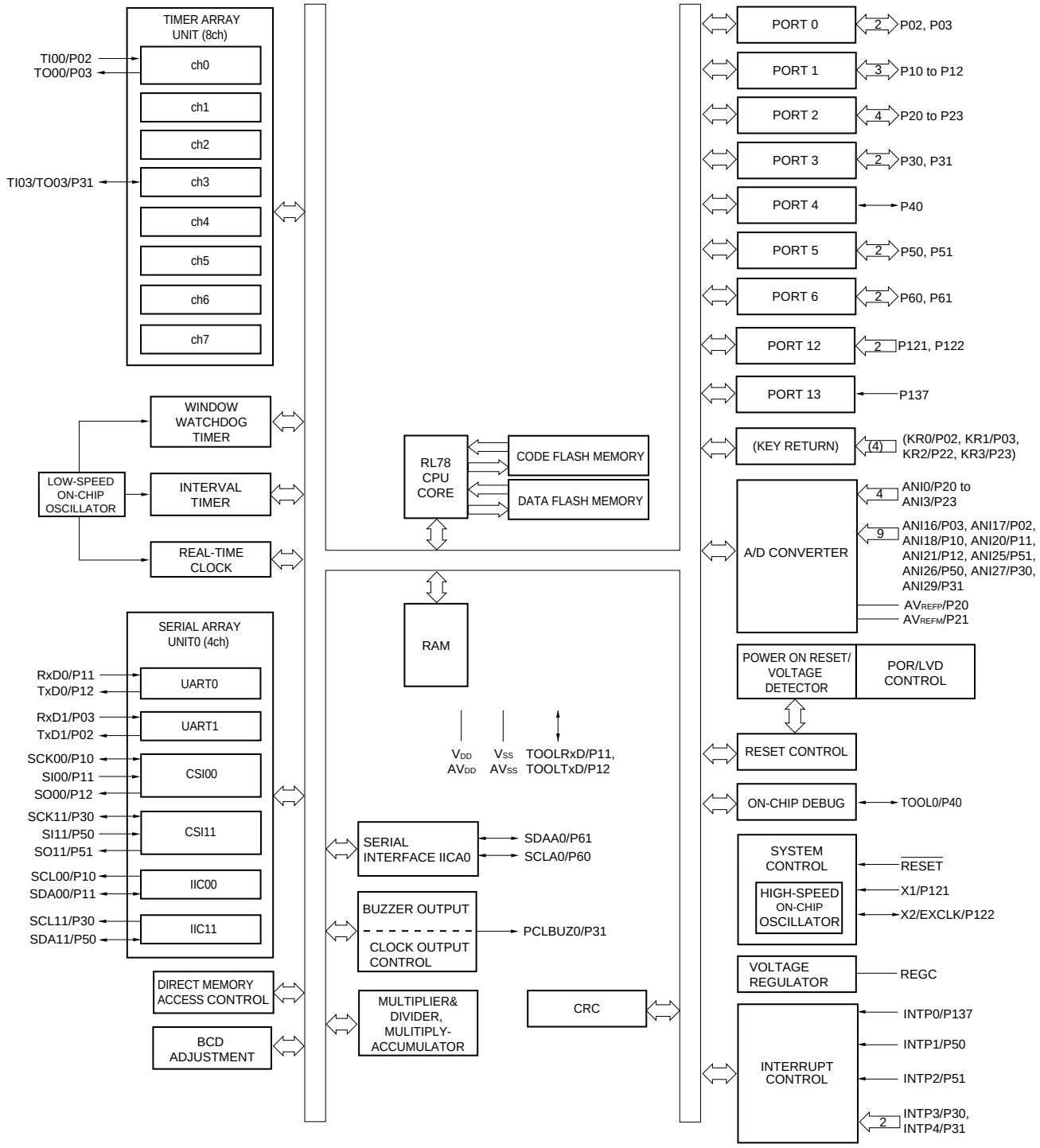
**2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

## 1.4 Pin Identification

| | | | |
|---|---|---|---|
| ANI0 to ANI12, ANI16 to ANI30: | Analog input | PCLBUZ0, PCLBUZ1: | Programmable clock output/buzzer output |
| $AV_{DD}$: | Analog power supply | REGC: | Regulator capacitance |
| $AV_{SS}$: | Analog ground | $\overline{RESET}$: | Reset |
| $AV_{REFM}$: | A/D converter reference potential (– side) input | RTC1HZ: | Real-time clock correction clock (1 Hz) output |
| $AV_{REFP}$: | A/D converter reference potential (+ side) input | RxD0 to RxD2: | Receive data |
| $EV_{DD0}$: | Power supply for port | SCK00, SCK01, SCK10, SCK11, SCK20, SCK21: | Serial clock input/output |
| $EV_{SS0}$: | Ground for port | SCLA0, SCL00, SCL01, SCL10, SCL11, SCL20, SCL21: | Serial clock output |
| EXCLK: | External clock input (main system clock) | SDAA0, SDA00, SDA01, SDA10, SDA11, SDA20, SDA21: | Serial data input/output |
| EXCLKS: | External clock input (subsystem clock) | SI00, SI01, SI10, SI11, SI20, SI21: | Serial data input |
| INTP0 to INTP11: | Interrupt Request from External | SO00, SO01, SO10, SO11, SO20, SO21: | Serial data output |
| KR0 to KR9: | Key return | TI00, TI01, TI03 to TI07: | Timer input |
| P00 to P06: | Port 0 | TO00, TO01, TO03 to TO07: | Timer output |
| P10 to P16: | Port 1 | TOOL0: | Data input/output for tool |
| P20 to P27: | Port 2 | TOOLRxD, TOOLTxD: | Data input/output for external device |
| P30, P31: | Port 3 | TxD0 to TxD2: | Transmit data |
| P40 to P43: | Port 4 | $V_{DD}$: | Power supply |
| P50, P51: | Port 5 | $V_{SS}$: | Ground |
| P60 to P63: | Port 6 | X1, X2: | Crystal oscillator (main system clock) |
| P70 to P77: | Port 7 | XT1, XT2: | Crystal oscillator (subsystem clock) |
| P120 to P124: | Port 12 | | |
| P130, P137: | Port 13 | | |
| P140, P141: | Port 14 | | |
| P150 to P154: | Port 15 | | |

## 1.5 Block Diagram

### 1.5.1 25-pin products




**Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

# 2. ELECTRICAL SPECIFICATIONS ($T_A$ = –40 to +85°C)

This chapter describes the following electrical specifications.

Target products A: Consumer applications $T_A$ = –40 to +85°C
R5F10E8AALA, R5F10E8CALA, R5F10E8DALA, R5F10E8EALA
R5F10EBAANA, R5F10EBCANA, R5F10EBDANA, R5F10EBEANA
R5F10EGAAFB, R5F10EGCAFB, R5F10EGDAFB, R5F10EGEAFB
R5F10EGAANA, R5F10EGCANA, R5F10EGDANA, R5F10EGEANA
R5F10ELCAFB, R5F10ELDAFB, R5F10ELEAFB
R5F10ELCABG, R5F10ELDABG, R5F10ELEABG

G: Industrial applications When $T_A$ = –40 to +105°C products is used in the range of $T_A$ = –40 to +85°C
R5F10EBAGNA, R5F10EBCGNA, R5F10EBDGNA, R5F10EBEGNA
R5F10EGAGFB, R5F10EGCGFB, R5F10EGDGFB, R5F10EGEGFB
R5F10EGAGNA, R5F10EGCGNA, R5F10EGDGNA, R5F10EGEGNA
R5F10ELCGFB, R5F10ELDGFB, R5F10ELEGFB

**Cautions 1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.**

**2. With products not provided with an $EV_{DD0}$ or $EV_{SS0}$ pin, replace $EV_{DD0}$ with $V_{DD}$, or replace $EV_{SS0}$ with $V_{SS}$.**

<R> **Notes 1.** Current flowing to $V_{DD}$.

**2.** When high-speed on-chip oscillator and high-speed system clock are stopped.

**3.** Current flowing only to the real-time clock (RTC) (excluding the operating current of the low-speed on-chip ocsillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either $I_{DD1}$ or $I_{DD2}$, and $I_{RTC}$, when the real-time clock operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, $I_{FIL}$ should be added. $I_{DD2}$ subsystem clock operation includes the operational current of the real-time clock.

**4.** Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip ocsillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either $I_{DD1}$ or $I_{DD2}$, and $I_{IT}$, when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, $I_{FIL}$ should be added.

**5.** Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontrollers is the sum of $I_{DD1}$, $I_{DD2}$, or $I_{DD3}$ and $I_{WDT}$ when the watchdog timer is in operation.

**6.** Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of $I_{DD1}$ or $I_{DD2}$ and $I_{ADC}$, $I_{AVREF}$, $I_{ADREF}$ when the A/D converter operates in an operation mode or the HALT mode.

**7.** Current flowing to the $AV_{DD}$.

**8.** Current flowing from the reference voltage source of A/D converter.

**9.** Operation current flowing to the internal reference voltage.

**10.** Current flowing to the $AV_{REFP}$.

**11.** Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of $I_{DD1}$, $I_{DD2}$ or $I_{DD3}$ and $I_{LVD}$ when the LVD circuit is in operation.

**12.** Current flowing only during data flash rewrite.

**13.** Current flowing only during self programming.

**Remarks 1.** $f_{IL}$: Low-speed on-chip oscillator clock frequency

**2.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

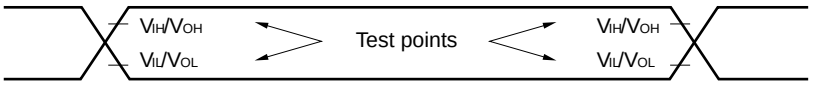
**3.** $f_{CLK}$: CPU/peripheral hardware clock frequency

**4.** Temperature condition of the TYP. value is $T_A$ = 25°C

## 2.5 Peripheral Functions Characteristics

**AC Timing Test Points**

<R>




### 2.5.1 Serial array unit

**(1) During communication at same potential (UART mode)**

**($T_A$ = –40 to +85°C, 1.6 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

| Parameter | Symbol | Conditions | HS[Note 1] | | LS[Note 2] | | LV[Note 3] | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Transfer rate[Note 4] | | 2.4 V ≤ $EV_{DD}$ ≤ 3.6 V | | $f_{MCK}$/6 | | $f_{MCK}$/6 | | $f_{MCK}$/6 | bps |
| | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$[Note 6] | | 5.3[Note 5] | | 1.3 | | 0.6 | Mbps |
| | | 1.8 V ≤ $EV_{DD}$ ≤ 3.6 V | | $f_{MCK}$/6 | | $f_{MCK}$/6 | | $f_{MCK}$/6 | bps |
| | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$[Note 6] | | 5.3[Note 5] | | 1.3 | | 0.6 | Mbps |
| | | 1.7 V ≤ $EV_{DD}$ ≤ 3.6 V | | $f_{MCK}$/6 | | $f_{MCK}$/6 | | $f_{MCK}$/6 | bps |
| | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$[Note 6] | | 5.3[Note 5] | | 1.3[Note 5] | | 0.6 | Mbps |
| | | 1.6 V ≤ $EV_{DD}$ ≤ 3.6 V | | – | | $f_{MCK}$/6 | | $f_{MCK}$/6 | bps |
| | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$[Note 6] | | – | | 1.3[Note 5] | | 0.6 | Mbps |

**Notes 1.** HS is condition of HS (high-speed main) mode.

**2.** LS is condition of LS (low-speed main) mode.

**3.** LV is condition of LV (low-voltage main) mode.

**4.** Transfer rate in the SNOOZE mode is 4800 bps.

**5.** The following conditions are required for low-voltage interface when $EV_{DD0}$ < $V_{DD}$.
2.4 V ≤ $EV_{DD0}$ < 2.7 V : MAX. 2.6 Mbps
1.8 V ≤ $EV_{DD0}$ < 2.4 V : MAX. 1.3 Mbps
1.6 V ≤ $EV_{DD0}$ < 1.8 V : MAX. 0.6 Mbps

**6.** $f_{CLK}$ in each operating mode is as below.
HS (high-speed main) mode: $f_{CLK}$ = 32 MHz
LS (low-speed main) mode: $f_{CLK}$ = 8 MHz
LV (low-voltage main) mode: $f_{CLK}$ = 4 MHz

**Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)**

**($T_A$ = –40 to +85°C, 2.7 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS[Note 1] | | LS[Note 2] | | LV[Note 3] | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time | $t_{KCY1}$ | 2.7 V ≤ $EV_{DD}$ ≤ 3.6 V | $t_{KCY1}$ ≥ 2/$f_{CLK}$ | 83.3 | | 250 | | 500 | | ns |
| SCKp high-/low-level width | $t_{KH1}$, $t_{KL1}$ | 2.7 V ≤ $EV_{DD}$ ≤ 3.6 V | | $t_{KCY1}$/2 –10 | | $t_{KCY1}$/2 –50 | | $t_{KCY1}$/2 –50 | | ns |
| SIp setup time (to SCKp↑)[Note 4] | $t_{SIK1}$ | 2.7 V ≤ $EV_{DD}$ ≤ 3.6 V | | 33 | | 110 | | 110 | | ns |
| SIp hold time (from SCKp↑)[Note 4] | $t_{KSI1}$ | 2.7 V ≤ $EV_{DD}$ ≤ 3.6 V | | 10 | | 10 | | 10 | | ns |
| Delay time from SCKp↓ to SOp output[Note 5] | $t_{KSO1}$ | C = 20 pF[Note 6] | | | 10 | | 10 | | 10 | ns |

**Notes 1.** HS is condition of HS (high-speed main) mode.

**2.** LS is condition of LS (low-speed main) mode.

**3.** LV is condition of LV (low-voltage main) mode.

**4.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time or SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**5.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

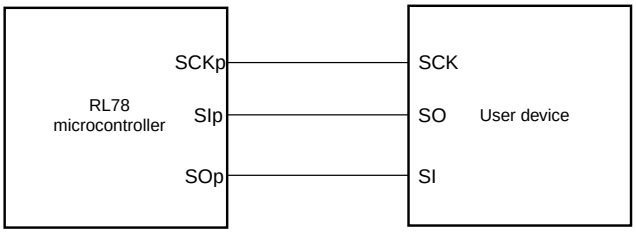
**6.** C is the load capacitance of the SCKp and SOp output lines.

**Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

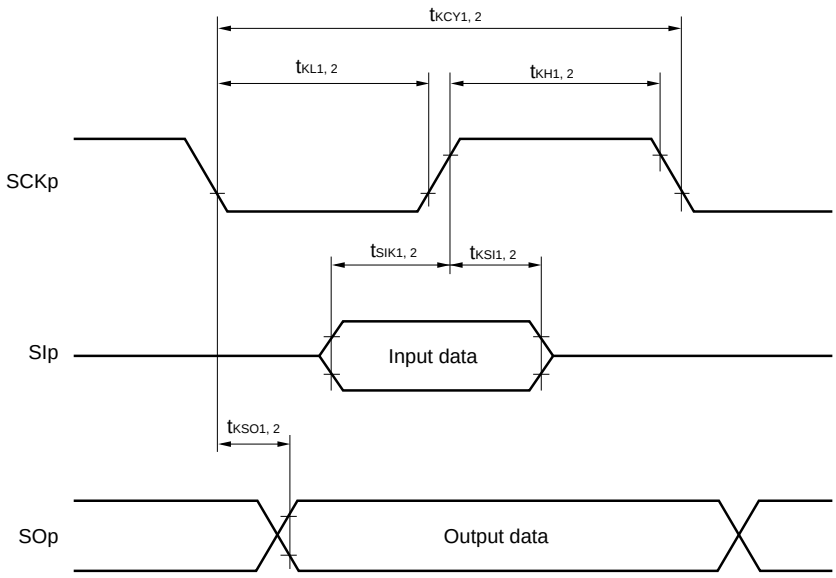
**Remarks 1.** p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM numbers (g = 1)

**2.** $f_{MCK}$: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

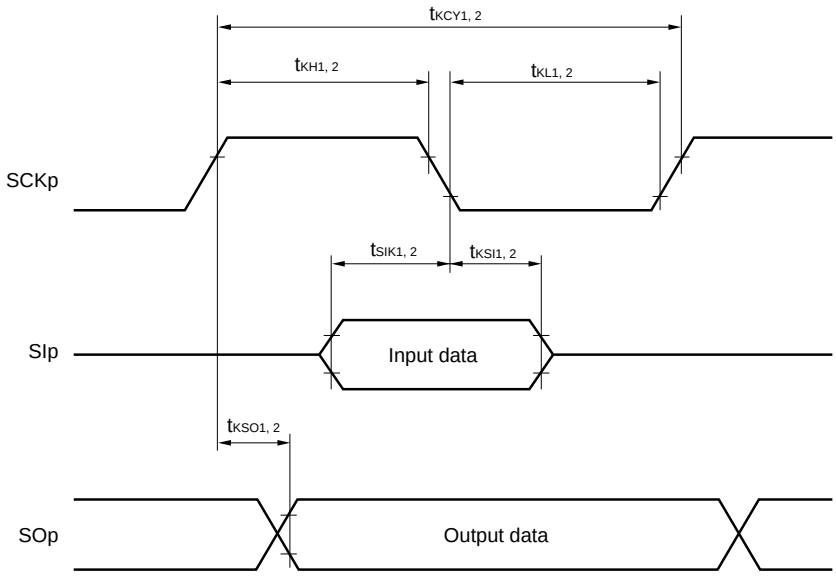
**CSI mode connection diagram (during communication at same potential)**




**CSI mode serial transfer timing (during communication at same potential)**
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**




**CSI mode serial transfer timing (during communication at same potential)**
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**




**Remarks 1.** p: CSI number (p = 00, 01, 10, 11, 20, 21)

**2.** m: Unit number, n: Channel number (mn = 00 to 03, 10, 11)

### (5) During communication at same potential (simplified I²C mode) (1/2)

**($T_A$ = –40 to +85°C, 1.6 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

| Parameter | Symbol | Conditions | HS[Note 1] | | LS[Note 2] | | LV[Note 3] | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCLr clock frequency | $f_{SCL}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | | 1000[Note 4] | | 400[Note 4] | | 400[Note 4] | kHz |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 3.6 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | | 400[Note 4] | | 400[Note 4] | | 400[Note 4] | kHz |
| | | 1.8 V ≤ $EV_{DD0}$ < 2.7 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | | 300[Note 4] | | 300[Note 4] | | 300[Note 4] | kHz |
| | | 1.7 V ≤ $EV_{DD0}$ < 1.8 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | | 250[Note 4] | | 250[Note 4] | | 250[Note 4] | kHz |
| | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | | – | | 250[Note 4] | | 250[Note 4] | kHz |
| Hold time when SCLr = “L” | $t_{LOW}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 475 | | 1150 | | 1150 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 3.6 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | 1150 | | 1150 | | 1150 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 2.7 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | 1550 | | 1550 | | 1550 | | ns |
| | | 1.7 V ≤ $EV_{DD0}$ < 1.8 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | 1850 | | 1850 | | 1850 | | ns |
| | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | – | | 1850 | | 1850 | | ns |
| Hold time when SCLr = “H” | $t_{HIGH}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 475 | | 1150 | | 1150 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 3.6 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | 1150 | | 1150 | | 1150 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 2.7 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | 1550 | | 1550 | | 1550 | | ns |
| | | 1.7 V ≤ $EV_{DD0}$ < 1.8 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | 1850 | | 1850 | | 1850 | | ns |
| | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | – | | 1850 | | 1850 | | ns |
| Data setup time (reception) | $t_{SU:DAT}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 1/$f_{MCK}$ + 85[Note 5] | | 1/$f_{MCK}$ + 145[Note 5] | | 1/$f_{MCK}$ + 145[Note 5] | | ns |
| | | 1.8 V ≤ $EV_{DD}$ ≤ 3.6 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | 1/$f_{MCK}$ + 145[Note 5] | | 1/$f_{MCK}$ + 145[Note 5] | | 1/$f_{MCK}$ + 145[Note 5] | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 2.7 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | 1/$f_{MCK}$+ 230[Note 5] | | 1/$f_{MCK}$+ 230[Note 5] | | 1/$f_{MCK}$+ 230[Note 5] | | ns |
| | | 1.7 V ≤ $EV_{DD}$ < 1.8 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | 1/$f_{MCK}$ + 290[Note 5] | | 1/$f_{MCK}$ + 290[Note 5] | | 1/$f_{MCK}$ + 290[Note 5] | | ns |
| | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | – | | 1/$f_{MCK}$ + 290[Note 5] | | 1/$f_{MCK}$ + 290[Note 5] | | ns |

(**Notes**, **Caution** and **Remarks** are listed on the next page.)

**(6) Communication at different potential (1.8 V, 2.5 V) (UART mode) (dedicated baud rate generator output) (1/2)**

**($T_A$ = –40 to +85°C, 1.8 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

| Parameter | Symbol | Conditions | | | HS[Note 1] | | LS[Note 2] | | LV[Note 3] | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Transfer rate[Note 4] | | Reception | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | | $f_{MCK}$/6 | | $f_{MCK}$/6 | | $f_{MCK}$/6 | bps |
| | | | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$[Note 7] | | 5.3 | | 1.3 | | 0.6 | Mbps |
| | | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V[Note 5] | | | $f_{MCK}$/6 | | $f_{MCK}$/6 | | $f_{MCK}$/6 | bps |
| | | | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$[Note 7] | | 5.3 [Note 6] | | 1.3 | | 0.6 | Mbps |

**Notes 1.** HS is condition of HS (high-speed main) mode.

**2.** LS is condition of LS (low-speed main) mode.

**3.** LV is condition of LV (low-voltage main) mode.

**4.** Transfer rate in the SNOOZE mode is 4800 bps.

**5.** Use it with $EV_{DD0} \geq V_b$.

**6.** The following conditions are required for low-voltage interface when $EV_{DD0} < V_{DD}$.

2.4 V ≤ $EV_{DD0}$ < 2.7 V : MAX. 2.6 Mbps

1.8 V ≤ $EV_{DD0}$ < 2.4 V : MAX. 1.3 Mbps

**7.** $f_{CLK}$ in each operating mode is as below.

HS (high-speed main) mode: $f_{CLK}$ = 32 MHz

LS (low-speed main) mode: $f_{CLK}$ = 8 MHz

LV (low-voltage main) mode: $f_{CLK}$ = 4 MHz

**Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output ($V_{DD}$ tolerance (When 25- to 48-pin products)/$EV_{DD}$ tolerance (When 64-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**Remarks 1.** $V_b$[V]: Communication line voltage

**2.** q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1)

**3.** $f_{MCK}$: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10, 11)

**(9) Communication at different potential (1.8 V, 2.5 V) (CSI mode) (slave mode, SCKp... external clock input)**
**($T_A$ = –40 to +85°C, 1.8 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS[Note 1] | | LS[Note 2] | | LV[Note 3] | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time[Note 4] | $t_{KCY2}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | 24 MHz < $f_{MCK}$ | 20/$f_{MCK}$ | | – | | – | | ns |
| | | | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 16/$f_{MCK}$ | | – | | – | | ns |
| | | | 16 MHz < $f_{MCK}$ ≤ 20 MHz | 14/$f_{MCK}$ | | – | | – | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 16 MHz | 12/$f_{MCK}$ | | – | | – | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 8/$f_{MCK}$ | | 16/$f_{MCK}$ | | – | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 6/$f_{MCK}$ | | 10/$f_{MCK}$ | | 10/$f_{MCK}$ | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V[Note 5] | 24 MHz < $f_{MCK}$ | 48/$f_{MCK}$ | | – | | – | | ns |
| | | | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 36/$f_{MCK}$ | | – | | – | | ns |
| | | | 16 MHz < $f_{MCK}$ ≤ 20 MHz | 32/$f_{MCK}$ | | – | | – | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 16 MHz | 26/$f_{MCK}$ | | – | | – | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 16/$f_{MCK}$ | | 16/$f_{MCK}$ | | – | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 10/$f_{MCK}$ | | 10/$f_{MCK}$ | | 10/$f_{MCK}$ | | ns |
| SCKp high-/low-level width | $t_{KH2}$, $t_{KL2}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | $t_{KCY2}$/2 – 18 | | $t_{KCY2}$/2 – 50 | | $t_{KCY2}$/2 – 50 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V[Note 5] | | $t_{KCY2}$/2 – 50 | | $t_{KCY2}$/2 – 50 | | $t_{KCY2}$/2 – 50 | | ns |
| SIp setup time (to SCKp↑)[Note 6] | $t_{SIK2}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | 1/$f_{MCK}$ + 20 | | 1/$f_{MCK}$ + 30 | | 1/$f_{MCK}$ + 30 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V[Note 5] | | 1/$f_{MCK}$ + 30 | | 1/$f_{MCK}$ + 30 | | 1/$f_{MCK}$ + 30 | | ns |
| SIp hold time (from SCKp↑)[Note 6] | $t_{KSI2}$ | | | 1/$f_{MCK}$ + 31 | | 1/$f_{MCK}$ + 31 | | 1/$f_{MCK}$ + 31 | | ns |
| Delay time from SCKp↓ to SOp output[Note 7] | $t_{KSO2}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | | 2/$f_{MCK}$ + 214 | | 2/$f_{MCK}$ + 573 | | 2/$f_{MCK}$ + 573 | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V[Note 5], $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | | 2/$f_{MCK}$ + 573 | | 2/$f_{MCK}$ + 573 | | 2/$f_{MCK}$ + 573 | ns |

**Notes 1.** HS is condition of HS (high-speed main) mode.
**2.** LS is condition of LS (low-speed main) mode.
**3.** LV is condition of LV (low-voltage main) mode.
**4.** Transfer rate in the SNOOZE mode : MAX. 1 Mbps
**5.** Use it with $EV_{DD0}$ ≥ $V_b$.
**6.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time or SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
**7.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Caution Select the TTL input buffer for the SIp pin and SCKp pin and the N-ch open drain output ($V_{DD}$ tolerance (When 25- to 48-pin products)/$EV_{DD}$ tolerance (When 64-pin products)) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

<R>

(**Remarks** are listed on the next page.)

### 2.5.2 Serial interface IICA

#### (1) $I^2C$ standard mode

**($T_A$ = –40 to +85°C, 1.6 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

| Parameter | Symbol | Conditions | Standard Mode[Note 1] | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | HS[Note 2] | | LS[Note 3] | | LV[Note 4] | | |
| | | | MIN. | MAX. | MIN. | MIN. | MAX. | MIN. | |
| SCLA0 clock frequency | $f_{SCL}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V | 0 | 100 | 0 | 100 | 0 | 100 | kHz |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 3.6 V | 0 | 100 | 0 | 100 | 0 | 100 | |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 3.6 V | 0 | 100 | 0 | 100 | 0 | 100 | |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 3.6 V | – | | 0 | 100 | 0 | 100 | |
| Setup time of restart condition | $t_{SU:STA}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V | 4.7 | | 4.7 | | 4.7 | | μs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 3.6 V | 4.7 | | 4.7 | | 4.7 | | |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 3.6 V | 4.7 | | 4.7 | | 4.7 | | |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 3.6 V | – | | 4.7 | | 4.7 | | |
| Hold time[Note 5] | $t_{HD:STA}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V | 4.0 | | 4.0 | | 4.0 | | μs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 3.6 V | 4.0 | | 4.0 | | 4.0 | | |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 3.6 V | 4.0 | | 4.0 | | 4.0 | | |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 3.6 V | – | | 4.0 | | 4.0 | | |
| Hold time when SCLA0 = “L” | $t_{LOW}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V | 4.7 | | 4.7 | | 4.7 | | μs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 3.6 V | 4.7 | | 4.7 | | 4.7 | | |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 3.6 V | 4.7 | | 4.7 | | 4.7 | | |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 3.6 V | – | | 4.7 | | 4.7 | | |
| Hold time when SCLA0 = “H” | $t_{HIGH}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V | 4.0 | | 4.0 | | 4.0 | | μs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 3.6 V | 4.0 | | 4.0 | | 4.0 | | |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 3.6 V | 4.0 | | 4.0 | | 4.0 | | |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 3.6 V | – | | 4.0 | | 4.0 | | |
| Data setup time (reception) | $t_{SU:DAT}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V | 250 | | 250 | | 250 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 3.6 V | 250 | | 250 | | 250 | | |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 3.6 V | 250 | | 250 | | 250 | | |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 3.6 V | – | | 250 | | 250 | | |
| Data hold time (transmission)[Note 6] | $t_{HD:DAT}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V | 0 | 3.45 | 0 | 3.45 | 0 | 3.45 | μs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 3.6 V | 0 | 3.45 | 0 | 3.45 | 0 | 3.45 | |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 3.6 V | 0 | 3.45 | 0 | 3.45 | 0 | 3.45 | |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 3.6 V | – | – | 0 | 3.45 | 0 | 3.45 | |
| Setup time of stop condition | $t_{SU:STO}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V | 4.0 | | 4.0 | | 4.0 | | μs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 3.6 V | 4.0 | | 4.0 | | 4.0 | | |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 3.6 V | 4.0 | | 4.0 | | 4.0 | | |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 3.6 V | – | | 4.0 | | 4.0 | | |
| Bus-free time | $t_{BUF}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V | 4.7 | | 4.7 | | 4.7 | | μs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 3.6 V | 4.7 | | 4.7 | | 4.7 | | |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 3.6 V | 4.7 | | 4.7 | | 4.7 | | |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 3.6 V | – | | 4.7 | | 4.7 | | |

(**Note** and **Remark** are listed on the next page.)

## 2.9 Dedicated Flash Memory Programmer Communication (UART)

**($T_A$ = –40 to +85°C, 1.8 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

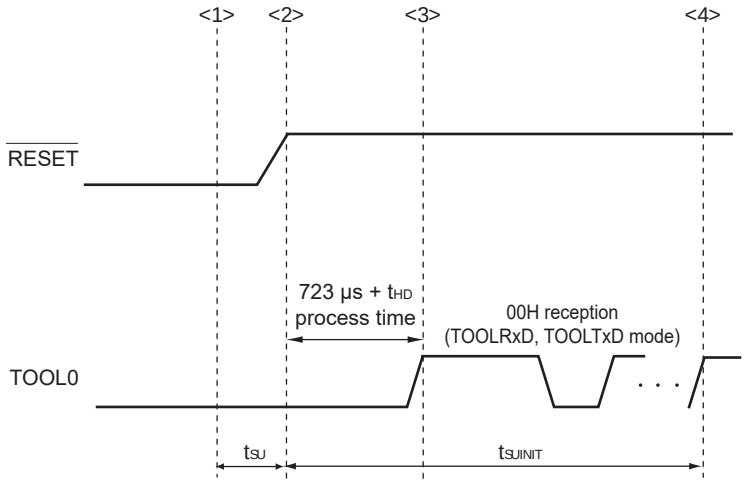
| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Transfer rate | | During flash memory programming | 115.2 k | | 1 M | bps |

## 2.10 Timing Specs for Switching Flash Memory Programming Modes

**($T_A$ = –40 to +85°C, 1.8 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| How long from when an external reset ends until the initial communication settings are specified | $t_{SUINIT}$ | POR and LVD reset must end before the external reset ends. | | | 100 | ms |
| How long from when the TOOL0 pin is placed at the low level until a external reset ends | $t_{SU}$ | POR and LVD reset must end before the external reset ends. | 10 | | | μs |
| <R> How long the TOOL0 pin must be kept at the low level after an external reset ends (except flash firmware processing time) | $t_{HD}$ | POR and LVD reset must end before the external reset ends. | 1 | | | ms |

<R>




<1> The low level is input to the TOOL0 pin.
<2> The pins reset ends (POR and LVD reset must end before the external reset ends.).
<3> The TOOL0 pin is set to the high level.
<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

**Remark** $t_{SUINIT}$: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the resets end.

$t_{SU}$: How long from when the TOOL0 pin is placed at the low level until a external reset ends

<R> $t_{HD}$: How long to keep the TOOL0 pin at the low level from when the external resets end (except flash firmware processing time)

**($T_A$ = –40 to +105°C, 2.4 V ≤ $AV_{DD}$ ≤ $V_{DD}$ ≤ 3.6 V, 2.4 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)** **(5/5)**

| Items | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Input leakage current, high | $I_{LIH1}$ | P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P60 to P63, P70 to P77, P120, P140, P141 | $V_I$ = $EV_{DD0}$ | | | | 1 | μA |
| | $I_{LIH2}$ | P137, $\overline{\text{RESET}}$ | $V_I$ = $V_{DD}$ | | | | 1 | μA |
| | $I_{LIH3}$ | P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS) | $V_I$ = $V_{DD}$ | In input port or external clock input | | | 1 | μA |
| | | | | In resonator connection | | | 10 | μA |
| | $I_{LIH4}$ | P20 to P27, P150 to P154 | $V_I$ = $AV_{DD}$ | | | | 1 | μA |
| Input leakage current, low | $I_{LIL1}$ | P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P60 to P67, P70 to P77, P120, P140, P141 | $V_I$ = $EV_{SS0}$ | | | | –1 | μA |
| | $I_{LIL2}$ | P137, $\overline{\text{RESET}}$ | $V_I$ = $V_{SS}$ | | | | –1 | μA |
| | $I_{LIL3}$ | P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS) | $V_I$ = $V_{SS}$ | In input port or external clock input | | | –1 | μA |
| | | | | In resonator connection | | | –10 | μA |
| | $I_{LIL4}$ | P20 to P27, P150 to P154 | $V_I$ = $AV_{SS}$ | | | | –1 | μA |
| On-chip pull-up resistance | $R_U$ | P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P140, P141 | $V_I$ = $EV_{SS0}$, In input port | | 10 | 20 | 100 | kΩ |

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)** **(2/3)**

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply current[Note 1] | $I_{DD2}$[Note 2] | HALT mode | HS (high-speed main) mode[Note 7] | $f_{IH}$ = 32 MHz[Note 4] | $V_{DD}$ = 3.0 V | | 0.54 | 2.90 | mA |
| | | | | $f_{IH}$ = 24 MHz[Note 4] | $V_{DD}$ = 3.0 V | | 0.44 | 2.30 | mA |
| | | | | $f_{IH}$ = 16 MHz[Note 4] | $V_{DD}$ = 3.0 V | | 0.40 | 1.70 | mA |
| | | | HS (high-speed main) mode[Note 7] | $f_{MX}$ = 20 MHz[Note 3], $V_{DD}$ = 3.0 V | Square wave input | | 0.28 | 1.90 | mA |
| | | | | | Resonator connection | | 0.45 | 2.00 | |
| | | | | $f_{MX}$ = 10 MHz[Note 3], $V_{DD}$ = 3.0 V | Square wave input | | 0.19 | 1.02 | mA |
| | | | | | Resonator connection | | 0.26 | 1.10 | |
| | | | Subsystem clock mode | $f_{SUB}$ = 32.768 kHz[Note 5] $T_A$ = –40°C | Square wave input | | 0.25 | 0.57 | μA |
| | | | | | Resonator connection | | 0.44 | 0.76 | |
| | | | | $f_{SUB}$ = 32.768 kHz[Note 5] $T_A$ = +25°C | Square wave input | | 0.30 | 0.57 | μA |
| | | | | | Resonator connection | | 0.49 | 0.76 | |
| | | | | $f_{SUB}$ = 32.768 kHz[Note 5] $T_A$ = +50°C | Square wave input | | 0.38 | 1.17 | μA |
| | | | | | Resonator connection | | 0.57 | 1.36 | |
| | | | | $f_{SUB}$ = 32.768 kHz[Note 5] $T_A$ = +70°C | Square wave input | | 0.52 | 1.97 | μA |
| | | | | | Resonator connection | | 0.71 | 2.16 | |
| | | | | $f_{SUB}$ = 32.768 kHz[Note 5] $T_A$ = +85°C | Square wave input | | 0.97 | 3.37 | μA |
| | | | | | Resonator connection | | 1.16 | 3.56 | |
| | | | | $f_{SUB}$ = 32.768 kHz[Note 5] $T_A$ = +105°C | Square wave input | | 3.01 | 15.37 | μA |
| | | | | | Resonator connection | | 3.20 | 15.56 | |
| | $I_{DD3}$[Note 6] | STOP mode[Note 8] | $T_A$ = –40°C | | | | 0.16 | 0.50 | μA |
| | | | $T_A$ = +25°C | | | | 0.23 | 0.50 | |
| | | | $T_A$ = +50°C | | | | 0.34 | 1.10 | |
| | | | $T_A$ = +70°C | | | | 0.46 | 1.90 | |
| | | | $T_A$ = +85°C | | | | 0.75 | 3.30 | |
| | | | $T_A$ = +105°C | | | | 2.94 | 15.30 | |

(**Notes** and **Remarks** are listed on the next page.)

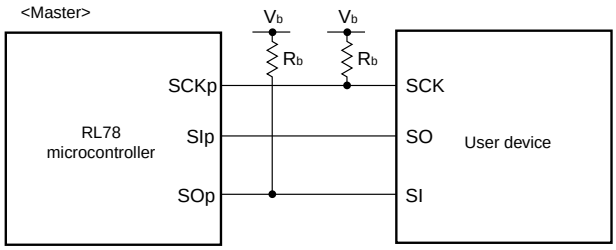
**(6) Communication at different potential (1.8 V, 2.5 V) (CSI mode) (master mode, SCKp... internal clock output) (2/2)**
**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| SIp setup time (to SCKp↑)Note 1 | $t_{SIK1}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 354 | | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 958 | | | ns |
| SIp hold time (from SCKp↑)Note 1 | $t_{KSI1}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 38 | | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 38 | | | ns |
| Delay time from SCKp↓ to SOp outputNote 1 | $t_{KSO1}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | | 390 | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | | 966 | ns |
| SIp setup time (to SCKp↓)Note 2 | $t_{SIK1}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 88 | | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 220 | | | ns |
| SIp hold time (from SCKp↓)Note 2 | $t_{KSI1}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 38 | | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 38 | | | ns |
| Delay time from SCKp↑ to SOp outputNote 2 | $t_{KSO1}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | | 50 | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | | 50 | ns |

**Notes 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
**2.** When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

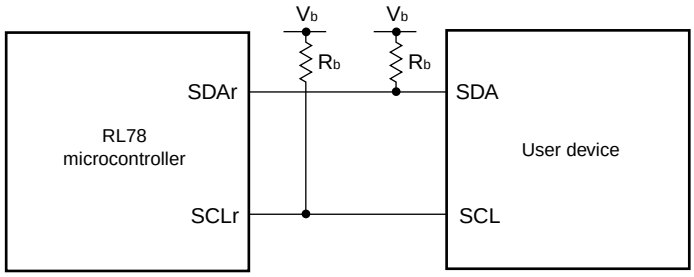
**Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance (When 25- to 48-pin products)/$EV_{DD}$ tolerance (When 64-pin products)) mode for the SOp pin and SCKp** <R> **pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**CSI mode connection diagram (during communication at different potential)**

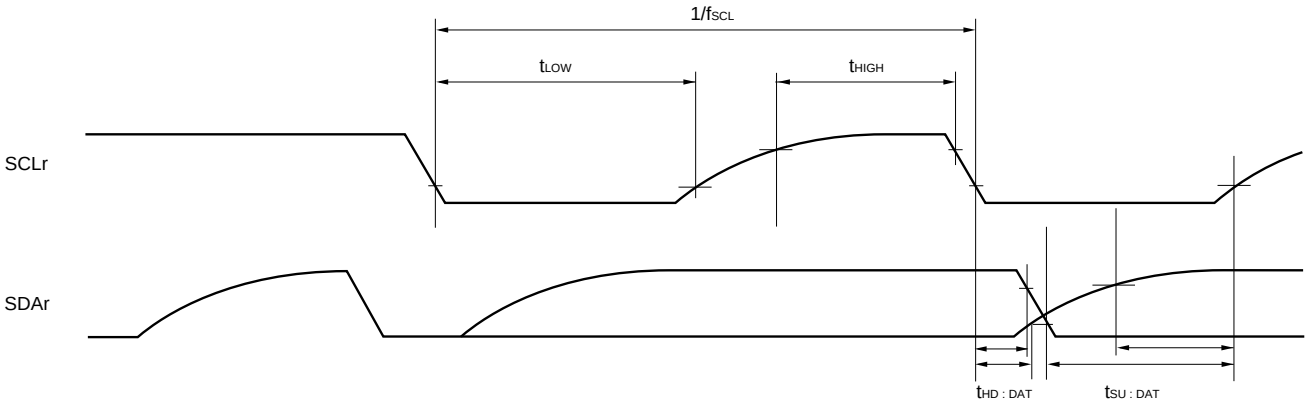



**Remarks 1.** $R_b$[Ω]: Communication line (SCKp, SOp) pull-up resistance, $C_b$[F]: Communication line (SCKp, SOp) load capacitance, $V_b$[V]: Communication line voltage
**2.** p: CSI number (p = 00, 10, 20), m: Unit number , n: Channel number (mn = 00, 02, 10), g: PIM and POM number (g = 0, 1)
**3.** CSI01, CSI11, and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

**Simplified $I^2C$ mode connection diagram (during communication at different potential)**




**Simplified $I^2C$ mode serial transfer timing (during communication at different potential)**




**Remarks 1.** $R_b$[Ω]: Communication line (SDAr, SCLr) pull-up resistance, $C_b$[F]: Communication line (SDAr, SCLr) load capacitance, $V_b$[V]: Communication line voltage

**2.** r: IIC number (r = 00, 10, 20), g: PIM, POM number (g = 0, 1)

**3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 02, 10)

**4.** IIC01, IIC11, and IIC21 cannot communicate at different potential. Use IIC00, IIC10, or IIC20 for communication at different potential.

<R> **(5) When reference voltage (+) = Internal reference voltage (1.45 V) (ADREFP1 = 1, ADREFP0 = 0), reference voltage (–) = $AV_{SS}$ (ADREFM = 0), target for conversion: ANI0 to ANI12, ANI16 to ANI30**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 3.6 V, 2.4 V ≤ $EV_{DD}$ ≤ $V_{DD}$, 2.4 V ≤ $AV_{DD}$ ≤ $V_{DD}$, $V_{SS}$ = $EV_{SS0}$ = 0 V, $AV_{SS}$ = 0 V, Reference voltage (+) = Internal reference voltage, Reference voltage (–) = $AV_{SS}$ = 0 V, HS (high-speed main) mode)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Resolution | $R_{ES}$ | | | 8 | | bit |
| Conversion time | $t_{CONV}$ | 8-bit resolution | 16.0 | | | μs |
| Zero-scale error[Note] | $E_{ZS}$ | 8-bit resolution | | | ±4.0 | LSB |
| Integral linearity error[Note] | ILE | 8-bit resolution | | | ±2.0 | LSB |
| Differential linearity error[Note] | DLE | 8-bit resolution | | | ±2.5 | LSB |
| Reference voltage (+) | $AV_{REF(+)}$ | = Internal reference voltage ($V_{BGR}$) | 1.38 | 1.45 | 1.50 | V |
| Analog input voltage | $V_{AIN}$ | | 0 | | $V_{BGR}$ | V |

**Note** Excludes quantization error (±1/2 LSB).

## 3.6.2 Temperature sensor, internal reference voltage output characteristics

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V, HS (high-speed main) mode)**

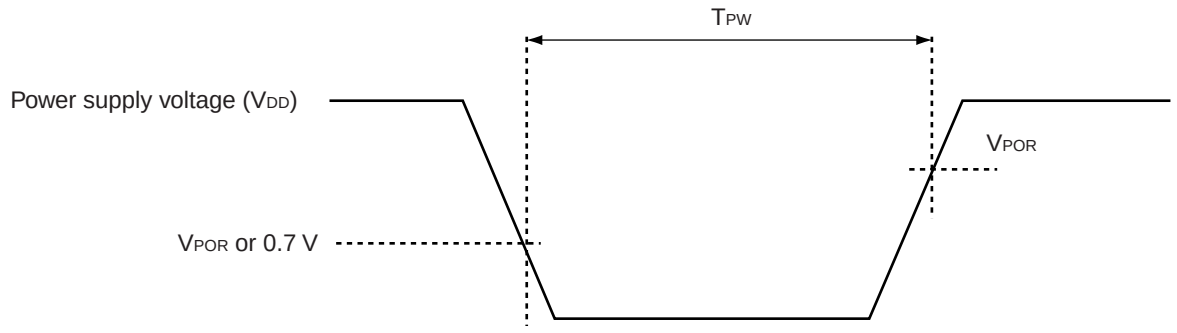
| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Temperature sensor output voltage | $V_{TMPS25}$ | Setting ADS register = 80H, $T_A$ = +25°C | | 1.05 | | V |
| Internal reference voltage | $V_{BGR}$ | Setting ADS register = 81H | 1.38 | 1.45 | 1.5 | V |
| Temperature coefficient | $F_{VTMPS}$ | Temperature sensor output voltage that depends on the temperature | | –3.6 | | mV/°C |
| Operation stabilization wait time | $t_{AMP}$ | | 10 | | | μs |

## 3.6.3 POR circuit characteristics

**($T_A$ = –40 to +105°C, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Detection voltage | $V_{POR}$ | Power supply rise time | 1.45 | 1.51 | 1.57 | V |
| | $V_{PDR}$ | Power supply fall time | 1.44 | 1.50 | 1.56 | V |
| Minimum pulse width[Note] | $T_{PW}$ | | 300 | | | μs |

**Note** This is the time required for the POR circuit to execute a reset when $V_{DD}$ falls below $V_{PDR}$. When the microcontroller enters STOP mode or if the main system clock ($f_{MAIN}$) has been stopped by setting bit 0 (HIOSTOP) and bit 7 (MSTOP) of the clock operation status control register (CSC), this is the time required for the POR circuit to execute a reset before $V_{DD}$ rises to $V_{POR}$ after having fallen below 0.7 V.



## 3.9 Dedicated Flash Memory Programmer Communication (UART)

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

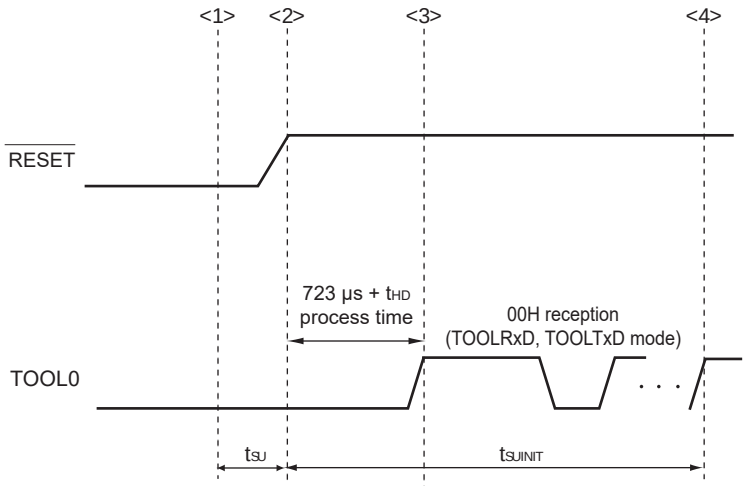
| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Transfer rate | | During flash memory programming | 115.2 k | | 1 M | bps |

## 3.10 Timing Specs for Switching Flash Memory Programming Modes

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| How long from when an external reset ends until the initial communication settings are specified | $t_{SUINIT}$ | POR and LVD reset must end before the external reset ends. | | | 100 | ms |
| How long from when the TOOL0 pin is placed at the low level until a external reset ends | $t_{SU}$ | POR and LVD reset must end before the external reset ends. | 10 | | | μs |
| <R> How long the TOOL0 pin must be kept at the low level after an external reset ends (except flash firmware processing time) | $t_{HD}$ | POR and LVD reset must end before the external reset ends. | 1 | | | ms |

<R>




<1> The low level is input to the TOOL0 pin.
<2> The pins reset ends (POR and LVD reset must end before the external reset ends.).
<3> The TOOL0 pin is set to the high level.
<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

**Remark** $t_{SUINIT}$: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the resets end.

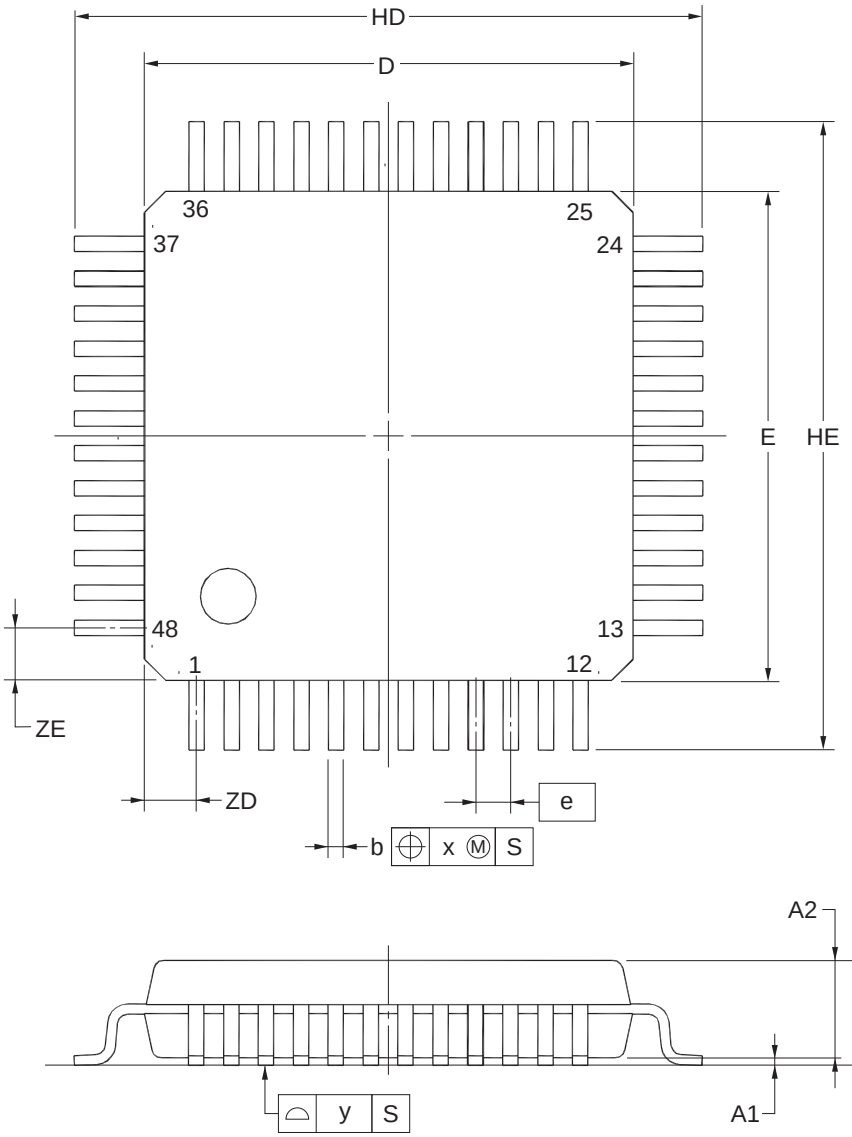
$t_{SU}$: How long from when the TOOL0 pin is placed at the low level until a external reset ends

<R> $t_{HD}$: How long to keep the TOOL0 pin at the low level from when the external resets end (except flash firmware processing time)

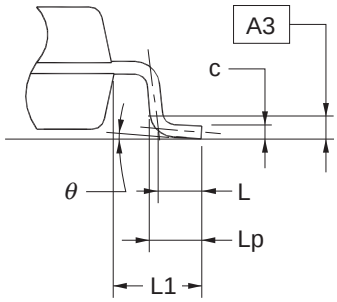
## 4.3 48-pin products

R5F10EGAAFB, R5F10EGCAFB, R5F10EGDAFB, R5F10EGEAFB
R5F10EGAGFB, R5F10EGCGFB, R5F10EGDGFB, R5F10EGEGFB

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-LFQFP48-7x7-0.50 | PLQP0048KF-A | P48GA-50-8EU-1 | 0.16 |




detail of lead end




(UNIT:mm)

| ITEM | DIMENSIONS |
|---|---|
| D | 7.00±0.20 |
| E | 7.00±0.20 |
| HD | 9.00±0.20 |
| HE | 9.00±0.20 |
| A | 1.60 MAX. |
| A1 | 0.10±0.05 |
| A2 | 1.40±0.05 |
| A3 | 0.25 |
| b | 0.22±0.05 |
| c | $0.145^{+0.055}_{-0.045}$ |
| L | 0.50 |
| Lp | 0.60±0.15 |
| L1 | 1.00±0.20 |
| θ | $3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$ |
| e | 0.50 |
| x | 0.08 |
| y | 0.08 |
| ZD | 0.75 |
| ZE | 0.75 |

**NOTE**
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.