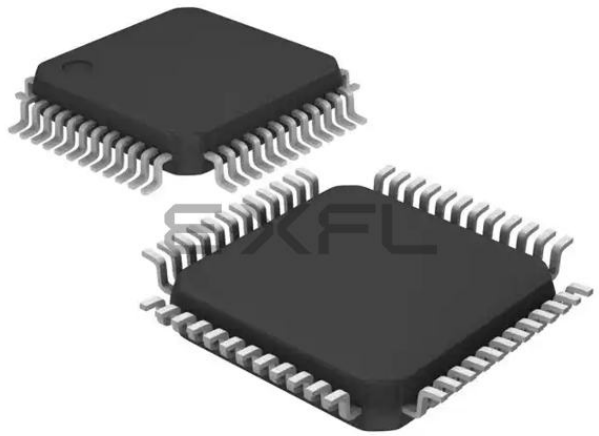

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | RL78 |
| Core Size | 16-Bit |
| Speed | 32MHz |
| Connectivity | CSI, I²C, LINbus, UART/USART |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 32 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 4K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.6V ~ 3.6V |
| Data Converters | A/D 24x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-LQFP |
| Supplier Device Package | 48-LFQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10egegfb-v0 |

○ ROM, RAM capacities

| Flash ROM | Data flash | RAM | RL78/G1A | | | |
|---|---|---|---|---|---|---|
| | | | 25 pins | 32 pins | 48 pins | 64 pins |
| 64 KB | 4 KB | 4 KB Note | R5F10E8E | R5F10EBE | R5F10EGE | R5F10ELE |
| 48 KB | 4 KB | 3 KB | R5F10E8D | R5F10EBD | R5F10EGD | R5F10ELD |
| 32 KB | 4 KB | 2 KB | R5F10E8C | R5F10EBC | R5F10EGC | R5F10ELC |
| 16 KB | 4 KB | 2 KB | R5F10E8A | R5F10EBA | R5F10EGA | – |

**Note** This is about 3 KB when the self-programming function and data flash function are used. (For details, see **3. ELECTRICAL SPECIFICATIONS (G: INDUSTRIAL APPLICATIONS $T_A$ = –40 to +105°C)**)

**($T_A$ = –40 to +85°C, 1.6 V ≤ $AV_{DD}$ ≤ $V_{DD}$ ≤ 3.6 V, 1.6 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)** **(2/5)**

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output current, low[Note 1] | $I_{OL1}$ | Per pin for P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P130, P140, P141 | | | | 20.0[Note 2] | mA |
| | | Per pin for P60 to P63 | | | | 15.0[Note 2] | mA |
| | | Total of P00 to P04, P40 to P43, P120, P130, P140, P141 (When duty ≤ 70%[Note 3]) | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V | | | 15.0 | mA |
| | | | 1.8 V ≤ $EV_{DD0}$ < 2.7 V | | | 9.0 | mA |
| | | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V | | | 4.5 | mA |
| | | Total of P05, P06, P10 to P16, P30, P31, P50, P51, P60 to P63, P70 to P77 (When duty ≤ 70%[Note 3]) | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V | | | 35.0 | mA |
| | | | 1.8 V ≤ $EV_{DD0}$ < 2.7 V | | | 20.0 | mA |
| | | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V | | | 10.0 | mA |
| | | Total of all pins (When duty ≤ 70%[Note 3]) | | | | 50.0 | mA |
| | $I_{OL2}$ | Per pin for P20 to P27, P150 to P154 | | | | 0.4[Note 2] | mA |
| | | Total of all pins (When duty ≤ 70%[Note 3]) | 1.6 V ≤ $AV_{DD}$ ≤ 3.6 V | | | 5.2 | mA |

**Notes 1.** Value of current at which the device operation is guaranteed even if the current flows from an output pin to the $EV_{SS0}$ and $V_{SS}$ pin.

**2.** However, do not exceed the total current value.

**3.** Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = ($I_{OL}$ × 0.7)/(n × 0.01)

<Example> Where n = 80% and $I_{OL}$ = 10.0 mA
Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≅ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

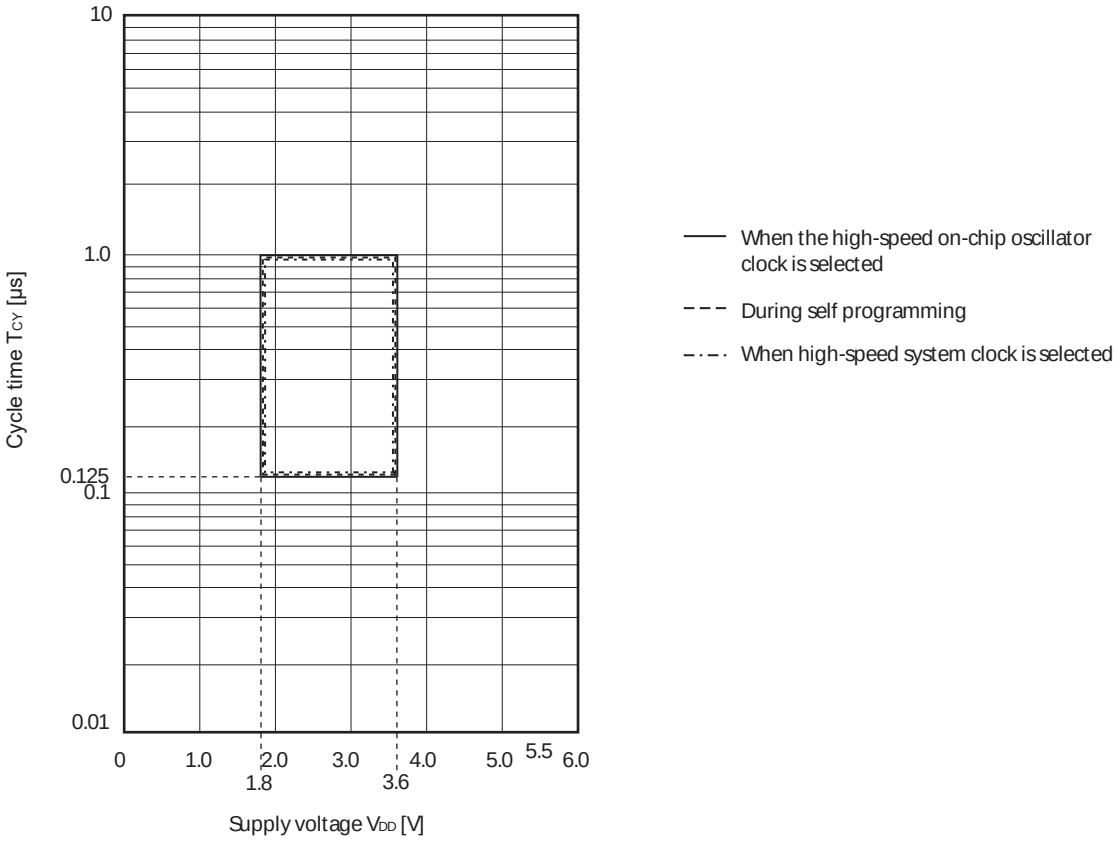
**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**($T_A$ = –40 to +85°C, 1.6 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)** **(2/3)**

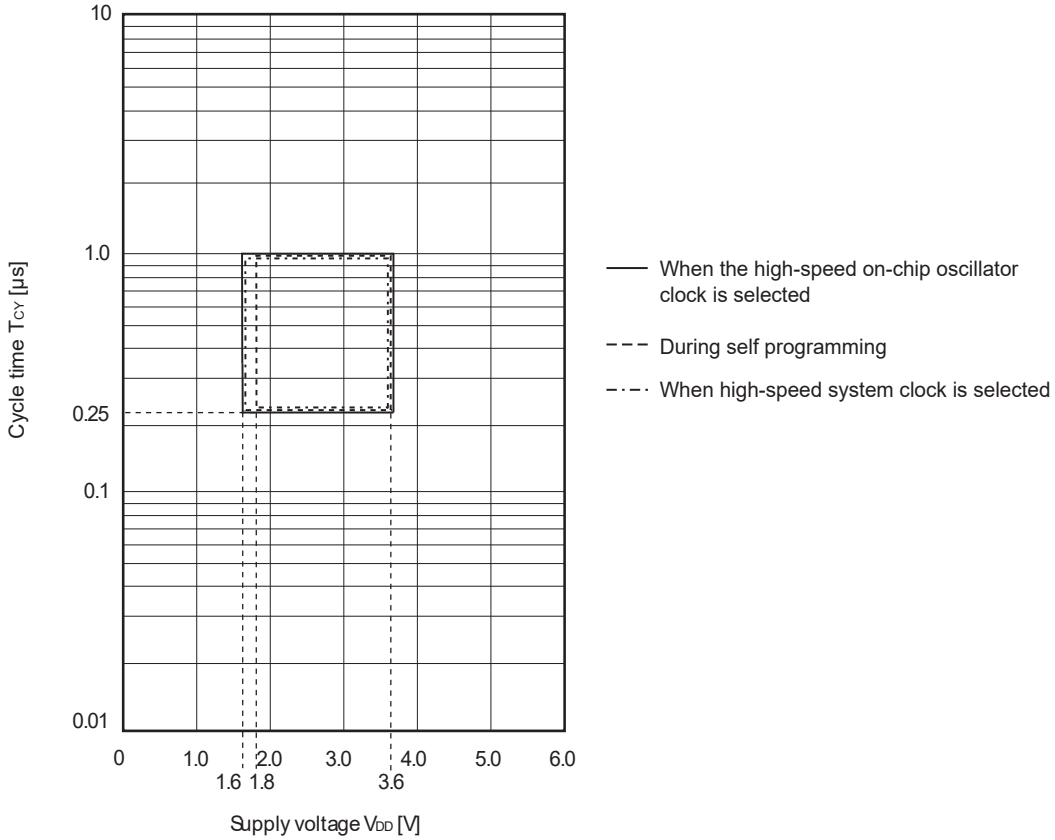
| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply current[Note 1] | $I_{DD2}$[Note 2] | HALT mode | HS (high-speed main) mode[Note 7] | $f_{IH}$ = 32 MHz[Note 4] | $V_{DD}$ = 3.0 V | | 0.54 | 1.63 | mA |
| | | | | $f_{IH}$ = 24 MHz[Note 4] | $V_{DD}$ = 3.0 V | | 0.44 | 1.28 | mA |
| | | | | $f_{IH}$ = 16 MHz[Note 4] | $V_{DD}$ = 3.0 V | | 0.40 | 1.00 | mA |
| | | | LS (low-speed main) mode[Note 7] | $f_{IH}$ = 8 MHz[Note 4] | $V_{DD}$ = 3.0 V | | 270 | 530 | μA |
| | | | | | $V_{DD}$ = 2.0 V | | 270 | 530 | |
| | | | LV (Low-voltage main) mode[Note 7] | $f_{IH}$ = 4 MHz[Note 4] | $V_{DD}$ = 3.0 V | | 435 | 640 | μA |
| | | | | | $V_{DD}$ = 2.0 V | | 435 | 640 | |
| | | | HS (high-speed main) mode[Note 7] | $f_{MX}$ = 20 MHz[Note 3], $V_{DD}$ = 3.0 V | Square wave input | | 0.28 | 1.00 | mA |
| | | | | | Resonator connection | | 0.45 | 1.17 | |
| | | | | $f_{MX}$ = 10 MHz[Note 3], $V_{DD}$ = 3.0 V | Square wave input | | 0.19 | 0.60 | mA |
| | | | | | Resonator connection | | 0.26 | 0.67 | |
| | | | LS (low-speed main) mode[Note 7] | $f_{MX}$ = 8 MHz[Note 3], $V_{DD}$ = 3.0 V | Square wave input | | 95 | 330 | μA |
| | | | | | Resonator connection | | 145 | 380 | |
| | | | | $f_{MX}$ = 8 MHz[Note 3], $V_{DD}$ = 2.0 V | Square wave input | | 95 | 330 | μA |
| | | | | | Resonator connection | | 145 | 380 | |
| | | | Subsystem clock mode | $f_{SUB}$ = 32.768 kHz[Note 5] $T_A$ = –40°C | Square wave input | | 0.25 | 0.57 | μA |
| | | | | | Resonator connection | | 0.44 | 0.76 | |
| | | | | $f_{SUB}$ = 32.768 kHz[Note 5] $T_A$ = +25°C | Square wave input | | 0.30 | 0.57 | μA |
| | | | | | Resonator connection | | 0.49 | 0.76 | |
| | | | | $f_{SUB}$ = 32.768 kHz[Note 5] $T_A$ = +50°C | Square wave input | | 0.38 | 1.17 | μA |
| | | | | | Resonator connection | | 0.57 | 1.36 | |
| | | | | $f_{SUB}$ = 32.768 kHz[Note 5] $T_A$ = +70°C | Square wave input | | 0.52 | 1.97 | μA |
| | | | | | Resonator connection | | 0.71 | 2.16 | |
| | | | | $f_{SUB}$ = 32.768 kHz[Note 5] $T_A$ = +85°C | Square wave input | | 0.97 | 3.37 | μA |
| | | | | | Resonator connection | | 1.16 | 3.56 | |
| | $I_{DD3}$[Note 6] | STOP mode[Note 8] | $T_A$ = –40°C | | | | 0.16 | 0.50 | μA |
| | | | $T_A$ = +25°C | | | | 0.23 | 0.50 | |
| | | | $T_A$ = +50°C | | | | 0.34 | 1.10 | |
| | | | $T_A$ = +70°C | | | | 0.46 | 1.90 | |
| | | | $T_A$ = +85°C | | | | 0.75 | 3.30 | |

(**Notes** and **Remarks** are listed on the next page.)

<R> $T_{CY}$ vs $V_{DD}$ (LS (low-speed main) mode)



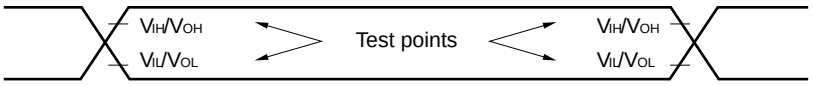

<R> $T_{CY}$ vs $V_{DD}$ (LV (low-voltage main) mode)



## 2.5 Peripheral Functions Characteristics

**AC Timing Test Points**

<R>




### 2.5.1 Serial array unit

**(1) During communication at same potential (UART mode)**

**($T_A$ = –40 to +85°C, 1.6 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

| Parameter | Symbol | Conditions | HS[Note 1] | | LS[Note 2] | | LV[Note 3] | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Transfer rate[Note 4] | | 2.4 V ≤ $EV_{DD}$ ≤ 3.6 V | | $f_{MCK}$/6 | | $f_{MCK}$/6 | | $f_{MCK}$/6 | bps |
| | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$[Note 6] | | 5.3[Note 5] | | 1.3 | | 0.6 | Mbps |
| | | 1.8 V ≤ $EV_{DD}$ ≤ 3.6 V | | $f_{MCK}$/6 | | $f_{MCK}$/6 | | $f_{MCK}$/6 | bps |
| | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$[Note 6] | | 5.3[Note 5] | | 1.3 | | 0.6 | Mbps |
| | | 1.7 V ≤ $EV_{DD}$ ≤ 3.6 V | | $f_{MCK}$/6 | | $f_{MCK}$/6 | | $f_{MCK}$/6 | bps |
| | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$[Note 6] | | 5.3[Note 5] | | 1.3[Note 5] | | 0.6 | Mbps |
| | | 1.6 V ≤ $EV_{DD}$ ≤ 3.6 V | | – | | $f_{MCK}$/6 | | $f_{MCK}$/6 | bps |
| | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$[Note 6] | | – | | 1.3[Note 5] | | 0.6 | Mbps |

**Notes 1.** HS is condition of HS (high-speed main) mode.

**2.** LS is condition of LS (low-speed main) mode.

**3.** LV is condition of LV (low-voltage main) mode.

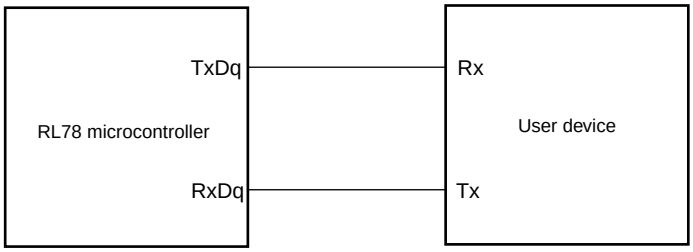
**4.** Transfer rate in the SNOOZE mode is 4800 bps.

**5.** The following conditions are required for low-voltage interface when $EV_{DD0}$ < $V_{DD}$.
2.4 V ≤ $EV_{DD0}$ < 2.7 V : MAX. 2.6 Mbps
1.8 V ≤ $EV_{DD0}$ < 2.4 V : MAX. 1.3 Mbps
1.6 V ≤ $EV_{DD0}$ < 1.8 V : MAX. 0.6 Mbps

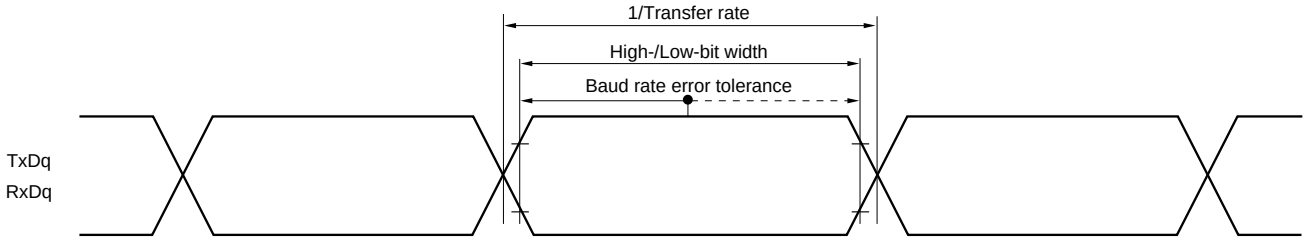
**6.** $f_{CLK}$ in each operating mode is as below.
HS (high-speed main) mode: $f_{CLK}$ = 32 MHz
LS (low-speed main) mode: $f_{CLK}$ = 8 MHz
LV (low-voltage main) mode: $f_{CLK}$ = 4 MHz

**Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**UART mode connection diagram (during communication at same potential)**




**UART mode bit width (during communication at same potential) (reference)**




**Remarks 1.** q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1)

**2.** $f_{MCK}$: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

**(5) During communication at same potential (simplified $I^2C$ mode) (2/2)**

**($T_A$ = –40 to +85°C, 1.6 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

| Parameter | Symbol | Conditions | HS[Note 1] | | LS[Note 2] | | LV[Note 3] | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Data hold time (transmission) | $t_{HD:DAT}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 0 | 305 | 0 | 305 | 0 | 305 | ns |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 3.6 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | 0 | 355 | 0 | 355 | 0 | 355 | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 2.7 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | 0 | 405 | 0 | 405 | 0 | 405 | ns |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 1.8 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | 0 | 405 | 0 | 405 | 0 | 405 | ns |
| | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | – | – | 0 | 405 | 0 | 405 | ns |

**Notes 1.** HS is condition of HS (high-speed main) mode.

**2.** LS is condition of LS (low-speed main) mode.

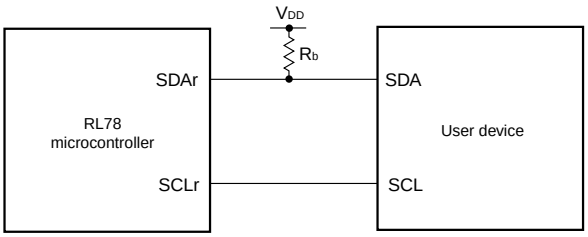
**3.** LV is condition of LV (low-voltage main) mode.

**4.** The value must also be $f_{CLK}$/4 or lower.

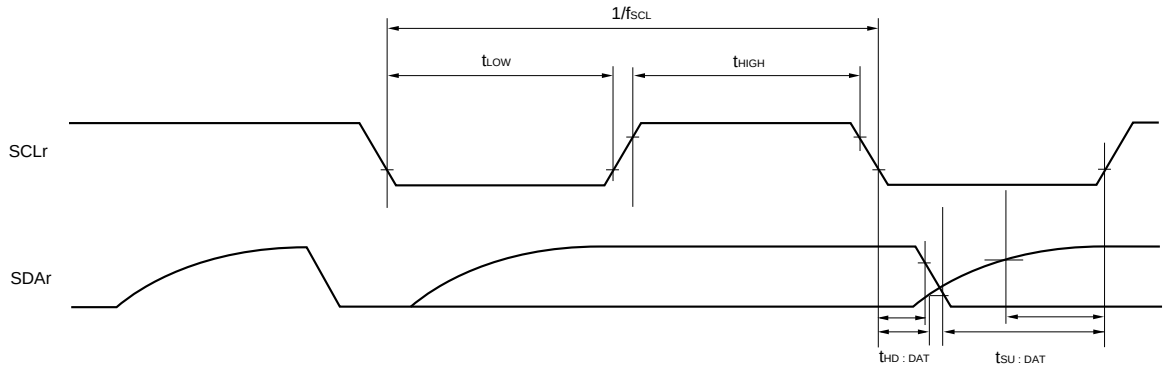
**5.** Set the $f_{MCK}$ value to keep the hold time of SCLr = “L” and SCLr = “H”.

**Caution Select the normal input buffer and the N-ch open drain output ($V_{DD}$ tolerance (When 25- to 48-pin products)/$EV_{DD}$ tolerance (When 64-pin products)) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).**

**Simplified $I^2C$ mode mode connection diagram (during communication at same potential)**




**Simplified $I^2C$ mode serial transfer timing (during communication at same potential)**




**Remarks 1.** $R_b$[Ω]: Communication line (SDAr) pull-up resistance, $C_b$[F]: Communication line (SDAr, SCLr) load capacitance

**2.** r: IIC number (r = 00, 01, 10, 11, 20, 21), g: PIM number (g = 0, 1), h: POM number (h = 0, 1)

**3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number, mn = 00 to 03, 10, 11)

**(6) Communication at different potential (1.8 V, 2.5 V) (UART mode) (dedicated baud rate generator output) (1/2)**

**($T_A$ = –40 to +85°C, 1.8 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

| Parameter | Symbol | Conditions | | | HS[Note 1] | | LS[Note 2] | | LV[Note 3] | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Transfer rate[Note 4] | | Reception | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | | $f_{MCK}$/6 | | $f_{MCK}$/6 | | $f_{MCK}$/6 | bps |
| | | | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$[Note 7] | | 5.3 | | 1.3 | | 0.6 | Mbps |
| | | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V[Note 5] | | | $f_{MCK}$/6 | | $f_{MCK}$/6 | | $f_{MCK}$/6 | bps |
| | | | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$[Note 7] | | 5.3 [Note 6] | | 1.3 | | 0.6 | Mbps |

**Notes 1.** HS is condition of HS (high-speed main) mode.

**2.** LS is condition of LS (low-speed main) mode.

**3.** LV is condition of LV (low-voltage main) mode.

**4.** Transfer rate in the SNOOZE mode is 4800 bps.

**5.** Use it with $EV_{DD0} \geq V_b$.

**6.** The following conditions are required for low-voltage interface when $EV_{DD0} < V_{DD}$.

2.4 V ≤ $EV_{DD0}$ < 2.7 V : MAX. 2.6 Mbps

1.8 V ≤ $EV_{DD0}$ < 2.4 V : MAX. 1.3 Mbps

**7.** $f_{CLK}$ in each operating mode is as below.

HS (high-speed main) mode: $f_{CLK}$ = 32 MHz

LS (low-speed main) mode: $f_{CLK}$ = 8 MHz

LV (low-voltage main) mode: $f_{CLK}$ = 4 MHz

**Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output ($V_{DD}$ tolerance (When 25- to 48-pin products)/$EV_{DD}$ tolerance (When 64-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

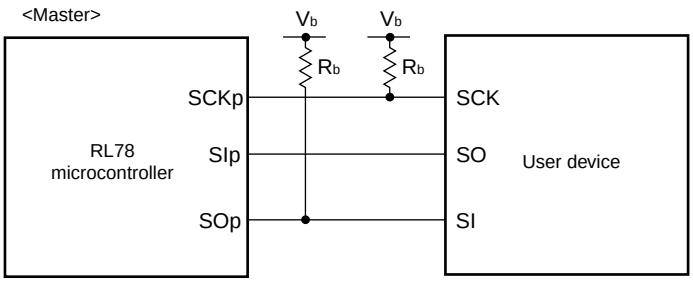
**Remarks 1.** $V_b$[V]: Communication line voltage

**2.** q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1)

**3.** $f_{MCK}$: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10, 11)

**CSI mode connection diagram (during communication at different potential)**




**Remarks 1.** $R_b$[Ω]: Communication line (SCKp, SOp) pull-up resistance, $C_b$[F]: Communication line (SCKp, SOp) load capacitance, $V_b$[V]: Communication line voltage

**2.** p: CSI number (p = 00, 10, 20), m: Unit number , n: Channel number (mn = 00, 02, 10), g: PIM and POM number (g = 0, 1)

**3.** CSI01, CSI11, and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

**(9) Communication at different potential (1.8 V, 2.5 V) (CSI mode) (slave mode, SCKp... external clock input)**
**($T_A$ = –40 to +85°C, 1.8 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS[Note 1] | | LS[Note 2] | | LV[Note 3] | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time[Note 4] | $t_{KCY2}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | 24 MHz < $f_{MCK}$ | 20/$f_{MCK}$ | | – | | – | | ns |
| | | | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 16/$f_{MCK}$ | | – | | – | | ns |
| | | | 16 MHz < $f_{MCK}$ ≤ 20 MHz | 14/$f_{MCK}$ | | – | | – | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 16 MHz | 12/$f_{MCK}$ | | – | | – | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 8/$f_{MCK}$ | | 16/$f_{MCK}$ | | – | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 6/$f_{MCK}$ | | 10/$f_{MCK}$ | | 10/$f_{MCK}$ | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V[Note 5] | 24 MHz < $f_{MCK}$ | 48/$f_{MCK}$ | | – | | – | | ns |
| | | | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 36/$f_{MCK}$ | | – | | – | | ns |
| | | | 16 MHz < $f_{MCK}$ ≤ 20 MHz | 32/$f_{MCK}$ | | – | | – | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 16 MHz | 26/$f_{MCK}$ | | – | | – | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 16/$f_{MCK}$ | | 16/$f_{MCK}$ | | – | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 10/$f_{MCK}$ | | 10/$f_{MCK}$ | | 10/$f_{MCK}$ | | ns |
| SCKp high-/low-level width | $t_{KH2}$, $t_{KL2}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | $t_{KCY2}$/2 – 18 | | $t_{KCY2}$/2 – 50 | | $t_{KCY2}$/2 – 50 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V[Note 5] | | $t_{KCY2}$/2 – 50 | | $t_{KCY2}$/2 – 50 | | $t_{KCY2}$/2 – 50 | | ns |
| SIp setup time (to SCKp↑)[Note 6] | $t_{SIK2}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | 1/$f_{MCK}$ + 20 | | 1/$f_{MCK}$ + 30 | | 1/$f_{MCK}$ + 30 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V[Note 5] | | 1/$f_{MCK}$ + 30 | | 1/$f_{MCK}$ + 30 | | 1/$f_{MCK}$ + 30 | | ns |
| SIp hold time (from SCKp↑)[Note 6] | $t_{KSI2}$ | | | 1/$f_{MCK}$ + 31 | | 1/$f_{MCK}$ + 31 | | 1/$f_{MCK}$ + 31 | | ns |
| Delay time from SCKp↓ to SOp output[Note 7] | $t_{KSO2}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | | 2/$f_{MCK}$ + 214 | | 2/$f_{MCK}$ + 573 | | 2/$f_{MCK}$ + 573 | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V[Note 5], $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | | 2/$f_{MCK}$ + 573 | | 2/$f_{MCK}$ + 573 | | 2/$f_{MCK}$ + 573 | ns |

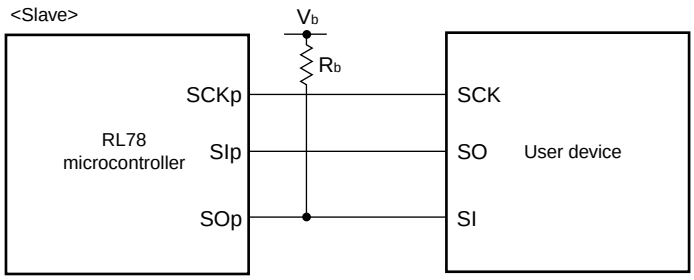
**Notes 1.** HS is condition of HS (high-speed main) mode.
**2.** LS is condition of LS (low-speed main) mode.
**3.** LV is condition of LV (low-voltage main) mode.
**4.** Transfer rate in the SNOOZE mode : MAX. 1 Mbps
**5.** Use it with $EV_{DD0}$ ≥ $V_b$.
**6.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time or SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
**7.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Caution Select the TTL input buffer for the SIp pin and SCKp pin and the N-ch open drain output ($V_{DD}$ tolerance (When 25- to 48-pin products)/$EV_{DD}$ tolerance (When 64-pin products)) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

<R>

(**Remarks** are listed on the next page.)

**CSI mode connection diagram (during communication at different potential)**




**Remarks 1.** $R_b$[Ω]: Communication line (SOp) pull-up resistance, $C_b$[F]: Communication line (SOp) load capacitance, $V_b$[V]: Communication line voltage

**2.** p: CSI number (p = 00, 10, 20), m: Unit number (m = 0, 1), n: Channel number (n = 00, 02, 10), g: PIM and POM number (g = 0, 1)

**3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 02, 10))

**4.** CSI01, CSI11, and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

**(10) Communication at different potential (1.8 V, 2.5 V) (simplified $I^2C$ mode) (2/2)**

**($T_A$ = –40 to +85°C, 1.8 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

| Parameter | Symbol | Conditions | HS[Note 1] | | LS[Note 2] | | LV[Note 3] | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Data setup time (reception) | $t_{SU:DAT}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 1/$f_{MCK}$ + 135[Note 6] | | 1/$f_{MCK}$ + 190[Note 6] | | 1/$f_{MCK}$ + 190[Note 6] | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 1/$f_{MCK}$ + 190[Note 6] | | 1/$f_{MCK}$ + 190[Note 6] | | 1/$f_{MCK}$ + 190[Note 6] | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V[Note 5], $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 1/$f_{MCK}$ + 190[Note 6] | | 1/$f_{MCK}$ + 190[Note 6] | | 1/$f_{MCK}$ + 190[Note 6] | | ns |
| Data hold time (transmission) | $t_{HD:DAT}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 0 | 305 | 0 | 305 | 0 | 305 | ns |
| | | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 0 | 355 | 0 | 355 | 0 | 355 | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V[Note 5], $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 0 | 405 | 0 | 405 | 0 | 405 | ns |

**Notes 1.** HS is condition of HS (high-speed main) mode.

**2.** LS is condition of LS (low-speed main) mode.

**3.** LV is condition of LV (low-voltage main) mode.

**4.** The value must also be $f_{CLK}$/4 or lower.

**5.** Use it with $EV_{DD0} \geq V_b$.

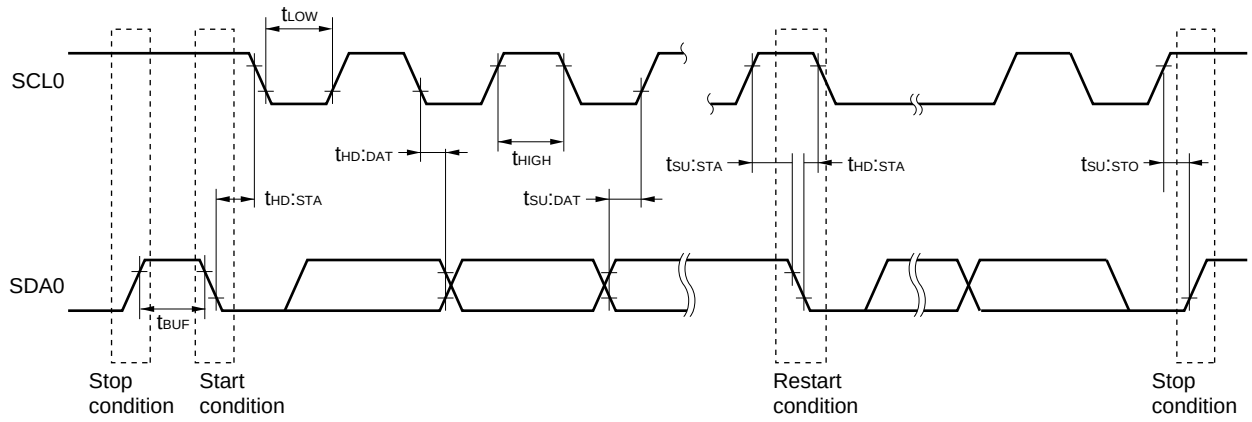
**6.** Set the $f_{MCK}$ value to keep the hold time of SCLr = “L” and SCLr = “H”.

**Caution Select the TTL input buffer and the N-ch open drain output ($V_{DD}$ tolerance (When 25- to 48-pin products)/$EV_{DD}$ tolerance (When 64-pin products)) mode for the SDAr pin and the N-ch open drain output ($V_{DD}$ tolerance (When 25- to 48-pin products)/$EV_{DD}$ tolerance (When 64-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

<R>

(**Remarks** are listed on the next page.)

**IICA serial transfer timing**



## 2.9 Dedicated Flash Memory Programmer Communication (UART)

**($T_A$ = –40 to +85°C, 1.8 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

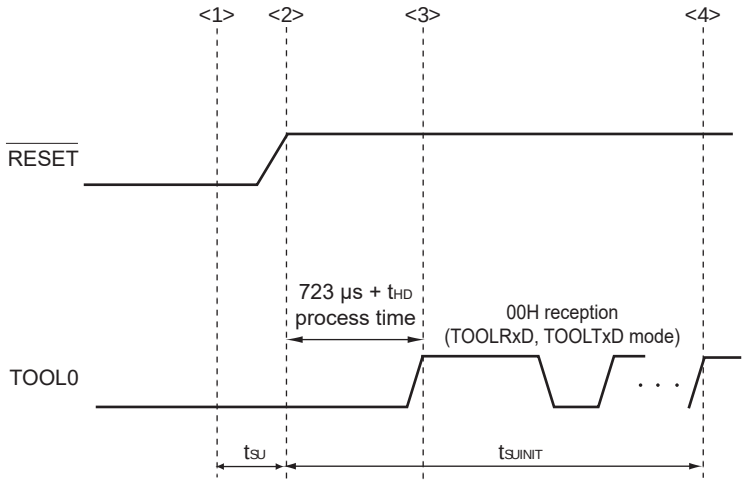
| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Transfer rate | | During flash memory programming | 115.2 k | | 1 M | bps |

## 2.10 Timing Specs for Switching Flash Memory Programming Modes

**($T_A$ = –40 to +85°C, 1.8 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| How long from when an external reset ends until the initial communication settings are specified | $t_{SUINIT}$ | POR and LVD reset must end before the external reset ends. | | | 100 | ms |
| How long from when the TOOL0 pin is placed at the low level until a external reset ends | $t_{SU}$ | POR and LVD reset must end before the external reset ends. | 10 | | | μs |
| <R> How long the TOOL0 pin must be kept at the low level after an external reset ends (except flash firmware processing time) | $t_{HD}$ | POR and LVD reset must end before the external reset ends. | 1 | | | ms |

<R>




<1> The low level is input to the TOOL0 pin.
<2> The pins reset ends (POR and LVD reset must end before the external reset ends.).
<3> The TOOL0 pin is set to the high level.
<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

**Remark** $t_{SUINIT}$: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the resets end.

$t_{SU}$: How long from when the TOOL0 pin is placed at the low level until a external reset ends

<R> $t_{HD}$: How long to keep the TOOL0 pin at the low level from when the external resets end (except flash firmware processing time)

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)** **(3/3)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Low-speed on-chip oscillator operating current | $I_{FIL}$ Note 1 | | | | 0.20 | | μA |
| RTC operating current | $I_{RTC}$ Notes 1, 2, 3 | | | | 0.02 | | μA |
| 12-bit interval timer operating current | $I_{IT}$ Notes 1, 2, 4 | | | | 0.02 | | μA |
| Watchdog timer operating current | $I_{WDT}$ Notes 1, 2, 5 | $f_{IL}$ = 15 kHz | | | 0.22 | | μA |
| A/D converter operating current | $I_{ADC}$ Notes 6, 7 | $AV_{DD}$ = 3.0 V, When conversion at maximum speed | | | 420 | 720 | μA |
| $AV_{REF(+)}$ current | $I_{AVREF}$ Note 8 | $AV_{DD}$ = 3.0 V, ADREFP1 = 0, ADREFP0 = 0 Note 7 | | | 14.0 | 25.0 | μA |
| | | $AV_{REFP}$ = 3.0 V, ADREFP1 = 0, ADREFP0 = 1 Note 10 | | | 14.0 | 25.0 | μA |
| | | ADREFP1 = 1, ADREFP0 = 0 Note 1 | | | 14.0 | 25.0 | μA |
| A/D converter reference voltage current | $I_{ADREF}$ Notes 1, 9 | $V_{DD}$ = 3.0 V | | | 75.0 | | μA |
| Temperature sensor operating current | $I_{TMPS}$ Note 1 | $V_{DD}$ = 3.0 V | | | 75.0 | | μA |
| LVD operating current | $I_{LVD}$ Notes 1, 11 | | | | 0.08 | | μA |
| BGO operating current | $I_{BGO}$ Notes 1, 12 | | | | 2.5 | 12.2 | mA |
| Self-programming operating current | $I_{FSP}$ Notes 1, 13 | | | | 2.5 | 12.2 | mA |
| SNOOZE operating current | $I_{SNOZ}$ | A/D converter operation ($AV_{DD}$ = 3.0 V) | The mode is performed Notes 1, 14 | | 0.50 | 1.10 | mA |
| | | | During A/D conversion Note 1 | | 0.60 | 1.34 | mA |
| | | | During A/D conversion Note 7 | | 420 | 720 | μA |
| | | CSI/UART operation Note 1 | | | 0.70 | 1.54 | mA |

(**Notes** and **Remarks** are listed on the next page.)

<R> **Notes 1.** Current flowing to $V_{DD}$.

**2.** When high-speed on-chip oscillator and high-speed system clock are stopped.

**3.** Current flowing only to the real-time clock (RTC) (excluding the operating current of the low-speed on-chip ocsillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either $I_{DD1}$ or $I_{DD2}$, and $I_{RTC}$, when the real-time clock operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, $I_{FIL}$ should be added. $I_{DD2}$ subsystem clock operation includes the operational current of the real-time clock.

**4.** Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip ocsillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either $I_{DD1}$ or $I_{DD2}$, and $I_{IT}$, when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, $I_{FIL}$ should be added.

**5.** Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontrollers is the sum of $I_{DD1}$, $I_{DD2}$, or $I_{DD3}$ and $I_{WDT}$ when the watchdog timer is in operation.

**6.** Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of $I_{DD1}$ or $I_{DD2}$ and $I_{ADC}$, $I_{AVREF}$, $I_{ADREF}$ when the A/D converter operates in an operation mode or the HALT mode.

**7.** Current flowing to the $AV_{DD}$.

**8.** Current flowing from the reference voltage source of A/D converter.

**9.** Operation current flowing to the internal reference voltage.

**10.** Current flowing to the $AV_{REFP}$.

**11.** Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of $I_{DD1}$, $I_{DD2}$ or $I_{DD3}$ and $I_{LVD}$ when the LVD circuit is in operation.

**12.** Current flowing only during data flash rewrite.

**13.** Current flowing only during self programming.

**Remarks 1.** $f_{IL}$: Low-speed on-chip oscillator clock frequency

**2.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**3.** $f_{CLK}$: CPU/peripheral hardware clock frequency

**4.** Temperature condition of the TYP. value is $T_A$ = 25°C

**(5) Communication at different potential (1.8 V, 2.5 V) (UART mode) (dedicated baud rate generator output) (1/2)**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

| Parameter | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Transfer rate[Note 1] | | Reception | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | | | $f_{MCK}$/12 | bps |
| | | | | Theoretical value of the maximum transfer rate $f_{CLK}$ = 32 MHz, $f_{MCK}$ = $f_{CLK}$ | | | 2.6 | Mbps |
| | | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | | | | $f_{MCK}$/12 | bps |
| | | | | Theoretical value of the maximum transfer rate $f_{CLK}$ = 32 MHz, $f_{MCK}$ = $f_{CLK}$ | | | 2.6[Note 2] | Mbps |

**Notes 1.** Transfer rate in the SNOOZE mode is 4800 bps.

**2.** The following conditions are required for low-voltage interface when $EV_{DD0}$ < $V_{DD}$.
2.4 V ≤ $EV_{DD0}$ < 2.7 V : MAX. 1.3 Mbps

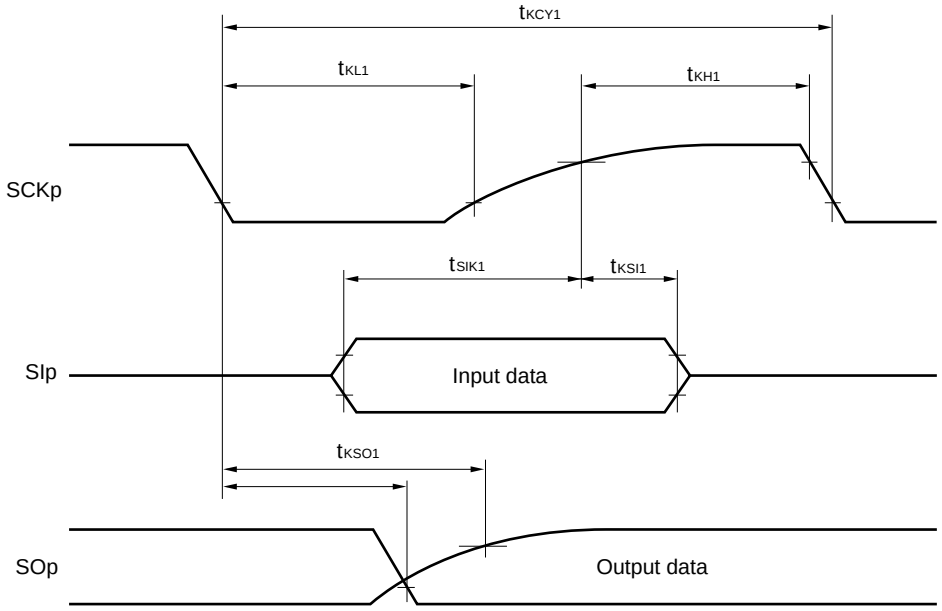
**Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output ($V_{DD}$ tolerance (When 25- to 48-pin products)/$EV_{DD}$ tolerance (When 64-pin products)) mode for the TxDq pin by using** <R> **port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**Remarks 1.** $V_b$[V]: Communication line voltage

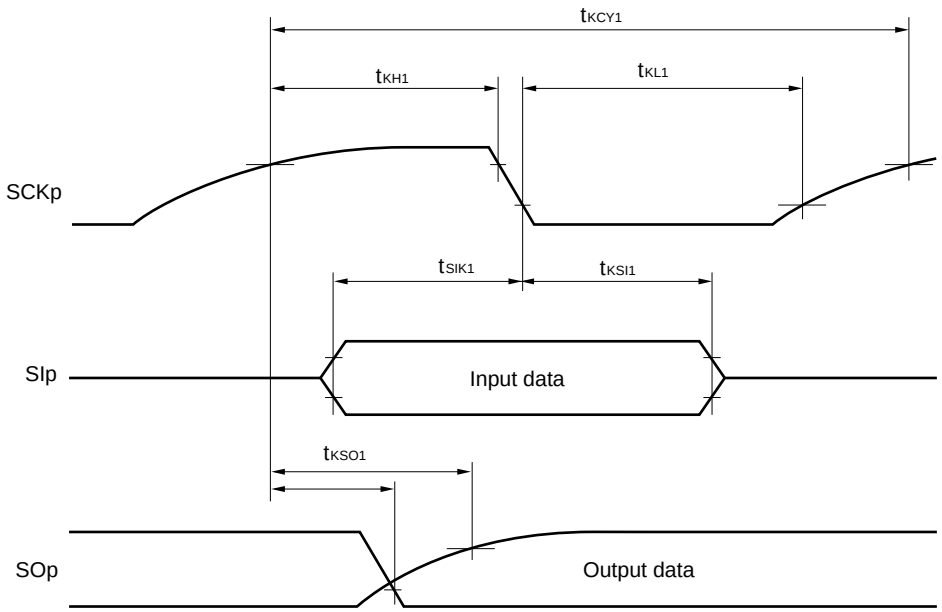
**2.** q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1)

**3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10, 11)

**CSI mode serial transfer timing (master mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**



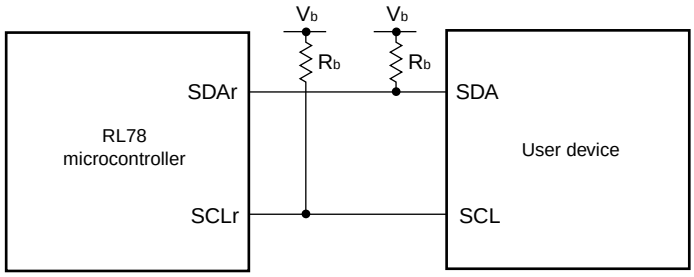

**CSI mode serial transfer timing (master mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**



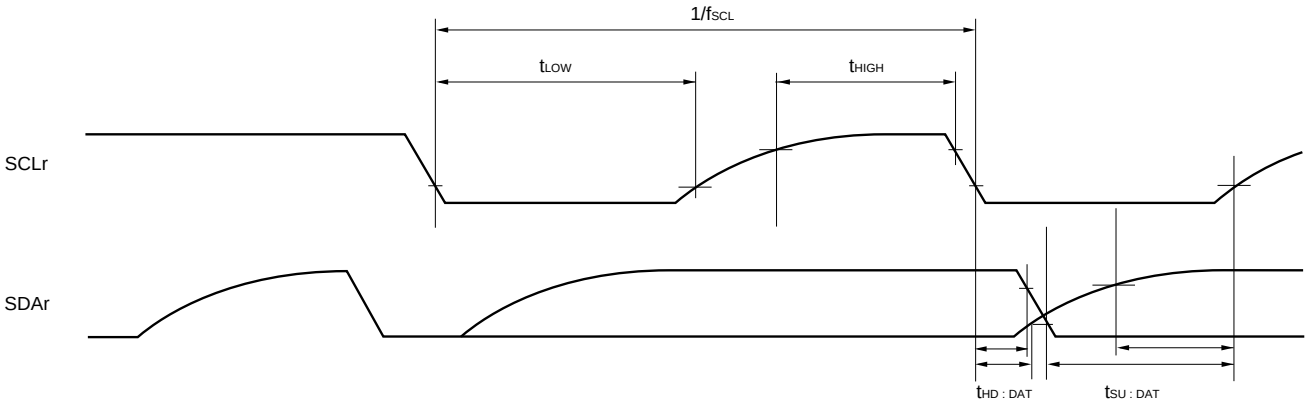

**Remarks 1.** p: CSI number (p = 00, 10, 20), m: Unit number, n: Channel number (m = 00, 02, 10), g: PIM and POM number (g = 0, 1)

**2.** CSI01, CSI11, and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

**Simplified $I^2C$ mode connection diagram (during communication at different potential)**




**Simplified $I^2C$ mode serial transfer timing (during communication at different potential)**




**Remarks 1.** $R_b$[Ω]: Communication line (SDAr, SCLr) pull-up resistance, $C_b$[F]: Communication line (SDAr, SCLr) load capacitance, $V_b$[V]: Communication line voltage

**2.** r: IIC number (r = 00, 10, 20), g: PIM, POM number (g = 0, 1)

**3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 02, 10)

**4.** IIC01, IIC11, and IIC21 cannot communicate at different potential. Use IIC00, IIC10, or IIC20 for communication at different potential.

### 3.5.2 Serial interface IICA

**(1) $I^2C$ standard mode, fast mode**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

| Parameter | Symbol | Conditions | | Standard Mode | | Fast Mode | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | |
| SCLA0 clock frequency | $f_{SCL}$ | Fast mode: $f_{CLK}$ ≥ 3.5 MHz | 2.4 V ≤ $EV_{DD0}$ ≤ 3.6 V | | | 0 | 400 | kHz |
| | | Normal mode: $f_{CLK}$ ≥ 1 MHz | 2.4 V ≤ $EV_{DD0}$ ≤ 3.6 V | 0 | 100 | | | kHz |
| Setup time of restart condition | $t_{SU:STA}$ | | | 4.7 | | 0.6 | | μs |
| Hold time[Note 1] | $t_{HD:STA}$ | | | 4.0 | | 0.6 | | μs |
| Hold time when SCLA0 = “L” | $t_{LOW}$ | | | 4.7 | | 1.3 | | μs |
| Hold time when SCLA0 = “H” | $t_{HIGH}$ | | | 4.0 | | 0.6 | | μs |
| Data setup time (reception) | $t_{SU:DAT}$ | | | 250 | | 100 | | ns |
| Data hold time (transmission)[Note 2] | $t_{HD:DAT}$ | | | 0 | 3.45 | 0 | 0.9 | μs |
| Setup time of stop condition | $t_{SU:STO}$ | | | 4.0 | | 0.6 | | μs |
| Bus-free time | $t_{BUF}$ | | | 4.7 | | 1.3 | | μs |

**Notes 1.** The first clock pulse is generated after this period when the start/restart condition is detected.

**2.** The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

**Remark** The maximum value of $C_b$ (communication line capacitance) and the value of $R_b$ (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: $C_b$ = 400 pF, $R_b$ = 2.7 kΩ

Fast mode: $C_b$ = 320 pF, $R_b$ = 1.1 kΩ

**IICA serial transfer timing**