# Renesas Electronics America Inc - R5F10ELEGFB#V0 Datasheet

**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

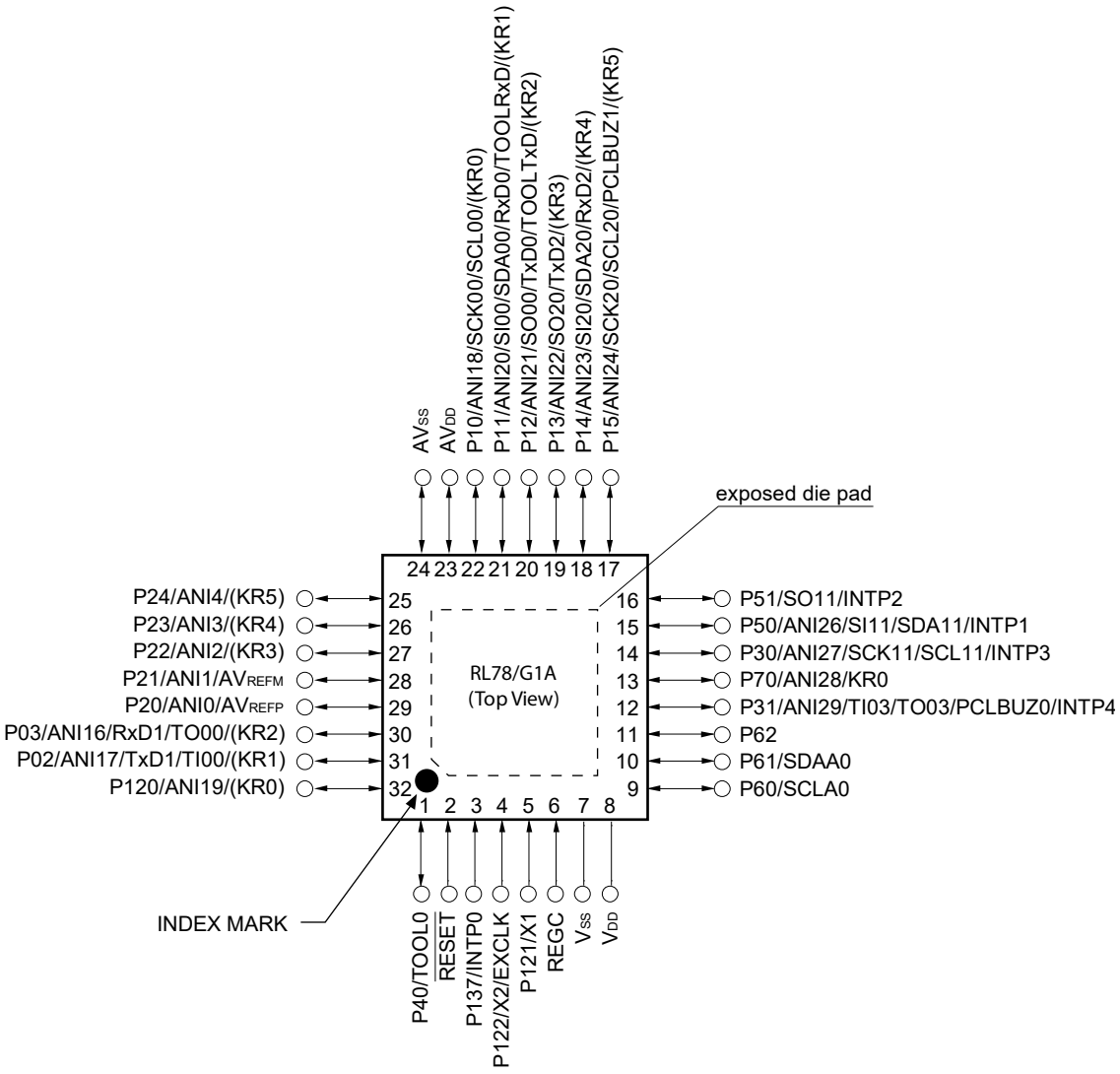
## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | RL78 |
| Core Size | 16-Bit |
| Speed | 32MHz |
| Connectivity | CSI, I²C, LINbus, UART/USART |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 46 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 4K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.6V ~ 3.6V |
| Data Converters | A/D 28x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP |
| Supplier Device Package | 64-LFQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10elegfb-v0 |

### 1.3.2 32-pin products

- 32-pin plastic HWQFN (5 × 5 mm, 0.5 mm pitch)

<R>




**Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).**

**Remarks 1.** For pin identification, see **1.4 Pin Identification**.

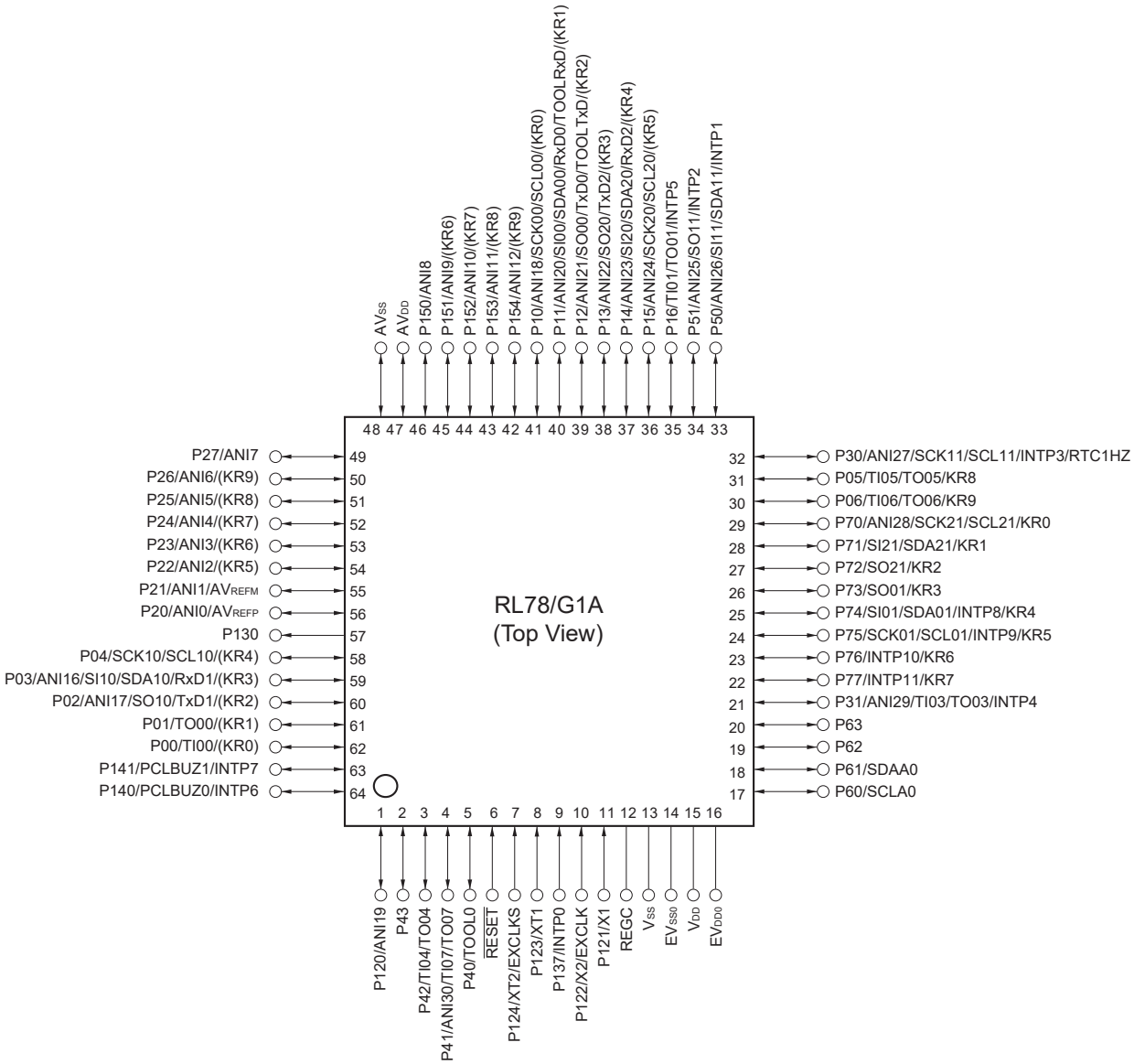
**2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

<R> **3.** It is recommended to connect an exposed die pad to $V_{SS}$.

### 1.3.4 64-pin products

- 64-pin plastic LFQFP (10 × 10 mm, 0.5 mm pitch)

<R>




**Cautions 1. Make $EV_{SS0}$ pin the same potential as $V_{SS}$ pin.**

**2. Make $V_{DD}$ pin the potential that is higher than $EV_{DD0}$ pin.**

**3. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).**

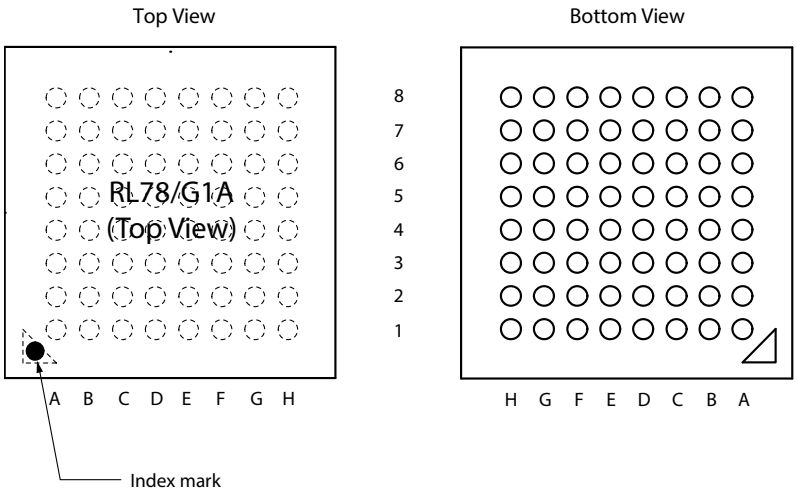
**Remarks 1.** For pin identification, see **1.4 Pin Identification.**

**2.** When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the $V_{DD}$ and $EV_{DD0}$ pins and connect the $V_{SS}$ and $EV_{SS}$0pins to separate ground lines.

**3.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

- 64-pin plastic VFBGA (4 × 4 mm, 0.4 mm pitch)

<R>




| Pin No. | Name | Pin No. | Name | Pin No. | Name | Pin No. | Name |
|---|---|---|---|---|---|---|---|
| A1 | P05/TI05/TO05/KR8 | C1 | P51/ANI25/SO11 /INTP2 | E1 | P153/ANI11/(KR8) | G1 | $AV_{DD}$ |
| A2 | P30/ANI27/SCK11 /SCL11/INTP3 /RTC1HZ | C2 | P71/SI21/SDA21/KR1 | E2 | P154/ANI12/(KR9) | G2 | P25/ANI5/(KR8) |
| A3 | P70/ANI28/SCK21 /SCL21/KR0 | C3 | P74/SI01/SDA01 /INTP8/KR4 | E3 | P10/ANI18/SCK00 /SCL00/(KR0) | G3 | P24/ANI4/(KR7) |
| A4 | P75/SCK01/SCL01 /INTP9/KR5 | C4 | P16/TI01/TO01/INTP5 | E4 | P11/ANI20/SI00 /SDA00/RxD0 /TOOLRxD/(KR1) | G4 | P22/ANI2/(KR5) |
| A5 | P77/INTP11/KR7 | C5 | P15/ANI24/SCK20 /SCL20/(KR5) | E5 | P03/ANI16/SI10 /SDA10/RxD1/(KR3) | G5 | P130 |
| A6 | P61/SDAA0 | C6 | P63 | E6 | P41/ANI30/TI07/TO07 | G6 | P02/ANI17/SO10/TxD1 /(KR2) |
| A7 | P60/SCLA0 | C7 | $V_{SS}$ | E7 | $\overline{RESET}$ | G7 | P00/TI00/(KR0) |
| A8 | $EV_{DD0}$ | C8 | P121/X1 | E8 | P137/INTP0 | G8 | P124/XT2/EXCLKS |
| B1 | P50/ANI26 /SI11 /SDA11/INTP1 | D1 | P13/ANI22/SO20 /TxD2/(KR3) | F1 | P150/ANI8 | H1 | $AV_{SS}$ |
| B2 | P72/SO21/KR2 | D2 | P06/TI06/TO06/KR9 | F2 | P151/ANI9/(KR6) | H2 | P27/ANI7 |
| B3 | P73/SO01/KR3 | D3 | P12/ANI21/SO00 /TxD0/TOOLTxD/(KR2) | F3 | P152/ANI10/(KR7) | H3 | P26/ANI6/(KR9) |
| B4 | P76/INTP10/KR6 | D4 | P14/ANI23/SI20/ SDA20/RxD2/(KR4) | F4 | $P21/ANI1/AV_{REFM}$ | H4 | P23/ANI3/(KR6) |
| B5 | P31/ANI29/TI03/TO03 /INTP4 | D5 | P42/TI04/TO04 | F5 | P04/SCK10/SCL10 /(KR4) | H5 | $P20/ANI0/AV_{REFP}$ |
| B6 | P62 | D6 | P40/TOOL0 | F6 | P43 | H6 | P141/PCLBUZ1/INTP7 |
| B7 | $V_{DD}$ | D7 | REGC | F7 | P01/TO00/(KR1) | H7 | P140/PCLBUZ0/INTP6 |
| B8 | $EV_{SS0}$ | D8 | P122/X2/EXCLK | F8 | P123/XT1 | H8 | P120/ANI19 |

**Cautions 1. Make $EV_{SS0}$ pin the same potential as $V_{SS}$ pin.**

**2. Make $V_{DD}$ pin the potential that is higher than $EV_{DD0}$ pin.**

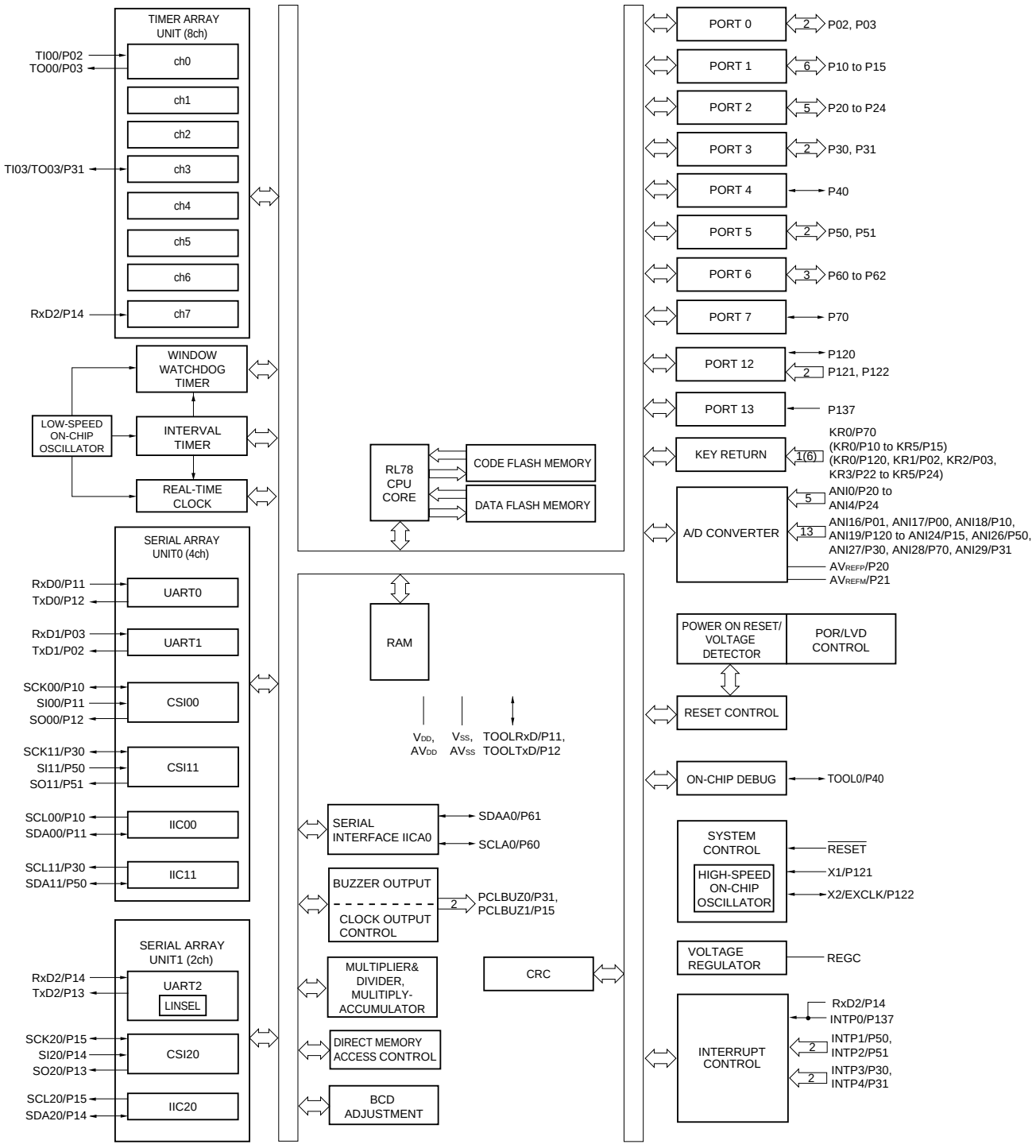
**3. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).**

**Remarks 1.** For pin identification, see **1.4 Pin Identification.**

**2.** When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the $V_{DD}$ and $EV_{DD0}$ pins and connect the $V_{SS}$ and $EV_{SS0}$ pins to separate ground lines.

**3.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

### <R> 1.5.2 32-pin products




**Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

## 2.3 DC Characteristics

### 2.3.1 Pin characteristics

**($T_A$ = –40 to +85°C, 1.6 V ≤ $AV_{DD}$ ≤ $V_{DD}$ ≤ 3.6 V, 1.6 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)** **(1/5)**

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output current, high[Note 1] | $I_{OH1}$ | Per pin for P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P130, P140, P141 | 1.6 V ≤ $EV_{DD0}$ ≤ 3.6 V | | | –10.0[Note 2] | mA |
| | | Total of P00 to P04, P40 to P43, P120, P130, P140, P141 (When duty ≤ 70%[Note 3]) | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V | | | –10.0 | mA |
| | | | 1.8 V ≤ $EV_{DD0}$ < 2.7 V | | | –5.0 | mA |
| | | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V | | | –2.5 | mA |
| | | Total of P05, P06, P10 to P16, P30, P31, P50, P51, P70 to P77, (When duty ≤ 70%[Note 3]) | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V | | | –19.0 | mA |
| | | | 1.8 V ≤ $EV_{DD0}$ < 2.7 V | | | –10.0 | mA |
| | | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V | | | –5.0 | mA |
| | | Total of all pins (When duty ≤ 70%[Note 3]) | 1.6 V ≤ $EV_{DD0}$ ≤ 3.6 V | | | –29.0 | mA |
| | $I_{OH2}$ | Per pin for P20 to P27, P150 to P154 | 1.6 V ≤ $AV_{DD}$ ≤ 3.6 V | | | –0.1[Note 2] | mA |
| | | Total of all pins (When duty ≤ 70%[Note 3]) | 1.6 V ≤ $AV_{DD}$ ≤ 3.6 V | | | –1.3 | mA |

**Notes 1.** Value of current at which the device operation is guaranteed even if the current flows from the $EV_{DD0}$, $V_{DD}$ pins to an output pin.

**2.** However, do not exceed the total current value.

**3.** Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = ($I_{OH}$ × 0.7)/(n × 0.01)

<Example> Where n = 80% and $I_{OH}$ = –10.0 mA
Total output current of pins = (–10.0 × 0.7)/(80 × 0.01) ≅ –8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

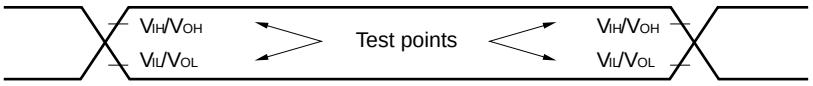
**Caution P00, P02 to P04, P10 to P15, P43, P50, P71, and P74 do not output high level in N-ch open-drain mode.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

## 2.5 Peripheral Functions Characteristics

**AC Timing Test Points**

<R>




### 2.5.1 Serial array unit

**(1) During communication at same potential (UART mode)**

**($T_A$ = –40 to +85°C, 1.6 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

| Parameter | Symbol | Conditions | HS[Note 1] | | LS[Note 2] | | LV[Note 3] | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Transfer rate[Note 4] | | 2.4 V ≤ $EV_{DD}$ ≤ 3.6 V | | $f_{MCK}$/6 | | $f_{MCK}$/6 | | $f_{MCK}$/6 | bps |
| | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$[Note 6] | | 5.3[Note 5] | | 1.3 | | 0.6 | Mbps |
| | | 1.8 V ≤ $EV_{DD}$ ≤ 3.6 V | | $f_{MCK}$/6 | | $f_{MCK}$/6 | | $f_{MCK}$/6 | bps |
| | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$[Note 6] | | 5.3[Note 5] | | 1.3 | | 0.6 | Mbps |
| | | 1.7 V ≤ $EV_{DD}$ ≤ 3.6 V | | $f_{MCK}$/6 | | $f_{MCK}$/6 | | $f_{MCK}$/6 | bps |
| | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$[Note 6] | | 5.3[Note 5] | | 1.3[Note 5] | | 0.6 | Mbps |
| | | 1.6 V ≤ $EV_{DD}$ ≤ 3.6 V | | – | | $f_{MCK}$/6 | | $f_{MCK}$/6 | bps |
| | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$[Note 6] | | – | | 1.3[Note 5] | | 0.6 | Mbps |

**Notes 1.** HS is condition of HS (high-speed main) mode.

**2.** LS is condition of LS (low-speed main) mode.

**3.** LV is condition of LV (low-voltage main) mode.

**4.** Transfer rate in the SNOOZE mode is 4800 bps.

**5.** The following conditions are required for low-voltage interface when $EV_{DD0}$ < $V_{DD}$.
2.4 V ≤ $EV_{DD0}$ < 2.7 V : MAX. 2.6 Mbps
1.8 V ≤ $EV_{DD0}$ < 2.4 V : MAX. 1.3 Mbps
1.6 V ≤ $EV_{DD0}$ < 1.8 V : MAX. 0.6 Mbps

**6.** $f_{CLK}$ in each operating mode is as below.
HS (high-speed main) mode: $f_{CLK}$ = 32 MHz
LS (low-speed main) mode: $f_{CLK}$ = 8 MHz
LV (low-voltage main) mode: $f_{CLK}$ = 4 MHz

**Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)**

**($T_A$ = –40 to +85°C, 1.6 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS[Note 1] | | LS[Note 2] | | LV[Note 3] | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time[Note 4] | $t_{KCY2}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V | 16 MHz < $f_{MCK}$ | 8/$f_{MCK}$ | | – | | – | | ns |
| | | | $f_{MCK}$ ≤ 16 MHz | 6/$f_{MCK}$ | | 6/$f_{MCK}$ | | 6/$f_{MCK}$ | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 3.6 V | | 6/$f_{MCK}$ and 500ns | | 6/$f_{MCK}$ and 500ns | | 6/$f_{MCK}$ and 500ns | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 3.6 V | | 6/$f_{MCK}$ and 750ns | | 6/$f_{MCK}$ and 750ns | | 6/$f_{MCK}$ and 750ns | | ns |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 3.6 V | | 6/$f_{MCK}$ and 1500ns | | 6/$f_{MCK}$ and 1500ns | | 6/$f_{MCK}$ and 1500ns | | ns |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 3.6 V | | – | | 6/$f_{MCK}$ and 1500ns | | 6/$f_{MCK}$ and 1500ns | | ns |
| SCKp high-/low-level width | $t_{KH2}$, $t_{KL2}$ | 2.7 V ≤ $EV_{DD}$ ≤ 3.6 V | | $t_{KCY2}$/2 –8 | | $t_{KCY2}$/2 –8 | | $t_{KCY2}$/2 –8 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 3.6 V | | $t_{KCY2}$/2 –18 | | $t_{KCY2}$/2 –18 | | $t_{KCY2}$/2 –18 | | ns |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 3.6 V | | $t_{KCY2}$/2 –66 | | $t_{KCY2}$/2 –66 | | $t_{KCY2}$/2 –66 | | ns |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 3.6 V | | – | | $t_{KCY2}$/2 –66 | | $t_{KCY2}$/2 –66 | | ns |
| SIp setup time (to SCKp↑)[Note 5] | $t_{SIK2}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V | | 1/$f_{MCK}$ +20 | | 1/$f_{MCK}$ +30 | | 1/$f_{MCK}$ +30 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 3.6 V | | 1/$f_{MCK}$ +30 | | 1/$f_{MCK}$ +30 | | 1/$f_{MCK}$ +30 | | ns |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 3.6 V | | 1/$f_{MCK}$ +40 | | 1/$f_{MCK}$ +40 | | 1/$f_{MCK}$ +40 | | ns |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 3.6 V | | – | | 1/$f_{MCK}$ +40 | | 1/$f_{MCK}$ +40 | | ns |
| SIp hold time (from SCKp↑)[Note 5] | $t_{KSI2}$ | 1.8 V ≤ $EV_{DD0}$ ≤ 3.6 V | | 1/$f_{MCK}$ +31 | | 1/$f_{MCK}$ +31 | | 1/$f_{MCK}$ +31 | | ns |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 3.6 V | | 1/$f_{MCK}$+ 250 | | 1/$f_{MCK}$+ 250 | | 1/$f_{MCK}$+ 250 | | ns |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 3.6 V | | – | | 1/$f_{MCK}$+ 250 | | 1/$f_{MCK}$+ 250 | | ns |
| Delay time from SCKp↓ to SOp output[Note 6] | $t_{KSO2}$ | C = 30 pF[Note 7] | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V | | 2/$f_{MCK}$ +44 | | 2/$f_{MCK}$ +110 | | 2/$f_{MCK}$ +110 | ns |
| | | | 2.4 V ≤ $EV_{DD0}$ ≤ 3.6 V | | 2/$f_{MCK}$ +75 | | 2/$f_{MCK}$ +110 | | 2/$f_{MCK}$ +110 | ns |
| | | | 1.8 V ≤ $EV_{DD0}$ ≤ 3.6 V | | 2/$f_{MCK}$ +110 | | 2/$f_{MCK}$ +110 | | 2/$f_{MCK}$ +110 | ns |
| | | | 1.7 V ≤ $EV_{DD0}$ ≤ 3.6 V | | 2/$f_{MCK}$ +220 | | 2/$f_{MCK}$ +220 | | 2/$f_{MCK}$ +220 | ns |
| | | | 1.6 V ≤ $EV_{DD0}$ ≤ 3.6 V | | – | | 2/$f_{MCK}$ +220 | | 2/$f_{MCK}$ +220 | ns |

(**Note, Caution** and **Remark** are listed on the next page.)

**(7) Communication at different potential (2.5 V) (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)**

**($T_A$ = –40 to +85°C, 2.7 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS[Note 1] | | LS[Note 2] | | LV[Note 3] | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time | $t_{KCY1}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | $t_{KCY1}$ ≥ 2/$f_{CLK}$ | 300 | | 1150 | | 1150 | | ns |
| SCKp high-level width | $t_{KH1}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 – 120 | | $t_{KCY1}$/2 – 120 | | $t_{KCY1}$/2 – 120 | | ns |
| SCKp low-level width | $t_{KL1}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 – 10 | | $t_{KCY1}$/2 – 50 | | $t_{KCY1}$/2 – 50 | | ns |
| SIp setup time (to SCKp↑)[Note 4] | $t_{SIK1}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | 121 | | 479 | | 479 | | ns |
| SIp hold time (from SCKp↑)[Note 4] | $t_{KSI1}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | 10 | | 10 | | 10 | | ns |
| Delay time from SCKp↓ to SOp output[Note 4] | $t_{KSO1}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | | 130 | | 130 | | 130 | ns |
| SIp setup time (to SCKp↓)[Note 5] | $t_{SIK1}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | 33 | | 110 | | 110 | | ns |
| SIp hold time (from SCKp↓)[Note 5] | $t_{KSI1}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | 10 | | 10 | | 10 | | ns |
| Delay time from SCKp↑ to SOp output[Note 5] | $t_{KSO1}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | | 10 | | 10 | | 10 | ns |

**Notes 1.** HS is condition of HS (high-speed main) mode.
**2.** LS is condition of LS (low-speed main) mode.
**3.** LV is condition of LV (low-voltage main) mode.
**4.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
**5.** When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance (When 25- to 48-pin products)/$EV_{DD}$ tolerance (When 64-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

<R>

**Remarks 1.** $R_b$[Ω]: Communication line (SCKp, SOp) pull-up resistance, $C_b$[F]: Communication line (SCKp, SOp) load capacitance, $V_b$[V]: Communication line voltage
**2.** p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 1)

**(9) Communication at different potential (1.8 V, 2.5 V) (CSI mode) (slave mode, SCKp... external clock input)**
**($T_A$ = –40 to +85°C, 1.8 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS[Note 1] | | LS[Note 2] | | LV[Note 3] | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time[Note 4] | $t_{KCY2}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | 24 MHz < $f_{MCK}$ | 20/$f_{MCK}$ | | – | | – | | ns |
| | | | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 16/$f_{MCK}$ | | – | | – | | ns |
| | | | 16 MHz < $f_{MCK}$ ≤ 20 MHz | 14/$f_{MCK}$ | | – | | – | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 16 MHz | 12/$f_{MCK}$ | | – | | – | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 8/$f_{MCK}$ | | 16/$f_{MCK}$ | | – | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 6/$f_{MCK}$ | | 10/$f_{MCK}$ | | 10/$f_{MCK}$ | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V[Note 5] | 24 MHz < $f_{MCK}$ | 48/$f_{MCK}$ | | – | | – | | ns |
| | | | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 36/$f_{MCK}$ | | – | | – | | ns |
| | | | 16 MHz < $f_{MCK}$ ≤ 20 MHz | 32/$f_{MCK}$ | | – | | – | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 16 MHz | 26/$f_{MCK}$ | | – | | – | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 16/$f_{MCK}$ | | 16/$f_{MCK}$ | | – | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 10/$f_{MCK}$ | | 10/$f_{MCK}$ | | 10/$f_{MCK}$ | | ns |
| SCKp high-/low-level width | $t_{KH2}$, $t_{KL2}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | $t_{KCY2}$/2 – 18 | | $t_{KCY2}$/2 – 50 | | $t_{KCY2}$/2 – 50 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V[Note 5] | | $t_{KCY2}$/2 – 50 | | $t_{KCY2}$/2 – 50 | | $t_{KCY2}$/2 – 50 | | ns |
| SIp setup time (to SCKp↑)[Note 6] | $t_{SIK2}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | 1/$f_{MCK}$ + 20 | | 1/$f_{MCK}$ + 30 | | 1/$f_{MCK}$ + 30 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V[Note 5] | | 1/$f_{MCK}$ + 30 | | 1/$f_{MCK}$ + 30 | | 1/$f_{MCK}$ + 30 | | ns |
| SIp hold time (from SCKp↑)[Note 6] | $t_{KSI2}$ | | | 1/$f_{MCK}$ + 31 | | 1/$f_{MCK}$ + 31 | | 1/$f_{MCK}$ + 31 | | ns |
| Delay time from SCKp↓ to SOp output[Note 7] | $t_{KSO2}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | | 2/$f_{MCK}$ + 214 | | 2/$f_{MCK}$ + 573 | | 2/$f_{MCK}$ + 573 | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V[Note 5], $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | | 2/$f_{MCK}$ + 573 | | 2/$f_{MCK}$ + 573 | | 2/$f_{MCK}$ + 573 | ns |

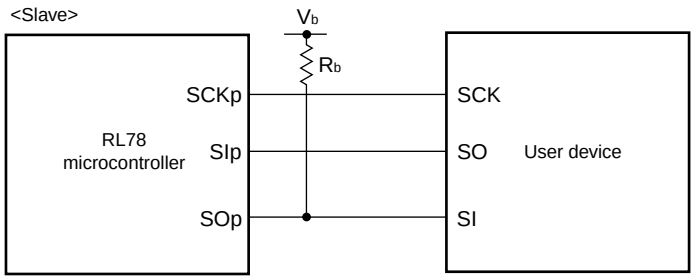
**Notes 1.** HS is condition of HS (high-speed main) mode.
**2.** LS is condition of LS (low-speed main) mode.
**3.** LV is condition of LV (low-voltage main) mode.
**4.** Transfer rate in the SNOOZE mode : MAX. 1 Mbps
**5.** Use it with $EV_{DD0}$ ≥ $V_b$.
**6.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time or SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
**7.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Caution Select the TTL input buffer for the SIp pin and SCKp pin and the N-ch open drain output ($V_{DD}$ tolerance (When 25- to 48-pin products)/$EV_{DD}$ tolerance (When 64-pin products)) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

<R>

(**Remarks** are listed on the next page.)

**CSI mode connection diagram (during communication at different potential)**




**Remarks 1.** $R_b$[Ω]: Communication line (SOp) pull-up resistance, $C_b$[F]: Communication line (SOp) load capacitance, $V_b$[V]: Communication line voltage

**2.** p: CSI number (p = 00, 10, 20), m: Unit number (m = 0, 1), n: Channel number (n = 00, 02, 10), g: PIM and POM number (g = 0, 1)

**3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 02, 10))

**4.** CSI01, CSI11, and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

**(10) Communication at different potential (1.8 V, 2.5 V) (simplified $I^2C$ mode) (1/2)**

**($T_A$ = –40 to +85°C, 1.8 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

| Parameter | Symbol | Conditions | HS[Note 1] | | LS[Note 2] | | LV[Note 3] | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCLr clock frequency | $f_{SCL}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | | 1000[Note 4] | | 300[Note 4] | | 300[Note 4] | kHz |
| | | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | | 400[Note 4] | | 300[Note 4] | | 300[Note 4] | kHz |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V[Note 5], $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | | 300[Note 4] | | 300[Note 4] | | 300[Note 4] | kHz |
| Hold time when SCLr = “L” | $t_{LOW}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 475 | | 1550 | | 1550 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 1150 | | 1550 | | 1550 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V[Note 5], $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 1550 | | 1550 | | 1550 | | ns |
| Hold time when SCLr = “H” | $t_{HIGH}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 200 | | 610 | | 610 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 600 | | 610 | | 610 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V[Note 5], $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 610 | | 610 | | 610 | | ns |

(**Notes**, **Caution** and **Remarks** are listed on the next page.)

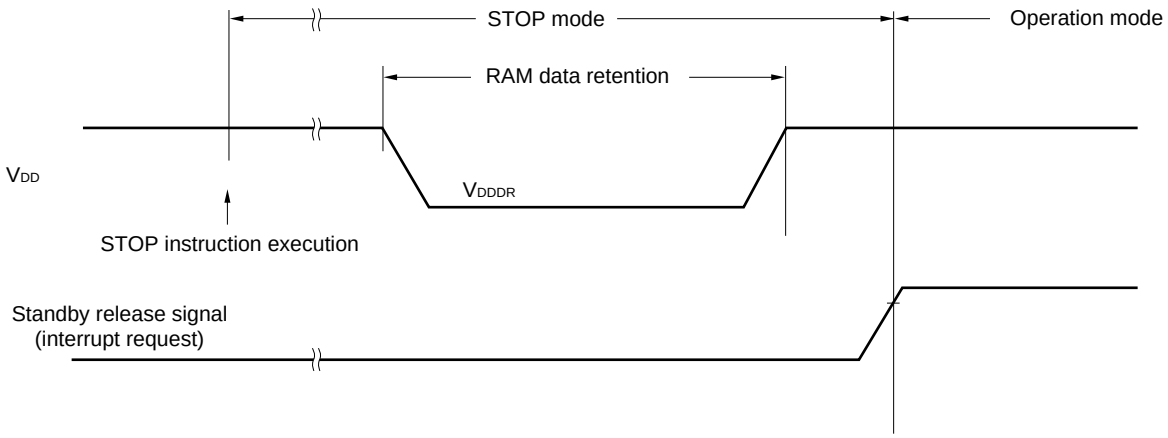
## <R> 2.7 RAM Data Retention Characteristics

<R> **($T_A$ = –40 to +85°C, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Data retention supply voltage | $V_{DDDR}$ | | 1.46 Note | | 3.6 | V |

<R> **Note** This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.

<R>




## <R> 2.8 Flash Memory Programming Characteristics

**($T_A$ = –40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| CPU/peripheral hardware clock frequency | $f_{CLK}$ | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | 1 | | 32 | MHz |
| Number of code flash rewrites Notes 1, 2 | $C_{erwr}$ | Retained for 20 years<br>$T_A$ = 85°C Note 3 | 1,000 | | | Times |
| Number of data flash rewrites Notes 1, 2 | | Retained for 1 years<br>$T_A$ = 25°C Note 3 | | 1,000,000 | | |
| | | Retained for 5 years<br>$T_A$ = 85°C Note 3 | 100,000 | | | |
| | | Retained for 20 years<br>$T_A$ = 85°C Note 3 | 10,000 | | | |

**Notes 1.** 1 erase + 1 write after the erase is regarded as 1 rewrite.
The retaining years are until next rewrite after the rewrite.

**2.** When using flash memory programmer and Renesas Electronics self programming library

**3.** These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

**($T_A$ = –40 to +105°C, 2.4 V ≤ $AV_{DD}$ ≤ $V_{DD}$ ≤ 3.6 V, 2.4 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)** **(5/5)**

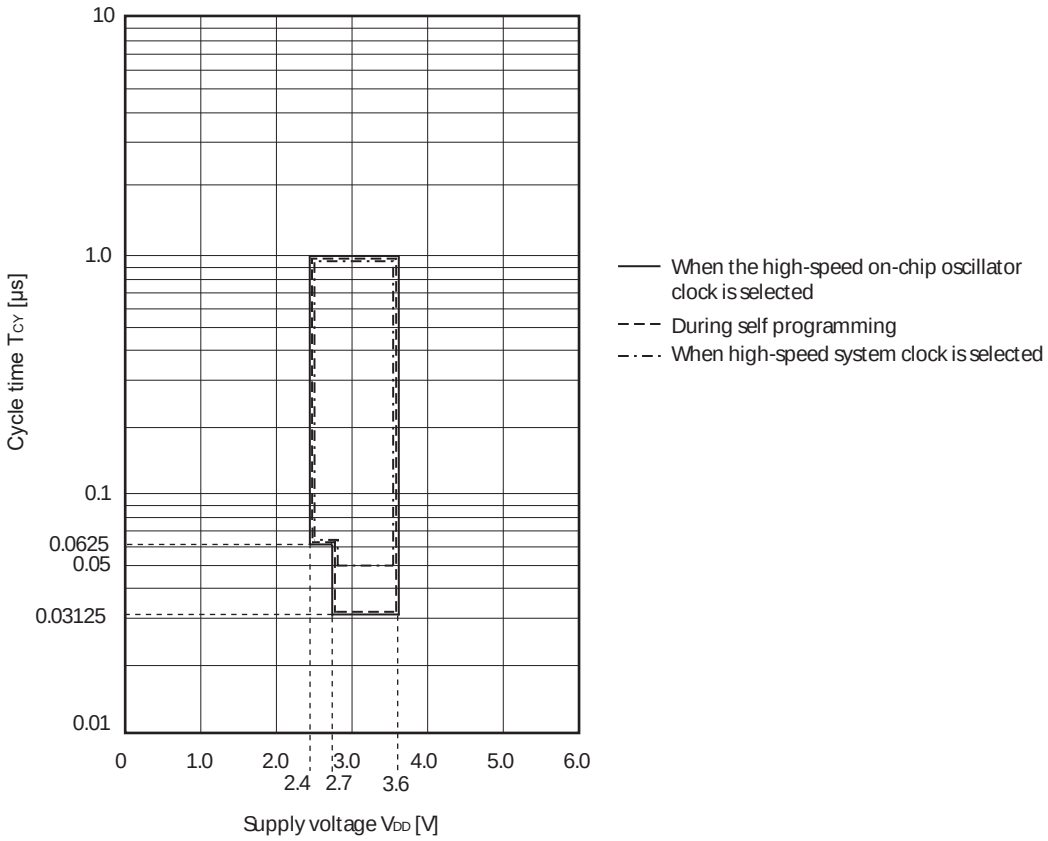
| Items | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Input leakage current, high | $I_{LIH1}$ | P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P60 to P63, P70 to P77, P120, P140, P141 | $V_I$ = $EV_{DD0}$ | | | | 1 | μA |
| | $I_{LIH2}$ | P137, $\overline{\text{RESET}}$ | $V_I$ = $V_{DD}$ | | | | 1 | μA |
| | $I_{LIH3}$ | P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS) | $V_I$ = $V_{DD}$ | In input port or external clock input | | | 1 | μA |
| | | | | In resonator connection | | | 10 | μA |
| | $I_{LIH4}$ | P20 to P27, P150 to P154 | $V_I$ = $AV_{DD}$ | | | | 1 | μA |
| Input leakage current, low | $I_{LIL1}$ | P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P60 to P67, P70 to P77, P120, P140, P141 | $V_I$ = $EV_{SS0}$ | | | | –1 | μA |
| | $I_{LIL2}$ | P137, $\overline{\text{RESET}}$ | $V_I$ = $V_{SS}$ | | | | –1 | μA |
| | $I_{LIL3}$ | P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS) | $V_I$ = $V_{SS}$ | In input port or external clock input | | | –1 | μA |
| | | | | In resonator connection | | | –10 | μA |
| | $I_{LIL4}$ | P20 to P27, P150 to P154 | $V_I$ = $AV_{SS}$ | | | | –1 | μA |
| On-chip pull-up resistance | $R_U$ | P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P140, P141 | $V_I$ = $EV_{SS0}$, In input port | | 10 | 20 | 100 | kΩ |

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**Minimum Instruction Execution Time during Main System Clock Operation**

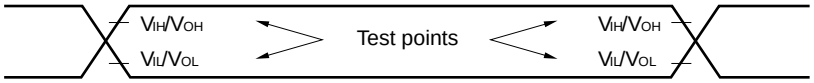
<R>

$T_{CY}$ vs $V_{DD}$ (HS (high-speed main) mode)

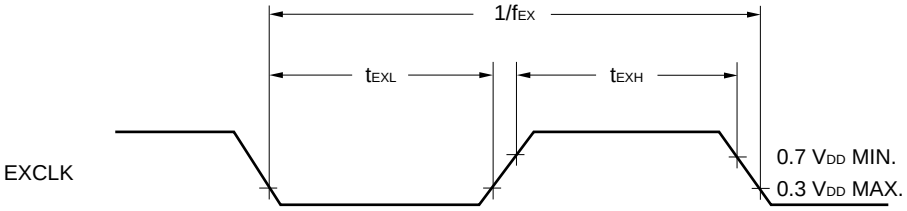


### AC Timing Test Points

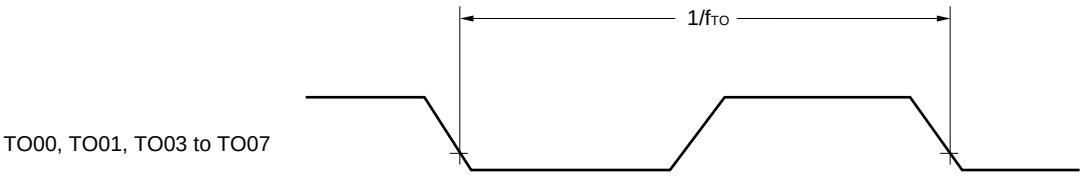
<R>



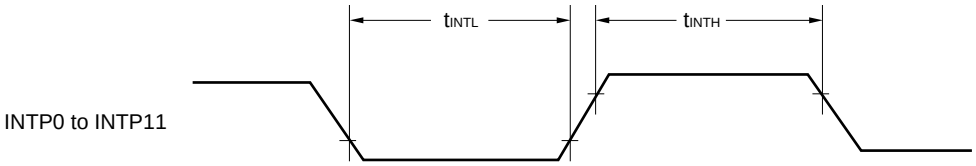

### External System Clock Timing



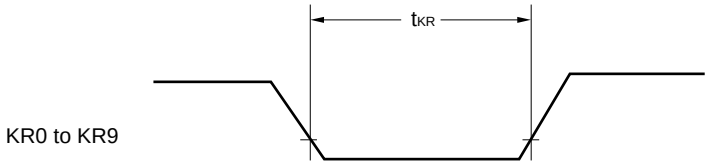

### <R> TI/TO Timing


### Interrupt Request Input Timing




### Key Interrupt Input Timing



<R> **(3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| SCKp cycle time[Note 1] | $t_{KCY2}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V | 16 MHz < $f_{MCK}$ | 16/$f_{MCK}$ | | | ns |
| | | | $f_{MCK}$ ≤ 16 MHz | 12/$f_{MCK}$ | | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 3.6 V | | 12/$f_{MCK}$ and 1000 | | | ns |
| SCKp high-/low-level width | $t_{KH2}$, $t_{KL2}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V | | $t_{KCY2}$/2–14 | | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 3.6 V | | $t_{KCY2}$/2–16 | | | ns |
| SIp setup time (to SCKp↑)[Note 2] | $t_{SIK2}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V | | 1/$f_{MCK}$ + 40 | | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 3.6 V | | 1/$f_{MCK}$ + 60 | | | ns |
| SIp hold time (from SCKp↑)[Note 2] | $t_{KSI2}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V | | 1/$f_{MCK}$+62 | | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 3.6 V | | 1/$f_{MCK}$+62 | | | ns |
| Delay time from SCKp↓ to SOp output[Note 3] | $t_{KSO2}$ | C = 30 pF[Note 4] | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V | | | 2/$f_{MCK}$+66 | ns |
| | | | 2.4 V ≤ $EV_{DD0}$ ≤ 3.6 V | | | 2/$f_{MCK}$+113 | ns |

**Notes 1.** Transfer rate in the SNOOZE mode : MAX. 1 Mbps

**2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time or SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

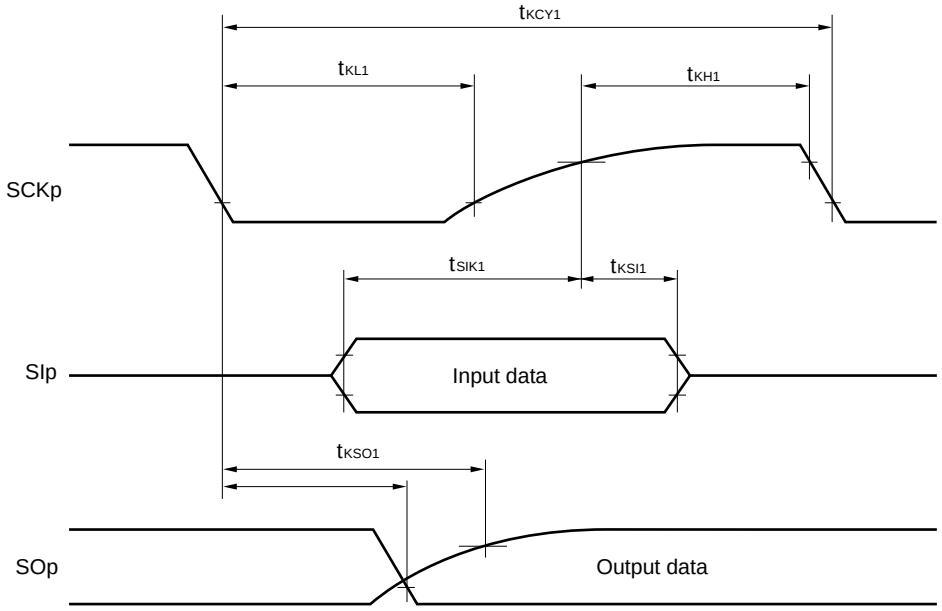
**4.** C is the load capacitance of the SOp output lines.

**Caution Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

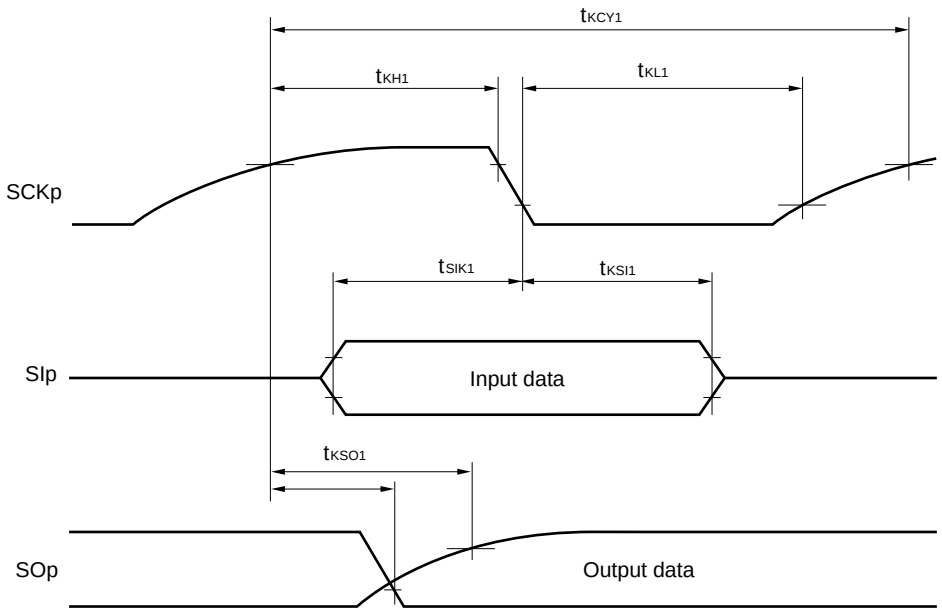
**Remarks 1.** p: CSI number (p = 00, 01, 10, 11, 20, 21), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),
g: PIM number (g = 0, 1)

**2.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

**CSI mode serial transfer timing (master mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**




**CSI mode serial transfer timing (master mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**




**Remarks 1.** p: CSI number (p = 00, 10, 20), m: Unit number, n: Channel number (m = 00, 02, 10), g: PIM and POM number (g = 0, 1)

**2.** CSI01, CSI11, and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

**(8) Communication at different potential (1.8 V, 2.5 V) (simplified $I^2C$ mode) (1/2)**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | MAX. | Unit |
|---|---|---|---|---|---|
| SCLr clock frequency | $f_{SCL}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | | 400 Note 1 | kHz |
| | | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | | 100 Note 1 | kHz |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | | 100 Note 1 | kHz |
| Hold time when SCLr = “L” | $t_{LOW}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 1200 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 4600 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 4650 | | ns |
| Hold time when SCLr = “H” | $t_{HIGH}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 500 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 2400 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 1830 | | ns |

(**Notes**, **Caution** and **Remarks** are listed on the next page.)

<R> **(3) When reference voltage (+) = $AV_{REFP}$/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = $AV_{REFM}$/ANI1 (ADREFM = 1), target for conversion: ANI16 to ANI30, interanal reference voltage, temperature sensor output voltage**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 3.6 V, 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = $EV_{SS0}$ = 0 V, $AV_{SS}$ = 0 V, Reference voltage (+) = $AV_{REFP}$, Reference voltage (–) = $AV_{REFM}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | $R_{ES}$ | | 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | 8 | | 12 | bit |
| Overall error[Note 1] | AINL | 12-bit resolution | 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±7.0 | LSB |
| Conversion time | $t_{CONV}$ | ADTYP = 0, 12-bit resolution | 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | 4.125 | | | μs |
| Zero-scale error[Note 1] | $E_{ZS}$ | 12-bit resolution | 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±5.0 | LSB |
| Full-scale error[Note 1] | $E_{FS}$ | 12-bit resolution | 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±5.0 | LSB |
| Integral linearity error[Note 1] | ILE | 12-bit resolution | 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±3.0 | LSB |
| Differential linearity error[Note 1] | DLE | 12-bit resolution | 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±2.0 | LSB |
| Analog input voltage | $V_{AIN}$ | | | 0. | | $AV_{REFP}$ and $EV_{DD0}$ | V |
| | | Interanal reference voltage (2.4 V ≤ $V_{DD}$ ≤ 3.6 V, HS (high-speed main) mode) | | $V_{BGR}$[Note 2] | | | V |
| | | Temperature sensor output voltage (2.4 V ≤ $V_{DD}$ ≤ 3.6 V, HS (high-speed main) mode) | | $V_{TMPS25}$[Note 2] | | | V |

**Notes 1.** Excludes quantization error (±1/2 LSB).

**2.** See **3.6.2 Temperature sensor, internal reference voltage output characteristics**.

# 4. PACKAGE DRAWINGS

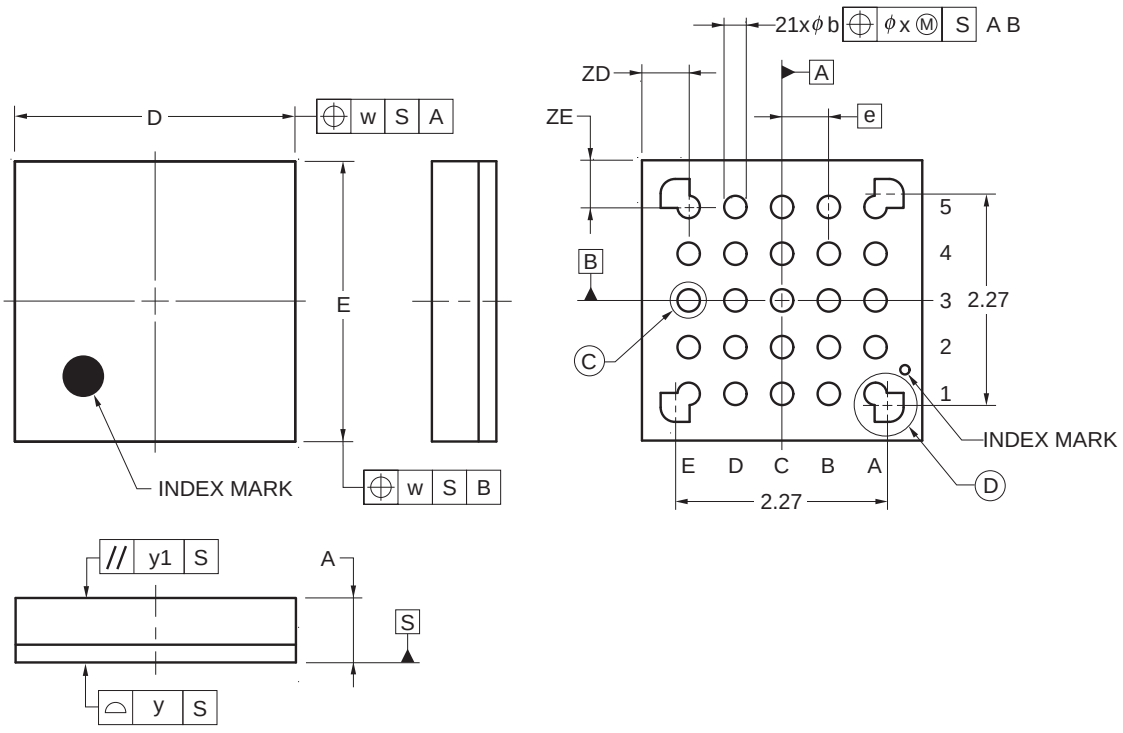
## 4.1 25-pin products

R5F10E8AALA, R5F10E8CALA, R5F10E8DALA, R5F10E8EALA

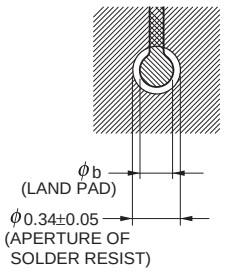
<R>

| JEITA Package Code | RENESAS Code | Previous Code | MASS (Typ) [g] |
|---|---|---|---|
| P-WFLGA25-3x3-0.50 | PWLG0025KA-A | P25FC-50-2N2-3 | 0.01 |

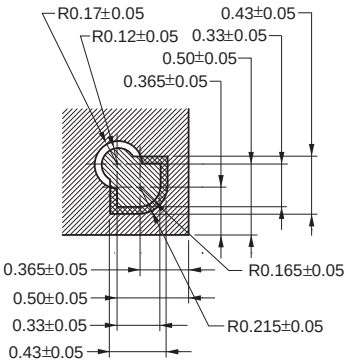
Unit: mm




DETAIL OF Ⓒ PART




DETAIL OF Ⓓ PART




| ITEM | DIMENSIONS |
|---|---|
| D | 3.00±0.10 |
| E | 3.00±0.10 |
| w | 0.20 |
| e | 0.50 |
| A | 0.69±0.07 |
| b | 0.24±0.05 |
| x | 0.05 |
| y | 0.08 |
| y1 | 0.20 |
| ZD | 0.50 |
| ZE | 0.50 |