Renesas Electronics America Inc - R5F10ELEGFB#X0 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	46
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 28x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10elegfb-x0

- 64-pin plastic VFBGA (4 × 4 mm, 0.4 mm pitch)

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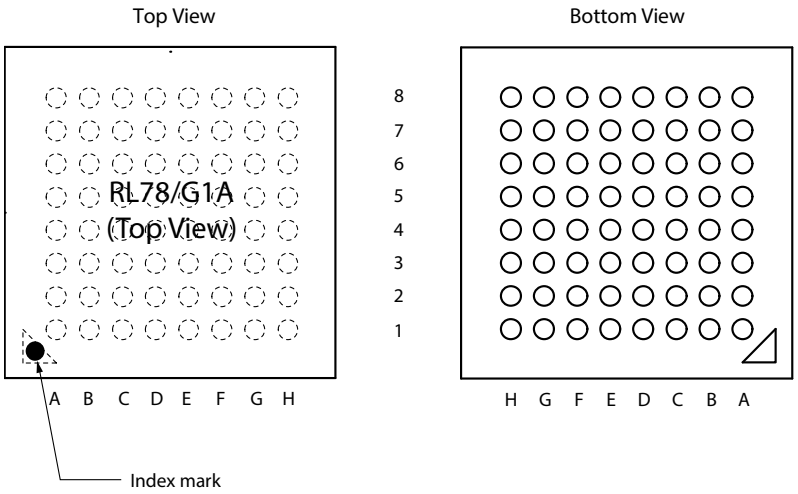


Pin No.	Name	Pin No.	Name	Pin No.	Name	Pin No.	Name
A1	P05/TI05/TO05/KR8	C1	P51/ANI25/SO11 /INTP2	E1	P153/ANI11/(KR8)	G1	AV_{DD}
A2	P30/ANI27/SCK11 /SCL11/INTP3 /RTC1HZ	C2	P71/SI21/SDA21/KR1	E2	P154/ANI12/(KR9)	G2	P25/ANI5/(KR8)
A3	P70/ANI28/SCK21 /SCL21/KR0	C3	P74/SI01/SDA01 /INTP8/KR4	E3	P10/ANI18/SCK00 /SCL00/(KR0)	G3	P24/ANI4/(KR7)
A4	P75/SCK01/SCL01 /INTP9/KR5	C4	P16/TI01/TO01/INTP5	E4	P11/ANI20/SI00 /SDA00/RxD0 /TOOLRxD/(KR1)	G4	P22/ANI2/(KR5)
A5	P77/INTP11/KR7	C5	P15/ANI24/SCK20 /SCL20/(KR5)	E5	P03/ANI16/SI10 /SDA10/RxD1/(KR3)	G5	P130
A6	P61/SDAA0	C6	P63	E6	P41/ANI30/TI07/TO07	G6	P02/ANI17/SO10/TxD1 /(KR2)
A7	P60/SCLA0	C7	V_{SS}	E7	$\overline{RESET}$	G7	P00/TI00/(KR0)
A8	EV_{DD0}	C8	P121/X1	E8	P137/INTP0	G8	P124/XT2/EXCLKS
B1	P50/ANI26 /SI11 /SDA11/INTP1	D1	P13/ANI22/SO20 /TxD2/(KR3)	F1	P150/ANI8	H1	AV_{SS}
B2	P72/SO21/KR2	D2	P06/TI06/TO06/KR9	F2	P151/ANI9/(KR6)	H2	P27/ANI7
B3	P73/SO01/KR3	D3	P12/ANI21/SO00 /TxD0/TOOLTxD/(KR2)	F3	P152/ANI10/(KR7)	H3	P26/ANI6/(KR9)
B4	P76/INTP10/KR6	D4	P14/ANI23/SI20/ SDA20/RxD2/(KR4)	F4	$P21/ANI1/AV_{REFM}$	H4	P23/ANI3/(KR6)
B5	P31/ANI29/TI03/TO03 /INTP4	D5	P42/TI04/TO04	F5	P04/SCK10/SCL10 /(KR4)	H5	$P20/ANI0/AV_{REFP}$
B6	P62	D6	P40/TOOL0	F6	P43	H6	P141/PCLBUZ1/INTP7
B7	V_{DD}	D7	REGC	F7	P01/TO00/(KR1)	H7	P140/PCLBUZ0/INTP6
B8	EV_{SS0}	D8	P122/X2/EXCLK	F8	P123/XT1	H8	P120/ANI19

Cautions 1. Make EV_{SS0} pin the same potential as V_{SS} pin.

2. Make V_{DD} pin the potential that is higher than EV_{DD0} pin.

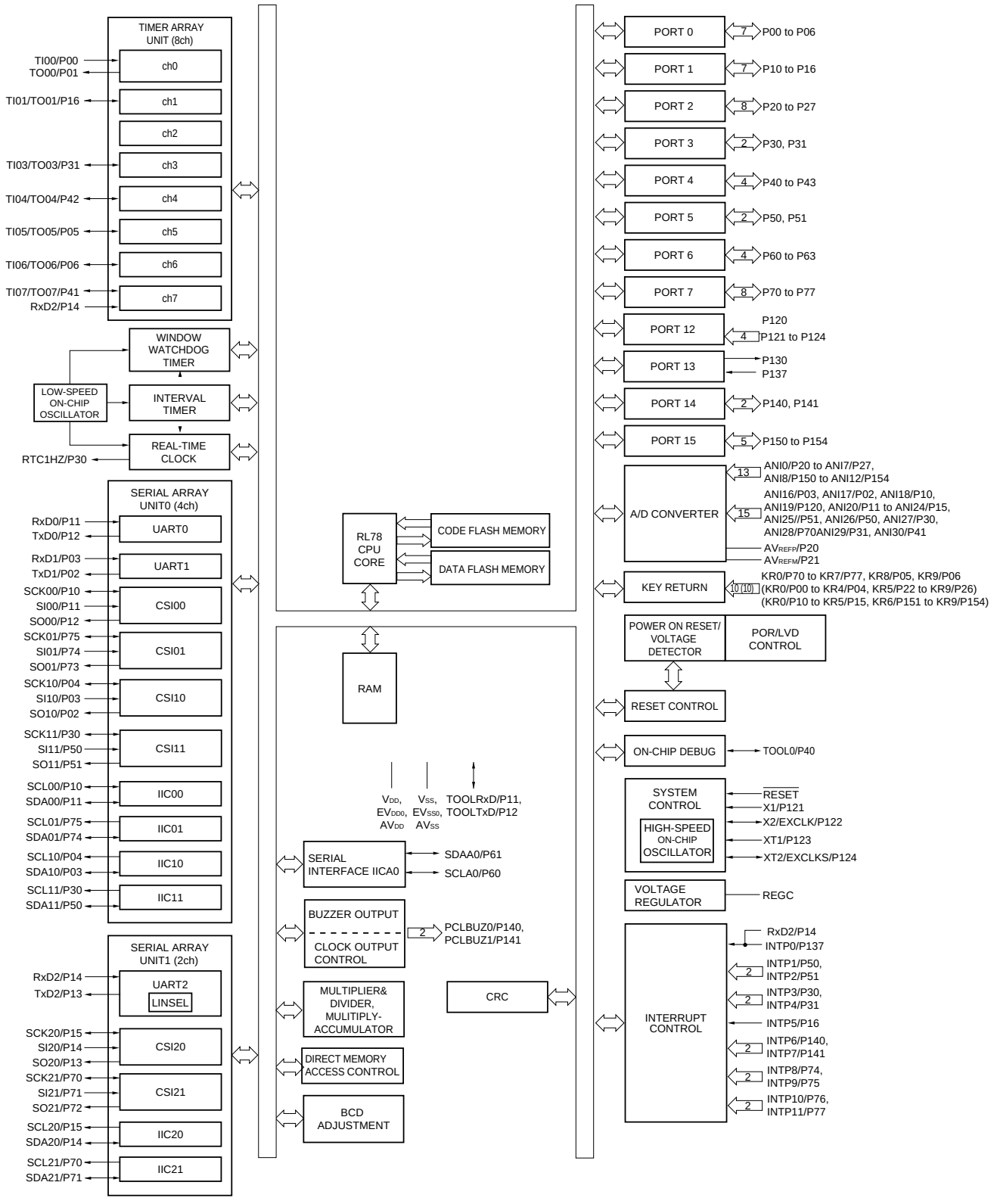
3. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification.**

2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD} and EV_{DD0} pins and connect the V_{SS} and EV_{SS0} pins to separate ground lines.

3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.5.4 64-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

<R> **(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)** **(3/3)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	I_{FIL} Note 1				0.20		μA
RTC operating current	I_{RTC} Notes 1, 2, 3				0.02		μA
12-bit interval timer operating current	I_{IT} Notes 1, 2, 4				0.02		μA
Watchdog timer operating current	I_{WDT} Notes 1, 2, 5	f_{IL} = 15 kHz			0.22		μA
A/D converter operating current	I_{ADC} Notes 6, 7	AV_{DD} = 3.0 V, When conversion at maximum speed			420	720	μA
$AV_{REF(+)}$ current	I_{AVREF} Note 8	AV_{DD} = 3.0 V, ADREFP1 = 0, ADREFP0 = 0 Note 7			14.0	25.0	μA
		AV_{REFP} = 3.0 V, ADREFP1 = 0, ADREFP0 = 1 Note 10			14.0	25.0	μA
		ADREFP1 = 1, ADREFP0 = 0 Note 1			14.0	25.0	μA
A/D converter reference voltage current	I_{ADREF} Notes 1, 9	V_{DD} = 3.0 V			75.0		μA
Temperature sensor operating current	I_{TMP} Note 1	V_{DD} = 3.0 V			75.0		μA
LVD operating current	I_{LVD} Notes 1, 11				0.08		μA
BGO operating current	I_{BGO} Notes 1, 12				2.5	12.2	mA
Self-programming operating current	I_{FSP} Notes 1, 13				2.5	12.2	mA
SNOOZE operating current	I_{SNOZ}	A/D converter operation (AV_{DD} = 3.0 V)	The mode is performed Notes 1, 14		0.50	0.60	mA
			During A/D conversion Note 1		0.60	0.75	mA
			During A/D conversion Note 7		420	720	μA
		CSI/UART operation Note 1			0.70	0.84	mA

(**Notes** and **Remarks** are listed on the next page.)

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)

(T_A = –40 to +85°C, 2.7 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions		HS[Note 1]		LS[Note 2]		LV[Note 3]		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	2.7 V ≤ EV_{DD} ≤ 3.6 V	t_{KCY1} ≥ 2/f_{CLK}	83.3		250		500		ns
SCKp high-/low-level width	t_{KH1}, t_{KL1}	2.7 V ≤ EV_{DD} ≤ 3.6 V		t_{KCY1}/2 –10		t_{KCY1}/2 –50		t_{KCY1}/2 –50		ns
SIp setup time (to SCKp↑)[Note 4]	t_{SIK1}	2.7 V ≤ EV_{DD} ≤ 3.6 V		33		110		110		ns
SIp hold time (from SCKp↑)[Note 4]	t_{KSI1}	2.7 V ≤ EV_{DD} ≤ 3.6 V		10		10		10		ns
Delay time from SCKp↓ to SOp output[Note 5]	t_{KSO1}	C = 20 pF[Note 6]			10		10		10	ns

Notes 1. HS is condition of HS (high-speed main) mode.

2. LS is condition of LS (low-speed main) mode.

3. LV is condition of LV (low-voltage main) mode.

4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time or SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

5. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

6. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM numbers (g = 1)

2. f_{MCK}: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions		HS[Note 1]		LS[Note 2]		LV[Note 3]		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time[Note 4]	t_{KCY2}	2.7 V ≤ EV_{DD0} ≤ 3.6 V	16 MHz < f_{MCK}	8/f_{MCK}		–		–		ns
			f_{MCK} ≤ 16 MHz	6/f_{MCK}		6/f_{MCK}		6/f_{MCK}		ns
		2.4 V ≤ EV_{DD0} ≤ 3.6 V		6/f_{MCK} and 500ns		6/f_{MCK} and 500ns		6/f_{MCK} and 500ns		ns
		1.8 V ≤ EV_{DD0} ≤ 3.6 V		6/f_{MCK} and 750ns		6/f_{MCK} and 750ns		6/f_{MCK} and 750ns		ns
		1.7 V ≤ EV_{DD0} ≤ 3.6 V		6/f_{MCK} and 1500ns		6/f_{MCK} and 1500ns		6/f_{MCK} and 1500ns		ns
		1.6 V ≤ EV_{DD0} ≤ 3.6 V		–		6/f_{MCK} and 1500ns		6/f_{MCK} and 1500ns		ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	2.7 V ≤ EV_{DD} ≤ 3.6 V		t_{KCY2}/2 –8		t_{KCY2}/2 –8		t_{KCY2}/2 –8		ns
		1.8 V ≤ EV_{DD0} ≤ 3.6 V		t_{KCY2}/2 –18		t_{KCY2}/2 –18		t_{KCY2}/2 –18		ns
		1.7 V ≤ EV_{DD0} ≤ 3.6 V		t_{KCY2}/2 –66		t_{KCY2}/2 –66		t_{KCY2}/2 –66		ns
		1.6 V ≤ EV_{DD0} ≤ 3.6 V		–		t_{KCY2}/2 –66		t_{KCY2}/2 –66		ns
SIp setup time (to SCKp↑)[Note 5]	t_{SIK2}	2.7 V ≤ EV_{DD0} ≤ 3.6 V		1/f_{MCK} +20		1/f_{MCK} +30		1/f_{MCK} +30		ns
		1.8 V ≤ EV_{DD0} ≤ 3.6 V		1/f_{MCK} +30		1/f_{MCK} +30		1/f_{MCK} +30		ns
		1.7 V ≤ EV_{DD0} ≤ 3.6 V		1/f_{MCK} +40		1/f_{MCK} +40		1/f_{MCK} +40		ns
		1.6 V ≤ EV_{DD0} ≤ 3.6 V		–		1/f_{MCK} +40		1/f_{MCK} +40		ns
SIp hold time (from SCKp↑)[Note 5]	t_{KSI2}	1.8 V ≤ EV_{DD0} ≤ 3.6 V		1/f_{MCK} +31		1/f_{MCK} +31		1/f_{MCK} +31		ns
		1.7 V ≤ EV_{DD0} ≤ 3.6 V		1/f_{MCK}+ 250		1/f_{MCK}+ 250		1/f_{MCK}+ 250		ns
		1.6 V ≤ EV_{DD0} ≤ 3.6 V		–		1/f_{MCK}+ 250		1/f_{MCK}+ 250		ns
Delay time from SCKp↓ to SOp output[Note 6]	t_{KSO2}	C = 30 pF[Note 7]	2.7 V ≤ EV_{DD0} ≤ 3.6 V		2/f_{MCK} +44		2/f_{MCK} +110		2/f_{MCK} +110	ns
			2.4 V ≤ EV_{DD0} ≤ 3.6 V		2/f_{MCK} +75		2/f_{MCK} +110		2/f_{MCK} +110	ns
			1.8 V ≤ EV_{DD0} ≤ 3.6 V		2/f_{MCK} +110		2/f_{MCK} +110		2/f_{MCK} +110	ns
			1.7 V ≤ EV_{DD0} ≤ 3.6 V		2/f_{MCK} +220		2/f_{MCK} +220		2/f_{MCK} +220	ns
			1.6 V ≤ EV_{DD0} ≤ 3.6 V		–		2/f_{MCK} +220		2/f_{MCK} +220	ns

(**Note, Caution** and **Remark** are listed on the next page.)

Notes 1. HS is condition of HS (high-speed main) mode.

2. LS is condition of LS (low-speed main) mode.

3. LV is condition of LV (low-voltage main) mode.

4. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

5. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time or SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

6. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

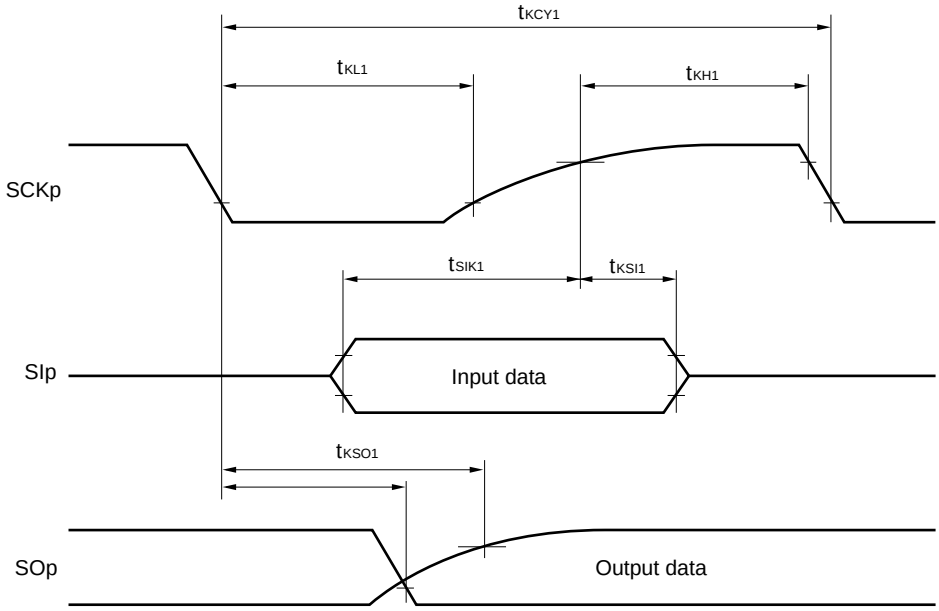
7. C is the load capacitance of the SOp output lines.

Caution Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

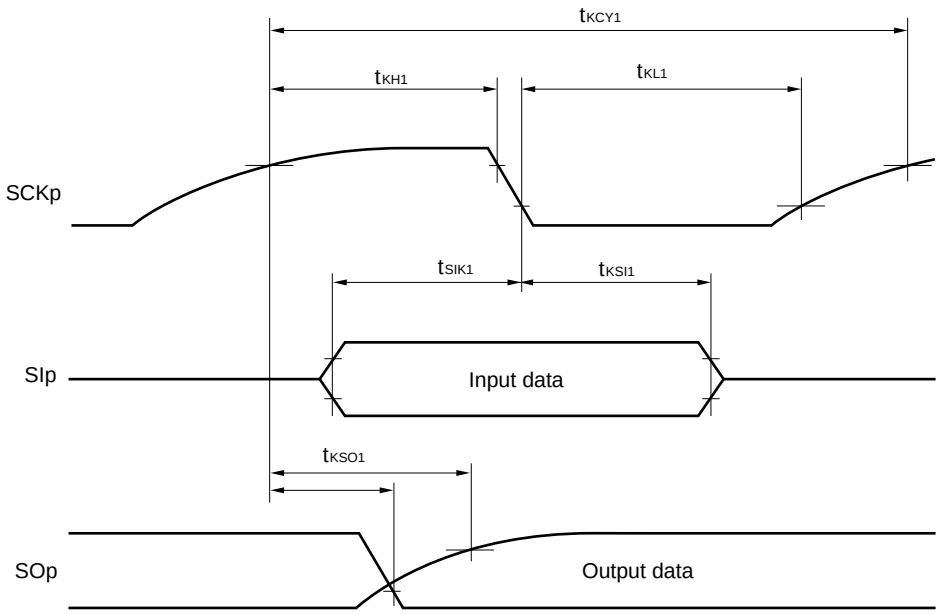
Remarks 1. p: CSI number (p = 00, 01, 10, 11, 20, 21), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),
g: PIM number (g = 0, 1)

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



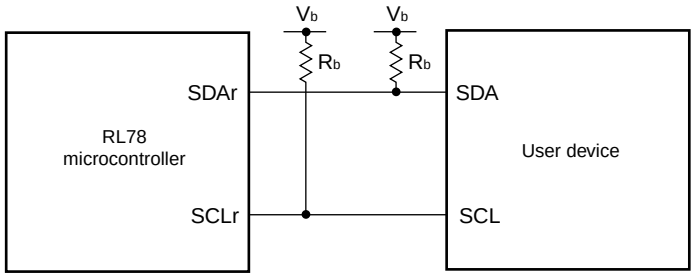
CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



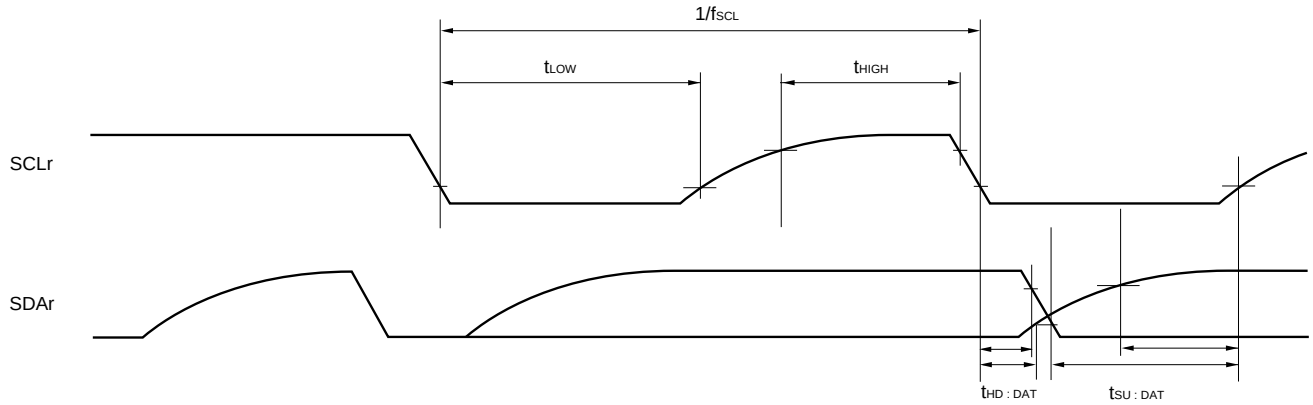
Remarks 1. p: CSI number (p = 00, 10, 20), m: Unit number, n: Channel number (m = 00, 02, 10), g: PIM and POM number (g = 0, 1)

2. CSI01, CSI11, and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

Simplified I²C mode connection diagram (during communication at different potential)



Simplified I²C mode serial transfer timing (during communication at different potential)



Remarks 1. R_b[Ω]: Communication line (SDAr, SCLr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance, V_b[V]: Communication line voltage

2. r: IIC number (r = 00, 10, 20), g: PIM, POM number (g = 0, 1)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 02, 10)

4. IIC01, IIC11, and IIC21 cannot communicate at different potential. Use IIC00, IIC10, or IIC20 for communication at different potential.

2.5.2 Serial interface IICA

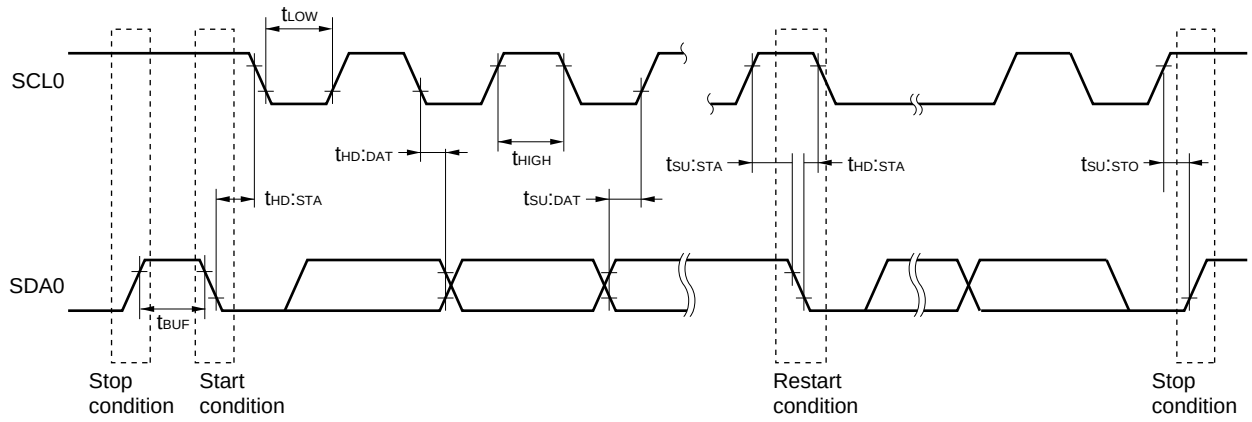
(1) I^2C standard mode

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions	Standard Mode[Note 1]						Unit
			HS[Note 2]		LS[Note 3]		LV[Note 4]		
			MIN.	MAX.	MIN.	MIN.	MAX.	MIN.	
SCLA0 clock frequency	f_{SCL}	2.7 V ≤ EV_{DD0} ≤ 3.6 V	0	100	0	100	0	100	kHz
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	0	100	0	100	0	100	
		1.7 V ≤ EV_{DD0} ≤ 3.6 V	0	100	0	100	0	100	
		1.6 V ≤ EV_{DD0} ≤ 3.6 V	–		0	100	0	100	
Setup time of restart condition	$t_{SU:STA}$	2.7 V ≤ EV_{DD0} ≤ 3.6 V	4.7		4.7		4.7		μs
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	4.7		4.7		4.7		
		1.7 V ≤ EV_{DD0} ≤ 3.6 V	4.7		4.7		4.7		
		1.6 V ≤ EV_{DD0} ≤ 3.6 V	–		4.7		4.7		
Hold time[Note 5]	$t_{HD:STA}$	2.7 V ≤ EV_{DD0} ≤ 3.6 V	4.0		4.0		4.0		μs
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	4.0		4.0		4.0		
		1.7 V ≤ EV_{DD0} ≤ 3.6 V	4.0		4.0		4.0		
		1.6 V ≤ EV_{DD0} ≤ 3.6 V	–		4.0		4.0		
Hold time when SCLA0 = “L”	t_{LOW}	2.7 V ≤ EV_{DD0} ≤ 3.6 V	4.7		4.7		4.7		μs
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	4.7		4.7		4.7		
		1.7 V ≤ EV_{DD0} ≤ 3.6 V	4.7		4.7		4.7		
		1.6 V ≤ EV_{DD0} ≤ 3.6 V	–		4.7		4.7		
Hold time when SCLA0 = “H”	t_{HIGH}	2.7 V ≤ EV_{DD0} ≤ 3.6 V	4.0		4.0		4.0		μs
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	4.0		4.0		4.0		
		1.7 V ≤ EV_{DD0} ≤ 3.6 V	4.0		4.0		4.0		
		1.6 V ≤ EV_{DD0} ≤ 3.6 V	–		4.0		4.0		
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ EV_{DD0} ≤ 3.6 V	250		250		250		ns
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	250		250		250		
		1.7 V ≤ EV_{DD0} ≤ 3.6 V	250		250		250		
		1.6 V ≤ EV_{DD0} ≤ 3.6 V	–		250		250		
Data hold time (transmission)[Note 6]	$t_{HD:DAT}$	2.7 V ≤ EV_{DD0} ≤ 3.6 V	0	3.45	0	3.45	0	3.45	μs
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	0	3.45	0	3.45	0	3.45	
		1.7 V ≤ EV_{DD0} ≤ 3.6 V	0	3.45	0	3.45	0	3.45	
		1.6 V ≤ EV_{DD0} ≤ 3.6 V	–	–	0	3.45	0	3.45	
Setup time of stop condition	$t_{SU:STO}$	2.7 V ≤ EV_{DD0} ≤ 3.6 V	4.0		4.0		4.0		μs
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	4.0		4.0		4.0		
		1.7 V ≤ EV_{DD0} ≤ 3.6 V	4.0		4.0		4.0		
		1.6 V ≤ EV_{DD0} ≤ 3.6 V	–		4.0		4.0		
Bus-free time	t_{BUF}	2.7 V ≤ EV_{DD0} ≤ 3.6 V	4.7		4.7		4.7		μs
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	4.7		4.7		4.7		
		1.7 V ≤ EV_{DD0} ≤ 3.6 V	4.7		4.7		4.7		
		1.6 V ≤ EV_{DD0} ≤ 3.6 V	–		4.7		4.7		

(**Note** and **Remark** are listed on the next page.)

IICA serial transfer timing



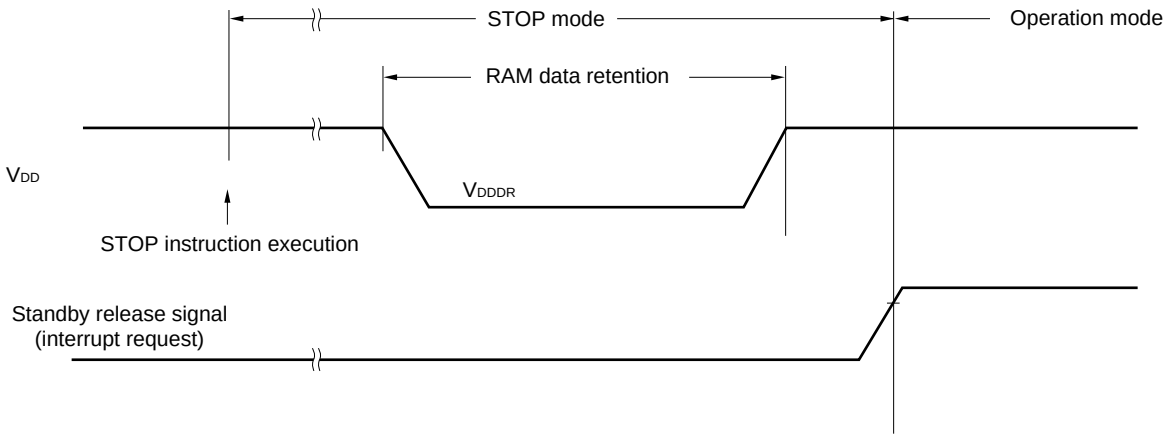
<R> 2.7 RAM Data Retention Characteristics

<R> **(T_A = –40 to +85°C, V_{SS} = 0 V)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.46 Note		3.6	V

<R> **Note** This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.

<R>



<R> 2.8 Flash Memory Programming Characteristics

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CPU/peripheral hardware clock frequency	f_{CLK}	1.8 V ≤ V_{DD} ≤ 3.6 V	1		32	MHz
Number of code flash rewrites Notes 1, 2	C_{erwr}	Retained for 20 years T_A = 85°C Note 3	1,000			Times
Number of data flash rewrites Notes 1, 2		Retained for 1 years T_A = 25°C Note 3		1,000,000		
		Retained for 5 years T_A = 85°C Note 3	100,000			
		Retained for 20 years T_A = 85°C Note 3	10,000			

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite.
The retaining years are until next rewrite after the rewrite.

2. When using flash memory programmer and Renesas Electronics self programming library

3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

2.9 Dedicated Flash Memory Programmer Communication (UART)

(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

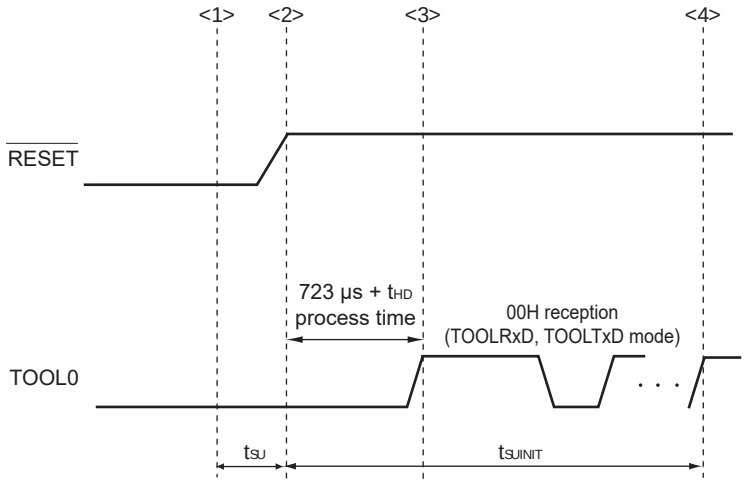
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During flash memory programming	115.2 k		1 M	bps

2.10 Timing Specs for Switching Flash Memory Programming Modes

(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
How long from when an external reset ends until the initial communication settings are specified	t_{SUINIT}	POR and LVD reset must end before the external reset ends.			100	ms
How long from when the TOOL0 pin is placed at the low level until a external reset ends	t_{SU}	POR and LVD reset must end before the external reset ends.	10			μs
<R> How long the TOOL0 pin must be kept at the low level after an external reset ends (except flash firmware processing time)	t_{HD}	POR and LVD reset must end before the external reset ends.	1			ms

<R>



<1> The low level is input to the TOOL0 pin.
<2> The pins reset ends (POR and LVD reset must end before the external reset ends.).
<3> The TOOL0 pin is set to the high level.
<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t_{SUINIT}: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the resets end.

t_{SU}: How long from when the TOOL0 pin is placed at the low level until a external reset ends

<R> t_{HD}: How long to keep the TOOL0 pin at the low level from when the external resets end (except flash firmware processing time)

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V) **(2/3)**

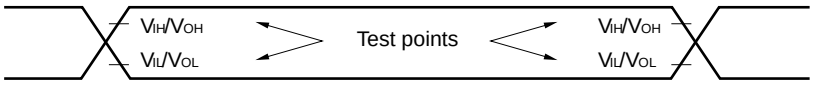
Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current[Note 1]	I_{DD2}[Note 2]	HALT mode	HS (high-speed main) mode[Note 7]	f_{IH} = 32 MHz[Note 4]	V_{DD} = 3.0 V		0.54	2.90	mA
				f_{IH} = 24 MHz[Note 4]	V_{DD} = 3.0 V		0.44	2.30	mA
				f_{IH} = 16 MHz[Note 4]	V_{DD} = 3.0 V		0.40	1.70	mA
			HS (high-speed main) mode[Note 7]	f_{MX} = 20 MHz[Note 3], V_{DD} = 3.0 V	Square wave input		0.28	1.90	mA
					Resonator connection		0.45	2.00	
				f_{MX} = 10 MHz[Note 3], V_{DD} = 3.0 V	Square wave input		0.19	1.02	mA
					Resonator connection		0.26	1.10	
			Subsystem clock mode	f_{SUB} = 32.768 kHz[Note 5] T_A = –40°C	Square wave input		0.25	0.57	μA
					Resonator connection		0.44	0.76	
				f_{SUB} = 32.768 kHz[Note 5] T_A = +25°C	Square wave input		0.30	0.57	μA
					Resonator connection		0.49	0.76	
				f_{SUB} = 32.768 kHz[Note 5] T_A = +50°C	Square wave input		0.38	1.17	μA
					Resonator connection		0.57	1.36	
				f_{SUB} = 32.768 kHz[Note 5] T_A = +70°C	Square wave input		0.52	1.97	μA
					Resonator connection		0.71	2.16	
				f_{SUB} = 32.768 kHz[Note 5] T_A = +85°C	Square wave input		0.97	3.37	μA
					Resonator connection		1.16	3.56	
				f_{SUB} = 32.768 kHz[Note 5] T_A = +105°C	Square wave input		3.01	15.37	μA
					Resonator connection		3.20	15.56	
	I_{DD3}[Note 6]	STOP mode[Note 8]	T_A = –40°C				0.16	0.50	μA
			T_A = +25°C				0.23	0.50	
			T_A = +50°C				0.34	1.10	
			T_A = +70°C				0.46	1.90	
			T_A = +85°C				0.75	3.30	
			T_A = +105°C				2.94	15.30	

(**Notes** and **Remarks** are listed on the next page.)

3.5 Peripheral Functions Characteristics

AC Timing Test Points

<R>



3.5.1 Serial array unit

(1) During communication at same potential (UART mode) (dedicated baud rate generator output)
(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

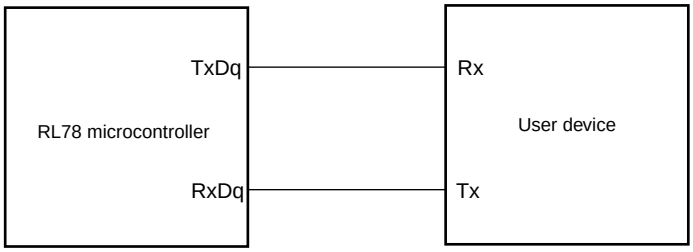
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate[Note 1]					f_{MCK}/12	bps
		Theoretical value of the maximum transfer rate f_{CLK} = 32 MHz, f_{MCK} = f_{CLK}			2.6[Note 2]	Mbps

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps.

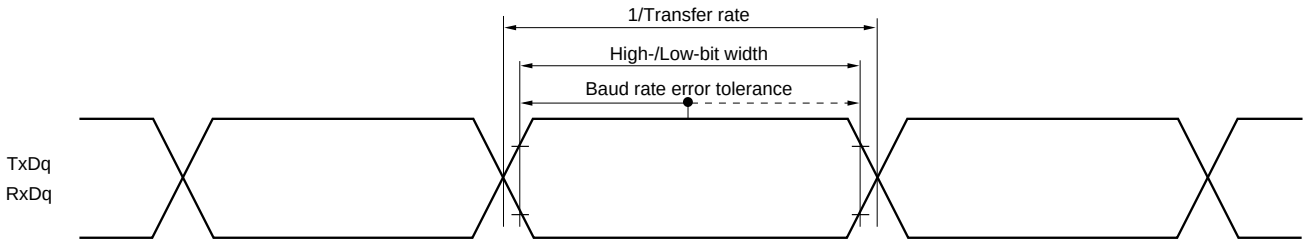
2. The following conditions are required for low-voltage interface when EV_{DD0} < V_{DD}.
2.4 V ≤ EV_{DD0} < 2.7 V : MAX. 1.3 Mbps

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

UART mode connection diagram (during communication at same potential)



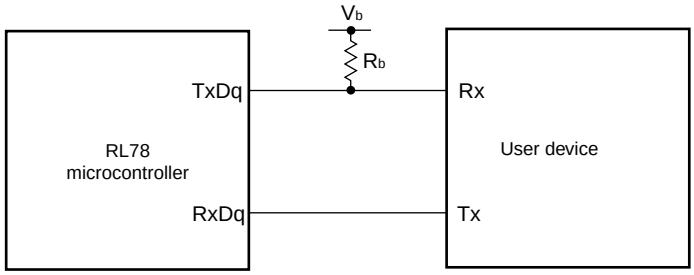
UART mode bit width (during communication at same potential) (reference)



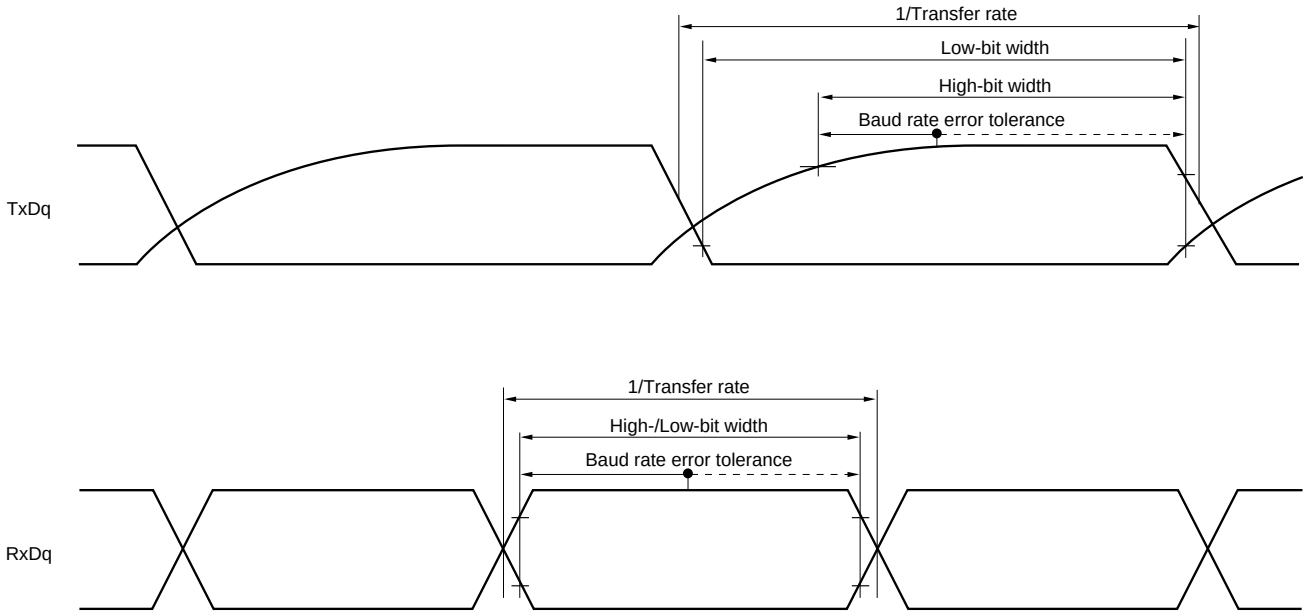
Remarks 1. q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1)

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

UART mode connection diagram (during communication at different potential)



UART mode bit width (during communication at different potential) (reference)



Remarks 1. R_b[Ω]: Communication line (TxDq) pull-up resistance,
C_b[F]: Communication line (TxDq) load capacitance, V_b[V]: Communication line voltage

2. q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1)

3. f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).

m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

(7) Communication at different potential (1.8 V, 2.5 V) (CSI mode) (slave mode, SCKp... external clock input)
(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCKp cycle time[Note 1]	t_{KCY2}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V	24 MHz < f_{MCK}	40/f_{MCK}			ns
			20 MHz < f_{MCK} ≤ 24 MHz	32/f_{MCK}			ns
			16 MHz < f_{MCK} ≤ 20 MHz	28/f_{MCK}			ns
			8 MHz < f_{MCK} ≤ 16 MHz	24/f_{MCK}			ns
			4 MHz < f_{MCK} ≤ 8 MHz	16/f_{MCK}			ns
			f_{MCK} ≤ 4 MHz	12/f_{MCK}			ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V	24 MHz < f_{MCK}	96/f_{MCK}			ns
			20 MHz < f_{MCK} ≤ 24 MHz	72/f_{MCK}			ns
			16 MHz < f_{MCK} ≤ 20 MHz	64/f_{MCK}			ns
			8 MHz < f_{MCK} ≤ 16 MHz	52/f_{MCK}			ns
			4 MHz < f_{MCK} ≤ 8 MHz	32/f_{MCK}			ns
			f_{MCK} ≤ 4 MHz	20/f_{MCK}			ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V		t_{KCY2}/2 – 36			ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V		t_{KCY2}/2 – 100			ns
SIp setup time (to SCKp↑)[Note 2]	t_{SIK2}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V		1/f_{MCK} + 40			ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V		1/f_{MCK} + 60			
SIp hold time (from SCKp↑)[Note 2]	t_{KSI2}			1/f_{MCK} + 62			ns
Delay time from SCKp↓ to SOp output[Note 3]	t_{KSO2}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ				2/f_{MCK} + 428	ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ				2/f_{MCK} + 1146	ns

Notes 1. Transfer rate in the SNOOZE mode : MAX. 1 Mbps

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time or SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the SIp pin and SCKp pin and the N-ch open drain output (V_{DD} tolerance (When 25- to 48-pin products)/EV_{DD} tolerance (When 64-pin products)) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

<R>

(**Remarks** are listed on the next page.)

<R> **(2) When reference voltage (+) = AV_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) = AV_{SS} (ADREFM = 0), target for conversion: ANI0 to ANI12**

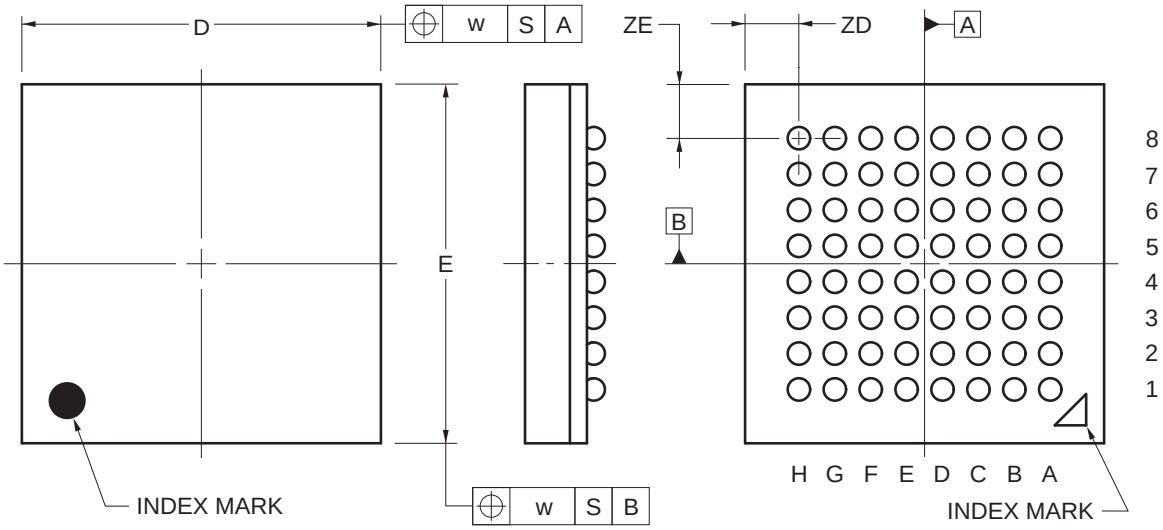
(T_A = –40 to +105°C, 2.4 V ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V, AV_{SS} = 0 V, Reference voltage (+) = AV_{DD}, Reference voltage (–) = AV_{SS} = 0 V)

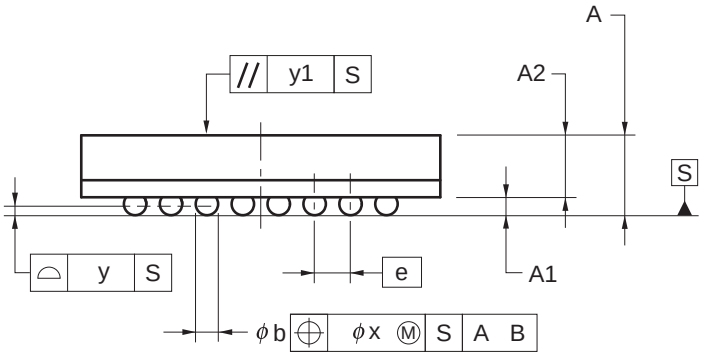
Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}		2.4 V ≤ AV_{DD} ≤ 3.6 V	8		12	bit
Overall error[Note]	AINL	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±7.5	LSB
Conversion time	t_{CONV}	ADTYP = 0, 12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V	3.375			μs
Zero-scale error[Note]	E_{ZS}	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±6.0	LSB
Full-scale error[Note]	E_{FS}	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±6.0	LSB
Integral linearity error[Note]	ILE	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±3.0	LSB
Differential linearity error[Note]	DLE	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±2.0	LSB
Analog input voltage	V_{AIN}			0		AV_{DD}	V

Note Excludes quantization error (±1/2 LSB).

R5F10ELCABG, R5F10ELDABG, R5F10ELEABG

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-VFBGA64-4x4-0.40	PVBG0064LA-A	P64F1-40-AA2-2	0.03





(UNIT:mm)

ITEM	DIMENSIONS
D	4.00±0.10
E	4.00±0.10
w	0.15
A	0.89±0.10
A1	0.20±0.05
A2	0.69
e	0.40
b	0.25±0.05
x	0.05
y	0.08
y1	0.20
ZD	0.60
ZE	0.60

Rev.	Date	Description	
		Page	Summary
0.01	Dec 26, 2011	-	First Edition issued
1.00	Sep 25, 2013	p.1	Modification of 1.1 Features
		p.4	Modification of Table 1-1. List of Ordering Part Numbers
		p.6	Modification of Remark 3 to 1.3.2 32-pin products.
		p.13	Modification of 1.5.2 32-pin products.
		p.14	Modification of 1.5.3 48-pin products.
		p.16	Modification of 1.6 Outline of Functions
		p.21	Modification of 2.2.1 X1, XT1 oscillator characteristics
		p.31, 32	Modification of Note 1 in 2.3.2 Supply current characteristics
		p.34, 35	Modification of Minimum Instruction Execution Time during Main System Clock Operation
		p.37	Modification of AC Timing Test Points in 2.5 Peripheral Functions Characteristics
		p.46 to 58	Modification of Caution to 2.5.1 Serial array unit.
		p.63 to 68	Modification of 2.6.1 A/D converter characteristics
		p.71	Modification of 2.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics
		p.71	Modification of 2.8 Flash Memory Programming Characteristics
		p.72	Modification of 2.10 Timing Specs for Switching Flash Memory Programming Modes
		p.73 to 117	Addition of 3 ELECTRICAL SPECIFICATIONS (G: INDUSTRIAL APPLICATIONS T_A = −40 to +105°C)
		p.118 to 123	Modification of 4. PACKAGE DRAWINGS
2.10	Nov 30, 2016	p.4	Modification of Table 1-1. List of Ordering Part Numbers
		p.5 to 10	Modification of the position of the index mark in 1.3.1 25-pin products to 1.3.4 64-pin products
		p.6	Modification of Remark 3
		p.13	Modification of 1.5.2 32-pin products
		p.14	Modification of 1.5.3 48-pin products
		p.16	Modification of description in 1.6 Outline of Functions
		p.21	Modification of 2.2.1 X1, XT1 oscillator characteristics
		p.31, 32	Modification of Note 1 in 2.3.2 Supply current characteristics
		p.34, 35	Modification of Minimum Instruction Execution Time during Main System Clock Operation
		p.36	Modification of AC Timing Test Points and TI/TO Timing
		p.38	Modification of AC Timing Test Points in 2.5 Peripheral Functions Characteristics
		p.48, 50 to 52, 55, 59	Modification of Caution in 2.5.1 Serial array unit
		p.64 to 69	Modification of conditions of 2.6.1 A/D converter characteristics
		p.72	Renamed to 2.7 RAM Data Retention Characteristics, and modification of note and figure
		p.72	Modification of 2.8 Flash Memory Programming Characteristics

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