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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, IrDA, LINbus, Microwire, SmartCard, SPI, SSP, UART/USART
Peripherals	Bluetooth, Brown-out Detect/Reset, LCD, LVD, POR, PWM, SmartCard, SmartSense, WDT
Number of I/O	36
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	56-UFQFN Exposed Pad
Supplier Device Package	56-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4247lqi-bl463t

More Information

Cypress provides a wealth of data at http://www.cypress.com to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the introduction page for Bluetooth® Low Energy (BLE) Products. Following is an abbreviated list for PRoC BLE:

- Overview: PSoC Portfolio, PSoC Roadmap
- Product Selectors: PSoC 1, PSoC 3, PSoC 4, PRoC BLE, PSoC 4 BLE, PSoC 5LP In addition, PSoC Creator includes a device selection tool.
- Application Notes: Cypress offers a large number of PSoC application notes coverting a broad range of topics, from basic to advanced level. Recommended application notes for getting started with PRoC BLE are:
  - AN94020: Getting Started with PRoC BLE
  - AN97060: PSoC 4 BLE and PRoC BLE - Over-The-Air (OTA) Device Firmware Upgrade (DFU) Guide
  - AN91184: PSoC 4 BLE - Designing BLE Applications
  - AN91162: Creating a BLE Custom Profile
  - AN91445: Antenna Design and RF Layout Guidelines
  - AN96841: Getting Started With EZ-BLE Module
  - AN85951: PSoC 4 CapSense Design Guide
  - AN95089: PSoC 4/PRoC BLE Crystal Oscillator Selection and Tuning Techniques
  - AN92584: Designing for Low Power and Estimating Battery Life for BLE Applications
- Technical Reference Manual (TRM) is in two documents:
  - Architecture TRM details each PRoC BLE functional block
  - Registers TRM describes each of the PRoC BLE registers
- Development Kits:
  - CY8CKIT-042-BLE-A Pioneer Kit, is a flexible, Arduino-compatible, Bluetooth LE development kit for PSoC 4 BLE and PRoC BLE.
  - CY8CKIT-142, PSoC 4 BLE Module, features a PSoC 4 BLE device, two crystals for the antenna matching network, a PCB antenna and other passives, while providing access to all GPIOs of the device.
  - CY8CKIT-143, PSoC 4 BLE 256KB Module, features a PSoC 4 BLE 256KB device, two crystals for the antenna matching network, a PCB antenna and other passives, while providing access to all GPIOs of the device.
  - The MiniProg3 device provides an interface for flash programming and debug.

PSoC Creator

PSoC Creator is a free Windows-based Integrated Design Environment (IDE). It enables concurrent hardware and firmware design of PSoC 3, PSoC 4, and PSoC 5LP based systems. Create designs using classic, familiar schematic capture supported by over 100 pre-verified, production-ready PSoC Components; see the list of component datasheets. With PSoC Creator, you can:

1. Drag and drop component icons to build your hardware system design in the main design workspace
2. Codesign your application firmware with the PSoC hardware, using the PSoC Creator IDE C compiler
3. Configure components using the configuration tools
4. Explore the library of 100+ components
5. Review component datasheets

Figure 1. Multiple-Sensor Example Project in PSoC Creator Contents

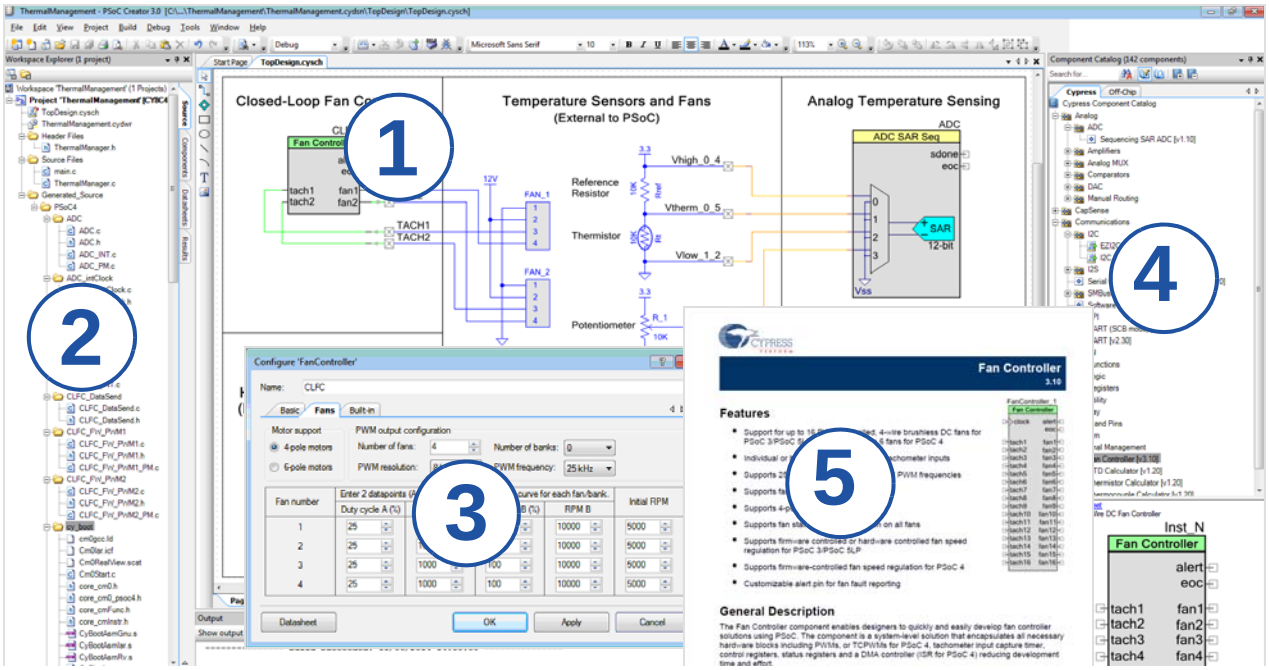
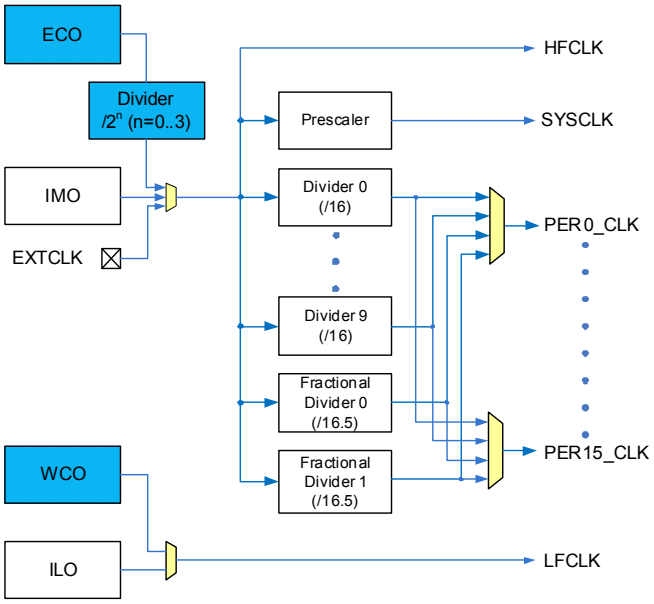


Figure 3. PSoC 4200_BL MCU Clocking Architecture



The HFCLK signal can be divided down (see Figure 3) to generate synchronous clocks for the UDBs, and the analog and digital peripherals. There are a total of 12 clock dividers for PSoC 4200_BL: ten with 16-bit divide capability and two with 16.5-bit divide capability. This allows the generation of 16 divided clock signals, which can be used by peripheral blocks. The analog clock leads the digital clocks to allow analog events to occur before the digital clock-related noise is generated. The 16-bit and 16.5-bit dividers allow a lot of flexibility in generating fine-grained frequency values and are fully supported in PSoC Creator.

Reset

PSoC 4200_BL device can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through resets and allows the software to determine the cause of the reset. An XRES pin is reserved for an external reset to avoid complications with the configuration and multiple pin functions during power-on or reconfiguration. The XRES pin has an internal pull-up resistor that is always enabled.

Voltage Reference

The PSoC 4200_BL reference system generates all internally required references. A one-percent voltage reference spec is provided for the 12-bit ADC. To allow better signal-to-noise ratios (SNR) and better absolute accuracy, it is possible to bypass the internal reference using a GPIO pin or use an external reference for the SAR. Refer to Table 19, “SAR ADC AC Specifications,” on page 26 for details.

BLE Radio and Subsystem

PSoC 4200_BL incorporates a Bluetooth Smart subsystem that contains the Physical Layer (PHY) and Link Layer (LL) engines with an embedded AES-128 security engine. The physical layer consists of the digital PHY and the RF transceiver that transmits and receives GFSK packets at 1 Mbps over a 2.4-GHz ISM band, which is compliant with Bluetooth Smart Bluetooth Specification 4.2. The baseband controller is a composite hardware and firmware implementation that supports both master and slave modes. Key protocol elements, such as HCI and link control, are implemented in firmware. Time-critical functional blocks, such as encryption, CRC, data whitening, and access code correlation, are implemented in hardware (in the LL engine).

The RF transceiver contains an integrated balun, which provides a single-ended RF port pin to drive a 50-Ω antenna via a matching/filtering network. In the receive direction, this block converts the RF signal from the antenna to a digital bit stream after performing GFSK demodulation. In the transmit direction, this block performs GFSK modulation and then converts a digital baseband signal to a radio frequency before transmitting it to air through the antenna.

The Bluetooth Smart Radio and Subsystem (BLESS) requires a 1.9-V minimum supply (the range varies from 1.9 V to 5.5 V).

Key features of BLESS are as follows:

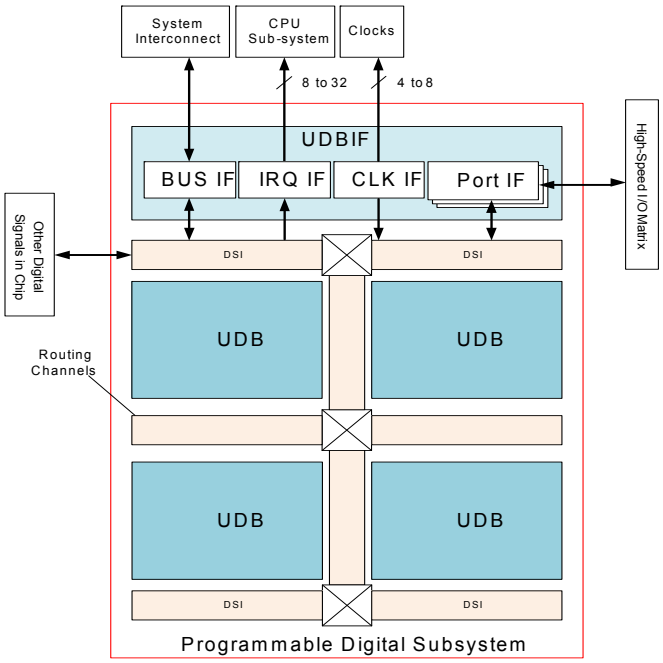
- Master and slave single-mode protocol stack with logical link control and adaptation protocol (L2CAP), attribute (ATT), and security manager (SM) protocols
- API access to generic attribute profile (GATT), generic access profile (GAP), and L2CAP
- L2CAP connection-oriented channel
- GAP features
  - Broadcaster, Observer, Peripheral, and Central roles
  - Security mode 1: Level 1, 2, 3, and 4
  - Security mode 2: Level 1 and 2
  - User-defined advertising data
  - Multiple bond support
- GATT features
  - GATT client and server
  - Supports GATT sub-procedures
  - 32-bit universally unique identifier (UUID)
- Security Manager (SM)
  - Pairing methods: Just works, Passkey Entry, Out of Band and Numeric Comparison
  - Authenticated man-in-the-middle (MITM) protection and data signing
  - LE Secure Connections (Bluetooth 4.2 feature)
- Link Layer (LL)
  - Master and Slave roles
  - 128-bit AES engine
  - Encryption
  - Low-duty cycle advertising
  - LE Ping
  - LE Data Packet Length Extension (Bluetooth 4.2 feature)
  - Link Layer Privacy (with extended scanning filter policy, Bluetooth 4.2 feature)
- Supports all SIG-adopted BLE profiles

Programmable Digital

Universal Digital Blocks (UDBs) and Port Interfaces

The PSoC 4XX8 BLE 4.2 has four UDBs; the UDB array also provides a switched Digital System Interconnect (DSI) fabric that allows signals from peripherals and ports to be routed to and through the UDBs for communication and control.

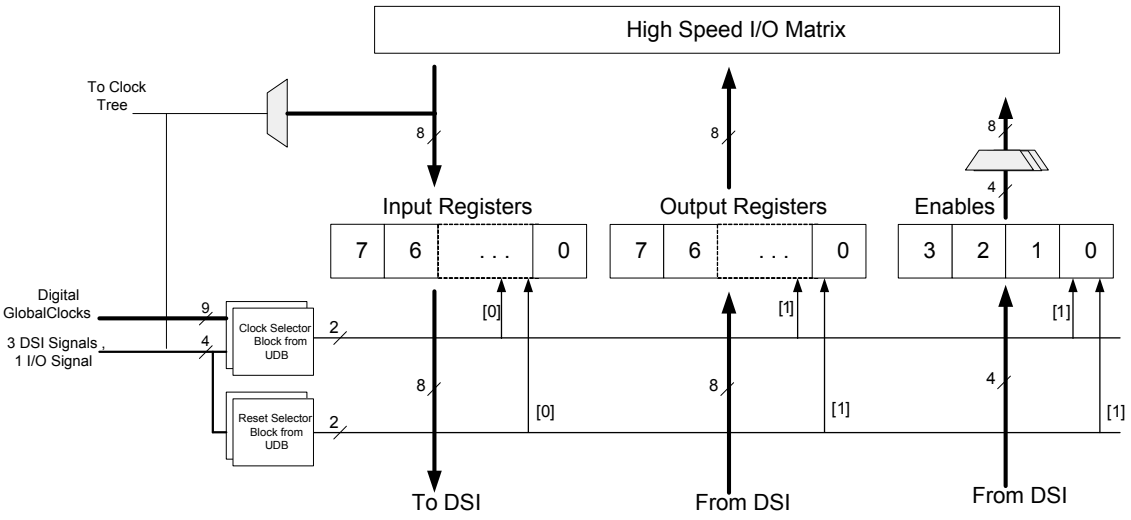
Figure 5. UDB Array



UDBs can be clocked from a clock-divider block, from a port interface (required for peripherals such as SPI), and from the DSI network directly or after synchronization.

A port interface is defined, which acts as a register that can be clocked with the same source as the PLDs inside the UDB array. This allows a faster operation because the inputs and outputs can be registered at the port interface close to the I/O pins and at the edge of the array. The port interface registers can be clocked by one of the I/Os from the same port. This allows interfaces such as SPI to operate at higher clock speeds by eliminating the delay for the port input to be routed over DSI and used to register other inputs (see Figure 6).

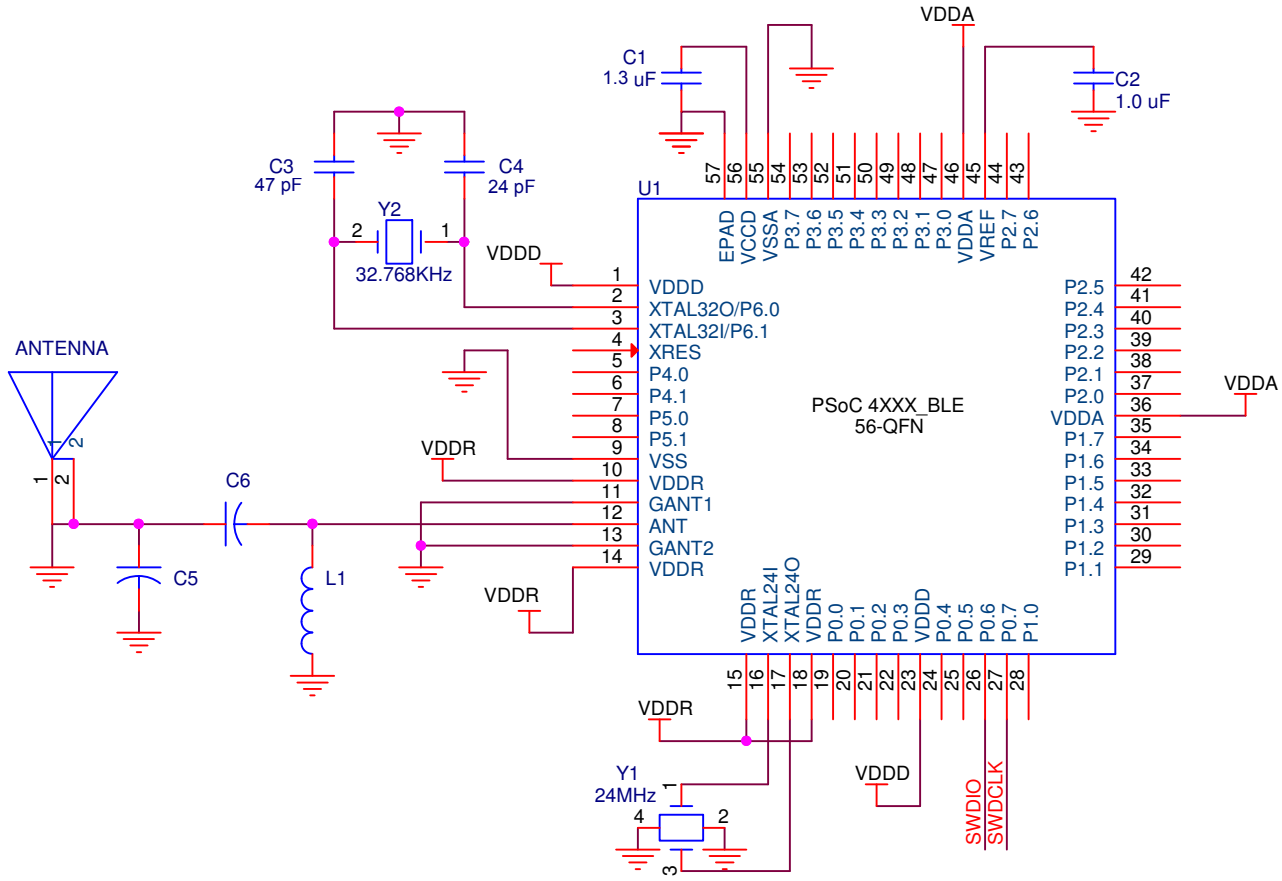
Figure 6. Port Interface



UDBs can generate interrupts (one UDB at a time) to the interrupt controller. UDBs retain the ability to connect to any pin on the chip through the DSI.

The possible pin connections are shown for all analog and digital peripherals (except the radio, LCD, and CSD blocks, which were shown in Table 1). A typical system application connection diagram is shown in Figure 7.

Figure 7. System Application Connection Diagram



Power

The PSoC 4200_BL device can be supplied from batteries with a voltage range of 1.9 V to 5.5 V by directly connecting to the digital supply (VDDD), analog supply (VDDA), and radio supply (VDDR) pins. Internal LDOs in the device regulate the supply voltage to the required levels for different blocks. The device has one regulator for the digital circuitry and separate regulators for radio circuitry for noise isolation. Analog circuits run directly from the analog supply (VDDA) input. The device uses separate regulators for Deep Sleep and Hibernate (lowered power supply and retention) modes to minimize the power consumption. The radio stops working below 1.9 V, but the device continues to function down to 1.71 V without RF.

Bypass capacitors must be used from VDDx (x = A, D, or R) to ground. The typical practice for systems in this frequency range is to use a capacitor in the 1-µF range in parallel with a smaller capacitor (for example, 0.1 µF). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

Power Supply	Bypass Capacitors
VDDD	The internal bandgap may be bypassed with a 1-µF to 10-µF.
VDDA	0.1-µF ceramic at each pin plus bulk capacitor 1-µF to 10-µF.
VDDR	0.1-µF ceramic at each pin plus bulk capacitor 1-µF to 10-µF.
VCCD	1.3-µF ceramic capacitor at the VCCD pin.
VREF (optional)	The internal bandgap may be bypassed with a 1-µF to 10-µF capacitor.

Table 6. DC Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID41	I_{DD31}	GPIO and reset active	–	–	–	nA	T = 25 °C
SID42	I_{DD32}	GPIO and reset active	–	–	–	nA	T = –40 °C to 85 °C
Stop Mode, V_{DD} = 1.8 to 3.6 V							
SID43	I_{DD33}	Stop mode current (V_{DD})	–	20	–	nA	T = 25 °C, V_{DD} = 3.3 V
SID44	I_{DD34}	Stop mode current (V_{DDR})	–	40	–-	nA	T = 25 °C, V_{DDR} = 3.3 V
SID45	I_{DD35}	Stop mode current (V_{DD})	–	–	–	nA	T = –40 °C to 85 °C
SID46	I_{DD36}	Stop mode current (V_{DDR})	–	–	–	nA	T = –40 °C to 85 °C, V_{DDR} = 1.9 V to 3.6 V
Stop Mode, V_{DD} = 3.6 to 5.5 V							
SID47	I_{DD37}	Stop mode current (V_{DD})	–	–	–	nA	T = 25 °C, V_{DD} = 5 V
SID48	I_{DD38}	Stop mode current (V_{DDR})	–	–	–	nA	T = 25 °C, V_{DDR} = 5 V
SID49	I_{DD39}	Stop mode current (V_{DD})	–	–	–	nA	T = –40 °C to 85 °C
SID50	I_{DD40}	Stop mode current (V_{DDR})	–	–	–	nA	T = –40 °C to 85 °C
Stop Mode, V_{DD} = 1.71 to 1.89 V (Regulator Bypassed)							
SID51	I_{DD41}	Stop mode current (V_{DD})	–	–	–	nA	T = 25 °C
SID52	I_{DD42}	Stop mode current (V_{DD})	–	–	–	nA	T = –40 °C to 85 °C

Table 7. AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID53	F_{CPU}	CPU frequency	DC	–	48	MHz	1.71 V ≤ V_{DD} ≤ 5.5 V
SID54	T_{SLEEP}	Wakeup from Sleep mode	–	0	–	µs	Guaranteed by characterization
SID55	$T_{DEEPSLEEP}$	Wakeup from Deep Sleep mode	–	–	25	µs	24-MHz IMO. Guaranteed by characterization.
SID56	$T_{HIBERNATE}$	Wakeup from Hibernate mode	–	–	0.7	ms	Guaranteed by characterization
SID57	T_{STOP}	Wakeup from Stop mode	–	–	2.2	ms	Guaranteed by characterization

Table 13. XRES AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID93	$T_{RESETWIDTH}$	Reset pulse width	1	–	–	µs	–

Analog Peripherals

Opamp

Table 14. Opamp Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
I_{DD} (Opamp Block Current. V_{DD} = 1.8 V. No Load)							
SID94	I_{DD_HI}	Power = high	–	1000	1850	µA	–
SID95	I_{DD_MED}	Power = medium	–	500	950	µA	–
SID96	I_{DD_LOW}	Power = low	–	250	350	µA	–
GBW (Load = 20 pF, 0.1 mA. V_{DDA} = 2.7 V)							
SID97	GBW_HI	Power = high	6	–	–	MHz	–
SID98	GBW_MED	Power = medium	4	–	–	MHz	–
SID99	GBW_LO	Power = low	–	1	–	MHz	–
I_{OUT_MAX} (V_{DDA} ≥ 2.7 V, 500 mV From Rail)							
SID100	$I_{OUT\_MAX\_HI}$	Power = high	10	–	–	mA	–
SID101	$I_{OUT\_MAX\_MID}$	Power = medium	10	–	–	mA	–
SID102	$I_{OUT\_MAX\_LO}$	Power = low	–	5	–	mA	–
I_{OUT} (V_{DDA} = 1.71 V, 500 mV From Rail)							
SID103	$I_{OUT\_MAX\_HI}$	Power = high	4	–	–	mA	–
SID104	$I_{OUT\_MAX\_MID}$	Power = medium	4	–	–	mA	–
SID105	$I_{OUT\_MAX\_LO}$	Power = low	–	2	–	mA	–
SID106	V_{IN}	Charge pump on, V_{DDA} ≥ 2.7 V	–0.05	–	V_{DDA} – 0.2	V	–
SID107	V_{CM}	Charge pump on, V_{DDA} ≥ 2.7 V	–0.05	–	V_{DDA} – 0.2	V	–
V_{OUT} (V_{DDA} ≥ 2.7 V)							
SID108	V_{OUT_1}	Power = high, I_{LOAD}=10 mA	0.5	–	V_{DDA} – 0.5	V	–
SID109	V_{OUT_2}	Power = high, I_{LOAD}=1 mA	0.2	–	V_{DDA} – 0.2	V	–
SID110	V_{OUT_3}	Power = medium, I_{LOAD}=1 mA	0.2	–	V_{DDA} – 0.2	V	–
SID111	V_{OUT_4}	Power = low, I_{LOAD}=0.1 mA	0.2	–	V_{DDA} – 0.2	V	–
SID112	V_{OS_TR}	Offset voltage, trimmed	1	±0.5	1	mV	High mode
SID113	V_{OS_TR}	Offset voltage, trimmed	–	±1	–	mV	Medium mode
SID114	V_{OS_TR}	Offset voltage, trimmed	–	±2	–	mV	Low mode
SID115	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–10	±3	10	µV/C	High mode
SID116	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–	±10	–	µV/C	Medium mode
SID117	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–	±10	–	µV/C	Low mode
SID118	CMRR	DC	70	80	–	dB	V_{DDD} = 3.6-V
SID119	PSRR	At 1 kHz, 100-mV ripple	70	85	–	dB	V_{DDD} = 3.6-V
Noise							
SID120	V_{N1}	Input referred, 1 Hz–1 GHz, power = high	–	94	–	µVrms	–
SID121	V_{N2}	Input referred, 1-kHz, power = high	–	72	–	nV/rtHz	–

Table 26. PWM AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID214	$T_{PWMFREQ}$	Operating frequency	F_{CLK}	–	48	MHz	–
SID215	$T_{PWMPWINT}$	Pulse width (internal)	2 × T_{CLK}	–	–	ns	–
SID216	T_{PWMEXT}	Pulse width (external)	2 × T_{CLK}	–	–	ns	–
SID217	$T_{PWMKILLINT}$	Kill pulse width (internal)	2 × T_{CLK}	–	–	ns	–
SID218	$T_{PWMKILLEXT}$	Kill pulse width (external)	2 × T_{CLK}	–	–	ns	–
SID219	$T_{PWMEINT}$	Enable pulse width (internal)	2 × T_{CLK}	–	–	ns	–
SID220	$T_{PWMENEXT}$	Enable pulse width (external)	2 × T_{CLK}	–	–	ns	–
SID221	$T_{PWMRESWINT}$	Reset pulse width (internal)	2 × T_{CLK}	–	–	ns	–
SID222	$T_{PWMRESWEXT}$	Reset pulse width (external)	2 × T_{CLK}	–	–	ns	–

I^2C

Table 27. Fixed I^2C DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID223	I_{I2C1}	Block current consumption at 100 kHz	–	–	50	µA	–
SID224	I_{I2C2}	Block current consumption at 400 kHz	–	–	155	µA	–
SID225	I_{I2C3}	Block current consumption at 1 Mbps	–	–	390	µA	–
SID226	I_{I2C4}	I^2C enabled in Deep Sleep mode	–	–	1.4	µA	–

Table 28. Fixed I^2C AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID227	F_{I2C1}	Bit rate	–	–	1	Mbps	–

LCD Direct Drive

Table 29. LCD Direct Drive DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID228	I_{LCDLOW}	Operating current in low-power mode	–	17.5	–	µA	16 × 4 small segment display at 50 Hz
SID229	C_{LCDCAP}	LCD capacitance per segment/common driver	–	500	5000	pF	–
SID230	LCD_{OFFSET}	Long-term segment offset	–	20	–	mV	–
SID231	I_{LCDOP1}	LCD system operating current V_{BIAS} = 5 V.	–	2	–	mA	32 × 4 segments. 50 Hz at 25 °C
SID232	I_{LCDOP2}	LCD system operating current. V_{BIAS} = 3.3 V	–	2	–	mA	32 × 4 segments 50 Hz at 25 °C

Table 30. LCD Direct Drive AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID233	F_{LCD}	LCD frame rate	10	50	150	Hz	–

Table 31. Fixed UART DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID234	I_{UART1}	Block current consumption at 100 kbps	–	–	55	µA	–
SID235	I_{UART2}	Block current consumption at 1000 kbps	–	–	360	µA	–

Table 32. Fixed UART AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID236	F_{UART}	Bit rate	–	–	1	Mbps	–

SPI Specifications

Table 33. Fixed SPI DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID237	I_{SPI1}	Block current consumption at 1 Mbps	–	–	360	µA	–
SID238	I_{SPI2}	Block current consumption at 4 Mbps	–	–	560	µA	–
SID239	I_{SPI3}	Block current consumption at 8 Mbps	–	–	600	µA	–

Table 34. Fixed SPI AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID240	F_{SPI}	SPI operating frequency (master; 6X oversampling)	–	–	8	MHz	–

Table 35. Fixed SPI Master Mode AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID241	T_{DMO}	MOSI valid after Sclock driving edge	–	–	18	ns	–
SID242	T_{DSI}	MISO valid before Sclock capturing edge. Full clock, late MISO sampling used	20	–	–	ns	Full clock, late MISO sampling
SID243	T_{HMO}	Previous MOSI data hold time	0	–	–	ns	Referred to Slave capturing edge

Table 36. Fixed SPI Slave Mode AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID244	T_{DMI}	MOSI valid before Sclock capturing edge	40	–	–	ns	–
SID245	T_{DSO}	MISO valid after Sclock driving edge	–	–	$42 + 3 \times T_{CPU}$	ns	–
SID246	T_{DSO_ext}	MISO valid after Sclock driving edge in external clock mode	–	–	53	ns	$V_{DD} < 3.0$ V
SID247	T_{HSO}	Previous MISO data hold time	0	–	–	ns	–
SID248	$T_{SSELSCK}$	SSEL valid to first SCK valid edge	100	–	–	ns	–

Memory

Table 37. Flash DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID249	V_{PE}	Erase and program voltage	1.71	–	5.5	V	–
SID309	T_{WS48}	Number of Wait states at 32–48 MHz	2	–	–		CPU execution from flash
SID310	T_{WS32}	Number of Wait states at 16–32 MHz	1	–	–		CPU execution from flash
SID311	T_{WS16}	Number of Wait states for 0–16 MHz	0	–	–		CPU execution from flash

Voltage Monitors

Table 43. Voltage Monitor DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID265	V_{LVI1}	LVI_A/D_SEL[3:0] = 0000b	1.71	1.75	1.79	V	–
SID266	V_{LVI2}	LVI_A/D_SEL[3:0] = 0001b	1.76	1.80	1.85	V	–
SID267	V_{LVI3}	LVI_A/D_SEL[3:0] = 0010b	1.85	1.90	1.95	V	–
SID268	V_{LVI4}	LVI_A/D_SEL[3:0] = 0011b	1.95	2.00	2.05	V	–
SID269	V_{LVI5}	LVI_A/D_SEL[3:0] = 0100b	2.05	2.10	2.15	V	–
SID270	V_{LVI6}	LVI_A/D_SEL[3:0] = 0101b	2.15	2.20	2.26	V	–
SID271	V_{LVI7}	LVI_A/D_SEL[3:0] = 0110b	2.24	2.30	2.36	V	–
SID272	V_{LVI8}	LVI_A/D_SEL[3:0] = 0111b	2.34	2.40	2.46	V	–
SID273	V_{LVI9}	LVI_A/D_SEL[3:0] = 1000b	2.44	2.50	2.56	V	–
SID274	V_{LVI10}	LVI_A/D_SEL[3:0] = 1001b	2.54	2.60	2.67	V	–
SID2705	V_{LVI11}	LVI_A/D_SEL[3:0] = 1010b	2.63	2.70	2.77	V	–
SID276	V_{LVI12}	LVI_A/D_SEL[3:0] = 1011b	2.73	2.80	2.87	V	–
SID277	V_{LVI13}	LVI_A/D_SEL[3:0] = 1100b	2.83	2.90	2.97	V	–
SID278	V_{LVI14}	LVI_A/D_SEL[3:0] = 1101b	2.93	3.00	3.08	V	–
SID279	V_{LVI15}	LVI_A/D_SEL[3:0] = 1110b	3.12	3.20	3.28	V	–
SID280	V_{LVI16}	LVI_A/D_SEL[3:0] = 1111b	4.39	4.50	4.61	V	–
SID281	LVI_IDD	Block current	–	–	100	µA	–

Table 44. Voltage Monitor AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID282	$T_{MONTRIP}$	Voltage monitor trip time	–	–	1	µs	–

SWD Interface

Table 45. SWD Interface Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID283	F_SWDCLK1	$3.3\ V \le V_{DD} \le 5.5\ V$	–	–	14	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID284	F_SWDCLK2	$1.71\ V \le V_{DD} \le 3.3\ V$	–	–	7	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID285	T_SWDI_SETUP	T = 1/f SWDCLK	0.25 × T	–	–	ns	–
SID286	T_SWDI_HOLD	T = 1/f SWDCLK	0.25 × T	–	–	ns	–
SID287	T_SWDO_VALID	T = 1/f SWDCLK	–	–	0.5 × T	ns	–
SID288	T_SWDO_HOLD	T = 1/f SWDCLK	1	–	–	ns	–

Internal Main Oscillator

Table 46. IMO DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID289	I_{IMO1}	IMO operating current at 48 MHz	–	–	1000	µA	–
SID290	I_{IMO2}	IMO operating current at 24 MHz	–	–	325	µA	–
SID291	I_{IMO3}	IMO operating current at 12 MHz	–	–	225	µA	–
SID292	I_{IMO4}	IMO operating current at 6 MHz	–	–	180	µA	–
SID293	I_{IMO5}	IMO operating current at 3 MHz	–	–	150	µA	–

Table 47. IMO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID296	$F_{IMOTOL3}$	Frequency variation from 3 to 48 MHz	–	–	±2	%	With API-called calibration
SID297	$F_{IMOTOL3}$	IMO startup time	–	–	12	µs	–

Internal Low-Speed Oscillator

Table 48. ILO DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID298	I_{ILO2}	ILO operating current at 32 kHz	–	0.3	1.05	µA	–

Table 49. ILO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID299	$T_{STARTILO1}$	ILO startup time	–	–	2	ms	–
SID300	$F_{ILOTRIM1}$	32-kHz trimmed frequency	15	32	50	kHz	–

Table 50. External Clock Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID301	ExtClkFreq	External clock input frequency	0	–	48	MHz	CMOS input level only
SID302	ExtClkDuty	Duty cycle; Measured at $V_{DD/2}$	45	–	55	%	CMOS input level only

Table 51. UDB AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
Data Path performance							
SID303	$F_{MAX-TIMER}$	Max frequency of 16-bit timer in a UDB pair	–	–	48	MHz	–
SID304	$F_{MAX-ADDER}$	Max frequency of 16-bit adder in a UDB pair	–	–	48	MHz	–
SID305	F_{MAX_CRC}	Max frequency of 16-bit CRC/PRS in a UDB pair	–	–	48	MHz	–
PLD Performance in UDB							
SID306	F_{MAX_PLD}	Max frequency of 2-pass PLD function in a UDB pair	–	–	48	MHz	–
Clock to Output Performance							
SID307	$T_{CLK\_OUT\_UDB1}$	Prop. delay for clock in to data out at 25 °C, Typical	–	15	–	ns	–
SID308	$T_{CLK\_OUT\_UDB2}$	Prop. delay for clock in to data out, Worst case	–	25	–	ns	–

Table 52. BLE Subsystem *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID378	ITX,-6dBm	TX current at –6-dBm setting (PA3)	–	14.5	–	mA	–
SID379	ITX,-12dBm	TX current at –12-dBm setting (PA2)	–	13.2	–	mA	–
SID380	ITX,-18dBm	TX current at –18-dBm setting (PA1)	–	12.5	–	mA	–
SID380A	Iavg_1sec, 0dBm	Average current at 1-second BLE connection interval	–	17.1	–	µA	TXP: 0 dBm; ±20-ppm master and slave clock accuracy.
SID380B	Iavg_4sec, 0dBm	Average current at 4-second BLE connection interval	–	6.1	–	µA	TXP: 0 dBm; ±20-ppm master and slave clock accuracy.
General RF Specifications							
SID381	FREQ	RF operating frequency	2400	–	2482	MHz	–
SID382	CHBW	Channel spacing	–	2	–	MHz	–
SID383	DR	On-air data rate	–	1000	–	kbps	–
SID384	IDLE2TX	BLE.IDLE to BLE. TX transition time	–	120	140	µs	–
SID385	IDLE2RX	BLE.IDLE to BLE. RX transition time	–	75	120	µs	–
RSSI Specifications							
SID386	RSSI, ACC	RSSI accuracy	–	±5	–	dB	–
SID387	RSSI, RES	RSSI resolution	–	1	–	dB	–
SID388	RSSI, PER	RSSI sample period	–	6	–	µs	–

Table 53. ECO Specifications

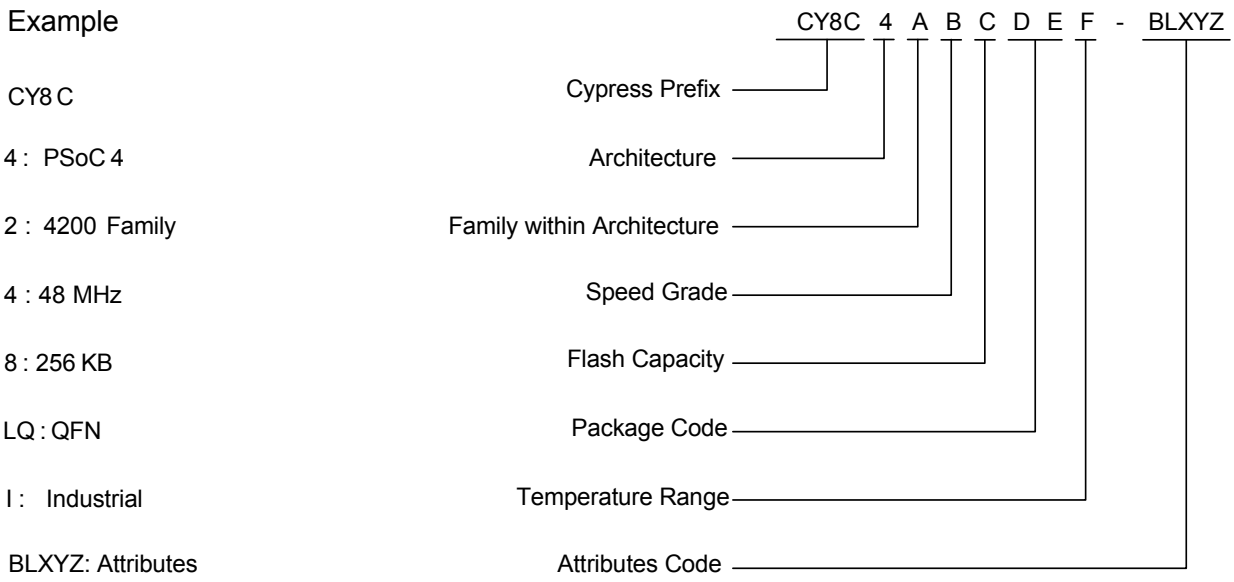
Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID389	F_{ECO}	Crystal frequency	–	24	–	MHz	–
SID390	F_{TOL}	Frequency tolerance	–50	–	50	ppm	–
SID391	ESR	Equivalent series resistance	–	–	60	Ω	–
SID392	PD	Drive level	–	–	100	µW	–
SID393	T_{START1}	Startup time (Fast Charge on)	–	–	850	µs	–
SID394	T_{START2}	Startup time (Fast Charge off)	–	–	3	ms	–
SID395	C_L	Load capacitance	–	8	–	pF	–
SID396	C0	Shunt capacitance	–	1.1	–	pF	–
SID397	I_{ECO}	Operating current	–	1400	–	µA	–

Table 54. WCO Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID398	F_{WCO}	Crystal frequency	–	32.768	–	kHz	–
SID399	FTOL	Frequency tolerance	–	50	–	ppm	–
SID400	ESR	Equivalent series resistance	–	50	–	kΩ	–
SID401	PD	Drive level	–	–	1	µW	–
SID402	T_{START}	Startup time	–	–	500	ms	–
SID403	C_L	Crystal load capacitance	6	–	12.5	pF	–
SID404	C0	Crystal shunt capacitance	–	1.35	–	pF	–
SID405	I_{WCO1}	Operating current (High-Power mode)	–	–	8	µA	–
SID406	I_{WCO2}	Operating current (Low-Power mode)	–	–	2.6	µA	–

PSoC 4 devices follow the part numbering convention described in the following table. All fields are single-character alphanumeric (0, 1, 2, …, 9, A,B, …, Z) unless stated otherwise.

Ordering Code Definitions



The Field Values are listed in the following table:

Field	Description	Values	Meaning
CY8C	Cypress Prefix		
4	Architecture	4	PSoC 4
A	Family within architecture	2	4200-BLE Family
B	CPU Speed	4	48 MHz
C	Flash Capacity	8, 7	256, 128 KB respectively
DE	Package Code	FN	WLCSP
		LQ	QFN
		FL	Thin CSP
F	Temperature Range	I	Industrial
BLXYZ	Attributes Code	BL400-BL499	Bluetooth 4.1 compliant
		BL500-BL599	Bluetooth 4.2 compliant

Packaging

Table 56. Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
T_A	Operating ambient temperature	–	–40	25.00	105	°C
T_J	Operating junction temperature	–	–40	–	125	°C
T_{JA}	Package θ_{JA} (56-pin QFN)	–	–	16.9	–	°C/watt
T_{JC}	Package θ_{JC} (56-pin QFN)	–	–	9.7	–	°C/watt
T_{JA}	Package θ_{JA} (76-ball WLCSP)	–	–	20.1	–	°C/watt
T_{JC}	Package θ_{JC} (76-ball WLCSP)	–	–	0.19	–	°C/watt
T_{JA}	Package θ_{JA} (76-ball Thin WLCSP)	–	–	20.9	–	°C/watt
T_{JC}	Package θ_{JC} (76-ball Thin WLCSP)	–	–	0.17	–	°C/watt
T_{JA}	Package θ_{JA} (68-ball WLCSP)		–	16.6	–	°C/watt
T_{JC}	Package θ_{JC} (68-ball WLCSP)		–	0.19	–	°C/watt
T_{JA}	Package θ_{JA} (68-ball Thin WLCSP)		–	16.6	–	°C/watt
T_{JC}	Package θ_{JC} (68-ball Thin WLCSP)		–	0.19	–	°C/watt

Table 57. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
All packages	260 °C	30 seconds

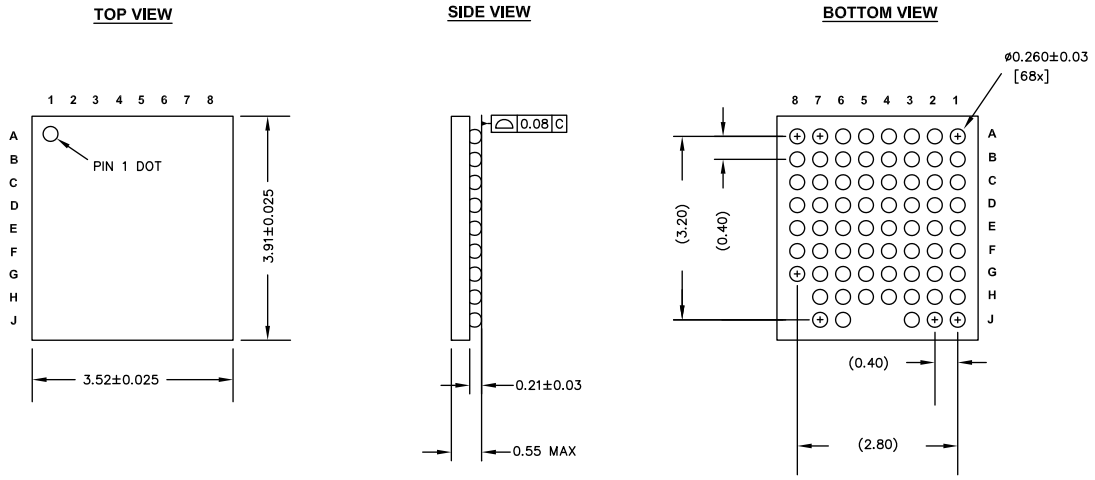
Table 58. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
56-pin QFN	MSL 3
All WLCSP packages	MSL 1

Table 59. Package Details

Spec ID	Package	Description
001-58740 Rev. *C	56-pin QFN	7.0 mm × 7.0 mm × 0.6 mm
001-96603 Rev. *A	76-ball WLCSP	4.04 mm × 3.87 mm × 0.55 mm
002-10658, Rev. **	76-ball thin WLCSP	4.04 mm × 3.87 mm × 0.4 mm
001-92343 Rev. *A	68-ball WLCSP	3.52 mm × 3.91 mm × 0.55 mm
001-99408 Rev **	68-ball Thin WLCSP	52 mm × 3.91 mm × 0.4 mm

Figure 10. 68-Ball WLCSP Package Outline

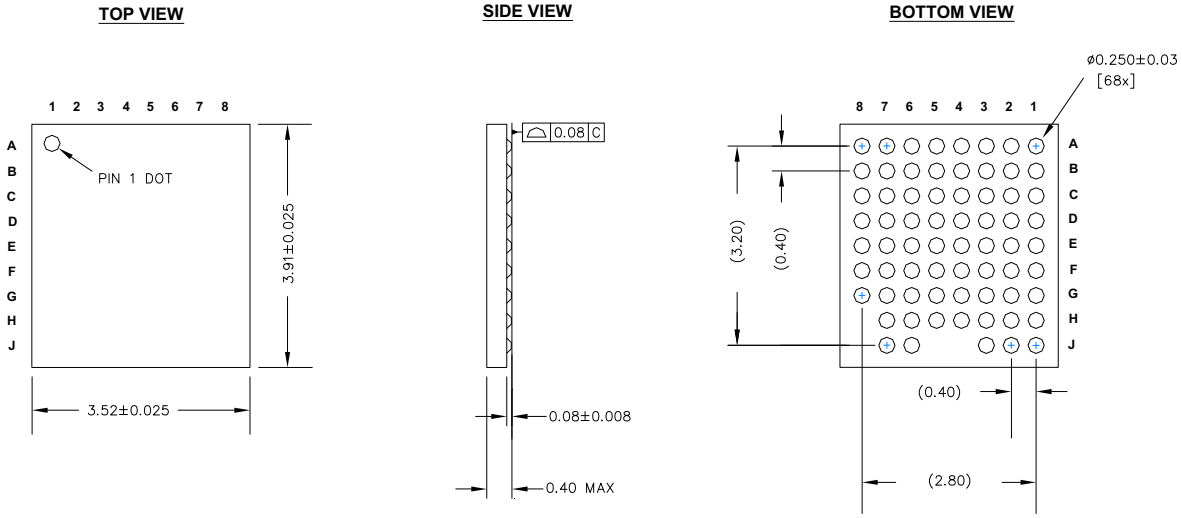


NOTES:

1. REFERENCE JEDEC PUBLICATION 95, DESIGN GUIDE 4.18
2. ALL DIMENSIONS ARE IN MILLIMETERS

001-92343 *A

Figure 11. 68-Ball Thin WLCSP

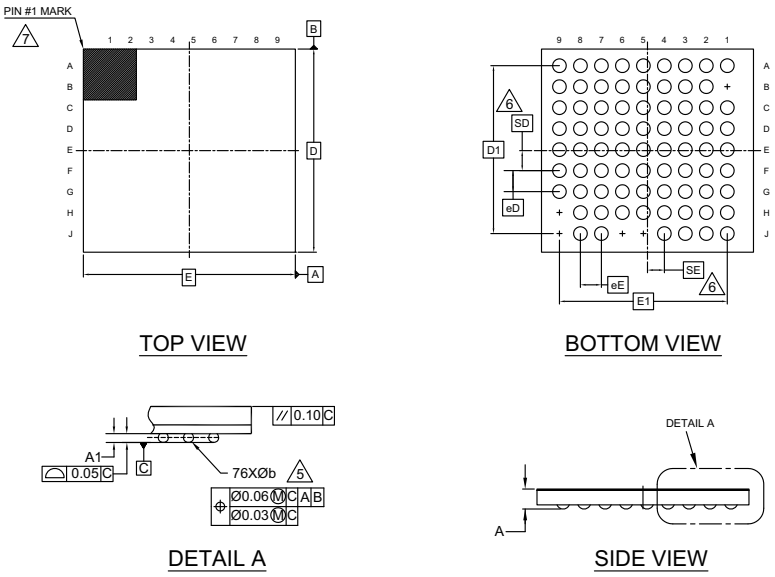


NOTES:

1. REFERENCE JEDEC PUBLICATION 95, DESIGN GUIDE 4.18
2. ALL DIMENSIONS ARE IN MILLIMETERS

001-99408 **

Figure 12. 76-Ball WLCSP Package Outline



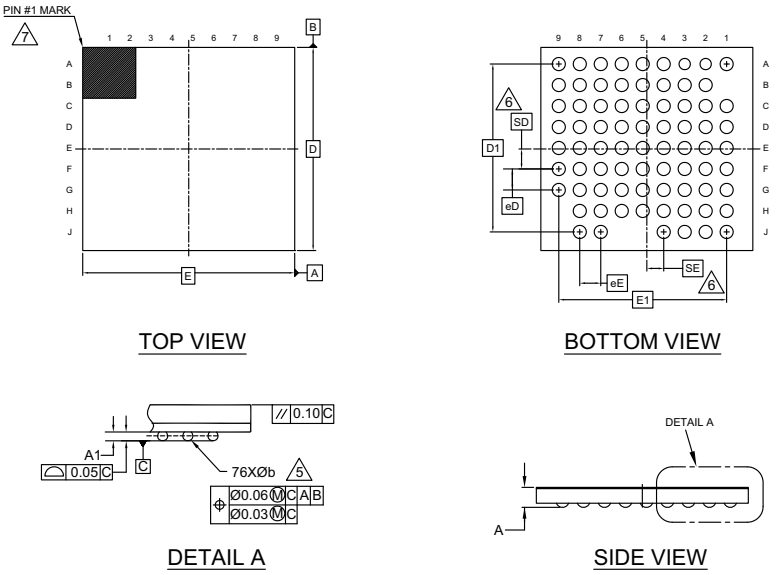
SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	0.55
A1	0.18	0.21	0.24
D	3.87 BSC		
E	4.04 BSC		
D1	3.20 BSC		
E1	3.20 BSC		
MD	9		
ME	9		
N	76		
Ø b	0.23	0.26	0.29
eD	0.40 BSC		
eE	0.40 BSC		
SD	0.381 BSC		
SE	0.321 BSC		

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
7. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.
9. JEDEC SPECIFICATION NO. REF : N/A

001-96603 *B

Figure 13. 76-Ball Thin WLCSP Package Outline



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	0.40
A1	0.072	0.08	0.088
D	3.87 BSC		
E	4.04 BSC		
D1	3.20 BSC		
E1	3.20 BSC		
MD	9		
ME	9		
N	76		
Ø b	0.22	0.25	0.28
eD	0.40 BSC		
eE	0.40 BSC		
SD	0.381		
SE	0.321		

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
7. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.

002-10658 **

Acronyms

Table 60. Acronyms Used in this Document

Acronym	Description
abus	analog local bus
ADC	analog-to-digital converter
AG	analog global
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an Arm data transfer bus
ALU	arithmetic logic unit
AMUXBUS	analog multiplexer bus
API	application programming interface
APSR	application program status register
Arm®	advanced RISC machine, a CPU architecture
ATM	automatic thump mode
BW	bandwidth
CAN	Controller Area Network, a communications protocol
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
DAC	digital-to-analog converter, see also IDAC, VDAC
DFB	digital filter block
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DMIPS	Dhrystone million instructions per second
DMA	direct memory access, see also TD
DNL	differential nonlinearity, see also INL
DNU	do not use
DR	port write data registers
DSI	digital system interconnect
DWT	data watchpoint and trace
ECC	error correcting code
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
EMIF	external memory interface
EOC	end of conversion
EOF	end of frame
EPSR	execution program status register
ESD	electrostatic discharge

Table 60. Acronyms Used in this Document *(continued)*

Acronym	Description
ETM	embedded trace macrocell
FIR	finite impulse response, see also IIR
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output, applies to a PSoC pin
HVI	high-voltage interrupt, see also LVI, LVD
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
IIR	infinite impulse response, see also FIR
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
I/O	input/output, see also GPIO, DIO, SIO, USBIO
IPOR	initial power-on reset
IPSR	interrupt program status register
IRQ	interrupt request
ITM	instrumentation trace macrocell
LCD	liquid crystal display
LIN	Local Interconnect Network, a communications protocol.
LR	link register
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVI	low-voltage interrupt, see also HVI
LVTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit
MISO	master-in slave-out
NC	no connect
NMI	nonmaskable interrupt
NRZ	non-return-to-zero
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL
opamp	operational amplifier
PAL	programmable array logic, see also PLD

Document Conventions

Units of Measure

Table 61. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
dB	decibel
fF	femto farad
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohour
kHz	kilohertz
kΩ	kilo ohm
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µH	microhenry
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
sqrtHz	square root of hertz
V	volt

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