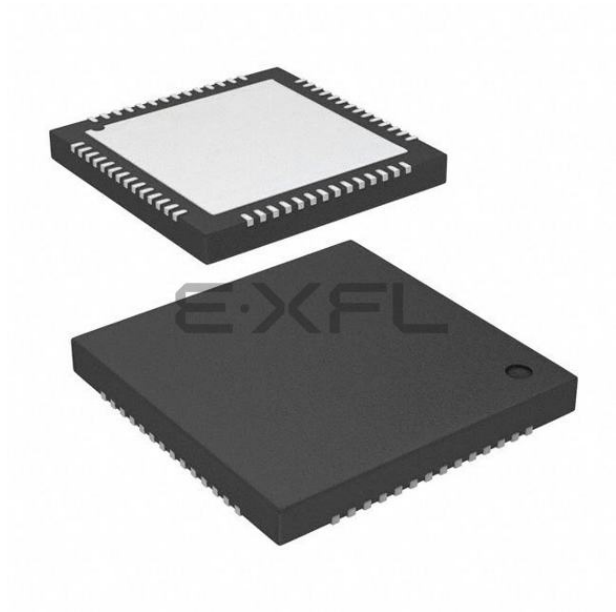

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, IrDA, LINbus, Microwire, SmartCard, SPI, SSP, UART/USART
Peripherals	Bluetooth, Brown-out Detect/Reset, Cap Sense, LCD, LVD, POR, PWM, SmartCard, SmartSense, WDT
Number of I/O	36
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	56-UFQFN Exposed Pad
Supplier Device Package	56-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4247lqi-bl483

More Information

Cypress provides a wealth of data at http://www.cypress.com to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the introduction page for Bluetooth® Low Energy (BLE) Products. Following is an abbreviated list for PRoC BLE:

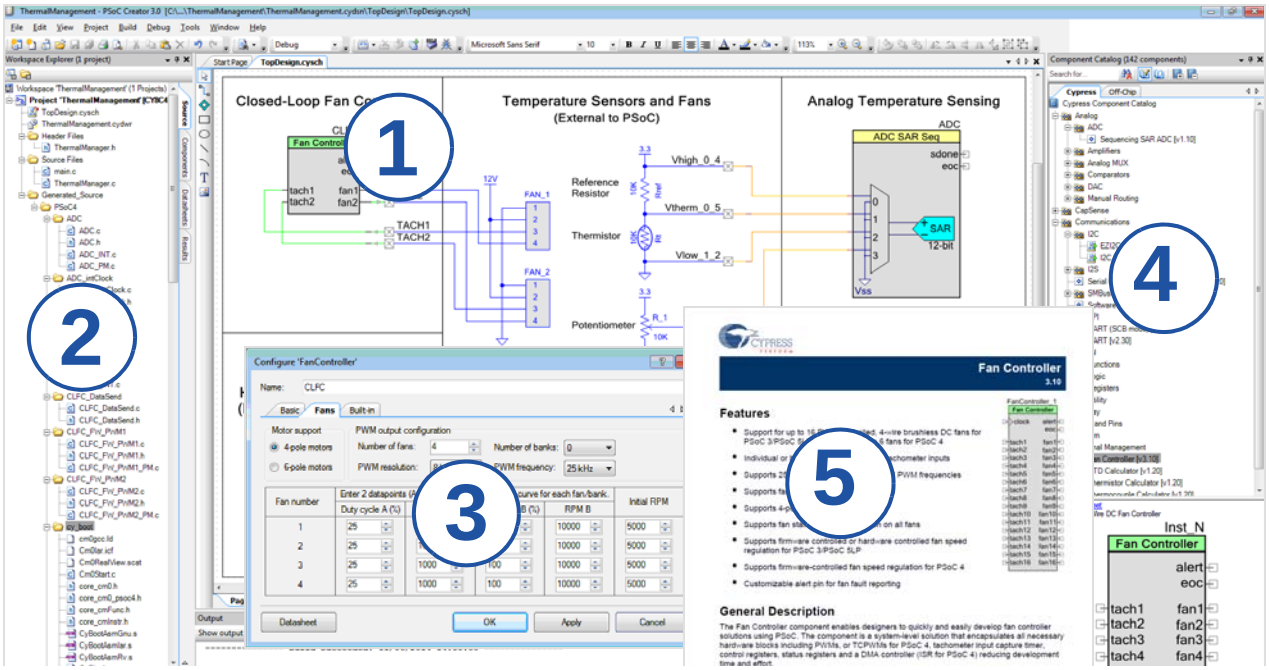
- Overview: PSoC Portfolio, PSoC Roadmap
- Product Selectors: PSoC 1, PSoC 3, PSoC 4, PRoC BLE, PSoC 4 BLE, PSoC 5LP In addition, PSoC Creator includes a device selection tool.
- Application Notes: Cypress offers a large number of PSoC application notes coverting a broad range of topics, from basic to advanced level. Recommended application notes for getting started with PRoC BLE are:
  - AN94020: Getting Started with PRoC BLE
  - AN97060: PSoC 4 BLE and PRoC BLE - Over-The-Air (OTA) Device Firmware Upgrade (DFU) Guide
  - AN91184: PSoC 4 BLE - Designing BLE Applications
  - AN91162: Creating a BLE Custom Profile
  - AN91445: Antenna Design and RF Layout Guidelines
  - AN96841: Getting Started With EZ-BLE Module
  - AN85951: PSoC 4 CapSense Design Guide
  - AN95089: PSoC 4/PRoC BLE Crystal Oscillator Selection and Tuning Techniques
  - AN92584: Designing for Low Power and Estimating Battery Life for BLE Applications
- Technical Reference Manual (TRM) is in two documents:
  - Architecture TRM details each PRoC BLE functional block
  - Registers TRM describes each of the PRoC BLE registers
- Development Kits:
  - CY8CKIT-042-BLE-A Pioneer Kit, is a flexible, Arduino-compatible, Bluetooth LE development kit for PSoC 4 BLE and PRoC BLE.
  - CY8CKIT-142, PSoC 4 BLE Module, features a PSoC 4 BLE device, two crystals for the antenna matching network, a PCB antenna and other passives, while providing access to all GPIOs of the device.
  - CY8CKIT-143, PSoC 4 BLE 256KB Module, features a PSoC 4 BLE 256KB device, two crystals for the antenna matching network, a PCB antenna and other passives, while providing access to all GPIOs of the device.
  - The MiniProg3 device provides an interface for flash programming and debug.

PSoC Creator

PSoC Creator is a free Windows-based Integrated Design Environment (IDE). It enables concurrent hardware and firmware design of PSoC 3, PSoC 4, and PSoC 5LP based systems. Create designs using classic, familiar schematic capture supported by over 100 pre-verified, production-ready PSoC Components; see the list of component datasheets. With PSoC Creator, you can:

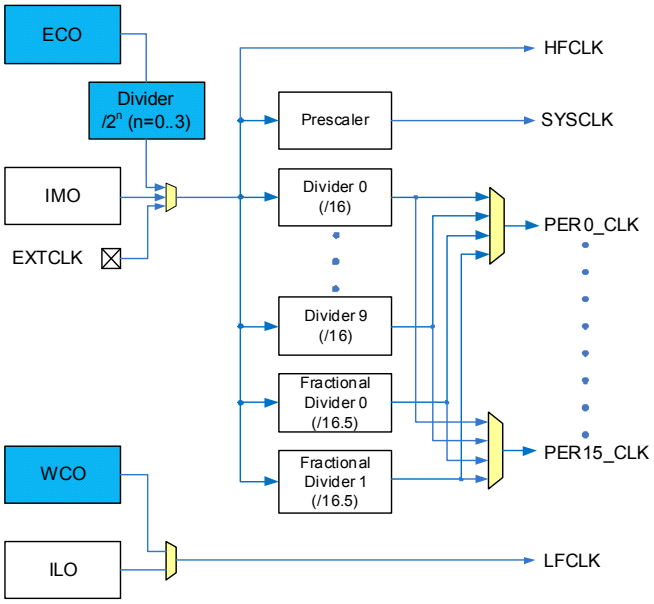
1. Drag and drop component icons to build your hardware system design in the main design workspace
2. Codesign your application firmware with the PSoC hardware, using the PSoC Creator IDE C compiler
3. Configure components using the configuration tools
4. Explore the library of 100+ components
5. Review component datasheets

Figure 1. Multiple-Sensor Example Project in PSoC Creator Contents



Contents

Figure 3. PSoC 4200_BL MCU Clocking Architecture



The HFCLK signal can be divided down (see Figure 3) to generate synchronous clocks for the UDBs, and the analog and digital peripherals. There are a total of 12 clock dividers for PSoC 4200_BL: ten with 16-bit divide capability and two with 16.5-bit divide capability. This allows the generation of 16 divided clock signals, which can be used by peripheral blocks. The analog clock leads the digital clocks to allow analog events to occur before the digital clock-related noise is generated. The 16-bit and 16.5-bit dividers allow a lot of flexibility in generating fine-grained frequency values and are fully supported in PSoC Creator.

Reset

PSoC 4200_BL device can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through resets and allows the software to determine the cause of the reset. An XRES pin is reserved for an external reset to avoid complications with the configuration and multiple pin functions during power-on or reconfiguration. The XRES pin has an internal pull-up resistor that is always enabled.

Voltage Reference

The PSoC 4200_BL reference system generates all internally required references. A one-percent voltage reference spec is provided for the 12-bit ADC. To allow better signal-to-noise ratios (SNR) and better absolute accuracy, it is possible to bypass the internal reference using a GPIO pin or use an external reference for the SAR. Refer to Table 19, “SAR ADC AC Specifications,” on page 26 for details.

BLE Radio and Subsystem

PSoC 4200_BL incorporates a Bluetooth Smart subsystem that contains the Physical Layer (PHY) and Link Layer (LL) engines with an embedded AES-128 security engine. The physical layer consists of the digital PHY and the RF transceiver that transmits and receives GFSK packets at 1 Mbps over a 2.4-GHz ISM band, which is compliant with Bluetooth Smart Bluetooth Specification 4.2. The baseband controller is a composite hardware and firmware implementation that supports both master and slave modes. Key protocol elements, such as HCI and link control, are implemented in firmware. Time-critical functional blocks, such as encryption, CRC, data whitening, and access code correlation, are implemented in hardware (in the LL engine).

The RF transceiver contains an integrated balun, which provides a single-ended RF port pin to drive a 50-Ω antenna via a matching/filtering network. In the receive direction, this block converts the RF signal from the antenna to a digital bit stream after performing GFSK demodulation. In the transmit direction, this block performs GFSK modulation and then converts a digital baseband signal to a radio frequency before transmitting it to air through the antenna.

The Bluetooth Smart Radio and Subsystem (BLESS) requires a 1.9-V minimum supply (the range varies from 1.9 V to 5.5 V).

Key features of BLESS are as follows:

- Master and slave single-mode protocol stack with logical link control and adaptation protocol (L2CAP), attribute (ATT), and security manager (SM) protocols
- API access to generic attribute profile (GATT), generic access profile (GAP), and L2CAP
- L2CAP connection-oriented channel
- GAP features
  - Broadcaster, Observer, Peripheral, and Central roles
  - Security mode 1: Level 1, 2, 3, and 4
  - Security mode 2: Level 1 and 2
  - User-defined advertising data
  - Multiple bond support
- GATT features
  - GATT client and server
  - Supports GATT sub-procedures
  - 32-bit universally unique identifier (UUID)
- Security Manager (SM)
  - Pairing methods: Just works, Passkey Entry, Out of Band and Numeric Comparison
  - Authenticated man-in-the-middle (MITM) protection and data signing
  - LE Secure Connections (Bluetooth 4.2 feature)
- Link Layer (LL)
  - Master and Slave roles
  - 128-bit AES engine
  - Encryption
  - Low-duty cycle advertising
  - LE Ping
  - LE Data Packet Length Extension (Bluetooth 4.2 feature)
  - Link Layer Privacy (with extended scanning filter policy, Bluetooth 4.2 feature)
- Supports all SIG-adopted BLE profiles

Pinouts

Table 1 shows the pin list for the PSoC 4200_BL device. Port 3 consists of the high-speed analog inputs for the SAR mux. All pins support CSD CapSense and analog mux bus connections.

Table 1. PSoC 4200_BL Pin List (QFN Package)

Pin	Name	Type	Description
1	VDDD	POWER	1.71-V to 5.5-V digital supply
2	XTAL32O/P6.0	CLOCK	32.768-kHz crystal
3	XTAL32I/P6.1	CLOCK	32.768-kHz crystal or external clock input
4	XRES	RESET	Reset, active LOW
5	P4.0	GPIO	Port 4 Pin 0, lcd, csd
6	P4.1	GPIO	Port 4 Pin 1, lcd, csd
7	P5.0	GPIO	Port 5 Pin 0, lcd, csd
8	P5.1	GPIO	Port 5 Pin 1, lcd, csd
9	VSSD	GROUND	Digital ground
10	VDDR	POWER	1.9-V to 5.5-V radio supply
11	GANT1	GROUND	Antenna shielding ground
12	ANT	ANTENNA	Antenna pin
13	GANT2	GROUND	Antenna shielding ground
14	VDDR	POWER	1.9-V to 5.5-V radio supply
15	VDDR	POWER	1.9-V to 5.5-V radio supply
16	XTAL24I	CLOCK	24-MHz crystal or external clock input
17	XTAL24O	CLOCK	24-MHz crystal
18	VDDR	POWER	1.9-V to 5.5-V radio supply
19	P0.0	GPIO	Port 0 Pin 0, lcd, csd
20	P0.1	GPIO	Port 0 Pin 1, lcd, csd
21	P0.2	GPIO	Port 0 Pin 2, lcd, csd
22	P0.3	GPIO	Port 0 Pin 3, lcd, csd
23	VDDD	POWER	1.71-V to 5.5-V digital supply
24	P0.4	GPIO	Port 0 Pin 4, lcd, csd
25	P0.5	GPIO	Port 0 Pin 5, lcd, csd
26	P0.6	GPIO	Port 0 Pin 6, lcd, csd
27	P0.7	GPIO	Port 0 Pin 7, lcd, csd
28	P1.0	GPIO	Port 1 Pin 0, lcd, csd
29	P1.1	GPIO	Port 1 Pin 1, lcd, csd
30	P1.2	GPIO	Port 1 Pin 2, lcd, csd
31	P1.3	GPIO	Port 1 Pin 3, lcd, csd
32	P1.4	GPIO	Port 1 Pin 4, lcd, csd
33	P1.5	GPIO	Port 1 Pin 5, lcd, csd
34	P1.6	GPIO	Port 1 Pin 6, lcd, csd
35	P1.7	GPIO	Port 1 Pin 7, lcd, csd
36	VDDA	POWER	1.71-V to 5.5-V analog supply
37	P2.0	GPIO	Port 2 Pin 0, lcd, csd
38	P2.1	GPIO	Port 2 Pin 1, lcd, csd
39	P2.2	GPIO	Port 2 Pin 2, lcd, csd

Table 1. PSoC 4200_BL Pin List (QFN Package) *(continued)*

Pin	Name	Type	Description
40	P2.3	GPIO	Port 2 Pin 3, lcd, csd
41	P2.4	GPIO	Port 2 Pin 4, lcd, csd
42	P2.5	GPIO	Port 2 Pin 5, lcd, csd
43	P2.6	GPIO	Port 2 Pin 6, lcd, csd
44	P2.7	GPIO	Port 2 Pin 7, lcd, csd
45	VREF	REF	1.024-V reference
46	VDDA	POWER	1.71-V to 5.5-V analog supply
47	P3.0	GPIO	Port 3 Pin 0, lcd, csd
48	P3.1	GPIO	Port 3 Pin 1, lcd, csd
49	P3.2	GPIO	Port 3 Pin 2, lcd, csd
50	P3.3	GPIO	Port 3 Pin 3, lcd, csd
51	P3.4	GPIO	Port 3 Pin 4, lcd, csd
52	P3.5	GPIO	Port 3 Pin 5, lcd, csd
53	P3.6	GPIO	Port 3 Pin 6, lcd, csd
54	P3.7	GPIO	Port 3 Pin 7, lcd, csd
55	VSSA	GROUND	Analog ground
56	VCCD	POWER	Regulated 1.8-V supply, connect to 1.3-µF capacitor.
57	EPAD	GROUND	Ground paddle for the QFN package

Table 2. PSoC 4200_BL Pin List (WLCSP Package)

Pin	Name	Type	Description
A1	NC	NC	Do not connect
A2	VREF	REF	1.024-V reference
A3	VSSA	GROUND	Analog ground
A4	P3.3	GPIO	Port 3 Pin 3, analog/digital/lcd/csd
A5	P3.7	GPIO	Port 3 Pin 7, analog/digital/lcd/csd
A6	VSSD	GROUND	Digital ground
A7	VSSA	GROUND	Analog ground
A8	VCCD	POWER	Regulated 1.8-V supply, connect to 1-µF capacitor
A9	VDDD	POWER	1.71-V to 5.5-V digital supply
B1	NB	NO BALL	No Ball
B2	P2.3	GPIO	Port 2 Pin 3, analog/digital/lcd/csd
B3	VSSA	GROUND	Analog ground
B4	P2.7	GPIO	Port 2 Pin 7, analog/digital/lcd/csd
B5	P3.4	GPIO	Port 3 Pin 4, analog/digital/lcd/csd
B6	P3.5	GPIO	Port 3 Pin 5, analog/digital/lcd/csd
B7	P3.6	GPIO	Port 3 Pin 6, analog/digital/lcd/csd
B8	XTAL32I/P6.1	CLOCK	32.768-kHz crystal or external clock input
B9	XTAL32O/P6.0	CLOCK	32.768-kHz crystal
C1	NC	NC	Do not connect

The selection of peripheral function for different GPIO pins is given in Table 4.

Table 4. Port Pin Connections

Name	Analog	Digital					
		GPIO	Active #0	Active #1	Active #2	Deep Sleep #0	Deep Sleep #1
P0.0	COMP0_INP	GPIO	TCPWM0_P[3]	SCB1_UART_RX[1]	–	SCB1_I2C_SDA[1]	SCB1_SPI_MOSI[1]
P0.1	COMP0_INN	GPIO	TCPWM0_N[3]	SCB1_UART_TX[1]	–	SCB1_I2C_SCL[1]	SCB1_SPI_MISO[1]
P0.2	–	GPIO	TCPWM1_P[3]	SCB1_UART_RTS[1]	–	COMP0_OUT[0]	SCB1_SPI_SS0[1]
P0.3	–	GPIO	TCPWM1_N[3]	SCB1_UART_CTS[1]	–	COMP1_OUT[0]	SCB1_SPI_SCLK[1]
P0.4	COMP1_INP	GPIO	TCPWM1_P[0]	SCB0_UART_RX[1]	EXT_CLK[0]/ ECO_OUT[0]	SCB0_I2C_SDA[1]	SCB0_SPI_MOSI[1]
P0.5	COMP1_INN	GPIO	TCPWM1_N[0]	SCB0_UART_TX[1]	–	SCB0_I2C_SCL[1]	SCB0_SPI_MISO[1]
P0.6	–	GPIO	TCPWM2_P[0]	SCB0_UART_RTS[1]	–	SWDIO[0]	SCB0_SPI_SS0[1]
P0.7	–	GPIO	TCPWM2_N[0]	SCB0_UART_CTS[1]	–	SWDCLK[0]	SCB0_SPI_SCLK[1]
P1.0	CTBm1_OA0_INP	GPIO	TCPWM0_P[1]	–	–	COMP0_OUT[1]	WCO_OUT[2]
P1.1	CTBm1_OA0_INN	GPIO	TCPWM0_N[1]	–	–	COMP1_OUT[1]	SCB1_SPI_SS1
P1.2	CTBm1_OA0_OUT	GPIO	TCPWM1_P[1]	–	–	–	SCB1_SPI_SS2
P1.3	CTBm1_OA1_OUT	GPIO	TCPWM1_N[1]	–	–	–	SCB1_SPI_SS3
P1.4	CTBm1_OA1_INN	GPIO	TCPWM2_P[1]	SCB0_UART_RX[0]	–	SCB0_I2C_SDA[0]	SCB0_SPI_MOSI[1]
P1.5	CTBm1_OA1_INP	GPIO	TCPWM2_N[1]	SCB0_UART_TX[0]	–	SCB0_I2C_SCL[0]	SCB0_SPI_MISO[1]
P1.6	CTBm1_OA0_INP	GPIO	TCPWM3_P[1]	SCB0_UART_RTS[0]	–	–	SCB0_SPI_SS0[1]
P1.7	CTBm1_OA1_INP	GPIO	TCPWM3_N[1]	SCB0_UART_CTS[0]	–	–	SCB0_SPI_SCLK[1]
P2.0	CTBm0_OA0_INP	GPIO	–	–	–	–	SCB0_SPI_SS1
P2.1	CTBm0_OA0_INN	GPIO	–	–	–	–	SCB0_SPI_SS2
P2.2	CTBm0_OA0_OUT	GPIO	–	–	–	WAKEUP	SCB0_SPI_SS3
P2.3	CTBm0_OA1_OUT	GPIO	–	–	–	–	WCO_OUT[1]
P2.4	CTBm0_OA1_INN	GPIO	–	–	–	–	–
P2.5	CTBm0_OA1_INP	GPIO	–	–	–	–	–
P2.6	CTBm0_OA0_INP	GPIO	–	–	–	–	–
P2.7	CTBm0_OA1_INP	GPIO	–	–	EXT_CLK[1]/ECO_OUT[1]	–	–
P3.0	SARMUX_0	GPIO	TCPWM0_P[2]	SCB0_UART_RX[2]	–	SCB0_I2C_SDA[2]	–
P3.1	SARMUX_1	GPIO	TCPWM0_N[2]	SCB0_UART_TX[2]	–	SCB0_I2C_SCL[2]	–
P3.2	SARMUX_2	GPIO	TCPWM1_P[2]	SCB0_UART_RTS[2]	–	–	–
P3.3	SARMUX_3	GPIO	TCPWM1_N[2]	SCB0_UART_CTS[2]	–	–	–
P3.4	SARMUX_4	GPIO	TCPWM2_P[2]	SCB1_UART_RX[2]	–	SCB1_I2C_SDA[2]	–
P3.5	SARMUX_5	GPIO	TCPWM2_N[2]	SCB1_UART_TX[2]	–	SCB1_I2C_SCL[2]	–
P3.6	SARMUX_6	GPIO	TCPWM3_P[2]	SCB1_UART_RTS[2]	–	–	–
P3.7	SARMUX_7	GPIO	TCPWM3_N[2]	SCB1_UART_CTS[2]	–	–	WCO_OUT[0]
P4.0	CMOD	GPIO	TCPWM0_P[0]	SCB1_UART_RTS[0]	–	–	SCB1_SPI_MOSI[0]
P4.1	CTANK	GPIO	TCPWM0_N[0]	SCB1_UART_CTS[0]	–	–	SCB1_SPI_MISO[0]
P5.0	–	GPIO	TCPWM3_P[0]	SCB1_UART_RX[0]	EXTPA_EN	SCB1_I2C_SDA[0]	SCB1_SPI_SS0[0]
P5.1	–	GPIO	TCPWM3_N[0]	SCB1_UART_TX[0]	EXT_CLK[2]/ECO_OUT[2]	SCB1_I2C_SCL[0]	SCB1_SPI_SCLK[0]
P6.0_XTAL32O	–	GPIO	–	–	–	–	–
P6.1_XTAL32I	–	GPIO	–	–	–	–	–

Table 6. DC Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID41	I_{DD31}	GPIO and reset active	–	–	–	nA	T = 25 °C
SID42	I_{DD32}	GPIO and reset active	–	–	–	nA	T = –40 °C to 85 °C
Stop Mode, V_{DD} = 1.8 to 3.6 V							
SID43	I_{DD33}	Stop mode current (V_{DD})	–	20	–	nA	T = 25 °C, V_{DD} = 3.3 V
SID44	I_{DD34}	Stop mode current (V_{DDR})	–	40	–-	nA	T = 25 °C, V_{DDR} = 3.3 V
SID45	I_{DD35}	Stop mode current (V_{DD})	–	–	–	nA	T = –40 °C to 85 °C
SID46	I_{DD36}	Stop mode current (V_{DDR})	–	–	–	nA	T = –40 °C to 85 °C, V_{DDR} = 1.9 V to 3.6 V
Stop Mode, V_{DD} = 3.6 to 5.5 V							
SID47	I_{DD37}	Stop mode current (V_{DD})	–	–	–	nA	T = 25 °C, V_{DD} = 5 V
SID48	I_{DD38}	Stop mode current (V_{DDR})	–	–	–	nA	T = 25 °C, V_{DDR} = 5 V
SID49	I_{DD39}	Stop mode current (V_{DD})	–	–	–	nA	T = –40 °C to 85 °C
SID50	I_{DD40}	Stop mode current (V_{DDR})	–	–	–	nA	T = –40 °C to 85 °C
Stop Mode, V_{DD} = 1.71 to 1.89 V (Regulator Bypassed)							
SID51	I_{DD41}	Stop mode current (V_{DD})	–	–	–	nA	T = 25 °C
SID52	I_{DD42}	Stop mode current (V_{DD})	–	–	–	nA	T = –40 °C to 85 °C

Table 7. AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID53	F_{CPU}	CPU frequency	DC	–	48	MHz	1.71 V ≤ V_{DD} ≤ 5.5 V
SID54	T_{SLEEP}	Wakeup from Sleep mode	–	0	–	µs	Guaranteed by characterization
SID55	$T_{DEEPSLEEP}$	Wakeup from Deep Sleep mode	–	–	25	µs	24-MHz IMO. Guaranteed by characterization.
SID56	$T_{HIBERNATE}$	Wakeup from Hibernate mode	–	–	0.7	ms	Guaranteed by characterization
SID57	T_{STOP}	Wakeup from Stop mode	–	–	2.2	ms	Guaranteed by characterization

Table 13. XRES AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID93	$T_{RESETWIDTH}$	Reset pulse width	1	–	–	µs	–

Analog Peripherals

Opamp

Table 14. Opamp Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
I_{DD} (Opamp Block Current. V_{DD} = 1.8 V. No Load)							
SID94	I_{DD_HI}	Power = high	–	1000	1850	µA	–
SID95	I_{DD_MED}	Power = medium	–	500	950	µA	–
SID96	I_{DD_LOW}	Power = low	–	250	350	µA	–
GBW (Load = 20 pF, 0.1 mA. V_{DDA} = 2.7 V)							
SID97	GBW_HI	Power = high	6	–	–	MHz	–
SID98	GBW_MED	Power = medium	4	–	–	MHz	–
SID99	GBW_LO	Power = low	–	1	–	MHz	–
I_{OUT_MAX} (V_{DDA} ≥ 2.7 V, 500 mV From Rail)							
SID100	$I_{OUT\_MAX\_HI}$	Power = high	10	–	–	mA	–
SID101	$I_{OUT\_MAX\_MID}$	Power = medium	10	–	–	mA	–
SID102	$I_{OUT\_MAX\_LO}$	Power = low	–	5	–	mA	–
I_{OUT} (V_{DDA} = 1.71 V, 500 mV From Rail)							
SID103	$I_{OUT\_MAX\_HI}$	Power = high	4	–	–	mA	–
SID104	$I_{OUT\_MAX\_MID}$	Power = medium	4	–	–	mA	–
SID105	$I_{OUT\_MAX\_LO}$	Power = low	–	2	–	mA	–
SID106	V_{IN}	Charge pump on, V_{DDA} ≥ 2.7 V	–0.05	–	V_{DDA} – 0.2	V	–
SID107	V_{CM}	Charge pump on, V_{DDA} ≥ 2.7 V	–0.05	–	V_{DDA} – 0.2	V	–
V_{OUT} (V_{DDA} ≥ 2.7 V)							
SID108	V_{OUT_1}	Power = high, I_{LOAD}=10 mA	0.5	–	V_{DDA} – 0.5	V	–
SID109	V_{OUT_2}	Power = high, I_{LOAD}=1 mA	0.2	–	V_{DDA} – 0.2	V	–
SID110	V_{OUT_3}	Power = medium, I_{LOAD}=1 mA	0.2	–	V_{DDA} – 0.2	V	–
SID111	V_{OUT_4}	Power = low, I_{LOAD}=0.1 mA	0.2	–	V_{DDA} – 0.2	V	–
SID112	V_{OS_TR}	Offset voltage, trimmed	1	±0.5	1	mV	High mode
SID113	V_{OS_TR}	Offset voltage, trimmed	–	±1	–	mV	Medium mode
SID114	V_{OS_TR}	Offset voltage, trimmed	–	±2	–	mV	Low mode
SID115	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–10	±3	10	µV/C	High mode
SID116	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–	±10	–	µV/C	Medium mode
SID117	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–	±10	–	µV/C	Low mode
SID118	CMRR	DC	70	80	–	dB	V_{DDD} = 3.6-V
SID119	PSRR	At 1 kHz, 100-mV ripple	70	85	–	dB	V_{DDD} = 3.6-V
Noise							
SID120	V_{N1}	Input referred, 1 Hz–1 GHz, power = high	–	94	–	µVrms	–
SID121	V_{N2}	Input referred, 1-kHz, power = high	–	72	–	nV/rtHz	–

Table 19. SAR ADC AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID167	A_psrr	Power supply rejection ratio	70	–	–	dB	Measured at 1-V reference
SID168	A_cmrr	Common mode rejection ratio	66	–	–	dB	–
SID169	A_samp	Sample rate	–	–	1	Msps	
SID313	Fsarintref	SAR operating speed without external ref. bypass	–	–	100	Ksps	12-bit resolution
SID170	A_snr	Signal-to-noise ratio (SNR)	65	–	–	dB	Fin = 10 kHz
SID171	A_bw	Input bandwidth without aliasing	–	–	A_samp/2	kHz	–
SID172	A_inl	Integral non linearity. V_{DD} = 1.71 to 5.5 V, 1 Msps	–1.7	–	2	LSB	Vref = 1 V to V_{DD}
SID173	A_INL	Integral non linearity. V_{DDD} = 1.71 to 3.6 V, 1 Msps	–1.5	–	1.7	LSB	Vref = 1.71 V to V_{DD}
SID174	A_INL	Integral non linearity. V_{DD} = 1.71 to 5.5 V, 500 Ksps	–1.5	–	1.7	LSB	Vref = 1 V to V_{DD}
SID175	A_dnl	Differential non linearity. V_{DD} = 1.71 to 5.5 V, 1 Msps	–1	–	2.2	LSB	Vref = 1 V to V_{DD}
SID176	A_DNL	Differential non linearity. V_{DD} = 1.71 to 3.6 V, 1 Msps	–1	–	2	LSB	Vref = 1.71 V to V_{DD}
SID177	A_DNL	Differential non linearity. V_{DD} = 1.71 to 5.5 V, 500 Ksps	–1	–	2.2	LSB	Vref = 1 V to V_{DD}
SID178	A_thd	Total harmonic distortion	–	–	–65	dB	Fin = 10 kHz

CSD

Table 20. CSD Block Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID179	V_{CSD}	Voltage range of operation	1.71	–	5.5	V	–
SID180	IDAC1	DNL for 8-bit resolution	–1	–	1	LSB	–
SID181	IDAC1	INL for 8-bit resolution	–3	–	3	LSB	–
SID182	IDAC2	DNL for 7-bit resolution	–1	–	1	LSB	–
SID183	IDAC2	INL for 7-bit resolution	–3	–	3	LSB	–
SID184	SNR	Ratio of counts of finger to noise	5	–	–	Ratio	Capacitance range of 9 to 35 pF, 0.1 pF sensitivity. Radio is not operating during the scan
SID185	I_{DAC1_CRT1}	Output current of IDAC1 (8 bits) in High range	–	612	–	µA	–
SID186	I_{DAC1_CRT2}	Output current of IDAC1 (8 bits) in Low range	–	306	–	µA	–
SID187	I_{DAC2_CRT1}	Output current of IDAC2 (7 bits) in High range	–	305	–	µA	–
SID188	I_{DAC2_CRT2}	Output current of IDAC2 (7 bits) in Low range	–	153	–	µA	–

Table 26. PWM AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID214	$T_{PWMFREQ}$	Operating frequency	F_{CLK}	–	48	MHz	–
SID215	$T_{PWMPWINT}$	Pulse width (internal)	2 × T_{CLK}	–	–	ns	–
SID216	T_{PWMEXT}	Pulse width (external)	2 × T_{CLK}	–	–	ns	–
SID217	$T_{PWMKILLINT}$	Kill pulse width (internal)	2 × T_{CLK}	–	–	ns	–
SID218	$T_{PWMKILLEXT}$	Kill pulse width (external)	2 × T_{CLK}	–	–	ns	–
SID219	$T_{PWMEINT}$	Enable pulse width (internal)	2 × T_{CLK}	–	–	ns	–
SID220	$T_{PWMENEXT}$	Enable pulse width (external)	2 × T_{CLK}	–	–	ns	–
SID221	$T_{PWMRESWINT}$	Reset pulse width (internal)	2 × T_{CLK}	–	–	ns	–
SID222	$T_{PWMRESWEXT}$	Reset pulse width (external)	2 × T_{CLK}	–	–	ns	–

I^2C

Table 27. Fixed I^2C DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID223	I_{I2C1}	Block current consumption at 100 kHz	–	–	50	µA	–
SID224	I_{I2C2}	Block current consumption at 400 kHz	–	–	155	µA	–
SID225	I_{I2C3}	Block current consumption at 1 Mbps	–	–	390	µA	–
SID226	I_{I2C4}	I^2C enabled in Deep Sleep mode	–	–	1.4	µA	–

Table 28. Fixed I^2C AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID227	F_{I2C1}	Bit rate	–	–	1	Mbps	–

LCD Direct Drive

Table 29. LCD Direct Drive DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID228	I_{LCDLOW}	Operating current in low-power mode	–	17.5	–	µA	16 × 4 small segment display at 50 Hz
SID229	C_{LCDCAP}	LCD capacitance per segment/common driver	–	500	5000	pF	–
SID230	LCD_{OFFSET}	Long-term segment offset	–	20	–	mV	–
SID231	I_{LCDOP1}	LCD system operating current V_{BIAS} = 5 V.	–	2	–	mA	32 × 4 segments. 50 Hz at 25 °C
SID232	I_{LCDOP2}	LCD system operating current. V_{BIAS} = 3.3 V	–	2	–	mA	32 × 4 segments 50 Hz at 25 °C

Table 30. LCD Direct Drive AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID233	F_{LCD}	LCD frame rate	10	50	150	Hz	–

Table 31. Fixed UART DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID234	I_{UART1}	Block current consumption at 100 kbps	–	–	55	µA	–
SID235	I_{UART2}	Block current consumption at 1000 kbps	–	–	360	µA	–

Table 32. Fixed UART AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID236	F_{UART}	Bit rate	–	–	1	Mbps	–

SPI Specifications

Table 33. Fixed SPI DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID237	I_{SPI1}	Block current consumption at 1 Mbps	–	–	360	µA	–
SID238	I_{SPI2}	Block current consumption at 4 Mbps	–	–	560	µA	–
SID239	I_{SPI3}	Block current consumption at 8 Mbps	–	–	600	µA	–

Table 34. Fixed SPI AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID240	F_{SPI}	SPI operating frequency (master; 6X oversampling)	–	–	8	MHz	–

Table 35. Fixed SPI Master Mode AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID241	T_{DMO}	MOSI valid after Sclock driving edge	–	–	18	ns	–
SID242	T_{DSI}	MISO valid before Sclock capturing edge. Full clock, late MISO sampling used	20	–	–	ns	Full clock, late MISO sampling
SID243	T_{HMO}	Previous MOSI data hold time	0	–	–	ns	Referred to Slave capturing edge

Table 36. Fixed SPI Slave Mode AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID244	T_{DMI}	MOSI valid before Sclock capturing edge	40	–	–	ns	–
SID245	T_{DSO}	MISO valid after Sclock driving edge	–	–	$42 + 3 \times T_{CPU}$	ns	–
SID246	T_{DSO_ext}	MISO valid after Sclock driving edge in external clock mode	–	–	53	ns	$V_{DD} < 3.0$ V
SID247	T_{HSO}	Previous MISO data hold time	0	–	–	ns	–
SID248	$T_{SSELSCK}$	SSEL valid to first SCK valid edge	100	–	–	ns	–

Memory

Table 37. Flash DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID249	V_{PE}	Erase and program voltage	1.71	–	5.5	V	–
SID309	T_{WS48}	Number of Wait states at 32–48 MHz	2	–	–		CPU execution from flash
SID310	T_{WS32}	Number of Wait states at 16–32 MHz	1	–	–		CPU execution from flash
SID311	T_{WS16}	Number of Wait states for 0–16 MHz	0	–	–		CPU execution from flash

Table 38. Flash AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID250	$T_{ROWWRITE}$[5]	Row (block) write time (erase and program)	–	–	20	ms	Row (block) = 128 bytes for 128 KB flash devices Row (block) = 256 bytes for 256 KB flash devices
SID251	$T_{ROWERASE}$[5]	Row erase time	–	–	13	ms	–
SID252	$T_{ROWPROGRAM}$[5]	Row program time after erase	–	–	7	ms	–
SID253	$T_{BULKERASE}$[5]	Bulk erase time (256 KB)	–	–	35	ms	–
SID254	$T_{DEVPROG}$[5]	Total device program time	–	–	50	seconds	256 KB
SID254A			–	–	25		128 KB
SID255	F_{END}	Flash endurance	100 K	–	–	cycles	–
SID256	F_{RET}	Flash retention. $T_A \leq 55$ °C, 100 K P/E cycles	20	–	–	years	–
SID257	F_{RET2}	Flash retention. $T_A \leq 85$ °C, 10 K P/E cycles	10	–	–	years	–

System Resources

Power-on-Reset (POR)

Table 39. POR DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID258	$V_{RISEIPOR}$	Rising trip voltage	0.80	–	1.45	V	–
SID259	$V_{FALLIPOR}$	Falling trip voltage	0.75	–	1.40	V	–
SID260	$V_{IPORHYST}$	Hysteresis	15	–	200	mV	–

Table 40. POR AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID264	T_{PPOR_TR}	PPOR response time in Active and Sleep modes	–	–	1	µs	–

Table 41. Brown-Out Detect

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID261	$V_{FALLPPOR}$	BOD trip voltage in Active and Sleep modes	1.64	–	–	V	–
SID262	$V_{FALLDPSLP}$	BOD trip voltage in Deep Sleep mode	1.4	–	–	V	–

Table 42. Hibernate Reset

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID263	$V_{HBRTRIP}$	BOD trip voltage in Hibernate mode	1.1	–	–	V	–

Note

5. It can take as much as 20 milliseconds to write to flash. During this time, the device should not be reset, or flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.

Voltage Monitors

Table 43. Voltage Monitor DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID265	V_{LVI1}	LVI_A/D_SEL[3:0] = 0000b	1.71	1.75	1.79	V	–
SID266	V_{LVI2}	LVI_A/D_SEL[3:0] = 0001b	1.76	1.80	1.85	V	–
SID267	V_{LVI3}	LVI_A/D_SEL[3:0] = 0010b	1.85	1.90	1.95	V	–
SID268	V_{LVI4}	LVI_A/D_SEL[3:0] = 0011b	1.95	2.00	2.05	V	–
SID269	V_{LVI5}	LVI_A/D_SEL[3:0] = 0100b	2.05	2.10	2.15	V	–
SID270	V_{LVI6}	LVI_A/D_SEL[3:0] = 0101b	2.15	2.20	2.26	V	–
SID271	V_{LVI7}	LVI_A/D_SEL[3:0] = 0110b	2.24	2.30	2.36	V	–
SID272	V_{LVI8}	LVI_A/D_SEL[3:0] = 0111b	2.34	2.40	2.46	V	–
SID273	V_{LVI9}	LVI_A/D_SEL[3:0] = 1000b	2.44	2.50	2.56	V	–
SID274	V_{LVI10}	LVI_A/D_SEL[3:0] = 1001b	2.54	2.60	2.67	V	–
SID2705	V_{LVI11}	LVI_A/D_SEL[3:0] = 1010b	2.63	2.70	2.77	V	–
SID276	V_{LVI12}	LVI_A/D_SEL[3:0] = 1011b	2.73	2.80	2.87	V	–
SID277	V_{LVI13}	LVI_A/D_SEL[3:0] = 1100b	2.83	2.90	2.97	V	–
SID278	V_{LVI14}	LVI_A/D_SEL[3:0] = 1101b	2.93	3.00	3.08	V	–
SID279	V_{LVI15}	LVI_A/D_SEL[3:0] = 1110b	3.12	3.20	3.28	V	–
SID280	V_{LVI16}	LVI_A/D_SEL[3:0] = 1111b	4.39	4.50	4.61	V	–
SID281	LVI_IDD	Block current	–	–	100	µA	–

Table 44. Voltage Monitor AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID282	$T_{MONTRIP}$	Voltage monitor trip time	–	–	1	µs	–

SWD Interface

Table 45. SWD Interface Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID283	F_SWDCLK1	$3.3\ V \le V_{DD} \le 5.5\ V$	–	–	14	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID284	F_SWDCLK2	$1.71\ V \le V_{DD} \le 3.3\ V$	–	–	7	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID285	T_SWDI_SETUP	T = 1/f SWDCLK	0.25 × T	–	–	ns	–
SID286	T_SWDI_HOLD	T = 1/f SWDCLK	0.25 × T	–	–	ns	–
SID287	T_SWDO_VALID	T = 1/f SWDCLK	–	–	0.5 × T	ns	–
SID288	T_SWDO_HOLD	T = 1/f SWDCLK	1	–	–	ns	–

Internal Main Oscillator

Table 46. IMO DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID289	I_{IMO1}	IMO operating current at 48 MHz	–	–	1000	µA	–
SID290	I_{IMO2}	IMO operating current at 24 MHz	–	–	325	µA	–
SID291	I_{IMO3}	IMO operating current at 12 MHz	–	–	225	µA	–
SID292	I_{IMO4}	IMO operating current at 6 MHz	–	–	180	µA	–
SID293	I_{IMO5}	IMO operating current at 3 MHz	–	–	150	µA	–

Table 52. BLE Subsystem *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID378	ITX,-6dBm	TX current at –6-dBm setting (PA3)	–	14.5	–	mA	–
SID379	ITX,-12dBm	TX current at –12-dBm setting (PA2)	–	13.2	–	mA	–
SID380	ITX,-18dBm	TX current at –18-dBm setting (PA1)	–	12.5	–	mA	–
SID380A	Iavg_1sec, 0dBm	Average current at 1-second BLE connection interval	–	17.1	–	µA	TXP: 0 dBm; ±20-ppm master and slave clock accuracy.
SID380B	Iavg_4sec, 0dBm	Average current at 4-second BLE connection interval	–	6.1	–	µA	TXP: 0 dBm; ±20-ppm master and slave clock accuracy.
General RF Specifications							
SID381	FREQ	RF operating frequency	2400	–	2482	MHz	–
SID382	CHBW	Channel spacing	–	2	–	MHz	–
SID383	DR	On-air data rate	–	1000	–	kbps	–
SID384	IDLE2TX	BLE.IDLE to BLE. TX transition time	–	120	140	µs	–
SID385	IDLE2RX	BLE.IDLE to BLE. RX transition time	–	75	120	µs	–
RSSI Specifications							
SID386	RSSI, ACC	RSSI accuracy	–	±5	–	dB	–
SID387	RSSI, RES	RSSI resolution	–	1	–	dB	–
SID388	RSSI, PER	RSSI sample period	–	6	–	µs	–

Table 53. ECO Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID389	F_{ECO}	Crystal frequency	–	24	–	MHz	–
SID390	F_{TOL}	Frequency tolerance	–50	–	50	ppm	–
SID391	ESR	Equivalent series resistance	–	–	60	Ω	–
SID392	PD	Drive level	–	–	100	µW	–
SID393	T_{START1}	Startup time (Fast Charge on)	–	–	850	µs	–
SID394	T_{START2}	Startup time (Fast Charge off)	–	–	3	ms	–
SID395	C_L	Load capacitance	–	8	–	pF	–
SID396	C0	Shunt capacitance	–	1.1	–	pF	–
SID397	I_{ECO}	Operating current	–	1400	–	µA	–

Table 54. WCO Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID398	F_{WCO}	Crystal frequency	–	32.768	–	kHz	–
SID399	FTOL	Frequency tolerance	–	50	–	ppm	–
SID400	ESR	Equivalent series resistance	–	50	–	kΩ	–
SID401	PD	Drive level	–	–	1	µW	–
SID402	T_{START}	Startup time	–	–	500	ms	–
SID403	C_L	Crystal load capacitance	6	–	12.5	pF	–
SID404	C0	Crystal shunt capacitance	–	1.35	–	pF	–
SID405	I_{WCO1}	Operating current (High-Power mode)	–	–	8	µA	–
SID406	I_{WCO2}	Operating current (Low-Power mode)	–	–	2.6	µA	–

Ordering Information

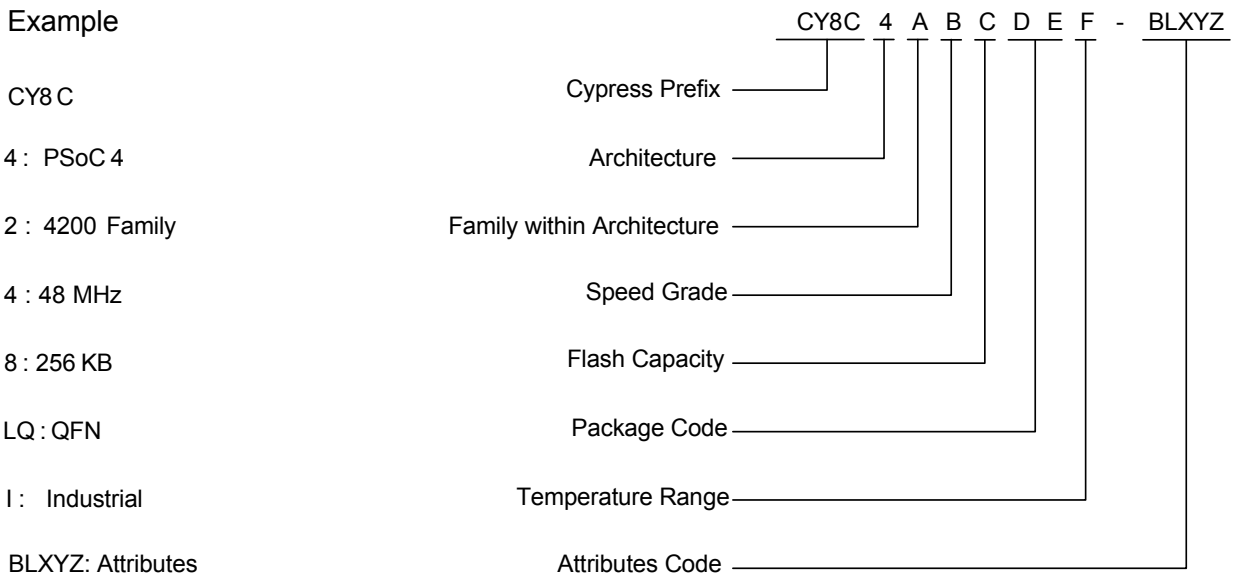
The PSoC 4200_BL part numbers and features are listed in Table 55.

Table 55. PSoC 4200_BL Part Numbers

Product Family	MPN	Max CPU Speed (MHz)	BLE subsystem	Flash (KB)	SRAM (KB)	UDB	Opamp	CapSense	TMG (Gestures)	Direct LCD Drive	12-bit SAR ADC	DMA	LP Comparators	TCPWM Blocks	SCB Blocks	GPIO	Package	Temperature Range
PSoC 4200_BL	CY8C4247LQI-BL473	48	4.1	128	16	4	4	–	–	–	1 Msps	–	2	4	2	36	QFN	85 °C
	CY8C4247FNI-BL473	48	4.1	128	16	4	4	–	–	–	1 Msps	–	2	4	2	36	CSP	85 °C
	CY8C4247LQI-BL453	48	4.1	128	16	4	4	1	–	–	1 Msps	–	2	4	2	36	QFN	85 °C
	CY8C4247LQI-BL463	48	4.1	128	16	4	4	–	–	1	1 Msps	–	2	4	2	36	QFN	85 °C
	CY8C4247LQI-BL483	48	4.1	128	16	4	4	1	–	1	1 Msps	–	2	4	2	36	QFN	85 °C
	CY8C4247LQI-BL493	48	4.1	128	16	4	4	1	1	1	1 Msps	–	2	4	2	36	QFN	85 °C
	CY8C4247FNI-BL483	48	4.1	128	16	4	4	1	–	1	1 Msps	–	2	4	2	36	68-CSP	85 °C
	CY8C4247FNI-BL493	48	4.1	128	16	4	4	1	1	1	1 Msps	–	2	4	2	36	68-CSP	85 °C
	CY8C4247FNQ-BL483	48	4.1	128	16	4	4	1	–	1	1 Msps	–	2	4	2	36	68-CSP	105 °C
	CY8C4247LQQ-BL483	48	4.1	128	16	4	4	1	–	1	1 Msps	–	2	4	2	36	QFN	105 °C
	CY8C4247FLI-BL493	48	4.1	128	16	4	4	1	1	1	1 Msps	–	2	4	2	36	Thin 68-CSP	85 °C
	CY8C4248LQI-BL473	48	4.1	256	32	4	4	–	–	–	1 Msps	1	2	4	2	36	QFN	85 °C
	CY8C4248LQI-BL453	48	4.1	256	32	4	4	1	–	–	1 Msps	1	2	4	2	36	QFN	85 °C
	CY8C4248LQI-BL483	48	4.1	256	32	4	4	1	–	1	1 Msps	1	2	4	2	36	QFN	85 °C
	CY8C4248FNI-BL483	48	4.1	256	32	4	4	1	–	1	1 Msps	1	2	4	2	36	76-CSP	85 °C
	CY8C4248FLI-BL483	48	4.1	256	32	4	4	1	–	1	1 Msps	1	2	4	2	36	Thin 76-CSP	85 °C
	CY8C4248LQI-BL543	48	4.2	256	32	–	2	–	–	–	1 Msps	1	–	4	2	36	QFN	85 °C
	CY8C4248FNI-BL543	48	4.2	256	32	–	2	–	–	–	1 Msps	1	–	4	2	36	76-CSP	85 °C
	CY8C4248LQI-BL573	48	4.2	256	32	4	4	–	–	–	1 Msps	1	2	4	2	36	QFN	85 °C
	CY8C4248FNI-BL573	48	4.2	256	32	4	4	–	–	–	1 Msps	1	2	4	2	36	76-CSP	85 °C
	CY8C4248LQI-BL553	48	4.2	256	32	4	4	1	–	–	1 Msps	1	2	4	2	36	QFN	85 °C
	CY8C4248FNI-BL553	48	4.2	256	32	4	4	1	–	–	1 Msps	1	2	4	2	36	76-CSP	85 °C
	CY8C4248LQI-BL563	48	4.2	256	32	4	4	–	–	1	1 Msps	1	2	4	2	36	QFN	85 °C
	CY8C4248FNI-BL563	48	4.2	256	32	4	4	–	–	1	1 Msps	1	2	4	2	36	76-CSP	85 °C
	CY8C4248LQI-BL583	48	4.2	256	32	4	4	1	–	1	1 Msps	1	2	4	2	36	QFN	85 °C
	CY8C4248FNI-BL583	48	4.2	256	32	4	4	1	–	1	1 Msps	1	2	4	2	36	76-CSP	85 °C
	CY8C4248FLI-BL583	48	4.2	256	32	4	4	1	–	1	1 Msps	1	2	4	2	36	Thin 76-CSP	85 °C
	CY8C4248LQQ-BL583	48	4.2	256	32	4	4	1	–	1	1 Msps	1	2	4	2	36	QFN	105 °C
	CY8C4248FNQ-BL583	48	4.2	256	32	4	4	1	–	1	1 Msps	1	2	4	2	36	76-CSP	105 °C
	CY8C4248LQI-BL593	48	4.2	256	32	4	4	1	1	1	1 Msps	1	2	4	2	36	QFN	85 °C
	CY8C4248FNI-BL593	48	4.2	256	32	4	4	1	1	1	1 Msps	1	2	4	2	36	76-CSP	85 °C

PSoC 4 devices follow the part numbering convention described in the following table. All fields are single-character alphanumeric (0, 1, 2, …, 9, A,B, …, Z) unless stated otherwise.

Ordering Code Definitions



The Field Values are listed in the following table:

Field	Description	Values	Meaning
CY8C	Cypress Prefix		
4	Architecture	4	PSoC 4
A	Family within architecture	2	4200-BLE Family
B	CPU Speed	4	48 MHz
C	Flash Capacity	8, 7	256, 128 KB respectively
DE	Package Code	FN	WLCSP
		LQ	QFN
		FL	Thin CSP
F	Temperature Range	I	Industrial
BLXYZ	Attributes Code	BL400-BL499	Bluetooth 4.1 compliant
		BL500-BL599	Bluetooth 4.2 compliant

Packaging

Table 56. Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
T_A	Operating ambient temperature	–	–40	25.00	105	°C
T_J	Operating junction temperature	–	–40	–	125	°C
T_{JA}	Package θ_{JA} (56-pin QFN)	–	–	16.9	–	°C/watt
T_{JC}	Package θ_{JC} (56-pin QFN)	–	–	9.7	–	°C/watt
T_{JA}	Package θ_{JA} (76-ball WLCSP)	–	–	20.1	–	°C/watt
T_{JC}	Package θ_{JC} (76-ball WLCSP)	–	–	0.19	–	°C/watt
T_{JA}	Package θ_{JA} (76-ball Thin WLCSP)	–	–	20.9	–	°C/watt
T_{JC}	Package θ_{JC} (76-ball Thin WLCSP)	–	–	0.17	–	°C/watt
T_{JA}	Package θ_{JA} (68-ball WLCSP)		–	16.6	–	°C/watt
T_{JC}	Package θ_{JC} (68-ball WLCSP)		–	0.19	–	°C/watt
T_{JA}	Package θ_{JA} (68-ball Thin WLCSP)		–	16.6	–	°C/watt
T_{JC}	Package θ_{JC} (68-ball Thin WLCSP)		–	0.19	–	°C/watt

Table 57. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
All packages	260 °C	30 seconds

Table 58. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
56-pin QFN	MSL 3
All WLCSP packages	MSL 1

Table 59. Package Details

Spec ID	Package	Description
001-58740 Rev. *C	56-pin QFN	7.0 mm × 7.0 mm × 0.6 mm
001-96603 Rev. *A	76-ball WLCSP	4.04 mm × 3.87 mm × 0.55 mm
002-10658, Rev. **	76-ball thin WLCSP	4.04 mm × 3.87 mm × 0.4 mm
001-92343 Rev. *A	68-ball WLCSP	3.52 mm × 3.91 mm × 0.55 mm
001-99408 Rev **	68-ball Thin WLCSP	52 mm × 3.91 mm × 0.4 mm

Table 60. Acronyms Used in this Document *(continued)*

Acronym	Description
PC	program counter
PCB	printed circuit board
PGA	programmable gain amplifier
PHUB	peripheral hub
PHY	physical layer
PICU	port interrupt control unit
PLA	programmable logic array
PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration data sheet
POR	power-on reset
PRES	precise power-on reset
PRS	pseudo random sequence
PS	port read data register
PSoC®	Programmable System-on-Chip™
PSRR	power supply rejection ratio
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I^2C serial clock
SDA	I^2C serial data
S/H	sample and hold
SINAD	signal to noise and distortion ratio
SIO	special input/output, GPIO with advanced features. See GPIO.
SOC	start of conversion
SOF	start of frame
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory
SRES	software reset
SWD	serial wire debug, a test protocol

Table 60. Acronyms Used in this Document *(continued)*

Acronym	Description
SWV	single-wire viewer
TD	transaction descriptor, see also DMA
THD	total harmonic distortion
TIA	transimpedance amplifier
TRM	technical reference manual
TTL	transistor-transistor logic
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UDB	universal digital block
USB	Universal Serial Bus
USBIO	USB input/output, PSoC pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset I/O pin
XTAL	crystal

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