# Infineon Technologies - CY8C4247LQI-BL493 Datasheet

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0 |
| Core Size | 32-Bit Single-Core |
| Speed | 48MHz |
| Connectivity | I²C, IrDA, LINbus, Microwire, SmartCard, SPI, SSP, UART/USART |
| Peripherals | Bluetooth, Brown-out Detect/Reset, Cap Sense, LCD, LVD, POR, PWM, SmartCard, SmartSense, WDT |
| Number of I/O | 36 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.71V ~ 5.5V |
| Data Converters | A/D 8x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 56-UFQFN Exposed Pad |
| Supplier Device Package | 56-QFN (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4247lqi-bl493 |

## More Information

Cypress provides a wealth of data at http://www.cypress.com to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the introduction page for Bluetooth® Low Energy (BLE) Products. Following is an abbreviated list for PRoC BLE:

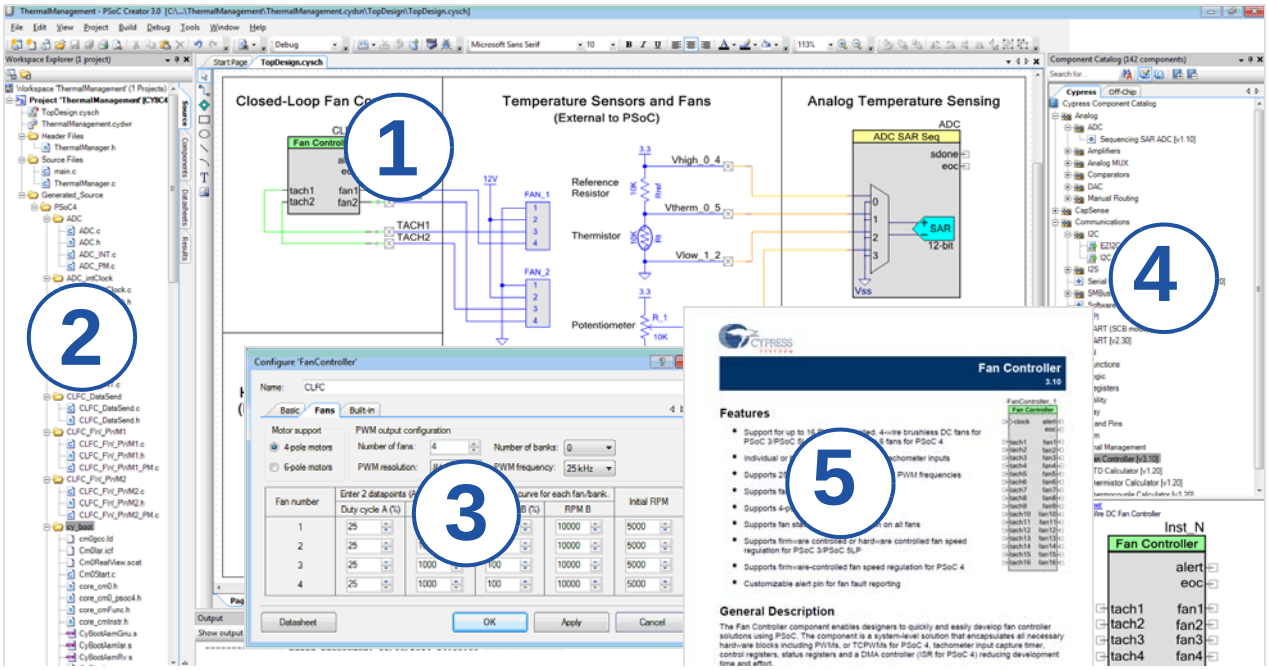
- Overview: PSoC Portfolio, PSoC Roadmap
- Product Selectors: PSoC 1, PSoC 3, PSoC 4, PRoC BLE, PSoC 4 BLE, PSoC 5LP In addition, PSoC Creator includes a device selection tool.
- Application Notes: Cypress offers a large number of PSoC application notes coverting a broad range of topics, from basic to advanced level. Recommended application notes for getting started with PRoC BLE are:
  - AN94020: Getting Started with PRoC BLE
  - AN97060: PSoC 4 BLE and PRoC BLE - Over-The-Air (OTA) Device Firmware Upgrade (DFU) Guide
  - AN91184: PSoC 4 BLE - Designing BLE Applications
  - AN91162: Creating a BLE Custom Profile
  - AN91445: Antenna Design and RF Layout Guidelines
  - AN96841: Getting Started With EZ-BLE Module
  - AN85951: PSoC 4 CapSense Design Guide
  - AN95089: PSoC 4/PRoC BLE Crystal Oscillator Selection and Tuning Techniques
  - AN92584: Designing for Low Power and Estimating Battery Life for BLE Applications
- Technical Reference Manual (TRM) is in two documents:
  - Architecture TRM details each PRoC BLE functional block
  - Registers TRM describes each of the PRoC BLE registers
- Development Kits:
  - CY8CKIT-042-BLE-A Pioneer Kit, is a flexible, Arduino-compatible, Bluetooth LE development kit for PSoC 4 BLE and PRoC BLE.
  - CY8CKIT-142, PSoC 4 BLE Module, features a PSoC 4 BLE device, two crystals for the antenna matching network, a PCB antenna and other passives, while providing access to all GPIOs of the device.
  - CY8CKIT-143, PSoC 4 BLE 256KB Module, features a PSoC 4 BLE 256KB device, two crystals for the antenna matching network, a PCB antenna and other passives, while providing access to all GPIOs of the device.
  - The MiniProg3 device provides an interface for flash programming and debug.

## PSoC Creator

PSoC Creator is a free Windows-based Integrated Design Environment (IDE). It enables concurrent hardware and firmware design of PSoC 3, PSoC 4, and PSoC 5LP based systems. Create designs using classic, familiar schematic capture supported by over 100 pre-verified, production-ready PSoC Components; see the list of component datasheets. With PSoC Creator, you can:

1. Drag and drop component icons to build your hardware system design in the main design workspace
2. Codesign your application firmware with the PSoC hardware, using the PSoC Creator IDE C compiler
3. Configure components using the configuration tools
4. Explore the library of 100+ components
5. Review component datasheets

**Figure 1. Multiple-Sensor Example Project in PSoC Creator Contents**



# Functional Definition

## CPU and Memory Subsystem

### *CPU*

The Cortex-M0 CPU in PSoC 4200_BL is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. It mostly uses 16-bit instructions and executes a subset of the Thumb-2 instruction set. This enables fully compatible binary upward migration of the code to higher-performance processors such as Cortex-M3 and M4. The Cypress implementation includes a hardware multiplier that provides a 32-bit result in one cycle. It includes a nested vectored interrupt controller (NVIC) block with 32 interrupt inputs and a wakeup interrupt controller (WIC). The WIC can wake the processor up from the Deep Sleep mode, allowing power to the main processor to be switched off when the chip is in the Deep Sleep mode. The Cortex-M0 CPU provides a nonmaskable interrupt (NMI) input, which is made available to the user when it is not in use for system functions requested by the user.

The CPU also includes an SWD interface, which is a 2-wire form of JTAG; the debug configuration used for PSoC 4200_BL has four break-point (address) comparators and two watchpoint (data) comparators.

### *Flash*

The PSoC 4200_BL device has a flash module with 256 KB of flash memory, tightly coupled to the CPU to improve average access times from the flash block. The flash block is designed to deliver 2 wait-state (WS) access time at 48 MHz and with 1-WS access time at 24 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average. Part of the flash module can be used to emulate EEPROM operation if required. Maximum erase and program time is 20 ms per row (256 bytes). This also applies to the emulated EEPROM.

### *SRAM*

SRAM memory is retained during Hibernate.

### *SROM*

The 8-KB supervisory ROM contains a library of executable functions for flash programming. These functions are accessed through supervisory calls (SVC) and enable in-system programming of the flash memory.

### *DMA*

A DMA engine, with eight channels, is provided that can do 32-bit transfers and has chainable ping-pong descriptors.

## System Resources

### *Power System*

The power system is described in detail in the section Power on page 16. It provides an assurance that the voltage levels are as required for the respective modes, and can either delay the mode entry (on power-on reset (POR), for example) until voltage levels are as required or generate resets (brownout detect (BOD)) or interrupts when the power supply reaches a particular programmable level between 1.8 and 4.5 V (low voltage detect (LVD)).

PSoC 4200_BL operates with a single external supply (1.71 to 5.5 V without radio, and 1.9 V to 5.5 V with radio). The device has five different power modes; transitions between these modes are managed by the power system. PSoC 4200_BL provides Sleep, Deep Sleep, Hibernate, and Stop low-power modes. Refer to the *Technical Reference Manual* for more details.

### *Clock System*

The PSoC 4200_BL clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that no metastable conditions occur.

The clock system for PSoC 4200_BL consists of the internal main oscillator (IMO), the internal low-speed oscillator (ILO), the 24-MHz external crystal oscillator (ECO) and the 32-kHz watch crystal oscillator (WCO). In addition, an external clock may be supplied from a pin.

### *IMO Clock Source*

The IMO is the primary source of internal clocking in PSoC 4200_BL. It is trimmed during testing to achieve the specified accuracy. Trim values are stored in nonvolatile latches (NVL). Additional trim settings from flash can be used to compensate for changes. The IMO default frequency is 24 MHz and it can be adjusted between 3 to 48 MHz in steps of 1 MHz. The IMO tolerance with Cypress-provided calibration settings is ±2%.

### *ILO Clock Source*

The ILO is a very low-power oscillator, which is primarily used to generate clocks for the peripheral operation in the Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy. Cypress provides a software component, which does the calibration.

### *External Crystal Oscillator (ECO)*

The ECO is used as the active clock for the BLE subsystem to meet the ±50-ppm clock accuracy of the Bluetooth 4.2 Specification. PSoC 4200_BL includes a tunable load capacitor to tune the crystal clock frequency by measuring the actual clock frequency. The high-accuracy ECO clock can also be used as a system clock.

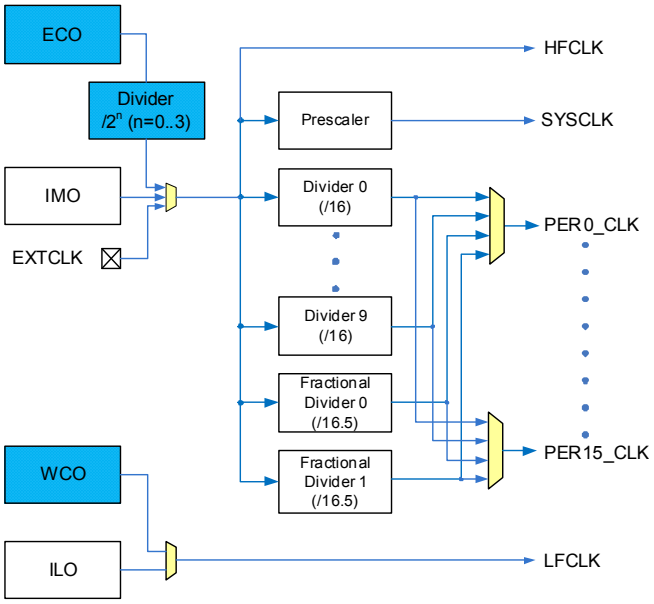
### *Watch Crystal Oscillator (WCO)*

The WCO is used as the sleep clock for the BLE subsystem to meet the ±500-ppm clock accuracy for the Bluetooth 4.2 Specification. The sleep clock provides an accurate sleep timing and enables wakeup at the specified advertisement and connection intervals. The WCO output can be used to realize the real-time clock (RTC) function in firmware.

### *Watchdog Timer*

A watchdog timer is implemented in the clock block running from the ILO or from the WCO; this allows the watchdog operation during Deep Sleep and generates a watchdog reset if not serviced before the timeout occurs. The watchdog reset is recorded in the Reset Cause register. With the WCO and firmware, an accurate real-time clock (within the bounds of the 32-kHz crystal accuracy) can be realized.

**Figure 3. PSoC 4200_BL MCU Clocking Architecture**




The HFCLK signal can be divided down (see Figure 3) to generate synchronous clocks for the UDBs, and the analog and digital peripherals. There are a total of 12 clock dividers for PSoC 4200_BL: ten with 16-bit divide capability and two with 16.5-bit divide capability. This allows the generation of 16 divided clock signals, which can be used by peripheral blocks. The analog clock leads the digital clocks to allow analog events to occur before the digital clock-related noise is generated. The 16-bit and 16.5-bit dividers allow a lot of flexibility in generating fine-grained frequency values and are fully supported in PSoC Creator.

*Reset*

PSoC 4200_BL device can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through resets and allows the software to determine the cause of the reset. An XRES pin is reserved for an external reset to avoid complications with the configuration and multiple pin functions during power-on or reconfiguration. The XRES pin has an internal pull-up resistor that is always enabled.

*Voltage Reference*

The PSoC 4200_BL reference system generates all internally required references. A one-percent voltage reference spec is provided for the 12-bit ADC. To allow better signal-to-noise ratios (SNR) and better absolute accuracy, it is possible to bypass the internal reference using a GPIO pin or use an external reference for the SAR. Refer to Table 19, “SAR ADC AC Specifications,” on page 26 for details.

## BLE Radio and Subsystem

PSoC 4200_BL incorporates a Bluetooth Smart subsystem that contains the Physical Layer (PHY) and Link Layer (LL) engines with an embedded AES-128 security engine. The physical layer consists of the digital PHY and the RF transceiver that transmits and receives GFSK packets at 1 Mbps over a 2.4-GHz ISM band, which is compliant with Bluetooth Smart Bluetooth Specification 4.2. The baseband controller is a composite hardware and firmware implementation that supports both master and slave modes. Key protocol elements, such as HCI and link control, are implemented in firmware. Time-critical functional blocks, such as encryption, CRC, data whitening, and access code correlation, are implemented in hardware (in the LL engine).

The RF transceiver contains an integrated balun, which provides a single-ended RF port pin to drive a 50-Ω antenna via a matching/filtering network. In the receive direction, this block converts the RF signal from the antenna to a digital bit stream after performing GFSK demodulation. In the transmit direction, this block performs GFSK modulation and then converts a digital baseband signal to a radio frequency before transmitting it to air through the antenna.

The Bluetooth Smart Radio and Subsystem (BLESS) requires a 1.9-V minimum supply (the range varies from 1.9 V to 5.5 V).

Key features of BLESS are as follows:

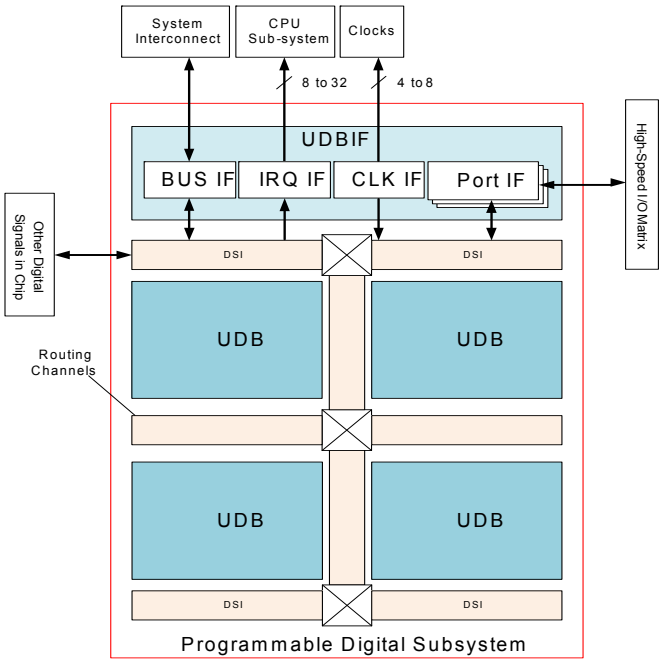
- Master and slave single-mode protocol stack with logical link control and adaptation protocol (L2CAP), attribute (ATT), and security manager (SM) protocols
- API access to generic attribute profile (GATT), generic access profile (GAP), and L2CAP
- L2CAP connection-oriented channel
- GAP features
  - Broadcaster, Observer, Peripheral, and Central roles
  - Security mode 1: Level 1, 2, 3, and 4
  - Security mode 2: Level 1 and 2
  - User-defined advertising data
  - Multiple bond support
- GATT features
  - GATT client and server
  - Supports GATT sub-procedures
  - 32-bit universally unique identifier (UUID)
- Security Manager (SM)
  - Pairing methods: Just works, Passkey Entry, Out of Band and Numeric Comparison
  - Authenticated man-in-the-middle (MITM) protection and data signing
  - LE Secure Connections (Bluetooth 4.2 feature)
- Link Layer (LL)
  - Master and Slave roles
  - 128-bit AES engine
  - Encryption
  - Low-duty cycle advertising
  - LE Ping
  - LE Data Packet Length Extension (Bluetooth 4.2 feature)
  - Link Layer Privacy (with extended scanning filter policy, Bluetooth 4.2 feature)
- Supports all SIG-adopted BLE profiles

## Programmable Digital

*Universal Digital Blocks (UDBs) and Port Interfaces*

The PSoC 4XX8 BLE 4.2 has four UDBs; the UDB array also provides a switched Digital System Interconnect (DSI) fabric that allows signals from peripherals and ports to be routed to and through the UDBs for communication and control.

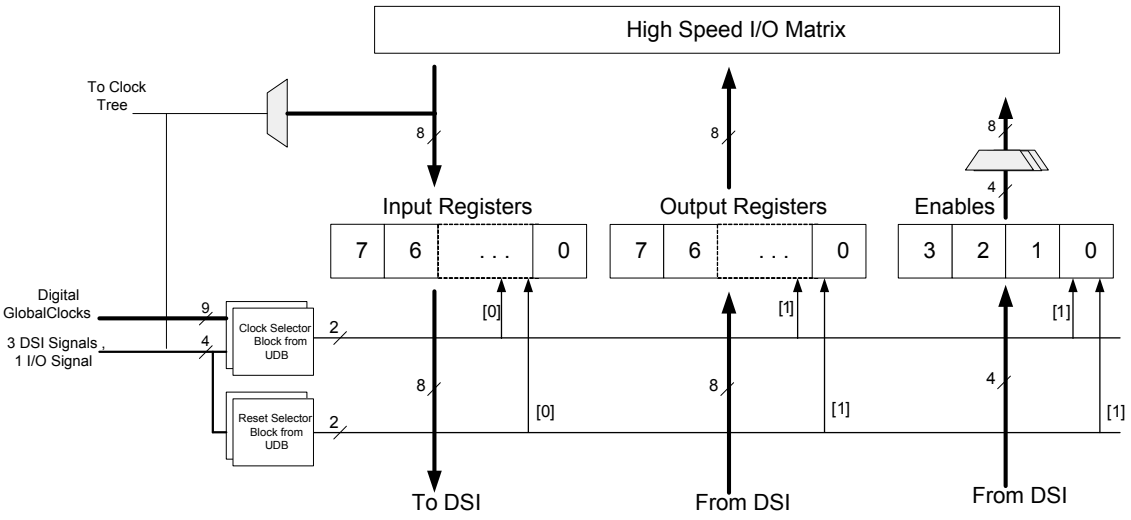
**Figure 5. UDB Array**




UDBs can be clocked from a clock-divider block, from a port interface (required for peripherals such as SPI), and from the DSI network directly or after synchronization.

A port interface is defined, which acts as a register that can be clocked with the same source as the PLDs inside the UDB array. This allows a faster operation because the inputs and outputs can be registered at the port interface close to the I/O pins and at the edge of the array. The port interface registers can be clocked by one of the I/Os from the same port. This allows interfaces such as SPI to operate at higher clock speeds by eliminating the delay for the port input to be routed over DSI and used to register other inputs (see Figure 6).

**Figure 6. Port Interface**




UDBs can generate interrupts (one UDB at a time) to the interrupt controller. UDBs retain the ability to connect to any pin on the chip through the DSI.

## Fixed-Function Digital

*Timer/Counter/PWM Block*

The timer/counter/PWM block consists of four 16-bit counters with user-programmable period length. There is a Capture register to record the count value at the time of an event (which may be an I/O event), a period register which is used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals which are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow the use as deadband programmable complementary PWM outputs. It also has a Kill input to force outputs to a predetermined state; for example, this is used in motor-drive systems when an overcurrent state is indicated and the PWMs driving the FETs need to be shut off immediately with no time for software intervention.

*Serial Communication Blocks (SCB)*

PSoC 4200_BL has two SCBs, each of which can implement an $I^2C$, UART, or SPI interface.

**$I^2C$ Mode**: The hardware $I^2C$ block implements a full multi-master and slave interface (it is capable of multimaster arbitration). This block is capable of operating at speeds of up to 1 Mbps (Fast Mode Plus) and has flexible buffering options to reduce the interrupt overhead and latency for the CPU. It also supports Ez$I^2C$ that creates a mailbox address range in the memory of PSoC 4200_BL and effectively reduces the $I^2C$ communication to reading from and writing to an array in the memory. In addition, the block supports an 8-deep FIFO for receive and transmit, which, by increasing the time given for the CPU to read the data, greatly reduces the need for clock stretching caused by the CPU not having read the data on time. The FIFO mode is available in all channels and is very useful in the absence of DMA.

The $I^2C$ peripheral is compatible with $I^2C$ Standard-mode, Fast-mode, and Fast-Mode Plus devices as defined in the NXP $I^2C$-bus specification and user manual (UM10204). The $I^2C$ bus I/O is implemented with GPIO in open-drain modes.

SCB1 is fully compliant with Standard mode (100 kHz), Fast mode (400 kHz), and Fast-Mode Plus (1 MHz) $I^2C$ signaling specifications when routed to GPIO pins P5[0] and P5[1], except for hot-swap capability during $I^2C$ active communication. The remaining GPIOs do not meet the hot-swap specification ($V_{DD}$ off; draw < 10-µA current) for Fast mode and Fast-Mode Plus, $I_{OL}$ Spec (20 mA) for Fast-Mode Plus, hysteresis spec (0.05 $V_{DD}$) for Fast mode and Fast-Mode Plus, and minimum fall time spec for Fast mode and Fast-Mode Plus.

- GPIO cells, including P5.0 and P5.1, cannot be hot-swapped or powered up independent of the rest of the $I^2C$ system.
- The GPIO pins P5.0 and P5.1 are over-voltage tolerant but cannot be hot-swapped or powered up independent of the rest of the $I^2C$ system
- Fast-Mode Plus has an $I_{OL}$ specification of 20 mA at a $V_{OL}$ of 0.4 V. The GPIO cells can sink a maximum of 8 mA $I_{OL}$ with a $V_{OL}$ maximum of 0.6 V.
- Fast-mode and Fast-Mode Plus specify minimum Fall times, which are not met with the GPIO cell; the Slow-Strong mode can help meet this spec depending on the bus load.

**UART Mode**: This is a full-feature UART operating at up to 1 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows the addressing of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break detect, and frame error are supported. An 8-deep FIFO allows much greater CPU service latencies to be tolerated. Note that hardware handshaking is not supported. This is not commonly used and can be implemented with a UDB-based UART in the system, if required.

**SPI Mode**: The SPI mode supports full Motorola SPI, TI Secure Simple Pairing (SSP) (essentially adds a start pulse that is used to synchronize SPI Codecs), and National Microwire (half-duplex form of SPI). The SPI block can use the FIFO for transmit and receive.

## GPIO

PSoC 4200_BL has 36 GPIOs. The GPIO block implements the following:

- Eight drive strength modes:
  - Analog input mode (input and output buffers disabled)
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL)
- Pins 0 and 1 of Port 5 are overvoltage-tolerant pins
- Individual control of input and output buffer enabling/disabling in addition to drive-strength modes
- Hold mode for latching previous state (used for retaining the I/O state in Deep Sleep and Hibernate modes)
- Selectable slew rates for dV/dt-related noise control to improve EMI

The pins are organized in logical entities called ports, which are 8-bit in width. During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix (HSIOM) is used to multiplex between various signals that may connect to an I/O pin. Pin locations for fixed-function peripherals are also fixed to reduce internal multiplexing complexity (these signals do not go through the DSI network). DSI signals are not affected by this and any pin may be routed to any UDB through the DSI network.

Data output and pin-state registers store, respectively, the values to be driven on the pins and the states of the pins themselves.

Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it (5 for PSoC 4200_BL).

## Pinouts

Table 1 shows the pin list for the PSoC 4200_BL device. Port 3 consists of the high-speed analog inputs for the SAR mux. All pins support CSD CapSense and analog mux bus connections.

**Table 1. PSoC 4200_BL Pin List (QFN Package)**

| Pin | Name | Type | Description |
|---|---|---|---|
| 1 | VDDD | POWER | 1.71-V to 5.5-V digital supply |
| 2 | XTAL32O/P6.0 | CLOCK | 32.768-kHz crystal |
| 3 | XTAL32I/P6.1 | CLOCK | 32.768-kHz crystal or external clock input |
| 4 | XRES | RESET | Reset, active LOW |
| 5 | P4.0 | GPIO | Port 4 Pin 0, lcd, csd |
| 6 | P4.1 | GPIO | Port 4 Pin 1, lcd, csd |
| 7 | P5.0 | GPIO | Port 5 Pin 0, lcd, csd |
| 8 | P5.1 | GPIO | Port 5 Pin 1, lcd, csd |
| 9 | VSSD | GROUND | Digital ground |
| 10 | VDDR | POWER | 1.9-V to 5.5-V radio supply |
| 11 | GANT1 | GROUND | Antenna shielding ground |
| 12 | ANT | ANTENNA | Antenna pin |
| 13 | GANT2 | GROUND | Antenna shielding ground |
| 14 | VDDR | POWER | 1.9-V to 5.5-V radio supply |
| 15 | VDDR | POWER | 1.9-V to 5.5-V radio supply |
| 16 | XTAL24I | CLOCK | 24-MHz crystal or external clock input |
| 17 | XTAL24O | CLOCK | 24-MHz crystal |
| 18 | VDDR | POWER | 1.9-V to 5.5-V radio supply |
| 19 | P0.0 | GPIO | Port 0 Pin 0, lcd, csd |
| 20 | P0.1 | GPIO | Port 0 Pin 1, lcd, csd |
| 21 | P0.2 | GPIO | Port 0 Pin 2, lcd, csd |
| 22 | P0.3 | GPIO | Port 0 Pin 3, lcd, csd |
| 23 | VDDD | POWER | 1.71-V to 5.5-V digital supply |
| 24 | P0.4 | GPIO | Port 0 Pin 4, lcd, csd |
| 25 | P0.5 | GPIO | Port 0 Pin 5, lcd, csd |
| 26 | P0.6 | GPIO | Port 0 Pin 6, lcd, csd |
| 27 | P0.7 | GPIO | Port 0 Pin 7, lcd, csd |
| 28 | P1.0 | GPIO | Port 1 Pin 0, lcd, csd |
| 29 | P1.1 | GPIO | Port 1 Pin 1, lcd, csd |
| 30 | P1.2 | GPIO | Port 1 Pin 2, lcd, csd |
| 31 | P1.3 | GPIO | Port 1 Pin 3, lcd, csd |
| 32 | P1.4 | GPIO | Port 1 Pin 4, lcd, csd |
| 33 | P1.5 | GPIO | Port 1 Pin 5, lcd, csd |
| 34 | P1.6 | GPIO | Port 1 Pin 6, lcd, csd |
| 35 | P1.7 | GPIO | Port 1 Pin 7, lcd, csd |
| 36 | VDDA | POWER | 1.71-V to 5.5-V analog supply |
| 37 | P2.0 | GPIO | Port 2 Pin 0, lcd, csd |
| 38 | P2.1 | GPIO | Port 2 Pin 1, lcd, csd |
| 39 | P2.2 | GPIO | Port 2 Pin 2, lcd, csd |

**Table 2. PSoC 4200_BL Pin List (WLCSP Package)** *(continued)*

| Pin | Name | Type | Description |
|---|---|---|---|
| C2 | VSSA | GROUND | Analog ground |
| C3 | P2.2 | GPIO | Port 2 Pin 2, analog/digital/lcd/csd |
| C4 | P2.6 | GPIO | Port 2 Pin 6, analog/digital/lcd/csd |
| C5 | P3.0 | GPIO | Port 3 Pin 0, analog/digital/lcd/csd |
| C6 | P3.1 | GPIO | Port 3 Pin 1, analog/digital/lcd/csd |
| C7 | P3.2 | GPIO | Port 3 Pin 2, analog/digital/lcd/csd |
| C8 | XRES | RESET | Reset, active LOW |
| C9 | P4.0 | GPIO | Port 4 Pin 0, analog/digital/lcd/csd |
| D1 | NC | NC | Do not connect |
| D2 | P1.7 | GPIO | Port 1 Pin 7, analog/digital/lcd/csd |
| D3 | VDDA | POWER | 1.71-V to 5.5-V analog supply |
| D4 | P2.0 | GPIO | Port 2 Pin 0, analog/digital/lcd/csd |
| D5 | P2.1 | GPIO | Port 2 Pin 1, analog/digital/lcd/csd |
| D6 | P2.5 | GPIO | Port 2 Pin 5, analog/digital/lcd/csd |
| D7 | VSSD | GROUND | Digital ground |
| D8 | P4.1 | GPIO | Port 4 Pin 1, analog/digital/lcd/csd |
| D9 | P5.0 | GPIO | Port 5 Pin 0, analog/digital/lcd/csd |
| E1 | NC | NC | Do not connect |
| E2 | P1.2 | GPIO | Port 1 Pin 2, analog/digital/lcd/csd |
| E3 | P1.3 | GPIO | Port 1 Pin 3, analog/digital/lcd/csd |
| E4 | P1.4 | GPIO | Port 1 Pin 4, analog/digital/lcd/csd |
| E5 | P1.5 | GPIO | Port 1 Pin 5, analog/digital/lcd/csd |
| E6 | P1.6 | GPIO | Port 1 Pin 6, analog/digital/lcd/csd |
| E7 | P2.4 | GPIO | Port 2 Pin 4, analog/digital/lcd/csd |
| E8 | P5.1 | GPIO | Port 5 Pin 1, analog/digital/lcd/csd |
| E9 | VSSD | GROUND | Digital ground |
| F1 | NC | NC | Do not connect |
| F2 | VSSD | GROUND | Digital ground |
| F3 | P0.7 | GPIO | Port 0 Pin 7, analog/digital/lcd/csd |
| F4 | P0.3 | GPIO | Port 0 Pin 3, analog/digital/lcd/csd |
| F5 | P1.0 | GPIO | Port 1 Pin 0, analog/digital/lcd/csd |
| F6 | P1.1 | GPIO | Port 1 Pin 1, analog/digital/lcd/csd |
| F7 | VSSR | GROUND | Radio ground |
| F8 | VSSR | GROUND | Radio ground |
| F9 | VDDR | POWER | 1.9-V to 5.5-V radio supply |
| G1 | NC | NC | Do not connect |
| G2 | P0.6 | GPIO | Port 0 Pin 6, analog/digital/lcd/csd |
| G3 | VDDD | POWER | 1.71-V to 5.5-V digital supply |
| G4 | P0.2 | GPIO | Port 0 Pin 2, analog/digital/lcd/csd |
| G5 | VSSD | GROUND | Digital ground |

The selection of peripheral function for different GPIO pins is given in Table 4.

**Table 4. Port Pin Connections**

| Name | Analog | Digital | | | | | |
|---|---|---|---|---|---|---|---|
| | | GPIO | Active #0 | Active #1 | Active #2 | Deep Sleep #0 | Deep Sleep #1 |
| P0.0 | COMP0_INP | GPIO | TCPWM0_P[3] | SCB1_UART_RX[1] | – | SCB1_I2C_SDA[1] | SCB1_SPI_MOSI[1] |
| P0.1 | COMP0_INN | GPIO | TCPWM0_N[3] | SCB1_UART_TX[1] | – | SCB1_I2C_SCL[1] | SCB1_SPI_MISO[1] |
| P0.2 | – | GPIO | TCPWM1_P[3] | SCB1_UART_RTS[1] | – | COMP0_OUT[0] | SCB1_SPI_SS0[1] |
| P0.3 | – | GPIO | TCPWM1_N[3] | SCB1_UART_CTS[1] | – | COMP1_OUT[0] | SCB1_SPI_SCLK[1] |
| P0.4 | COMP1_INP | GPIO | TCPWM1_P[0] | SCB0_UART_RX[1] | EXT_CLK[0]/ ECO_OUT[0] | SCB0_I2C_SDA[1] | SCB0_SPI_MOSI[1] |
| P0.5 | COMP1_INN | GPIO | TCPWM1_N[0] | SCB0_UART_TX[1] | – | SCB0_I2C_SCL[1] | SCB0_SPI_MISO[1] |
| P0.6 | – | GPIO | TCPWM2_P[0] | SCB0_UART_RTS[1] | – | SWDIO[0] | SCB0_SPI_SS0[1] |
| P0.7 | – | GPIO | TCPWM2_N[0] | SCB0_UART_CTS[1] | – | SWDCLK[0] | SCB0_SPI_SCLK[1] |
| P1.0 | CTBm1_OA0_INP | GPIO | TCPWM0_P[1] | – | – | COMP0_OUT[1] | WCO_OUT[2] |
| P1.1 | CTBm1_OA0_INN | GPIO | TCPWM0_N[1] | – | – | COMP1_OUT[1] | SCB1_SPI_SS1 |
| P1.2 | CTBm1_OA0_OUT | GPIO | TCPWM1_P[1] | – | – | – | SCB1_SPI_SS2 |
| P1.3 | CTBm1_OA1_OUT | GPIO | TCPWM1_N[1] | – | – | – | SCB1_SPI_SS3 |
| P1.4 | CTBm1_OA1_INN | GPIO | TCPWM2_P[1] | SCB0_UART_RX[0] | – | SCB0_I2C_SDA[0] | SCB0_SPI_MOSI[1] |
| P1.5 | CTBm1_OA1_INP | GPIO | TCPWM2_N[1] | SCB0_UART_TX[0] | – | SCB0_I2C_SCL[0] | SCB0_SPI_MISO[1] |
| P1.6 | CTBm1_OA0_INP | GPIO | TCPWM3_P[1] | SCB0_UART_RTS[0] | – | – | SCB0_SPI_SS0[1] |
| P1.7 | CTBm1_OA1_INP | GPIO | TCPWM3_N[1] | SCB0_UART_CTS[0] | – | – | SCB0_SPI_SCLK[1] |
| P2.0 | CTBm0_OA0_INP | GPIO | – | – | – | – | SCB0_SPI_SS1 |
| P2.1 | CTBm0_OA0_INN | GPIO | – | – | – | – | SCB0_SPI_SS2 |
| P2.2 | CTBm0_OA0_OUT | GPIO | – | – | – | WAKEUP | SCB0_SPI_SS3 |
| P2.3 | CTBm0_OA1_OUT | GPIO | – | – | – | – | WCO_OUT[1] |
| P2.4 | CTBm0_OA1_INN | GPIO | – | – | – | – | – |
| P2.5 | CTBm0_OA1_INP | GPIO | – | – | – | – | – |
| P2.6 | CTBm0_OA0_INP | GPIO | – | – | – | – | – |
| P2.7 | CTBm0_OA1_INP | GPIO | – | – | EXT_CLK[1]/ECO_OUT[1] | – | – |
| P3.0 | SARMUX_0 | GPIO | TCPWM0_P[2] | SCB0_UART_RX[2] | – | SCB0_I2C_SDA[2] | – |
| P3.1 | SARMUX_1 | GPIO | TCPWM0_N[2] | SCB0_UART_TX[2] | – | SCB0_I2C_SCL[2] | – |
| P3.2 | SARMUX_2 | GPIO | TCPWM1_P[2] | SCB0_UART_RTS[2] | – | – | – |
| P3.3 | SARMUX_3 | GPIO | TCPWM1_N[2] | SCB0_UART_CTS[2] | – | – | – |
| P3.4 | SARMUX_4 | GPIO | TCPWM2_P[2] | SCB1_UART_RX[2] | – | SCB1_I2C_SDA[2] | – |
| P3.5 | SARMUX_5 | GPIO | TCPWM2_N[2] | SCB1_UART_TX[2] | – | SCB1_I2C_SCL[2] | – |
| P3.6 | SARMUX_6 | GPIO | TCPWM3_P[2] | SCB1_UART_RTS[2] | – | – | – |
| P3.7 | SARMUX_7 | GPIO | TCPWM3_N[2] | SCB1_UART_CTS[2] | – | – | WCO_OUT[0] |
| P4.0 | CMOD | GPIO | TCPWM0_P[0] | SCB1_UART_RTS[0] | – | – | SCB1_SPI_MOSI[0] |
| P4.1 | CTANK | GPIO | TCPWM0_N[0] | SCB1_UART_CTS[0] | – | – | SCB1_SPI_MISO[0] |
| P5.0 | – | GPIO | TCPWM3_P[0] | SCB1_UART_RX[0] | EXTPA_EN | SCB1_I2C_SDA[0] | SCB1_SPI_SS0[0] |
| P5.1 | – | GPIO | TCPWM3_N[0] | SCB1_UART_TX[0] | EXT_CLK[2]/ECO_OUT[2] | SCB1_I2C_SCL[0] | SCB1_SPI_SCLK[0] |
| P6.0_XTAL32O | – | GPIO | – | – | – | – | – |
| P6.1_XTAL32I | – | GPIO | – | – | – | – | – |

**Table 6. DC Specifications** *(continued)*

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|---|---|---|---|---|---|---|
| SID41 | $I_{DD31}$ | GPIO and reset active | – | – | – | nA | T = 25 °C |
| SID42 | $I_{DD32}$ | GPIO and reset active | – | – | – | nA | T = –40 °C to 85 °C |
| **Stop Mode, $V_{DD}$ = 1.8 to 3.6 V** | | | | | | | |
| SID43 | $I_{DD33}$ | Stop mode current ($V_{DD}$) | – | 20 | – | nA | T = 25 °C, $V_{DD}$ = 3.3 V |
| SID44 | $I_{DD34}$ | Stop mode current ($V_{DDR}$) | – | 40 | –- | nA | T = 25 °C, $V_{DDR}$ = 3.3 V |
| SID45 | $I_{DD35}$ | Stop mode current ($V_{DD}$) | – | – | – | nA | T = –40 °C to 85 °C |
| SID46 | $I_{DD36}$ | Stop mode current ($V_{DDR}$) | – | – | – | nA | T = –40 °C to 85 °C, $V_{DDR}$ = 1.9 V to 3.6 V |
| **Stop Mode, $V_{DD}$ = 3.6 to 5.5 V** | | | | | | | |
| SID47 | $I_{DD37}$ | Stop mode current ($V_{DD}$) | – | – | – | nA | T = 25 °C, $V_{DD}$ = 5 V |
| SID48 | $I_{DD38}$ | Stop mode current ($V_{DDR}$) | – | – | – | nA | T = 25 °C, $V_{DDR}$ = 5 V |
| SID49 | $I_{DD39}$ | Stop mode current ($V_{DD}$) | – | – | – | nA | T = –40 °C to 85 °C |
| SID50 | $I_{DD40}$ | Stop mode current ($V_{DDR}$) | – | – | – | nA | T = –40 °C to 85 °C |
| **Stop Mode, $V_{DD}$ = 1.71 to 1.89 V (Regulator Bypassed)** | | | | | | | |
| SID51 | $I_{DD41}$ | Stop mode current ($V_{DD}$) | – | – | – | nA | T = 25 °C |
| SID52 | $I_{DD42}$ | Stop mode current ($V_{DD}$) | – | – | – | nA | T = –40 °C to 85 °C |

**Table 7. AC Specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|---|---|---|---|---|---|---|
| SID53 | $F_{CPU}$ | CPU frequency | DC | – | 48 | MHz | 1.71 V ≤ $V_{DD}$ ≤ 5.5 V |
| SID54 | $T_{SLEEP}$ | Wakeup from Sleep mode | – | 0 | – | µs | Guaranteed by characterization |
| SID55 | $T_{DEEPSLEEP}$ | Wakeup from Deep Sleep mode | – | – | 25 | µs | 24-MHz IMO. Guaranteed by characterization. |
| SID56 | $T_{HIBERNATE}$ | Wakeup from Hibernate mode | – | – | 0.7 | ms | Guaranteed by characterization |
| SID57 | $T_{STOP}$ | Wakeup from Stop mode | – | – | 2.2 | ms | Guaranteed by characterization |

**Table 14. Opamp Specifications** *(continued)*

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|---|---|---|---|---|---|---|
| SID122 | $V_{N3}$ | Input referred, 10-kHz, power = high | – | 28 | – | nV/rtHz | – |
| SID123 | $V_{N4}$ | Input referred, 100-kHz, power = high | – | 15 | – | nV/rtHz | – |
| SID124 | $C_{LOAD}$ | Stable up to maximum load. Performance specs at 50 pF | – | – | 125 | pF | – |
| SID125 | Slew_rate | Cload = 50 pF, Power = High, $V_{DDA} \geq 2.7$ V | 6 | – | – | V/µsec | – |
| SID126 | T_op_wake | From disable to enable, no external RC dominating | – | 300 | – | µsec | – |
| **Comp_mode (Comparator Mode; 50-mV Drive, $T_{RISE} = T_{FALL}$ (Approx.)** | | | | | | | |
| SID127 | $T_{PD1}$ | Response time; power = high | – | 150 | – | nsec | – |
| SID128 | $T_{PD2}$ | Response time; power = medium | – | 400 | – | nsec | – |
| SID129 | $T_{PD3}$ | Response time; power = low | – | 2000 | – | nsec | – |
| SID130 | Vhyst_op | Hysteresis | – | 10 | – | mV | – |
| **Deep Sleep (Deep Sleep mode operation is only guaranteed for $V_{DDA} > 2.5$ V)** | | | | | | | |
| SID131 | GBW_DS | Gain bandwidth product | – | 50 | – | kHz | – |
| SID132 | IDD_DS | Current | – | 15 | – | µA | – |
| SID133 | Vos_DS | Offset voltage | – | 5 | – | mV | – |
| SID134 | Vos_dr_DS | Offset voltage drift | – | 20 | – | µV/°C | – |
| SID135 | Vout_DS | Output voltage | 0.2 | – | $V_{DD}$–0.2 | V | – |
| SID136 | Vcm_DS | Common mode voltage | 0.2 | – | $V_{DD}$–1.8 | V | – |

**Table 15. Comparator DC Specifications**[3]

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|---|---|---|---|---|---|---|
| SID140 | $V_{OFFSET1}$ | Input offset voltage, Factory trim | – | – | ±10 | mV | – |
| SID141 | $V_{OFFSET2}$ | Input offset voltage, Custom trim | – | – | ±6 | mV | – |
| SID141A | $V_{OFFSET3}$ | Input offset voltage, ultra-low-power mode | – | ±12 | – | mV | $V_{DDD} \geq 2.6$ V for Temp < 0°C, $V_{DDD} \geq 1.8$ V for Temp > 0 °C |
| SID142 | $V_{HYST}$ | Hysteresis when enabled. Common Mode voltage range from 0 to VDD –1 | – | 10 | 35 | mV | – |
| SID143 | $V_{ICM1}$ | Input common mode voltage in normal mode | 0 | – | $V_{DDD}$ –0.1 | V | Modes 1 and 2 |
| SID144 | $V_{ICM2}$ | Input common mode voltage in low power mode | 0 | – | $V_{DDD}$ | V | – |
| SID145 | $V_{ICM3}$ | Input common mode voltage in ultra low power mode | 0 | – | $V_{DDD}$ –1.15 | V | $V_{DDD} \geq 2.6$ V for Temp < 0°C, $V_{DDD} \geq 1.8$ V for Temp > 0 °C |
| SID146 | CMRR | Common mode rejection ratio | 50 | – | – | dB | $V_{DDD} \geq 2.7$ V |
| SID147 | CMRR | Common mode rejection ratio | 42 | – | – | dB | $V_{DDD} \leq 2.7$ V |
| SID148 | $I_{CMP1}$ | Block current, normal mode | – | – | 400 | µA | – |
| SID149 | $I_{CMP2}$ | Block current, low power mode | – | – | 100 | µA | – |

**Note**
3. ULP LCOMP operating conditions:
   - $V_{DDD}$ 2.6 V-5.5 V for datasheet temp range < 0 °C
   - $V_{DDD}$ 1.8 V-5.5 V for datasheet temp range ≥ 0 °C

**Table 26. PWM AC Specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID214 | $T_{PWMFREQ}$ | Operating frequency | $F_{CLK}$ | – | 48 | MHz | – |
| SID215 | $T_{PWMPWINT}$ | Pulse width (internal) | 2 × $T_{CLK}$ | – | – | ns | – |
| SID216 | $T_{PWMEXT}$ | Pulse width (external) | 2 × $T_{CLK}$ | – | – | ns | – |
| SID217 | $T_{PWMKILLINT}$ | Kill pulse width (internal) | 2 × $T_{CLK}$ | – | – | ns | – |
| SID218 | $T_{PWMKILLEXT}$ | Kill pulse width (external) | 2 × $T_{CLK}$ | – | – | ns | – |
| SID219 | $T_{PWMEINT}$ | Enable pulse width (internal) | 2 × $T_{CLK}$ | – | – | ns | – |
| SID220 | $T_{PWMENEXT}$ | Enable pulse width (external) | 2 × $T_{CLK}$ | – | – | ns | – |
| SID221 | $T_{PWMRESWINT}$ | Reset pulse width (internal) | 2 × $T_{CLK}$ | – | – | ns | – |
| SID222 | $T_{PWMRESWEXT}$ | Reset pulse width (external) | 2 × $T_{CLK}$ | – | – | ns | – |

*$I^2C$*

**Table 27. Fixed $I^2C$ DC Specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID223 | $I_{I2C1}$ | Block current consumption at 100 kHz | – | – | 50 | µA | – |
| SID224 | $I_{I2C2}$ | Block current consumption at 400 kHz | – | – | 155 | µA | – |
| SID225 | $I_{I2C3}$ | Block current consumption at 1 Mbps | – | – | 390 | µA | – |
| SID226 | $I_{I2C4}$ | $I^2C$ enabled in Deep Sleep mode | – | – | 1.4 | µA | – |

**Table 28. Fixed $I^2C$ AC Specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID227 | $F_{I2C1}$ | Bit rate | – | – | 1 | Mbps | – |

*LCD Direct Drive*

**Table 29. LCD Direct Drive DC Specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID228 | $I_{LCDLOW}$ | Operating current in low-power mode | – | 17.5 | – | µA | 16 × 4 small segment display at 50 Hz |
| SID229 | $C_{LCDCAP}$ | LCD capacitance per segment/common driver | – | 500 | 5000 | pF | – |
| SID230 | $LCD_{OFFSET}$ | Long-term segment offset | – | 20 | – | mV | – |
| SID231 | $I_{LCDOP1}$ | LCD system operating current $V_{BIAS}$ = 5 V. | – | 2 | – | mA | 32 × 4 segments. 50 Hz at 25 °C |
| SID232 | $I_{LCDOP2}$ | LCD system operating current. $V_{BIAS}$ = 3.3 V | – | 2 | – | mA | 32 × 4 segments 50 Hz at 25 °C |

**Table 30. LCD Direct Drive AC Specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID233 | $F_{LCD}$ | LCD frame rate | 10 | 50 | 150 | Hz | – |

**Table 31. Fixed UART DC Specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID234 | $I_{UART1}$ | Block current consumption at 100 kbps | – | – | 55 | µA | – |
| SID235 | $I_{UART2}$ | Block current consumption at 1000 kbps | – | – | 360 | µA | – |

**Table 32. Fixed UART AC Specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID236 | $F_{UART}$ | Bit rate | – | – | 1 | Mbps | – |

*SPI Specifications*

**Table 33. Fixed SPI DC Specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID237 | $I_{SPI1}$ | Block current consumption at 1 Mbps | – | – | 360 | µA | – |
| SID238 | $I_{SPI2}$ | Block current consumption at 4 Mbps | – | – | 560 | µA | – |
| SID239 | $I_{SPI3}$ | Block current consumption at 8 Mbps | – | – | 600 | µA | – |

**Table 34. Fixed SPI AC Specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID240 | $F_{SPI}$ | SPI operating frequency (master; 6X oversampling) | – | – | 8 | MHz | – |

**Table 35. Fixed SPI Master Mode AC Specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID241 | $T_{DMO}$ | MOSI valid after Sclock driving edge | – | – | 18 | ns | – |
| SID242 | $T_{DSI}$ | MISO valid before Sclock capturing edge. Full clock, late MISO sampling used | 20 | – | – | ns | Full clock, late MISO sampling |
| SID243 | $T_{HMO}$ | Previous MOSI data hold time | 0 | – | – | ns | Referred to Slave capturing edge |

**Table 36. Fixed SPI Slave Mode AC Specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID244 | $T_{DMI}$ | MOSI valid before Sclock capturing edge | 40 | – | – | ns | – |
| SID245 | $T_{DSO}$ | MISO valid after Sclock driving edge | – | – | $42 + 3 \times T_{CPU}$ | ns | – |
| SID246 | $T_{DSO\_ext}$ | MISO valid after Sclock driving edge in external clock mode | – | – | 53 | ns | $V_{DD} < 3.0$ V |
| SID247 | $T_{HSO}$ | Previous MISO data hold time | 0 | – | – | ns | – |
| SID248 | $T_{SSELSCK}$ | SSEL valid to first SCK valid edge | 100 | – | – | ns | – |

## Memory

**Table 37. Flash DC Specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID249 | $V_{PE}$ | Erase and program voltage | 1.71 | – | 5.5 | V | – |
| SID309 | $T_{WS48}$ | Number of Wait states at 32–48 MHz | 2 | – | – | | CPU execution from flash |
| SID310 | $T_{WS32}$ | Number of Wait states at 16–32 MHz | 1 | – | – | | CPU execution from flash |
| SID311 | $T_{WS16}$ | Number of Wait states for 0–16 MHz | 0 | – | – | | CPU execution from flash |

**Table 38. Flash AC Specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID250 | $T_{ROWWRITE}$[5] | Row (block) write time (erase and program) | – | – | 20 | ms | Row (block) = 128 bytes for 128 KB flash devices<br>Row (block) = 256 bytes for 256 KB flash devices |
| SID251 | $T_{ROWERASE}$[5] | Row erase time | – | – | 13 | ms | – |
| SID252 | $T_{ROWPROGRAM}$[5] | Row program time after erase | – | – | 7 | ms | – |
| SID253 | $T_{BULKERASE}$[5] | Bulk erase time (256 KB) | – | – | 35 | ms | – |
| SID254 | $T_{DEVPROG}$[5] | Total device program time | – | – | 50 | seconds | 256 KB |
| SID254A | | | – | – | 25 | | 128 KB |
| SID255 | $F_{END}$ | Flash endurance | 100 K | – | – | cycles | – |
| SID256 | $F_{RET}$ | Flash retention. $T_A \leq 55$ °C, 100 K P/E cycles | 20 | – | – | years | – |
| SID257 | $F_{RET2}$ | Flash retention. $T_A \leq 85$ °C, 10 K P/E cycles | 10 | – | – | years | – |

## System Resources

*Power-on-Reset (POR)*

**Table 39. POR DC Specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID258 | $V_{RISEIPOR}$ | Rising trip voltage | 0.80 | – | 1.45 | V | – |
| SID259 | $V_{FALLIPOR}$ | Falling trip voltage | 0.75 | – | 1.40 | V | – |
| SID260 | $V_{IPORHYST}$ | Hysteresis | 15 | – | 200 | mV | – |

**Table 40. POR AC Specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID264 | $T_{PPOR\_TR}$ | PPOR response time in Active and Sleep modes | – | – | 1 | µs | – |

**Table 41. Brown-Out Detect**

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|---|---|---|---|---|---|---|
| SID261 | $V_{FALLPPOR}$ | BOD trip voltage in Active and Sleep modes | 1.64 | – | – | V | – |
| SID262 | $V_{FALLDPSLP}$ | BOD trip voltage in Deep Sleep mode | 1.4 | – | – | V | – |

**Table 42. Hibernate Reset**

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|---|---|---|---|---|---|---|
| SID263 | $V_{HBRTRIP}$ | BOD trip voltage in Hibernate mode | 1.1 | – | – | V | – |

**Note**

5. It can take as much as 20 milliseconds to write to flash. During this time, the device should not be reset, or flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.

**Table 54. WCO Specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|---|---|---|---|---|---|---|
| SID398 | $F_{WCO}$ | Crystal frequency | – | 32.768 | – | kHz | – |
| SID399 | FTOL | Frequency tolerance | – | 50 | – | ppm | – |
| SID400 | ESR | Equivalent series resistance | – | 50 | – | kΩ | – |
| SID401 | PD | Drive level | – | – | 1 | µW | – |
| SID402 | $T_{START}$ | Startup time | – | – | 500 | ms | – |
| SID403 | $C_L$ | Crystal load capacitance | 6 | – | 12.5 | pF | – |
| SID404 | C0 | Crystal shunt capacitance | – | 1.35 | – | pF | – |
| SID405 | $I_{WCO1}$ | Operating current (High-Power mode) | – | – | 8 | µA | – |
| SID406 | $I_{WCO2}$ | Operating current (Low-Power mode) | – | – | 2.6 | µA | – |

## Ordering Information

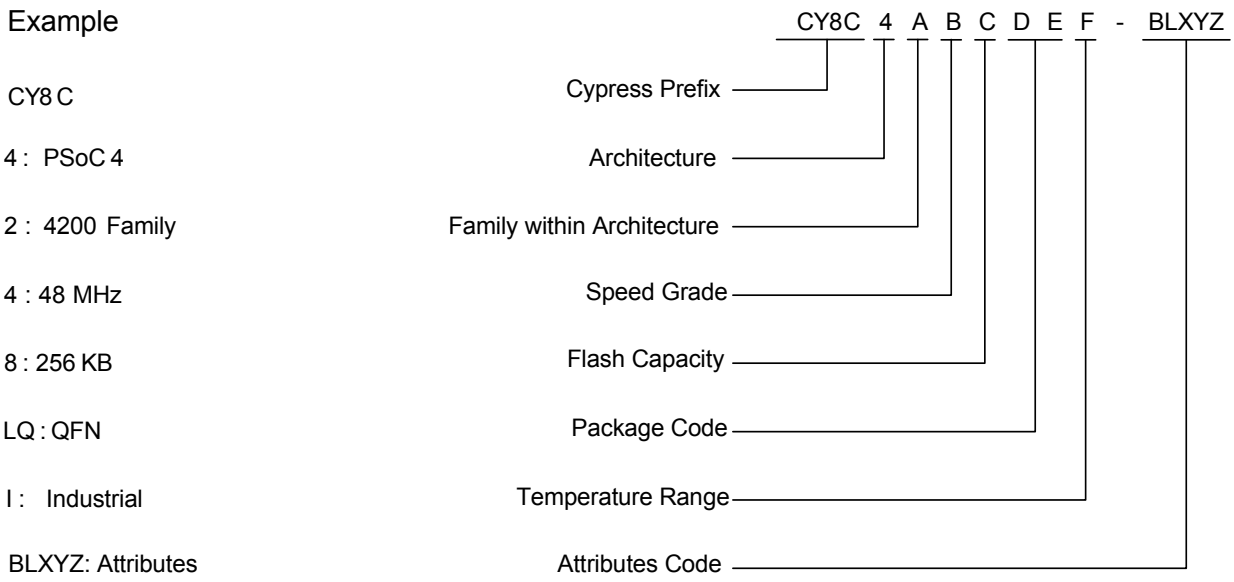
The PSoC 4200_BL part numbers and features are listed in Table 55.

**Table 55. PSoC 4200_BL Part Numbers**

| Product Family | MPN | Max CPU Speed (MHz) | BLE subsystem | Flash (KB) | SRAM (KB) | UDB | Opamp | CapSense | TMG (Gestures) | Direct LCD Drive | 12-bit SAR ADC | DMA | LP Comparators | TCPWM Blocks | SCB Blocks | GPIO | Package | Temperature Range |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PSoC 4200_BL | CY8C4247LQI-BL473 | 48 | 4.1 | 128 | 16 | 4 | 4 | – | – | – | 1 Msps | – | 2 | 4 | 2 | 36 | QFN | 85 °C |
| | CY8C4247FNI-BL473 | 48 | 4.1 | 128 | 16 | 4 | 4 | – | – | – | 1 Msps | – | 2 | 4 | 2 | 36 | CSP | 85 °C |
| | CY8C4247LQI-BL453 | 48 | 4.1 | 128 | 16 | 4 | 4 | 1 | – | – | 1 Msps | – | 2 | 4 | 2 | 36 | QFN | 85 °C |
| | CY8C4247LQI-BL463 | 48 | 4.1 | 128 | 16 | 4 | 4 | – | – | 1 | 1 Msps | – | 2 | 4 | 2 | 36 | QFN | 85 °C |
| | CY8C4247LQI-BL483 | 48 | 4.1 | 128 | 16 | 4 | 4 | 1 | – | 1 | 1 Msps | – | 2 | 4 | 2 | 36 | QFN | 85 °C |
| | CY8C4247LQI-BL493 | 48 | 4.1 | 128 | 16 | 4 | 4 | 1 | 1 | 1 | 1 Msps | – | 2 | 4 | 2 | 36 | QFN | 85 °C |
| | CY8C4247FNI-BL483 | 48 | 4.1 | 128 | 16 | 4 | 4 | 1 | – | 1 | 1 Msps | – | 2 | 4 | 2 | 36 | 68-CSP | 85 °C |
| | CY8C4247FNI-BL493 | 48 | 4.1 | 128 | 16 | 4 | 4 | 1 | 1 | 1 | 1 Msps | – | 2 | 4 | 2 | 36 | 68-CSP | 85 °C |
| | CY8C4247FNQ-BL483 | 48 | 4.1 | 128 | 16 | 4 | 4 | 1 | – | 1 | 1 Msps | – | 2 | 4 | 2 | 36 | 68-CSP | 105 °C |
| | CY8C4247LQQ-BL483 | 48 | 4.1 | 128 | 16 | 4 | 4 | 1 | – | 1 | 1 Msps | – | 2 | 4 | 2 | 36 | QFN | 105 °C |
| | CY8C4247FLI-BL493 | 48 | 4.1 | 128 | 16 | 4 | 4 | 1 | 1 | 1 | 1 Msps | – | 2 | 4 | 2 | 36 | Thin 68-CSP | 85 °C |
| | CY8C4248LQI-BL473 | 48 | 4.1 | 256 | 32 | 4 | 4 | – | – | – | 1 Msps | 1 | 2 | 4 | 2 | 36 | QFN | 85 °C |
| | CY8C4248LQI-BL453 | 48 | 4.1 | 256 | 32 | 4 | 4 | 1 | – | – | 1 Msps | 1 | 2 | 4 | 2 | 36 | QFN | 85 °C |
| | CY8C4248LQI-BL483 | 48 | 4.1 | 256 | 32 | 4 | 4 | 1 | – | 1 | 1 Msps | 1 | 2 | 4 | 2 | 36 | QFN | 85 °C |
| | CY8C4248FNI-BL483 | 48 | 4.1 | 256 | 32 | 4 | 4 | 1 | – | 1 | 1 Msps | 1 | 2 | 4 | 2 | 36 | 76-CSP | 85 °C |
| | CY8C4248FLI-BL483 | 48 | 4.1 | 256 | 32 | 4 | 4 | 1 | – | 1 | 1 Msps | 1 | 2 | 4 | 2 | 36 | Thin 76-CSP | 85 °C |
| | CY8C4248LQI-BL543 | 48 | 4.2 | 256 | 32 | – | 2 | – | – | – | 1 Msps | 1 | – | 4 | 2 | 36 | QFN | 85 °C |
| | CY8C4248FNI-BL543 | 48 | 4.2 | 256 | 32 | – | 2 | – | – | – | 1 Msps | 1 | – | 4 | 2 | 36 | 76-CSP | 85 °C |
| | CY8C4248LQI-BL573 | 48 | 4.2 | 256 | 32 | 4 | 4 | – | – | – | 1 Msps | 1 | 2 | 4 | 2 | 36 | QFN | 85 °C |
| | CY8C4248FNI-BL573 | 48 | 4.2 | 256 | 32 | 4 | 4 | – | – | – | 1 Msps | 1 | 2 | 4 | 2 | 36 | 76-CSP | 85 °C |
| | CY8C4248LQI-BL553 | 48 | 4.2 | 256 | 32 | 4 | 4 | 1 | – | – | 1 Msps | 1 | 2 | 4 | 2 | 36 | QFN | 85 °C |
| | CY8C4248FNI-BL553 | 48 | 4.2 | 256 | 32 | 4 | 4 | 1 | – | – | 1 Msps | 1 | 2 | 4 | 2 | 36 | 76-CSP | 85 °C |
| | CY8C4248LQI-BL563 | 48 | 4.2 | 256 | 32 | 4 | 4 | – | – | 1 | 1 Msps | 1 | 2 | 4 | 2 | 36 | QFN | 85 °C |
| | CY8C4248FNI-BL563 | 48 | 4.2 | 256 | 32 | 4 | 4 | – | – | 1 | 1 Msps | 1 | 2 | 4 | 2 | 36 | 76-CSP | 85 °C |
| | CY8C4248LQI-BL583 | 48 | 4.2 | 256 | 32 | 4 | 4 | 1 | – | 1 | 1 Msps | 1 | 2 | 4 | 2 | 36 | QFN | 85 °C |
| | CY8C4248FNI-BL583 | 48 | 4.2 | 256 | 32 | 4 | 4 | 1 | – | 1 | 1 Msps | 1 | 2 | 4 | 2 | 36 | 76-CSP | 85 °C |
| | CY8C4248FLI-BL583 | 48 | 4.2 | 256 | 32 | 4 | 4 | 1 | – | 1 | 1 Msps | 1 | 2 | 4 | 2 | 36 | Thin 76-CSP | 85 °C |
| | CY8C4248LQQ-BL583 | 48 | 4.2 | 256 | 32 | 4 | 4 | 1 | – | 1 | 1 Msps | 1 | 2 | 4 | 2 | 36 | QFN | 105 °C |
| | CY8C4248FNQ-BL583 | 48 | 4.2 | 256 | 32 | 4 | 4 | 1 | – | 1 | 1 Msps | 1 | 2 | 4 | 2 | 36 | 76-CSP | 105 °C |
| | CY8C4248LQI-BL593 | 48 | 4.2 | 256 | 32 | 4 | 4 | 1 | 1 | 1 | 1 Msps | 1 | 2 | 4 | 2 | 36 | QFN | 85 °C |
| | CY8C4248FNI-BL593 | 48 | 4.2 | 256 | 32 | 4 | 4 | 1 | 1 | 1 | 1 Msps | 1 | 2 | 4 | 2 | 36 | 76-CSP | 85 °C |

PSoC 4 devices follow the part numbering convention described in the following table. All fields are single-character alphanumeric (0, 1, 2, …, 9, A,B, …, Z) unless stated otherwise.

### Ordering Code Definitions




The Field Values are listed in the following table:

| Field | Description | Values | Meaning |
|---|---|---|---|
| CY8C | Cypress Prefix | | |
| 4 | Architecture | 4 | PSoC 4 |
| A | Family within architecture | 2 | 4200-BLE Family |
| B | CPU Speed | 4 | 48 MHz |
| C | Flash Capacity | 8, 7 | 256, 128 KB respectively |
| DE | Package Code | FN | WLCSP |
| | | LQ | QFN |
| | | FL | Thin CSP |
| F | Temperature Range | I | Industrial |
| BLXYZ | Attributes Code | BL400-BL499 | Bluetooth 4.1 compliant |
| | | BL500-BL599 | Bluetooth 4.2 compliant |

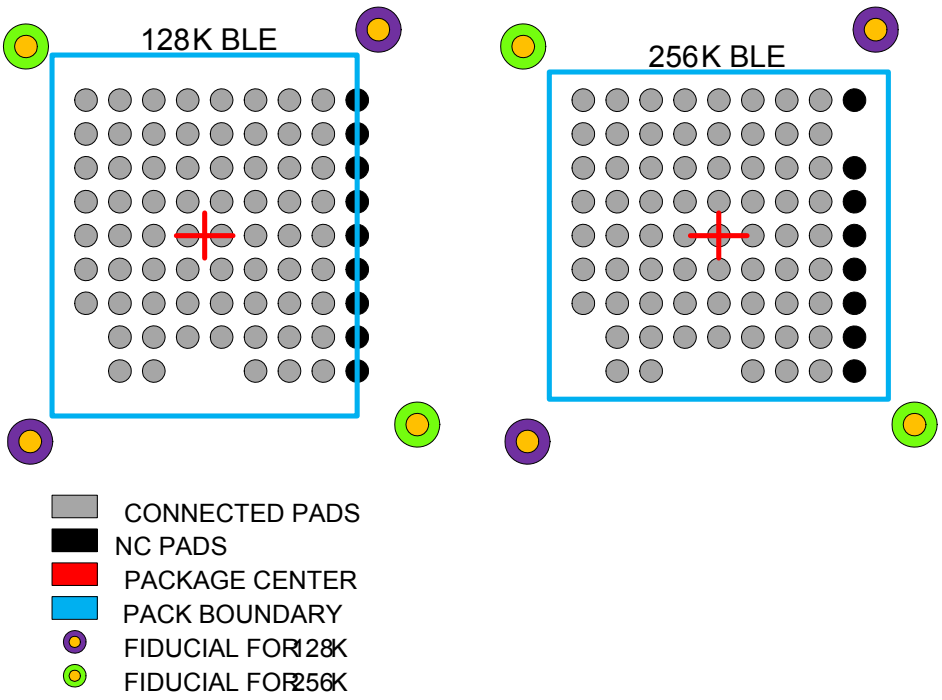
### WLCSP Compatibility

The PSoC 4XXX_BLE family has products with 128 KB (16KB SRAM) and 256 KB (32KB SRAM) Flash. Package pin-outs and sizes are identical for the 56-pin QFN package but are different in one dimension for the 68-ball WLCSP.

The 256KB Flash product has an extra column of balls which are required for mechanical integrity purposes in the Chip-Scale package. With consideration for this difference, the land pattern on the PCB may be designed such that either product may be used with no change to the PCB design.

Figure 9 shows the 128KB and 256 KB Flash CSP packages.

**Figure 9. 128KB and 256 KB Flash CSP Packages**




The rightmost column of (all NC, No Connect) balls in the 256K BLE WLCSP is for mechanical integrity purposes. The package is thus wider (3.2 mm versus 2.8 mm). All other dimensions are identical. Cypress will provide layout symbols for PCB layout.

The scheme in Figure 9 is implemented to design the PCB for the 256K BLE package with the appropriate space requirements thus allowing use of either package at a later time without redesigning the Printed Circuit Board.

**Table 60. Acronyms Used in this Document** *(continued)*

| Acronym | Description |
|---|---|
| PC | program counter |
| PCB | printed circuit board |
| PGA | programmable gain amplifier |
| PHUB | peripheral hub |
| PHY | physical layer |
| PICU | port interrupt control unit |
| PLA | programmable logic array |
| PLD | programmable logic device, see also PAL |
| PLL | phase-locked loop |
| PMDD | package material declaration data sheet |
| POR | power-on reset |
| PRES | precise power-on reset |
| PRS | pseudo random sequence |
| PS | port read data register |
| PSoC® | Programmable System-on-Chip™ |
| PSRR | power supply rejection ratio |
| PWM | pulse-width modulator |
| RAM | random-access memory |
| RISC | reduced-instruction-set computing |
| RMS | root-mean-square |
| RTC | real-time clock |
| RTL | register transfer language |
| RTR | remote transmission request |
| RX | receive |
| SAR | successive approximation register |
| SC/CT | switched capacitor/continuous time |
| SCL | $I^2C$ serial clock |
| SDA | $I^2C$ serial data |
| S/H | sample and hold |
| SINAD | signal to noise and distortion ratio |
| SIO | special input/output, GPIO with advanced features. See GPIO. |
| SOC | start of conversion |
| SOF | start of frame |
| SPI | Serial Peripheral Interface, a communications protocol |
| SR | slew rate |
| SRAM | static random access memory |
| SRES | software reset |
| SWD | serial wire debug, a test protocol |

**Table 60. Acronyms Used in this Document** *(continued)*

| Acronym | Description |
|---|---|
| SWV | single-wire viewer |
| TD | transaction descriptor, see also DMA |
| THD | total harmonic distortion |
| TIA | transimpedance amplifier |
| TRM | technical reference manual |
| TTL | transistor-transistor logic |
| TX | transmit |
| UART | Universal Asynchronous Transmitter Receiver, a communications protocol |
| UDB | universal digital block |
| USB | Universal Serial Bus |
| USBIO | USB input/output, PSoC pins used to connect to a USB port |
| VDAC | voltage DAC, see also DAC, IDAC |
| WDT | watchdog timer |
| WOL | write once latch, see also NVL |
| WRES | watchdog timer reset |
| XRES | external reset I/O pin |
| XTAL | crystal |

# Document Conventions

## Units of Measure

**Table 61. Units of Measure**

| Symbol | Unit of Measure |
|---|---|
| °C | degrees Celsius |
| dB | decibel |
| fF | femto farad |
| Hz | hertz |
| KB | 1024 bytes |
| kbps | kilobits per second |
| Khr | kilohour |
| kHz | kilohertz |
| kΩ | kilo ohm |
| ksps | kilosamples per second |
| LSB | least significant bit |
| Mbps | megabits per second |
| MHz | megahertz |
| MΩ | mega-ohm |
| Msps | megasamples per second |
| µA | microampere |
| µF | microfarad |
| µH | microhenry |
| µs | microsecond |
| µV | microvolt |
| µW | microwatt |
| mA | milliampere |
| ms | millisecond |
| mV | millivolt |
| nA | nanoampere |
| ns | nanosecond |
| nV | nanovolt |
| Ω | ohm |
| pF | picofarad |
| ppm | parts per million |
| ps | picosecond |
| s | second |
| sps | samples per second |
| sqrtHz | square root of hertz |
| V | volt |

## Revision History

| Description Title: PSoC® 4: 4200_BLE Family Datasheet Programmable System-on-Chip (PSoC®)<br>Document Number: 002-23053 | | | | |
|---|---|---|---|---|
| **Revision** | **ECN** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| ** | 6078076 | PMAD/ WKA | 02/22/2018 | New datasheet |