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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, IrDA, LINbus, Microwire, SmartCard, SPI, SSP, UART/USART
Peripherals	Bluetooth, Brown-out Detect/Reset, Cap Sense, LCD, LVD, POR, PWM, SmartCard, SmartSense, WDT
Number of I/O	36
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	56-UFQFN Exposed Pad
Supplier Device Package	56-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4247lqq-bl483

More Information

Cypress provides a wealth of data at http://www.cypress.com to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the introduction page for Bluetooth® Low Energy (BLE) Products. Following is an abbreviated list for PRoC BLE:

- Overview: PSoC Portfolio, PSoC Roadmap
- Product Selectors: PSoC 1, PSoC 3, PSoC 4, PRoC BLE, PSoC 4 BLE, PSoC 5LP In addition, PSoC Creator includes a device selection tool.
- Application Notes: Cypress offers a large number of PSoC application notes coverting a broad range of topics, from basic to advanced level. Recommended application notes for getting started with PRoC BLE are:
  - AN94020: Getting Started with PRoC BLE
  - AN97060: PSoC 4 BLE and PRoC BLE - Over-The-Air (OTA) Device Firmware Upgrade (DFU) Guide
  - AN91184: PSoC 4 BLE - Designing BLE Applications
  - AN91162: Creating a BLE Custom Profile
  - AN91445: Antenna Design and RF Layout Guidelines
  - AN96841: Getting Started With EZ-BLE Module
  - AN85951: PSoC 4 CapSense Design Guide
  - AN95089: PSoC 4/PRoC BLE Crystal Oscillator Selection and Tuning Techniques
  - AN92584: Designing for Low Power and Estimating Battery Life for BLE Applications
- Technical Reference Manual (TRM) is in two documents:
  - Architecture TRM details each PRoC BLE functional block
  - Registers TRM describes each of the PRoC BLE registers
- Development Kits:
  - CY8CKIT-042-BLE-A Pioneer Kit, is a flexible, Arduino-compatible, Bluetooth LE development kit for PSoC 4 BLE and PRoC BLE.
  - CY8CKIT-142, PSoC 4 BLE Module, features a PSoC 4 BLE device, two crystals for the antenna matching network, a PCB antenna and other passives, while providing access to all GPIOs of the device.
  - CY8CKIT-143, PSoC 4 BLE 256KB Module, features a PSoC 4 BLE 256KB device, two crystals for the antenna matching network, a PCB antenna and other passives, while providing access to all GPIOs of the device.
  - The MiniProg3 device provides an interface for flash programming and debug.

PSoC Creator

PSoC Creator is a free Windows-based Integrated Design Environment (IDE). It enables concurrent hardware and firmware design of PSoC 3, PSoC 4, and PSoC 5LP based systems. Create designs using classic, familiar schematic capture supported by over 100 pre-verified, production-ready PSoC Components; see the list of component datasheets. With PSoC Creator, you can:

1. Drag and drop component icons to build your hardware system design in the main design workspace
2. Codesign your application firmware with the PSoC hardware, using the PSoC Creator IDE C compiler
3. Configure components using the configuration tools
4. Explore the library of 100+ components
5. Review component datasheets

Figure 1. Multiple-Sensor Example Project in PSoC Creator Contents

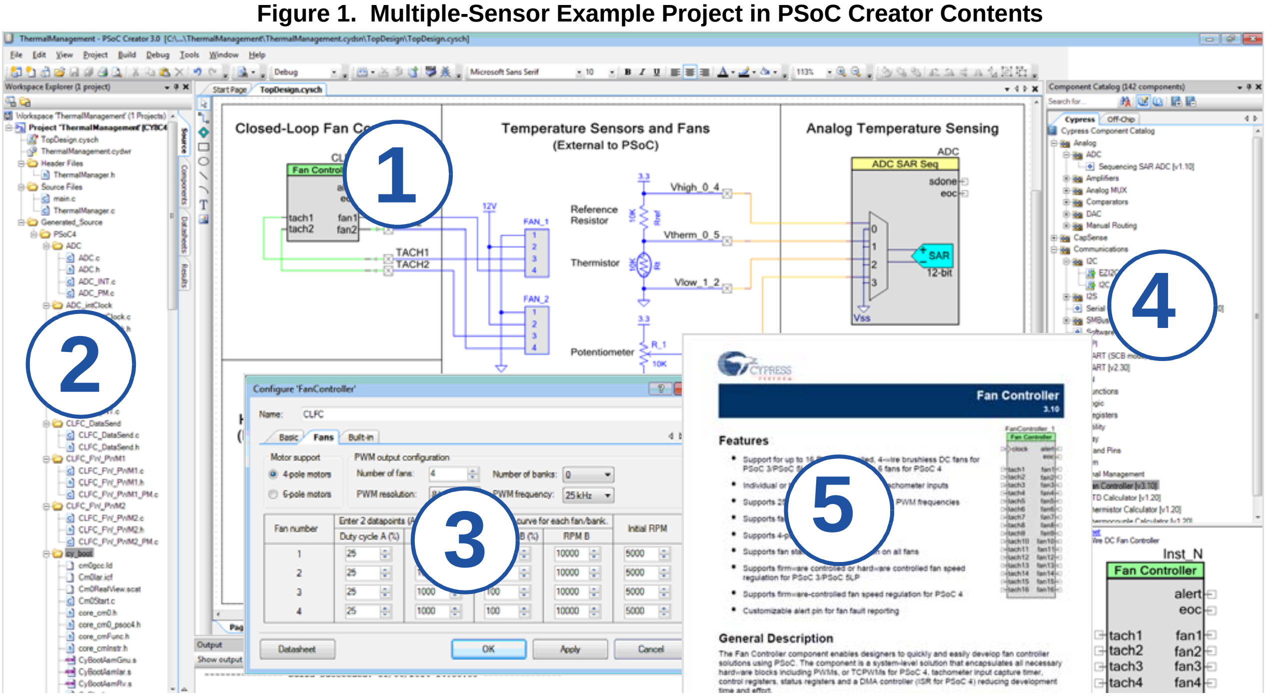

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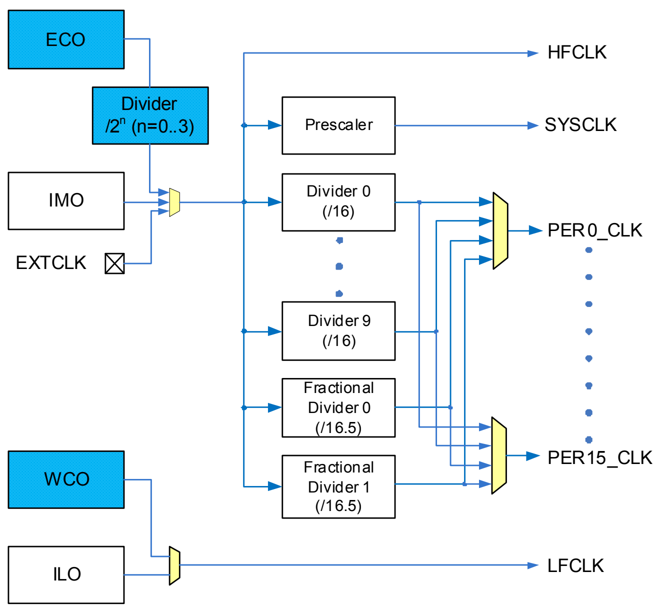
Figure 3. PSoC 4200_BL MCU Clocking Architecture



The HFCLK signal can be divided down (see Figure 3) to generate synchronous clocks for the UDBs, and the analog and digital peripherals. There are a total of 12 clock dividers for PSoC 4200_BL: ten with 16-bit divide capability and two with 16.5-bit divide capability. This allows the generation of 16 divided clock signals, which can be used by peripheral blocks. The analog clock leads the digital clocks to allow analog events to occur before the digital clock-related noise is generated. The 16-bit and 16.5-bit dividers allow a lot of flexibility in generating fine-grained frequency values and are fully supported in PSoC Creator.

Reset

PSoC 4200_BL device can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through resets and allows the software to determine the cause of the reset. An XRES pin is reserved for an external reset to avoid complications with the configuration and multiple pin functions during power-on or reconfiguration. The XRES pin has an internal pull-up resistor that is always enabled.

Voltage Reference

The PSoC 4200_BL reference system generates all internally required references. A one-percent voltage reference spec is provided for the 12-bit ADC. To allow better signal-to-noise ratios (SNR) and better absolute accuracy, it is possible to bypass the internal reference using a GPIO pin or use an external reference for the SAR. Refer to Table 19, “SAR ADC AC Specifications,” on page 26 for details.

BLE Radio and Subsystem

PSoC 4200_BL incorporates a Bluetooth Smart subsystem that contains the Physical Layer (PHY) and Link Layer (LL) engines with an embedded AES-128 security engine. The physical layer consists of the digital PHY and the RF transceiver that transmits and receives GFSK packets at 1 Mbps over a 2.4-GHz ISM band, which is compliant with Bluetooth Smart Bluetooth Specification 4.2. The baseband controller is a composite hardware and firmware implementation that supports both master and slave modes. Key protocol elements, such as HCI and link control, are implemented in firmware. Time-critical functional blocks, such as encryption, CRC, data whitening, and access code correlation, are implemented in hardware (in the LL engine).

The RF transceiver contains an integrated balun, which provides a single-ended RF port pin to drive a 50-Ω antenna via a matching/filtering network. In the receive direction, this block converts the RF signal from the antenna to a digital bit stream after performing GFSK demodulation. In the transmit direction, this block performs GFSK modulation and then converts a digital baseband signal to a radio frequency before transmitting it to air through the antenna.

The Bluetooth Smart Radio and Subsystem (BLESS) requires a 1.9-V minimum supply (the range varies from 1.9 V to 5.5 V).

Key features of BLESS are as follows:

- Master and slave single-mode protocol stack with logical link control and adaptation protocol (L2CAP), attribute (ATT), and security manager (SM) protocols
- API access to generic attribute profile (GATT), generic access profile (GAP), and L2CAP
- L2CAP connection-oriented channel
- GAP features
  - Broadcaster, Observer, Peripheral, and Central roles
  - Security mode 1: Level 1, 2, 3, and 4
  - Security mode 2: Level 1 and 2
  - User-defined advertising data
  - Multiple bond support
- GATT features
  - GATT client and server
  - Supports GATT sub-procedures
  - 32-bit universally unique identifier (UUID)
- Security Manager (SM)
  - Pairing methods: Just works, Passkey Entry, Out of Band and Numeric Comparison
  - Authenticated man-in-the-middle (MITM) protection and data signing
  - LE Secure Connections (Bluetooth 4.2 feature)
- Link Layer (LL)
  - Master and Slave roles
  - 128-bit AES engine
  - Encryption
  - Low-duty cycle advertising
  - LE Ping
  - LE Data Packet Length Extension (Bluetooth 4.2 feature)
  - Link Layer Privacy (with extended scanning filter policy, Bluetooth 4.2 feature)
- Supports all SIG-adopted BLE profiles

Analog Blocks

12-bit SAR ADC

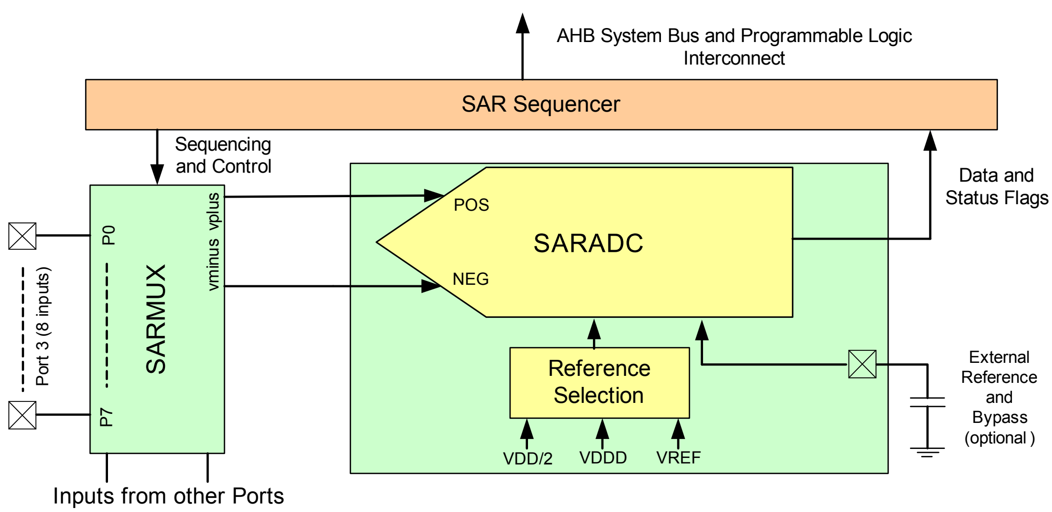
The 12-bit, 1-Msps SAR ADC can operate at a maximum clock rate of 18 MHz and requires a minimum of 18 clocks at that frequency to do a 12-bit conversion.

The block functionality is augmented for the user by adding a reference buffer to it (trimmable to ±1%) and by providing the choice of three internal voltage references, V_{DD}, $V_{DD}/2$, and V_{REF} (nominally 1.024 V), as well as an external reference through a GPIO pin. The Sample-and-Hold (S/H) aperture is programmable; it allows the gain bandwidth requirements of the amplifier driving the SAR inputs, which determine its settling time, to be relaxed if required. System performance will be 65 dB for true 12-bit precision provided appropriate references are used and system noise levels permit it. To improve the performance in noisy conditions, it is possible to provide an external bypass (through a fixed pin location) for the internal reference amplifier.

The SAR is connected to a fixed set of pins through an 8-input sequencer. The sequencer cycles through the selected channels autonomously (sequencer scan) and does so with zero switching overhead (that is, the aggregate sampling bandwidth is equal to 1 Msps whether it is for a single channel or distributed over several channels). The sequencer switching is effected through a state machine or through firmware-driven switching. A feature provided by the sequencer is the buffering of each channel to reduce CPU interrupt-service requirements. To accommodate signals with varying source impedances and frequencies, it is possible to have different sample times programmable for each channel. Also, the signal range specification through a pair of range registers (low and high range values) is implemented with a corresponding out-of-range interrupt if the digitized value exceeds the programmed range; this allows fast detection of out-of-range values without having to wait for a sequencer scan to be completed and the CPU to read the values and check for out-of-range values in software.

The SAR is able to digitize the output of the on-chip temperature sensor for calibration and other temperature-dependent functions. The SAR is not available in Deep Sleep and Hibernate modes as it requires a high-speed clock (up to 18 MHz). The SAR operating range is 1.71 to 5.5 V.

Figure 4. SAR ADC System Diagram



Opamps (CTBm Block)

PSoC 42X8_BLE has four opamps with Comparator modes, which allow most common analog functions to be performed on-chip, eliminating external components. PGAs, voltage buffers, filters, transimpedance amplifiers, and other functions can be realized with external passives saving power, cost, and space. The on-chip opamps are designed with enough bandwidth to drive the sample-and-hold circuit of the ADC without requiring external buffering.

Temperature Sensor

PSoC 4200_BL has an on-chip temperature sensor. This consists of a diode, which is biased by a current source that can be disabled to save power. The temperature sensor is connected to the ADC, which digitizes the reading and produces a temperature value by using a Cypress-supplied software that includes calibration and linearization.

Low-Power Comparators

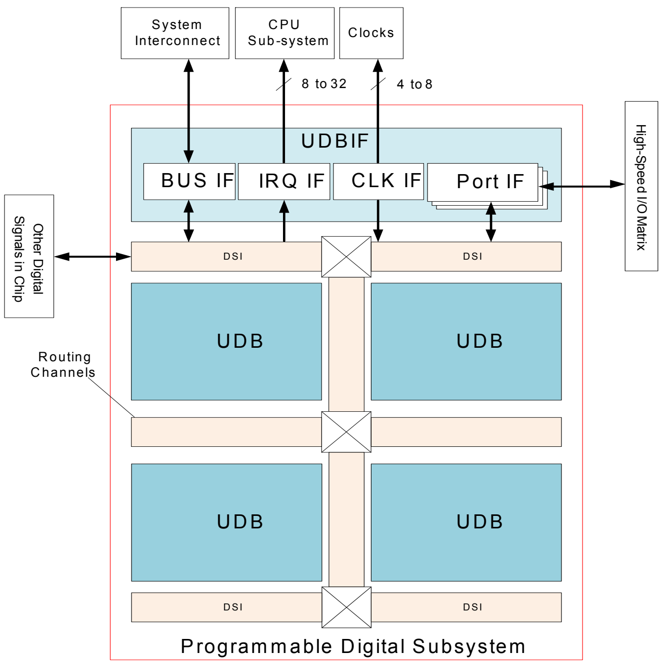
PSoC 4200_BL has a pair of low-power comparators, which can also operate in Deep Sleep and Hibernate modes. This allows the analog system blocks to be disabled while retaining the ability to monitor external voltage levels during low-power modes. The comparator outputs are normally synchronized to avoid metastability unless operating in an asynchronous power mode (Hibernate) where the system wake-up circuit is activated by a comparator-switch event.

Programmable Digital

Universal Digital Blocks (UDBs) and Port Interfaces

The PSoC 4XX8 BLE 4.2 has four UDBs; the UDB array also provides a switched Digital System Interconnect (DSI) fabric that allows signals from peripherals and ports to be routed to and through the UDBs for communication and control.

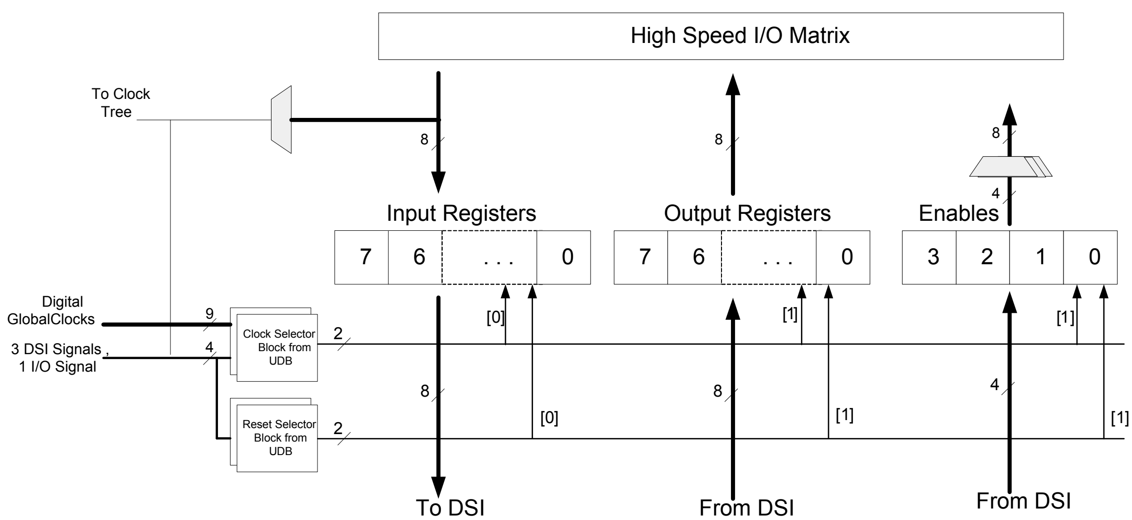
Figure 5. UDB Array



UDBs can be clocked from a clock-divider block, from a port interface (required for peripherals such as SPI), and from the DSI network directly or after synchronization.

A port interface is defined, which acts as a register that can be clocked with the same source as the PLDs inside the UDB array. This allows a faster operation because the inputs and outputs can be registered at the port interface close to the I/O pins and at the edge of the array. The port interface registers can be clocked by one of the I/Os from the same port. This allows interfaces such as SPI to operate at higher clock speeds by eliminating the delay for the port input to be routed over DSI and used to register other inputs (see Figure 6).

Figure 6. Port Interface



UDBs can generate interrupts (one UDB at a time) to the interrupt controller. UDBs retain the ability to connect to any pin on the chip through the DSI.

Special-Function Peripherals

LCD Segment Drive

PSoC 4200_BL has an LCD controller, which can drive up to four commons and up to 32 segments. It uses full digital methods to drive the LCD segments requiring no generation of internal LCD voltages. The two methods used are referred to as digital correlation and PWM.

The digital correlation method modulates the frequency and levels of the common and segment signals to generate the highest RMS voltage across a segment to light it up or to keep the RMS signal zero. This method is good for STN displays but may result in reduced contrast with TN (cheaper) displays.

The PWM method drives the panel with PWM signals to effectively use the capacitance of the panel to provide the integration of the modulated pulse-width to generate the desired LCD voltage. This method results in higher power consumption but can result in better results when driving TN displays. LCD operation is supported during Deep Sleep mode, refreshing a small display buffer (four bits; one 32-bit register per port).

CapSense

CapSense is supported on all pins in PSoC 4200_BL through a CapSense Sigma-Delta (CSD) block that can be connected to any pin through an analog mux bus that any GPIO pin can be connected to via an Analog switch. CapSense function can thus be provided on any pin or group of pins in a system under software control. A Component is provided for the CapSense block to make it easy for the user.

The shield voltage can be driven on another mux bus to provide liquid-tolerance capability. Liquid tolerance is provided by driving the shield electrode in phase with the sense electrode to keep the shield capacitance from attenuating the sensed input.

The CapSense block has two IDACs which can be used for general purposes if CapSense is not being used (both IDACs are available in that case) or if CapSense is used without liquid tolerance (one IDAC is available).

Pinouts

Table 1 shows the pin list for the PSoC 4200_BL device. Port 3 consists of the high-speed analog inputs for the SAR mux. All pins support CSD CapSense and analog mux bus connections.

Table 1. PSoC 4200_BL Pin List (QFN Package)

Pin	Name	Type	Description
1	VDDD	POWER	1.71-V to 5.5-V digital supply
2	XTAL32O/P6.0	CLOCK	32.768-kHz crystal
3	XTAL32I/P6.1	CLOCK	32.768-kHz crystal or external clock input
4	XRES	RESET	Reset, active LOW
5	P4.0	GPIO	Port 4 Pin 0, lcd, csd
6	P4.1	GPIO	Port 4 Pin 1, lcd, csd
7	P5.0	GPIO	Port 5 Pin 0, lcd, csd
8	P5.1	GPIO	Port 5 Pin 1, lcd, csd
9	VSSD	GROUND	Digital ground
10	VDDR	POWER	1.9-V to 5.5-V radio supply
11	GANT1	GROUND	Antenna shielding ground
12	ANT	ANTENNA	Antenna pin
13	GANT2	GROUND	Antenna shielding ground
14	VDDR	POWER	1.9-V to 5.5-V radio supply
15	VDDR	POWER	1.9-V to 5.5-V radio supply
16	XTAL24I	CLOCK	24-MHz crystal or external clock input
17	XTAL24O	CLOCK	24-MHz crystal
18	VDDR	POWER	1.9-V to 5.5-V radio supply
19	P0.0	GPIO	Port 0 Pin 0, lcd, csd
20	P0.1	GPIO	Port 0 Pin 1, lcd, csd
21	P0.2	GPIO	Port 0 Pin 2, lcd, csd
22	P0.3	GPIO	Port 0 Pin 3, lcd, csd
23	VDDD	POWER	1.71-V to 5.5-V digital supply
24	P0.4	GPIO	Port 0 Pin 4, lcd, csd
25	P0.5	GPIO	Port 0 Pin 5, lcd, csd
26	P0.6	GPIO	Port 0 Pin 6, lcd, csd
27	P0.7	GPIO	Port 0 Pin 7, lcd, csd
28	P1.0	GPIO	Port 1 Pin 0, lcd, csd
29	P1.1	GPIO	Port 1 Pin 1, lcd, csd
30	P1.2	GPIO	Port 1 Pin 2, lcd, csd
31	P1.3	GPIO	Port 1 Pin 3, lcd, csd
32	P1.4	GPIO	Port 1 Pin 4, lcd, csd
33	P1.5	GPIO	Port 1 Pin 5, lcd, csd
34	P1.6	GPIO	Port 1 Pin 6, lcd, csd
35	P1.7	GPIO	Port 1 Pin 7, lcd, csd
36	VDDA	POWER	1.71-V to 5.5-V analog supply
37	P2.0	GPIO	Port 2 Pin 0, lcd, csd
38	P2.1	GPIO	Port 2 Pin 1, lcd, csd
39	P2.2	GPIO	Port 2 Pin 2, lcd, csd

GPIO

Table 8. GPIO DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID58	V_{IH}	Input voltage HIGH threshold	0.7 × V_{DD}	–	–	V	CMOS input
SID59	V_{IL}	Input voltage LOW threshold	–	–	0.3 × V_{DD}	V	CMOS input
SID60	V_{IH}	LVTTL input, V_{DD} < 2.7 V	0.7 × V_{DD}	–	-	V	–
SID61	V_{IL}	LVTTL input, V_{DD} < 2.7 V	–	–	0.3× V_{DD}	V	–
SID62	V_{IH}	LVTTL input, V_{DD} >= 2.7 V	2.0	–	-	V	–
SID63	V_{IL}	LVTTL input, V_{DD} >= 2.7 V	–	–	0.8	V	–
SID64	V_{OH}	Output voltage HIGH level	V_{DD} –0.6	–	–	V	Ioh = 4-mA at 3.3-V V_{DD}
SID65	V_{OH}	Output voltage HIGH level	V_{DD} –0.5	–	–	V	Ioh = 1-mA at 1.8-V V_{DD}
SID66	V_{OL}	Output voltage LOW level	–	–	0.6	V	Iol = 8-mA at 3.3-V V_{DD}
SID67	V_{OL}	Output voltage LOW level	–	–	0.6	V	Iol = 4-mA at 1.8-V V_{DD}
SID68	V_{OL}	Output voltage LOW level	–	–	0.4	V	Iol = 3-mA at 3.3-V V_{DD}
SID69	Rpullup	Pull-up resistor	3.5	5.6	8.5	kΩ	–
SID70	Rpulldown	Pull-down resistor	3.5	5.6	8.5	kΩ	–
SID71	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	25 °C, V_{DD} = 3.3 V
SID72	I_{IL_CTBM}	Input leakage on CTBm input pins	–	–	4	nA	–
SID73	C_{IN}	Input capacitance	–	–	7	pF	–
SID74	Vhysttl	Input hysteresis LVTTL	25	40		mV	V_{DD} > 2.7 V
SID75	Vhyscmos	Input hysteresis CMOS	0.05 × V_{DD}	–	–	mV	–
SID76	Idiode	Current through protection diode to V_{DD}/V_{SS}	–	–	100	µA	–
SID77	I_{TOT_GPIO}	Maximum total source or sink chip current	–	–	200	mA	–

Table 9. GPIO AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID78	T_{RISEF}	Rise time in Fast-Strong mode	2	–	12	ns	3.3-V V_{DDD}, C_{LOAD} = 25-pF
SID79	T_{FALLF}	Fall time in Fast-Strong mode	2	–	12	ns	3.3-V V_{DDD}, C_{LOAD} = 25-pF
SID80	T_{RISES}	Rise time in Slow-Strong mode	10	–	60	–	3.3-V V_{DDD}, C_{LOAD} = 25-pF
SID81	T_{FALLS}	Fall time in Slow-Strong mode	10	–	60	–	3.3-V V_{DDD}, C_{LOAD} = 25-pF
SID82	$F_{GPIOUT1}$	GPIO Fout; 3.3 V ≤ V_{DD} ≤ 5.5 V. Fast-Strong mode	–	–	33	MHz	90/10%, 25-pF load, 60/40 duty cycle

Note
2. V_{IH} must not exceed V_{DDD} + 0.2 V.

Table 19. SAR ADC AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID167	A_psrr	Power supply rejection ratio	70	–	–	dB	Measured at 1-V reference
SID168	A_cmrr	Common mode rejection ratio	66	–	–	dB	–
SID169	A_samp	Sample rate	–	–	1	Msps	
SID313	Fsarintref	SAR operating speed without external ref. bypass	–	–	100	Ksps	12-bit resolution
SID170	A_snr	Signal-to-noise ratio (SNR)	65	–	–	dB	Fin = 10 kHz
SID171	A_bw	Input bandwidth without aliasing	–	–	A_samp/2	kHz	–
SID172	A_inl	Integral non linearity. V_{DD} = 1.71 to 5.5 V, 1 Msps	–1.7	–	2	LSB	Vref = 1 V to V_{DD}
SID173	A_INL	Integral non linearity. V_{DDD} = 1.71 to 3.6 V, 1 Msps	–1.5	–	1.7	LSB	Vref = 1.71 V to V_{DD}
SID174	A_INL	Integral non linearity. V_{DD} = 1.71 to 5.5 V, 500 Ksps	–1.5	–	1.7	LSB	Vref = 1 V to V_{DD}
SID175	A_dnl	Differential non linearity. V_{DD} = 1.71 to 5.5 V, 1 Msps	–1	–	2.2	LSB	Vref = 1 V to V_{DD}
SID176	A_DNL	Differential non linearity. V_{DD} = 1.71 to 3.6 V, 1 Msps	–1	–	2	LSB	Vref = 1.71 V to V_{DD}
SID177	A_DNL	Differential non linearity. V_{DD} = 1.71 to 5.5 V, 500 Ksps	–1	–	2.2	LSB	Vref = 1 V to V_{DD}
SID178	A_thd	Total harmonic distortion	–	–	–65	dB	Fin = 10 kHz

CSD

Table 20. CSD Block Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID179	V_{CSD}	Voltage range of operation	1.71	–	5.5	V	–
SID180	IDAC1	DNL for 8-bit resolution	–1	–	1	LSB	–
SID181	IDAC1	INL for 8-bit resolution	–3	–	3	LSB	–
SID182	IDAC2	DNL for 7-bit resolution	–1	–	1	LSB	–
SID183	IDAC2	INL for 7-bit resolution	–3	–	3	LSB	–
SID184	SNR	Ratio of counts of finger to noise	5	–	–	Ratio	Capacitance range of 9 to 35 pF, 0.1 pF sensitivity. Radio is not operating during the scan
SID185	I_{DAC1_CRT1}	Output current of IDAC1 (8 bits) in High range	–	612	–	µA	–
SID186	I_{DAC1_CRT2}	Output current of IDAC1 (8 bits) in Low range	–	306	–	µA	–
SID187	I_{DAC2_CRT1}	Output current of IDAC2 (7 bits) in High range	–	305	–	µA	–
SID188	I_{DAC2_CRT2}	Output current of IDAC2 (7 bits) in Low range	–	153	–	µA	–

Digital Peripherals

Timer

Table 21. Timer DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID189	I_{TIM1}	Block current consumption at 3 MHz	–	–	50	µA	16-bit timer
SID190	I_{TIM2}	Block current consumption at 12 MHz	–	–	175	µA	16-bit timer
SID191	I_{TIM3}	Block current consumption at 48 MHz	–	–	712	µA	16-bit timer

Table 22. Timer AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID192	$T_{TIMFREQ}$	Operating frequency	F_{CLK}	–	48	MHz	–
SID193	$T_{CAPWINT}$	Capture pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	–
SID194	$T_{CAPWEXT}$	Capture pulse width (external)	$2 \times T_{CLK}$	–	–	ns	–
SID195	T_{TIMRES}	Timer resolution	T_{CLK}	–	–	ns	–
SID196	$T_{TENWIDINT}$	Enable pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	–
SID197	$T_{TENWIDEXT}$	Enable pulse width (external)	$2 \times T_{CLK}$	–	–	ns	–
SID198	$T_{TIMRESWINT}$	Reset pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	–
SID199	$T_{TIMRESEXT}$	Reset pulse width (external)	$2 \times T_{CLK}$	–	–	ns	–

Counter

Table 23. Counter DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID200	I_{CTR1}	Block current consumption at 3 MHz	–	–	50	µA	16-bit counter
SID201	I_{CTR2}	Block current consumption at 12 MHz	–	–	175	µA	16-bit counter
SID202	I_{CTR3}	Block current consumption at 48 MHz	–	–	712	µA	16-bit counter

Table 24. Counter AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID203	$T_{CTRFREQ}$	Operating frequency	F_{CLK}	–	48	MHz	–
SID204	$T_{CTRPWINT}$	Capture pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	–
SID205	$T_{CTRPWEXT}$	Capture pulse width (external)	$2 \times T_{CLK}$	–	–	ns	–
SID206	T_{CTRES}	Counter Resolution	T_{CLK}	–	–	ns	–
SID207	$T_{CENWIDINT}$	Enable pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	–
SID208	$T_{CENWIDEXT}$	Enable pulse width (external)	$2 \times T_{CLK}$	–	–	ns	–
SID209	$T_{CTRRESWINT}$	Reset pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	–
SID210	$T_{CTRRESWEXT}$	Reset pulse width (external)	$2 \times T_{CLK}$	–	–	ns	–

Pulse Width Modulation (PWM)

Table 25. PWM DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID211	I_{PWM1}	Block current consumption at 3 MHz	–	–	50	µA	16-bit PWM
SID212	I_{PWM2}	Block current consumption at 12 MHz	–	–	175	µA	16-bit PWM
SID213	I_{PWM3}	Block current consumption at 48 MHz	–	–	741	µA	16-bit PWM

Table 47. IMO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID296	$F_{IMOTOL3}$	Frequency variation from 3 to 48 MHz	–	–	±2	%	With API-called calibration
SID297	$F_{IMOTOL3}$	IMO startup time	–	–	12	µs	–

Internal Low-Speed Oscillator

Table 48. ILO DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID298	I_{ILO2}	ILO operating current at 32 kHz	–	0.3	1.05	µA	–

Table 49. ILO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID299	$T_{STARTILO1}$	ILO startup time	–	–	2	ms	–
SID300	$F_{ILOTRIM1}$	32-kHz trimmed frequency	15	32	50	kHz	–

Table 50. External Clock Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID301	ExtClkFreq	External clock input frequency	0	–	48	MHz	CMOS input level only
SID302	ExtClkDuty	Duty cycle; Measured at $V_{DD/2}$	45	–	55	%	CMOS input level only

Table 51. UDB AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
Data Path performance							
SID303	$F_{MAX\text{-}TIMER}$	Max frequency of 16-bit timer in a UDB pair	–	–	48	MHz	–
SID304	$F_{MAX\text{-}ADDER}$	Max frequency of 16-bit adder in a UDB pair	–	–	48	MHz	–
SID305	F_{MAX_CRC}	Max frequency of 16-bit CRC/PRS in a UDB pair	–	–	48	MHz	–
PLD Performance in UDB							
SID306	F_{MAX_PLD}	Max frequency of 2-pass PLD function in a UDB pair	–	–	48	MHz	–
Clock to Output Performance							
SID307	$T_{CLK\_OUT\_UDB1}$	Prop. delay for clock in to data out at 25 °C, Typical	–	15	–	ns	–
SID308	$T_{CLK\_OUT\_UDB2}$	Prop. delay for clock in to data out, Worst case	–	25	–	ns	–

Table 52. BLE Subsystem

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
RF Receiver Specification							
SID340	RXS, IDLE	RX sensitivity with idle transmitter	–	–89	–	dBm	–
SID340A		RX sensitivity with idle transmitter excluding Balun loss	–	–91	–	dBm	Guaranteed by design simulation
SID341	RXS, DIRTY	RX sensitivity with dirty transmitter	–	–87	–70	dBm	RF-PHY Specification (RCV-LE/CA/01/C)
SID342	RXS, HIGHGAIN	RX sensitivity in high-gain mode with idle transmitter	–	–91	–	dBm	–
SID343	PRXMAX	Maximum input power	–10	–1	–	dBm	RF-PHY Specification (RCV-LE/CA/06/C)
SID344	CI1	Co-channel interference, Wanted signal at –67 dBm and Interferer at FRX	–	9	21	dB	RF-PHY Specification (RCV-LE/CA/03/C)
SID345	CI2	Adjacent channel interference Wanted signal at –67 dBm and Interferer at FRX ±1 MHz	–	3	15	dB	RF-PHY Specification (RCV-LE/CA/03/C)
SID346	CI3	Adjacent channel interference Wanted signal at –67 dBm and Interferer at FRX ±2 MHz	–	–29	–	dB	RF-PHY Specification (RCV-LE/CA/03/C)
SID347	CI4	Adjacent channel interference Wanted signal at –67 dBm and Interferer at ≥FRX ±3 MHz	–	–39	–	dB	RF-PHY Specification (RCV-LE/CA/03/C)
SID348	CI5	Adjacent channel interference Wanted Signal at –67 dBm and Interferer at Image frequency (F_{IMAGE})	–	–20	–	dB	RF-PHY Specification (RCV-LE/CA/03/C)
SID349	CI6	Adjacent channel interference Wanted signal at –67 dBm and Interferer at Image frequency (F_{IMAGE} ± 1 MHz)	–	–30	–	dB	RF-PHY Specification (RCV-LE/CA/03/C)
SID350	OBB1	Out-of-band blocking, Wanted signal at –67 dBm and Interferer at F = 30–2000 MHz	–30	–27	–	dBm	RF-PHY Specification (RCV-LE/CA/04/C)
SID351	OBB2	Out-of-band blocking, Wanted signal at –67 dBm and Interferer at F = 2003–2399 MHz	–35	–27	–	dBm	RF-PHY Specification (RCV-LE/CA/04/C)
SID352	OBB3	Out-of-band blocking, Wanted signal at –67 dBm and Interferer at F = 2484–2997 MHz	–35	–27	–	dBm	RF-PHY Specification (RCV-LE/CA/04/C)
SID353	OBB4	Out-of-band blocking, Wanted signal a –67 dBm and Interferer at F = 3000–12750 MHz	–30	–27	–	dBm	RF-PHY Specification (RCV-LE/CA/04/C)
SID354	IMD	Intermodulation performance Wanted signal at –64 dBm and 1-Mbps BLE, third, fourth, and fifth offset channel	–50	–	–	dBm	RF-PHY Specification (RCV-LE/CA/05/C)
SID355	RXSE1	Receiver spurious emission 30 MHz to 1.0 GHz	–	–	–57	dBm	100-kHz measurement bandwidth ETSI EN300 328 V1.8.1

Table 52. BLE Subsystem *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID378	ITX,-6dBm	TX current at –6-dBm setting (PA3)	–	14.5	–	mA	–
SID379	ITX,-12dBm	TX current at –12-dBm setting (PA2)	–	13.2	–	mA	–
SID380	ITX,-18dBm	TX current at –18-dBm setting (PA1)	–	12.5	–	mA	–
SID380A	Iavg_1sec, 0dBm	Average current at 1-second BLE connection interval	–	17.1	–	µA	TXP: 0 dBm; ±20-ppm master and slave clock accuracy.
SID380B	Iavg_4sec, 0dBm	Average current at 4-second BLE connection interval	–	6.1	–	µA	TXP: 0 dBm; ±20-ppm master and slave clock accuracy.
General RF Specifications							
SID381	FREQ	RF operating frequency	2400	–	2482	MHz	–
SID382	CHBW	Channel spacing	–	2	–	MHz	–
SID383	DR	On-air data rate	–	1000	–	kbps	–
SID384	IDLE2TX	BLE.IDLE to BLE. TX transition time	–	120	140	µs	–
SID385	IDLE2RX	BLE.IDLE to BLE. RX transition time	–	75	120	µs	–
RSSI Specifications							
SID386	RSSI, ACC	RSSI accuracy	–	±5	–	dB	–
SID387	RSSI, RES	RSSI resolution	–	1	–	dB	–
SID388	RSSI, PER	RSSI sample period	–	6	–	µs	–

Table 53. ECO Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID389	F_{ECO}	Crystal frequency	–	24	–	MHz	–
SID390	F_{TOL}	Frequency tolerance	–50	–	50	ppm	–
SID391	ESR	Equivalent series resistance	–	–	60	Ω	–
SID392	PD	Drive level	–	–	100	µW	–
SID393	T_{START1}	Startup time (Fast Charge on)	–	–	850	µs	–
SID394	T_{START2}	Startup time (Fast Charge off)	–	–	3	ms	–
SID395	C_L	Load capacitance	–	8	–	pF	–
SID396	C0	Shunt capacitance	–	1.1	–	pF	–
SID397	I_{ECO}	Operating current	–	1400	–	µA	–

Table 54. WCO Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID398	F_{WCO}	Crystal frequency	–	32.768	–	kHz	–
SID399	FTOL	Frequency tolerance	–	50	–	ppm	–
SID400	ESR	Equivalent series resistance	–	50	–	kΩ	–
SID401	PD	Drive level	–	–	1	µW	–
SID402	T_{START}	Startup time	–	–	500	ms	–
SID403	C_L	Crystal load capacitance	6	–	12.5	pF	–
SID404	C0	Crystal shunt capacitance	–	1.35	–	pF	–
SID405	I_{WCO1}	Operating current (High-Power mode)	–	–	8	µA	–
SID406	I_{WCO2}	Operating current (Low-Power mode)	–	–	2.6	µA	–

Ordering Information

The PSoC 4200_BL part numbers and features are listed in Table 55.

Table 55. PSoC 4200_BL Part Numbers

Product Family	MPN	Max CPU Speed (MHz)	BLE subsystem	Flash (KB)	SRAM (KB)	UDB	Opamp	CapSense	TMG (Gestures)	Direct LCD Drive	12-bit SAR ADC	DMA	LP Comparators	TCPWM Blocks	SCB Blocks	GPIO	Package	Temperature Range
PSoC 4200_BL	CY8C4247LQI-BL473	48	4.1	128	16	4	4	–	–	–	1 Msps	–	2	4	2	36	QFN	85 °C
	CY8C4247FNI-BL473	48	4.1	128	16	4	4	–	–	–	1 Msps	–	2	4	2	36	CSP	85 °C
	CY8C4247LQI-BL453	48	4.1	128	16	4	4	1	–	–	1 Msps	–	2	4	2	36	QFN	85 °C
	CY8C4247LQI-BL463	48	4.1	128	16	4	4	–	–	1	1 Msps	–	2	4	2	36	QFN	85 °C
	CY8C4247LQI-BL483	48	4.1	128	16	4	4	1	–	1	1 Msps	–	2	4	2	36	QFN	85 °C
	CY8C4247LQI-BL493	48	4.1	128	16	4	4	1	1	1	1 Msps	–	2	4	2	36	QFN	85 °C
	CY8C4247FNI-BL483	48	4.1	128	16	4	4	1	–	1	1 Msps	–	2	4	2	36	68-CSP	85 °C
	CY8C4247FNI-BL493	48	4.1	128	16	4	4	1	1	1	1 Msps	–	2	4	2	36	68-CSP	85 °C
	CY8C4247FNQ-BL483	48	4.1	128	16	4	4	1	–	1	1 Msps	–	2	4	2	36	68-CSP	105 °C
	CY8C4247LQQ-BL483	48	4.1	128	16	4	4	1	–	1	1 Msps	–	2	4	2	36	QFN	105 °C
	CY8C4247FLI-BL493	48	4.1	128	16	4	4	1	1	1	1 Msps	–	2	4	2	36	Thin 68-CSP	85 °C
	CY8C4248LQI-BL473	48	4.1	256	32	4	4	–	–	–	1 Msps	1	2	4	2	36	QFN	85 °C
	CY8C4248LQI-BL453	48	4.1	256	32	4	4	1	–	–	1 Msps	1	2	4	2	36	QFN	85 °C
	CY8C4248LQI-BL483	48	4.1	256	32	4	4	1	–	1	1 Msps	1	2	4	2	36	QFN	85 °C
	CY8C4248FNI-BL483	48	4.1	256	32	4	4	1	–	1	1 Msps	1	2	4	2	36	76-CSP	85 °C
	CY8C4248FLI-BL483	48	4.1	256	32	4	4	1	–	1	1 Msps	1	2	4	2	36	Thin 76-CSP	85 °C
	CY8C4248LQI-BL543	48	4.2	256	32	–	2	–	–	–	1 Msps	1	–	4	2	36	QFN	85 °C
	CY8C4248FNI-BL543	48	4.2	256	32	–	2	–	–	–	1 Msps	1	–	4	2	36	76-CSP	85 °C
	CY8C4248LQI-BL573	48	4.2	256	32	4	4	–	–	–	1 Msps	1	2	4	2	36	QFN	85 °C
	CY8C4248FNI-BL573	48	4.2	256	32	4	4	–	–	–	1 Msps	1	2	4	2	36	76-CSP	85 °C
	CY8C4248LQI-BL553	48	4.2	256	32	4	4	1	–	–	1 Msps	1	2	4	2	36	QFN	85 °C
	CY8C4248FNI-BL553	48	4.2	256	32	4	4	1	–	–	1 Msps	1	2	4	2	36	76-CSP	85 °C
	CY8C4248LQI-BL563	48	4.2	256	32	4	4	–	–	1	1 Msps	1	2	4	2	36	QFN	85 °C
	CY8C4248FNI-BL563	48	4.2	256	32	4	4	–	–	1	1 Msps	1	2	4	2	36	76-CSP	85 °C
	CY8C4248LQI-BL583	48	4.2	256	32	4	4	1	–	1	1 Msps	1	2	4	2	36	QFN	85 °C
	CY8C4248FNI-BL583	48	4.2	256	32	4	4	1	–	1	1 Msps	1	2	4	2	36	76-CSP	85 °C
	CY8C4248FLI-BL583	48	4.2	256	32	4	4	1	–	1	1 Msps	1	2	4	2	36	Thin 76-CSP	85 °C
	CY8C4248LQQ-BL583	48	4.2	256	32	4	4	1	–	1	1 Msps	1	2	4	2	36	QFN	105 °C
	CY8C4248FNQ-BL583	48	4.2	256	32	4	4	1	–	1	1 Msps	1	2	4	2	36	76-CSP	105 °C
	CY8C4248LQI-BL593	48	4.2	256	32	4	4	1	1	1	1 Msps	1	2	4	2	36	QFN	85 °C
	CY8C4248FNI-BL593	48	4.2	256	32	4	4	1	1	1	1 Msps	1	2	4	2	36	76-CSP	85 °C

PSoC 4 devices follow the part numbering convention described in the following table. All fields are single-character alphanumeric (0, 1, 2, …, 9, A,B, …, Z) unless stated otherwise.

Ordering Code Definitions

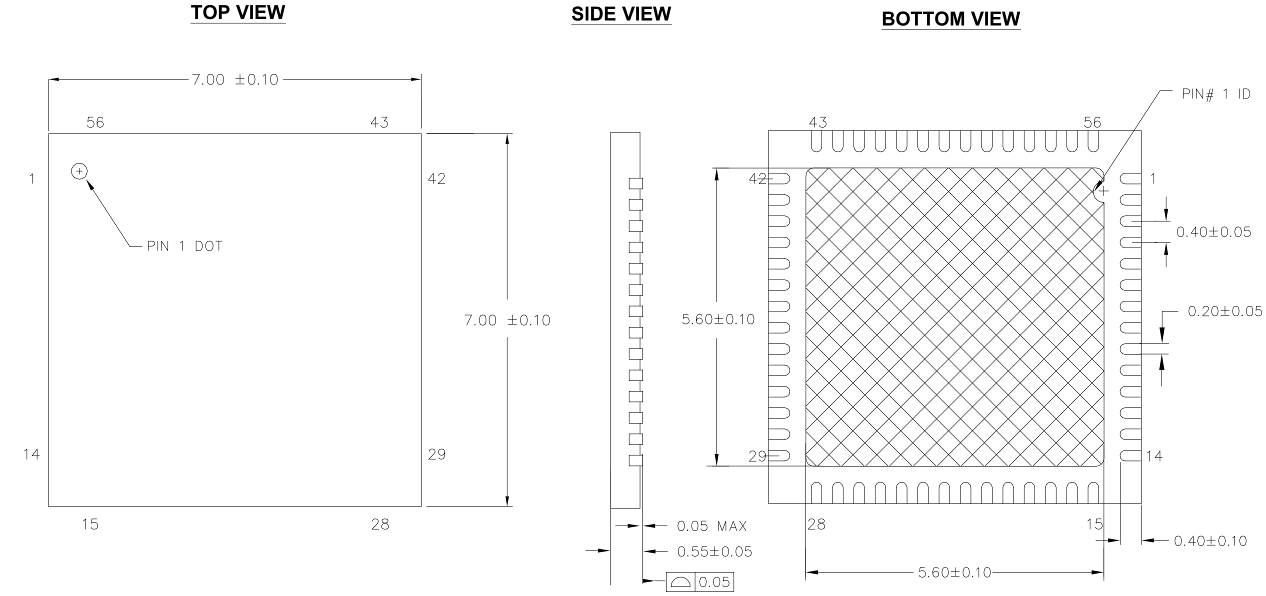
Example: CY8C 4 A B C D E F - BLXYZ

Example	
CY8 C	Cypress Prefix
4 : PSoC 4	Architecture
2 : 4200 Family	Family within Architecture
4 : 48 MHz	Speed Grade
8 : 256 KB	Flash Capacity
LQ : QFN	Package Code
I : Industrial	Temperature Range
BLXYZ: Attributes	Attributes Code

The Field Values are listed in the following table:

Field	Description	Values	Meaning
CY8C	Cypress Prefix		
4	Architecture	4	PSoC 4
A	Family within architecture	2	4200-BLE Family
B	CPU Speed	4	48 MHz
C	Flash Capacity	8, 7	256, 128 KB respectively
DE	Package Code	FN	WLCSP
		LQ	QFN
		FL	Thin CSP
F	Temperature Range	I	Industrial
BLXYZ	Attributes Code	BL400-BL499	Bluetooth 4.1 compliant
		BL500-BL599	Bluetooth 4.2 compliant

Figure 8. 56-Pin QFN 7 × 7 × 0.6 mm



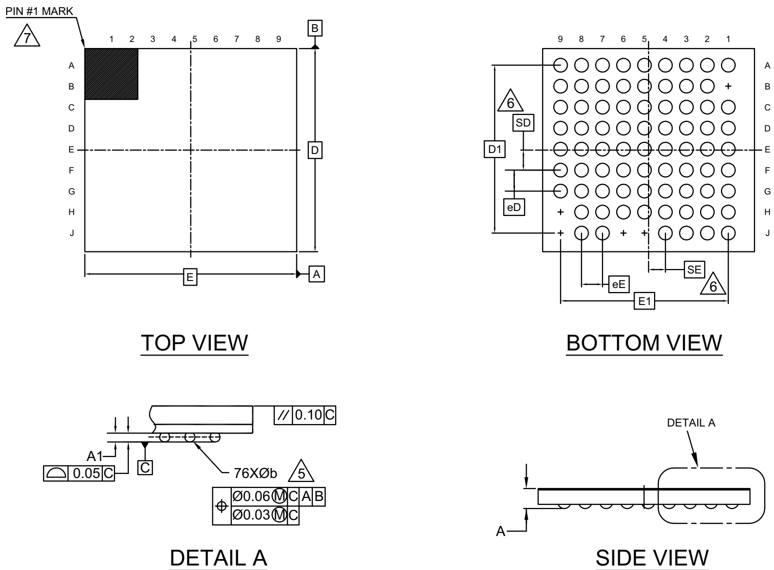
NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO-248
3. ALL DIMENSIONS ARE IN MILLIMETERS

001-58740 *C

The center pad on the QFN package should be connected to ground (VSS) for best mechanical, thermal, and electrical performance.

Figure 12. 76-Ball WLCSP Package Outline



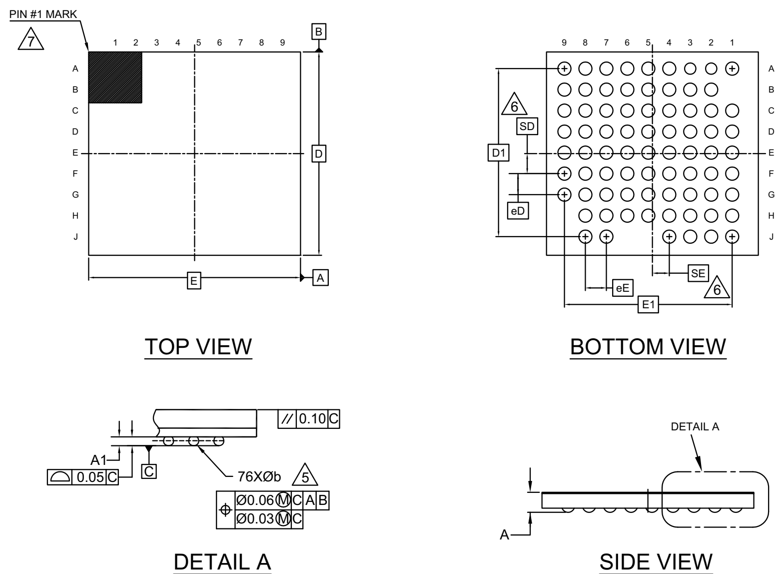
SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	0.55
A1	0.18	0.21	0.24
D	3.87 BSC		
E	4.04 BSC		
D1	3.20 BSC		
E1	3.20 BSC		
MD	9		
ME	9		
N	76		
Ø b	0.23	0.26	0.29
eD	0.40 BSC		
eE	0.40 BSC		
SD	0.381 BSC		
SE	0.321 BSC		

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
7. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.
9. JEDEC SPECIFICATION NO. REF : N/A

001-96603 *B

Figure 13. 76-Ball Thin WLCSP Package Outline



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	0.40
A1	0.072	0.08	0.088
D	3.87 BSC		
E	4.04 BSC		
D1	3.20 BSC		
E1	3.20 BSC		
MD	9		
ME	9		
N	76		
Ø b	0.22	0.25	0.28
eD	0.40 BSC		
eE	0.40 BSC		
SD	0.381		
SE	0.321		

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
7. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.

002-10658 **

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