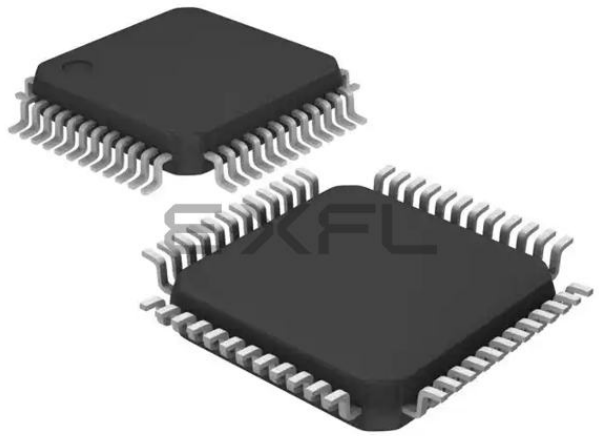

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Details	
Product Status	Not For New Designs
Core Processor	8051
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/n79e875alg

- Up to two channels PWM independent from paired PWM channels.

- One build-in OP amplifier.
- Eight-channel multiplexed with 10-bits A/D converter.
  - Support synchronized trigger with PWM period.
  - Support OP amplifier output conversion.
  - Support digital compare function.
- Two analog comparators with optional internal reference voltage input at negative end.
- Eight-keypad interrupt inputs.
- Built-in power management.
  - Idle mode
  - Power down mode
- LED drive capability (20mA) on all port pins.
- Config-bits selectable 3 levels(4.5V/3.8V/2.6V) Brown-Out voltage detect interrupt and reset.
- Independent Programmable Watchdog Timer.
- Program and Data Flash security protection.
- Development Tools:
  - JTAG ICE(In Circuit Emulation) tool
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  - Lead Free (RoHS) LQFP 48: N79E875ALG series (-40°C ~85°C)
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7-0	DPL.[7:0]	This is the low byte of the standard 8052 16-bit data pointer.

DATA POINTER HIGH **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	DPH.7	DPH.6	DPH.5	DPH.4	DPH.3	DPH.2	DPH.1	DPH.0

Mnemonic: DPH Address: 83h

BIT	NAME	FUNCTION
7-0	DPH.[7:0]	This is the high byte of the standard 8052 16-bit data pointer. This is the high byte of the DPTR 16-bit data pointer.

DIVIDER **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	CCDIV.1	CCDIV.0	PWMDIV.1	PWMDIV.0	T3DIV.1	T3DIV.0	T0DIV.1	T0DIV.0

Mnemonic: DIV Address: 86h

BIT	NAME	FUNCTION
7~6	CCDIV.1~0	Timer 2 clock select: CCDIV.1 / CCDIV.0 0 / 0 : Timer 2 clock = Fcpu 0 / 1 : Timer 2 clock = Fcpu/4 1 / 0 : Timer 2 clock = Fcpu/16 1 / 1 : Timer 2 clock = Fcpu/32
5~4	PWMDIV.1~0	PWM clock select: PWMDIV.1 / PWMDIV.0 0 / 0 : PWM clock = Fcpu 0 / 1 : PWM clock = Fcpu/2 1 / 0 : PWM clock = Fcpu/4 1 / 1 : PWM clock = Fcpu/16
3~2	T3DIV.1~0	Timer 3 clock select: T3DIV.1 / T3DIV.0 0 / 0 : Timer 3 clock = Fcpu/4 0 / 1 : Timer 3 clock = Fcpu/16 1 / 0 : Timer 3 clock = Fcpu/32

		automatically when the program does a timer 1 interrupt service routine. Software can also set or clear this bit.
6	TR1	Timer 1 Run Control. This bit is set or cleared by software to turn timer/counter on or off.
5	TF0	Timer 0 Overflow Flag. This bit is set when Timer 0 overflows. It is cleared automatically when the program does a timer 0 interrupt service routine. Software can also set or clear this bit.
4	TR0	Timer 0 Run Control. This bit is set or cleared by software to turn timer/counter on or off.
3	IE1	Interrupt 1 Edge Detect Flag: Set by hardware when an edge/level is detected on $\overline{INT1}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the inverse of the pin.
2	IT1	Interrupt 1 Type Control. Set/cleared by software to specify falling edge/ low level triggered external inputs.
1	IE0	Interrupt 0 Edge Detect Flag. Set by hardware when an edge/level is detected on $\overline{INT0}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the inverse of the pin.
0	IT0	Interrupt 0 Type Control: Set/cleared by software to specify falling edge/ low level triggered external inputs.

TIMER MODE CONTROL **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
	TIMER1				TIMER0			

Mnemonic: TMOD Address: 89h

BIT	NAME	FUNCTION
7	GATE	Gating control: When this bit is set, Timer/counter 1 is enabled only while the $\overline{INT1}$ pin is high and the TR1 control bit is set. When cleared, the $\overline{INT1}$ pin has no effect, and Timer 1 is enabled whenever TR1 control bit is set.
6	C/$\overline{T}$	Timer or Counter Select: When clear, Timer 1 is incremented by the internal clock. When set, the timer counts falling edges on the T1 pin.
5	M1	Timer 1 mode select bit 1. See table below.
4	M0	Timer 1 mode select bit 0. See table below.
3	GATE	Gating control: When this bit is set, Timer/counter 0 is enabled only while the $\overline{INT0}$ pin is high and the TR0 control bit is set. When cleared, the $\overline{INT0}$ pin has no effect, and Timer 0 is enabled whenever TR0 control bit is set.

These alternate functions are described below.

BIT	NAME	FUNCTION
7	P2.7	T1 or I/O pin by alternative.
6	P2.6	IC2 or MOSI or I/O pin by alternative.
5	P2.5	IC1 or MISO or I/O pin by alternative.
4	P2.4	IC0 or $\overline{SS}$ pin or I/O pin by alternative.
3	P2.3	T3 or SCLK or I/O pin by alternative.
2	P2.2	PWM4 or I/O pin by alternative.
1	P2.1	PWM2 or CP1O or I/O pin by alternative.
0	P2.0	PWM0 or CP2O or I/O pin by alternative.

KEYBOARD INTERRUPT **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	KBI.7	KBI.6	KBI.5	KBI.4	KBI.3	KBI.2	KBI.1	KBI.0

Mnemonic: KBI Address: A1h

BIT	NAME	FUNCTION
7	KBI.7	1: Enable P0.7 as a cause of a Keyboard interrupt.
6	KBI.6	1: Enable P0.6 as a cause of a Keyboard interrupt.
5	KBI.5	1: Enable P0.5 as a cause of a Keyboard interrupt.
4	KBI.4	1: Enable P0.4 as a cause of a Keyboard interrupt.
3	KBI.3	1: Enable P0.3 as a cause of a Keyboard interrupt.
2	KBI.2	1: Enable P0.2 as a cause of a Keyboard interrupt.
1	KBI.1	1: Enable P0.1 as a cause of a Keyboard interrupt.
0	KBI.0	1: Enable P0.0 as a cause of a Keyboard interrupt.

AUX FUNCTION REGISTER 1 **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	KBF	BOD	BOI	LPBOD	SRST	ADCEN	RCCLK	BOS

Mnemonic: AUXR1 Address: A2h

BIT	NAME	FUNCTION

PORT 4 **Initial=xxxx 1111b/xxxx 0000b**

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	P4.3	P4.2	P4.1	P4.0

Mnemonic: P4 Address: A5h

P4.3-0: General purpose Input/Output port. Most instructions will read the port pins in case of a port read access, however in case of read-modify-write instructions, the port latch is read. If config0.PRHI=1, the initial value is xxxx_1111b at reset. If config0.PRHI=0, the initial value is xxxx_0000b at reset. These alternate functions are described below.

BIT	NAME	FUNCTION
7-4	-	Reserved.
3	P4.3	Dedicated I/O pin.
2	P4.2	Dedicated I/O pin.
1	P4.1	CP2PB or I/O pin by alternative.
0	P4.0	CP2NB or I/O pin by alternative.

INPUT CAPTURE 2 LOW REGISTER **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	CCL2.7	CCL2.6	CCL2.5	CCL2.4	CCL2.3	CCL2.2	CCL2.1	CCL2.0

Mnemonic: CCL2 Address: A6h

BIT	NAME	FUNCTION
7~0	CCL2.7~0	Capture 2 LSB bits.

INPUT CAPTURE 2 HIGH REGISTER **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	CCH2.7	CCH2.6	CCH2.5	CCH2.4	CCH2.3	CCH2.2	CCH2.1	CCH2.0

Mnemonic: CCH2 Address: A7h

BIT	NAME	FUNCTION
7~0	CCH2.7~0	Capture 2 MSB bits.

INTERRUPT ENABLE **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	EA	EADC	EBO	ES	ET1	EX1	ET0	EX0

Mnemonic: IE Address: A8h

BIT	NAME	FUNCTION

1	DTENB2	Enable dead-time insertion for PWM pair (PWM2, PWM3): Dead-time insertion is only active when this pair of complementary PWM is enabled. If dead-time insertion is inactive, the outputs of pin pair are complementary without any delay. 0: Disable dead-time insertion on the pin pair (PWM2, PWM3). 1: Enable dead-time insertion on the pin pair (PWM2, PWM3).
0	DTENB0	Enable dead-time insertion for PWM pair (PWM0, PWM1): Dead-time insertion is only active when this pair of complementary PWM is enabled. If dead-time insertion is inactive, the outputs of pin pair are complementary without any delay. 0: Disable dead-time insertion on the pin pair (PWM0, PWM1). 1: Enable dead-time insertion on the pin pair (PWM0, PWM1).

Note: This SFR is TA protected.

ADC DELAY START REGISTER **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	ADCDLY.7	ADCDLY.6	ADCDLY.5	ADCDLY.4	ADCDLY.3	ADCDLY.2	ADCDLY.1	ADCDLY.0

Mnemonic: ADCDLY Address: AFh

BIT	NAME	FUNCTION
7~0	ADCDLY	These are 8 bits start register to delay start of ADC conversion after detection of ADC start conversion edge by PWM trigger source (controllable through SFR ADCCON1.PWMSRC.1~0) and trigger type (controllable through SFR ADCCON1.STADCT.1~0). An internal 8 bits delay counter will run on PWM clock. When the internal counter matches ADCDLY value, ADC will start conversion. PMU trigger delay time = (ADCDLY+1)/(Fcpu/(4*Divider)). Divider is defined in SFR ADCCON1.3.

Note: User required to clear ADCEN (ADCEN = 0) when re-configure this SFR.

PORT 3 **Initial=1111 1111b/0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0

Mnemonic: P3 Address: B0h

P3.7-0: General purpose Input/Output port. Most instructions will read the port pins in case of a port read access, however in case of read-modify-write instructions, the port latch is read. If config0.PRHI=1, the initial value is 1111_1111b at reset. If config0.PRHI=0, the initial value is 0000_0000b at reset. These alternate functions are described below.

BIT	NAME	FUNCTION

T		
7-0	I2DAT.[7:0]	The data register of I2C.

I2C STATUS REGISTER **Initial=1111 1000b**

Bit:	7	6	5	4	3	2	1	0
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

Mnemonic: I2STATUS Address: BDh

BIT	NAME	FUNCTION
7-0	I2STATUS.[7:0]	The status register of I2C: The three least significant bits are always 0. The five most significant bits contain the status code. There are 26 possible status codes. When I2STATUS contains F8H, no serial interrupt is requested. All other I2STATUS values correspond to defined I2C states. When each of these states is entered, a status interrupt is requested (SI = 1). A valid status code is present in I2STATUS one machine cycle after SI is set by hardware and is still present one machine cycle after SI has been reset by software. In addition, states 00H stands for a Bus Error. A Bus Error occurs when a START or STOP condition is present at an illegal position in the formation frame. Example of illegal position are during the serial transfer of an address byte, a data byte or an acknowledge bit.

I2C BAUD RATE CONTROL REGISTER **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	I2CLK.7	I2CLK.6	I2CLK.5	I2CLK.4	I2CLK.3	I2CLK.2	I2CLK.1	I2CLK.0

Mnemonic: I2CLK Address: BEh

BIT	NAME	FUNCTION
7-0	I2CLK.[7:0]	The I2C clock rate bits.

I2C TIMER-OUT COUNTER REGISTER **Initial=xxxx x000b**

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	ENTI	DIV4	TIF

Mnemonic: I2TOC Address: BFh

BIT	NAME	FUNCTION
7~3	-	Reserved.
2	ENTI	Enable I2C 14-bits Timer Counter: 0: Disable 14-bits Timer Counter count. 1: Enable 14-bits Timer Counter count. After enable ENTI and ENSI, the 14-bit

RS.1-0: Register Bank Selection Bits:

RS1	RS0	REGISTER BANK	ADDRESS
0	0	0	00-07h
0	1	1	08-0Fh
1	0	2	10-17h
1	1	3	18-1Fh

PWM COUNTER HIGH BITS REGISTER **Initial=xxxx 0000b**

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	PWMP.11	PWMP.10	PWMP.9	PWMP.8

Mnemonic: PWMPH Address: D1h

BIT	NAME	FUNCTION
7-4	-	Reserved.
3-0	PWMP.[11:8]	The PWM Counter Register bits 11~8.

PWM 0 HIGH BITS REGISTER **Initial=xxxx 0000b**

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	PWM0.11	PWM0.10	PWM0.9	PWM0.8

Mnemonic: PWM0H Address: D2h

BIT	NAME	FUNCTION
7~4	-	Reserved.
3~0	PWM0.11~8	The PWM 0 Register bit 11~8.

EXTENDED INTERRUPT ENABLE 2 REGISTER **Initial=x0xx 0x00b**

Bit:	7	6	5	4	3	2	1	0
	-	ET2	-	-	ESPI	-	EADCP	ET3

Mnemonic: EIE2 Address: D4h

BIT	NAME	FUNCTION
7	-	Reserved.
6	ET2	Timer 2 interrupt enable: 0: Disable Timer 2 Interrupt. 1: Enable Timer 2 Interrupt.

1	PADIDS.1	P0.1 digital input disable bit. 0: Default (With digital/analog input). 1: Disable Digital Input of ADC Input Channel 1/Comparator 2 (CP2P) input.
0	PADIDS.0	P0.0 digital input disable bit. 0: Default (With digital/analog input). 1: Disable Digital Input of ADC Input Channel 0.

INTERRUPT HIGH PRIORITY 1 **Initial=0000 x000b**

Bit: 7 6 5 4 3 2 1 0

PCAPH	PPWMH	PBRKH	PWDIH	-	PCIH	PKBH	PI2H

Mnemonic: IP1H Address: F7h

BIT	NAME	FUNCTION
7	PCAPH	1: To set interrupt high priority of Capture 0/1/2 as highest priority level.
6	PPWMH	1: To set interrupt high priority of PWM's counter match/underflow is highest priority level.
5	PBRKH	1: To set interrupt high priority of PWM's brake is highest priority level.
4	PWDIH	1: To set interrupt high priority of Watchdog is highest priority level.
3	-	Reserved.
2	PCIH	1: To set interrupt high priority of Comparator 1 and 2, is highest priority level.
1	PKBH	1: To set interrupt high priority of Keypad is highest priority level.
0	PI2H	1: To set interrupt high priority of I2C is highest priority level.

INTERRUPT PRIORITY 1 **Initial=0000 x000b**

Bit: 7 6 5 4 3 2 1 0

PCAP	PPWM	PBRK	PWDI	-	PCI	PKB	PI2

Mnemonic: IP1 Address: F8h

BIT	NAME	FUNCTION
7	PCAP	1: To set interrupt priority of Capture 0/1/2 as higher priority level.
6	PPWM	1: To set interrupt priority of PWM's counter match/underflow is higher priority level.
5	PBRK	1: To set interrupt priority of PWM's brake is higher priority level.
4	PWDI	1: To set interrupt priority of Watchdog is higher priority level.
3	-	Reserved.
2	PC1	1: To set interrupt priority of Comparator 1 and 2, is higher priority level.

9 POWER MANAGEMENT

N79E875 series are provided with idle mode and power-down mode to control power consumption. These modes are discussed in the next two sections, followed by a discussion of resets.

9.1 Idle Mode

The user can put the device into idle mode by writing 1 to the bit PCON.0. The instruction that sets the idle bit is the last instruction that will be executed before the device goes into Idle Mode. In the Idle mode, the clock to the CPU is halted, but not to the peripheral blocks. This forces the CPU state to be frozen; the Program counter, the Stack Pointer, the Program Status Word, the Accumulator and the other registers hold their contents. The port pins hold the logical states they had at the time Idle was activated. The Idle mode can be terminated in two ways. Since the interrupt controller is still active, the activation of any enabled interrupt can wake up the processor. This will automatically clear the Idle bit, terminate the Idle mode, and the Interrupt Service Routine (ISR) will be executed. After the ISR is completed, the program execution returns to the instruction after one which put the device into Idle mode and continues from there.

The Idle mode can also be exited by activating the reset. The device can put into reset either by applying a low on the external /RST pin, a Power on reset condition or a Watchdog timer reset. The external reset pin has to be held low for at least two machine cycles i.e. 8 clock periods to be recognized as a valid reset. In the reset condition the program counter is reset to 0000h and all the SFRs are set to the reset condition. Since the clock is already running there is no delay and execution starts immediately. In the Idle mode, the Watchdog timer continues to run, and if enabled, a time-out will cause a watchdog timer interrupt which will wake up the device. The software must reset the Watchdog timer in order to preempt the reset which will occur after 512 clock periods of the time-out. When N79E875series are exiting from Idle Mode with a reset, the instruction following the one which put the device into Idle Mode is not executed. So there is no danger of unexpected writes.

9.2 Power Down Mode

The device can be put into Power Down mode by writing 1 to bit PCON.1. The instruction that does this will be the last instruction to be executed before the device goes into Power Down mode. In the Power Down mode, all the clocks are stopped and the device comes to a halt. All activity, except the functions of Brownout reset, KBI, $\overline{\text{INT1}}$, $\overline{\text{INT0}}$, watchdog timer(Config0.WDTCK=0), ADC(RCCLK=1) and Analog Comparator(if enabled), is completely stopped and the power consumption is reduced to the lowest possible value. The port pins hold at the states of the values held by their respective SFRs.

The interrupt sources that can wake up CPU from the power down mode **are external interrupts, keyboard interrupt (KBI), brownout reset (BOR), comparators interrupt(CMF1/CMF2), ADC interrupt(if ADC clock is from internal RC) and watchdog timer interrupt (if WDTCK = 0).** The device will then execute the interrupt service routine for the corresponding external interrupt. After the interrupt service routine is completed, the program execution returns to the instruction after one which put the device into Power Down mode and continues from there.

Besides, the /RST pin trigger by a low pulse of at least two machine cycle terminates the Power Down mode and restarts the clock. The program execution will restart from 0000h.

Note:

1. Either **a low-level or a falling-edge at external interrupt pins /INT0 and INT1** will re-start the oscillator if the global interrupt is enabled(EA=1) and the corresponding interrupt is enabled.
2. **The /INT0 pin is permanently in open-drain type therefore it is recommended with an external pull-up resistor on pin in application**

10 RESET CONDITIONS

The user has several hardware related options for placing N79E875 series into reset condition. In general, most register bits go to their reset value irrespective of the reset condition, but there are a few flags whose state depends on the source of reset. The user can use these flags to determine the cause of reset using software. The sources of resets are external reset, power-on-reset, watchdog timer reset and software reset (brownout is also able to reset the device if enabled).

10.1 External Reset

The device continuously samples the /RST pin at state C4 of every machine cycle. Therefore the /RST pin must be held low for at least 2 machine cycles to ensure detection of a valid /RST low. The reset circuitry then synchronously applies the internal reset signal. Thus the reset is a synchronous operation and requires the clock to be running to cause an external reset.

Once the device is in reset condition, it will remain so as long as /RST is 0. Even after /RST is deactivated, the device will continue to be in reset state for up to two machine cycles, and then begin program execution from 0000h. There is no flag associated with the external reset condition. However since the other two reset sources have flags, the external reset can be considered as the default reset if those two flags are cleared.

10.2 Power-On Reset (POR)

When power up, the device performs a power-on reset and sets the POR flag. The software should clear the POR flag, or it will be difficult to determine the source of future resets. During power-on-reset, all port pins will be tri-stated. After power-on-reset, the port pins state will determined by PRHI value.

10.3 Watchdog Timer Reset

The Watchdog timer is a free running timer with programmable time-out intervals. The user can clear the watchdog timer at any time, causing it to restart the count. When the time-out interval is reached an interrupt flag (WDIF at WDCON.3) will be set by hardware. If the Watchdog reset is enabled (WDRUN at WDCON.7) and the watchdog timer is not cleared before the time-out of 512 clock period since WINTF is set, the watchdog timer will set watchdog reset flag (WTRF at WDCON.2) and generate a reset. This places the device into the reset condition. The reset condition is maintained by hardware for two machine cycles. Once the reset is removed the device will begin execution from 0000h. The watchdog reset flag WTRF keeps high after watchdog reset, it must be cleared by software.

10.4 Software Reset

User can software reset the device by setting SRST bit in SFR AUXR1. The reset condition is maintained by hardware for two machine cycles. Once the reset is removed the device will begin execution from 0000h. **User must specially take care of setting SRST when a write access on AUXR1.**

10.5 Brownout Reset

When the power voltage(V_{DD}) is lower than brownout voltage(V_{BOD}), the brownout detector will set brownout interrupt flag(BOF at PCON.5), if brownout reset function is enabled(BOD=1 and BOI=0 at AUXR1) a hardware brownout reset will be triggered and the device keeps in reset state until the V_{DD} raises above brownout voltage. Note that BOF won't be cleared by brownout reset, it must be cleared by software

10.6 Reset State

12 NVM MEMORY

The N79E875 series have NVM data memory of **128** bytes for customer's data store used. The NVM data memory has **8** pages area and each page has **16** bytes. The page addresses are shown on Figure 12-1.

The NVM memory can be read/write by customer program to access. Read NVM data is by MOVC A,@A+DPTR instruction, and write data is by SFR of NVMADDRL, NVMDAT and NVMCON. Before write data to NVM memory, the page must be erased by providing page address on NVMADDRL, which high and low byte address of On-Chip Code Memory space will decode, then set EER of NVMCON.7. This will automatically hold fetch program code and PC Counter, and execute page erase. After finished, this bit will be cleared by hardware. The erase time is ~ 5ms.

For writing data to NVM memory, user must set address and data to NVMADDRL and NVMDAT, then set EWR of NVMCON.6 to initiate NVM data write. The uC will hold program code and PC Counter, and then write data to mapping address. Upon write completion, the EWR bit will be cleared by hardware, the uC will continue execute next instruction. The program time is ~50us.

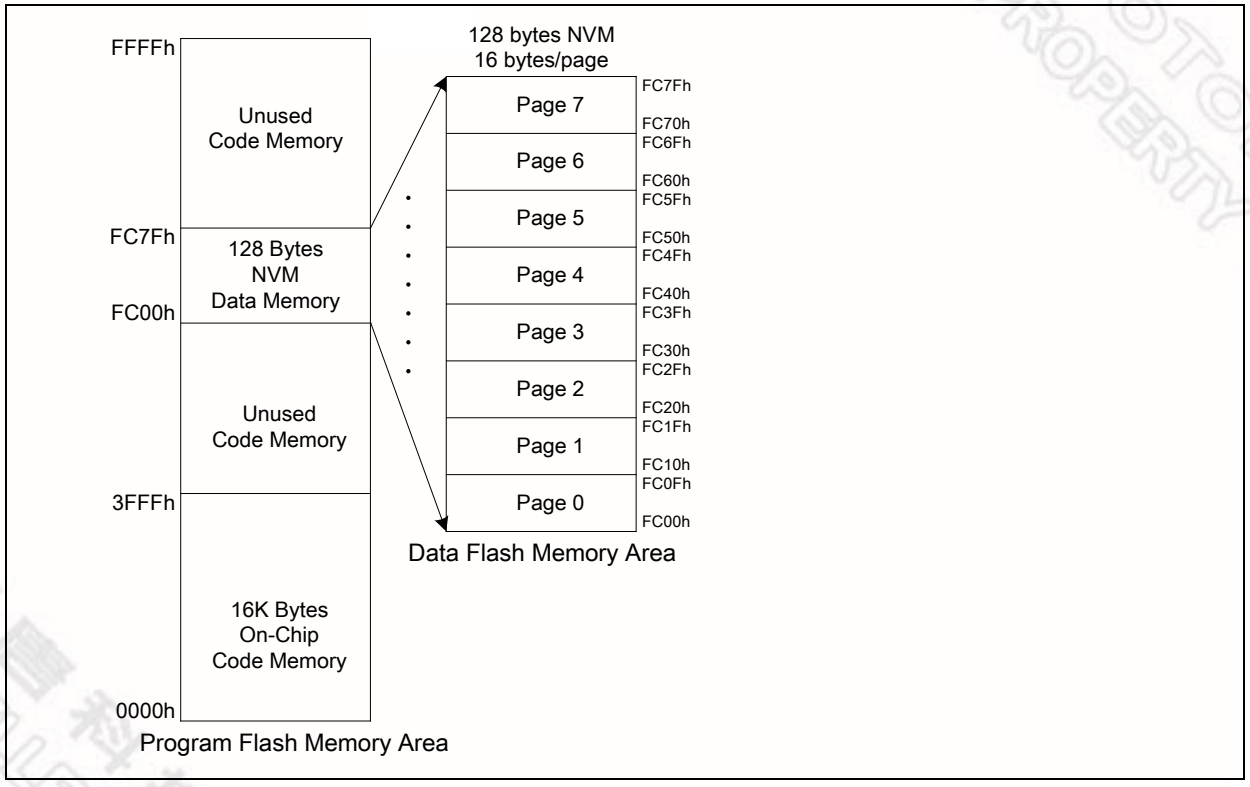

Figure 12-1 N79E875 On-chip Flash Memory Space

The default Watchdog time-out is 2^{12} clocks, which is the shortest time-out period. The WDRUN, WD0, WD1, EWRST, WDIF and WDCLR bits are protected by the Timed Access procedure. This prevents software from accidentally enabling or disabling the watchdog timer. More importantly, it makes it highly improbable that errant code can enable or disable the Watchdog Timer.

The security bit WDTCK is located at bit 7 of CONFIG0 register. This bit is for user to configure the clock source of watchdog timer either from the internal RC or from the uC clock.

best of three bases. The bit detector samples the RxD pin, at the 8th, 9th and 10th counter states. By using a majority 2 of 3 voting system, the bit value is selected. This is done to improve the noise rejection feature of the serial port. If the first bit detected after the falling edge of RxD pin is not 0, then this indicates an invalid start bit, and the reception is immediately aborted. The serial port again looks for a falling edge in the RxD line. If a valid start bit is detected, then the rest of the bits are also detected and shifted into the SBUF.

After shifting in 8 data bits, there is one more shift to do, after which the SBUF and RB8 are loaded and RI is set. However certain conditions must be met before the loading and setting of RI can be done.

1. RI must be 0 and
2. Either SM2 = 0, or the received stop bit = 1.

If these conditions are met, then the stop bit goes to RB8, the 8 data bits go into SBUF and RI is set. Otherwise the received frame may be lost. After the middle of the stop bit, the receiver goes back to looking for a 1-to-0 transition on the RxD pin.

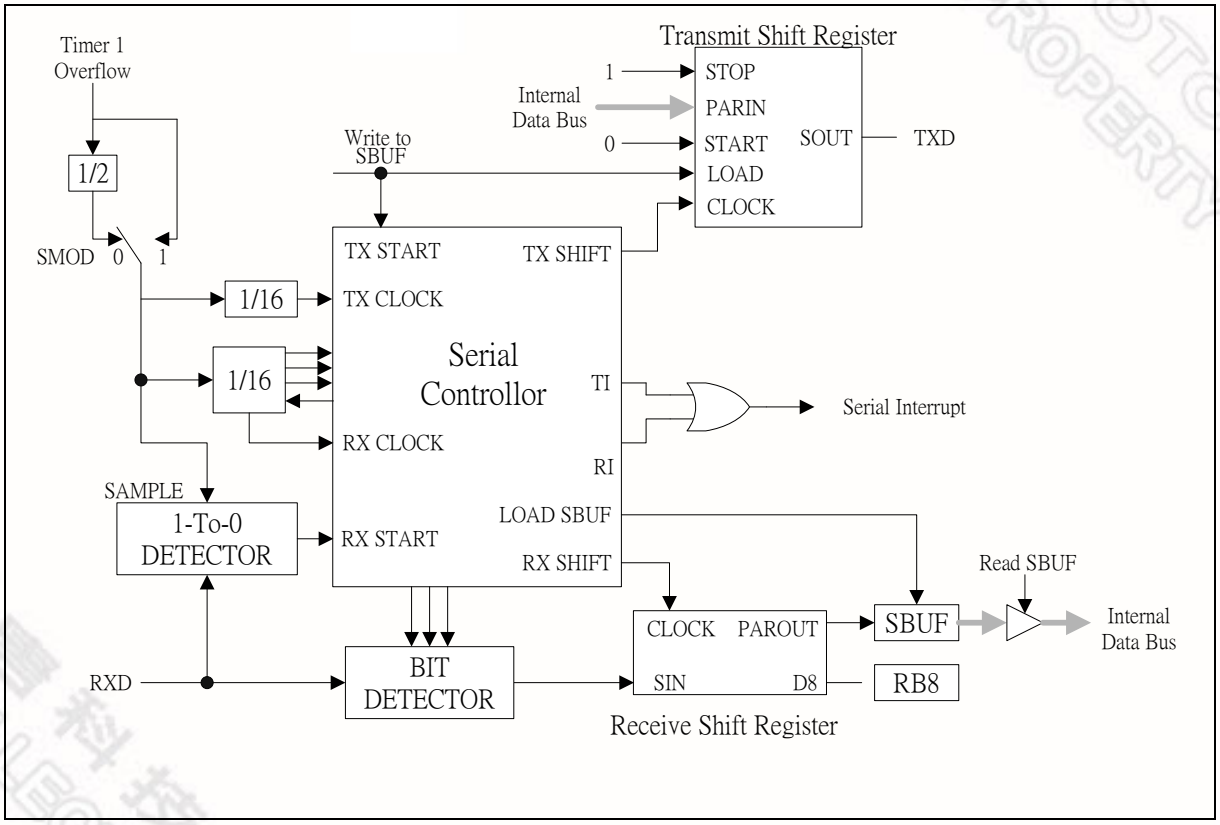

Figure 17-2: Serial Port Mode 1

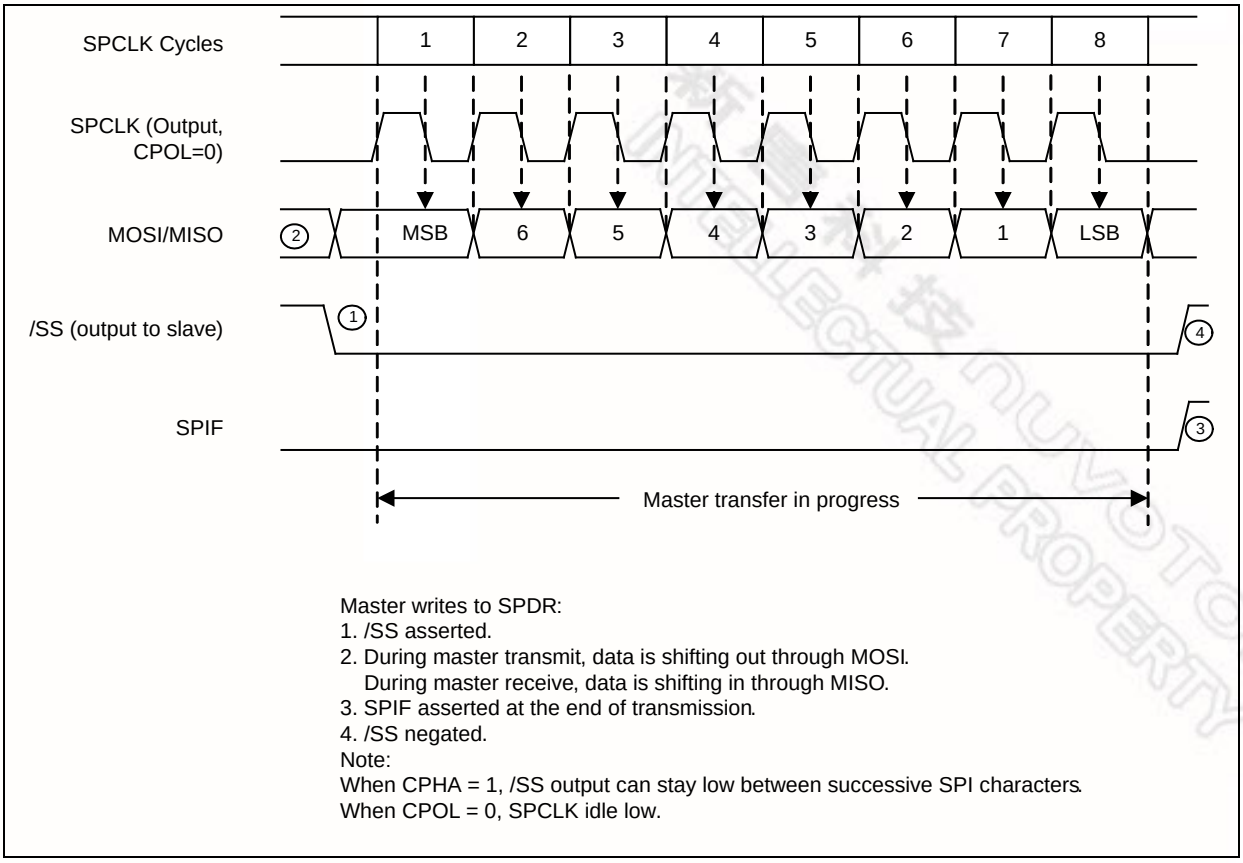

Figure 19-4 Master Mode Transmission (CPOL = 0, CPHA = 1)

PORTS SFR bits can enable Schmitt trigger inputs on each I/O port. The AUXR2 register has bits to enable toggle outputs from Timer 0 and Timer 1, and enable a clock output if either the internal RC oscillator or external clock input is being used. The last two functions are described in the Timer/Counters and Oscillator sections respectively. Each I/O port of this device may be selected to use TTL level inputs or Schmitt inputs with hysteresis. A single configuration bit determines this selection for the entire port. Port pin P1.4 always has a Schmitt trigger input.

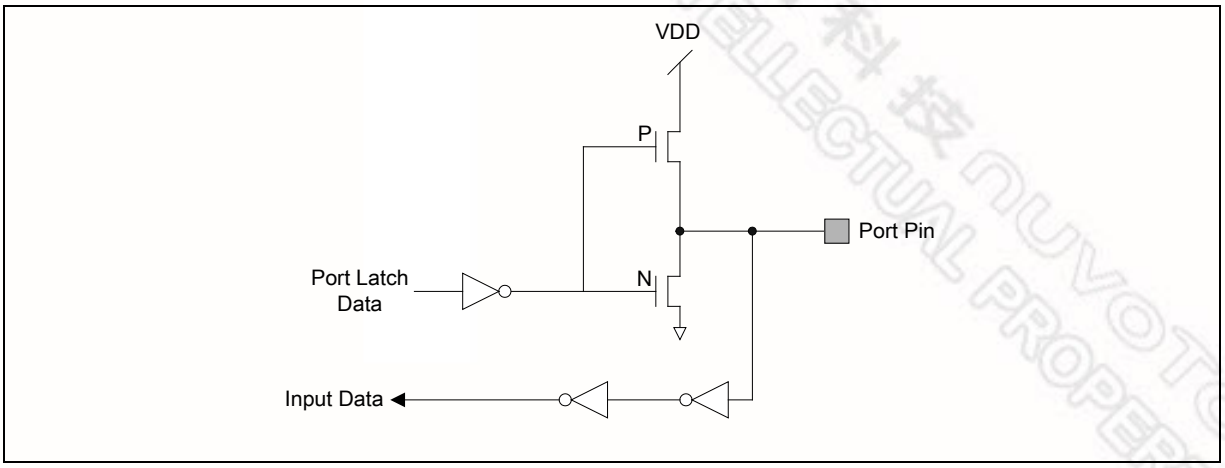

Figure 22-3: Push-Pull Output

22.4 Input Only Configuration

By configure this mode, the ports are only digital input and disable digital output. The N79E875 series can select input pin to Schmitt trigger or TTL level input by PxM1.y and PxM2.y registers.

22.5 SFR of I/O Port Configuration

SYMBOL	DEFINITION	ADDRESS	MSB			BIT ADDRESS, SYMBOL				LSB	RESET
P4M2	PORT 4 OUTPUT MODE 2	FBH	-	-	-	-	P4M2.3	P4M2.2	P4M2.1	P4M2.0	XXXX 0000b
P4M1	PORT 4 OUTPUT MODE 1	FAH	-	-	-	-	P4M1.3	P4M1.2	P4M1.1	P4M1.0	XXXX 0000b
PORTS	PORT SHMITT REGISTER	ECH	-	-	-	P4S	P3S	P2S	P1S	P0S	XXX0 0000B
P2M2	PORT 2 OUTPUT MODE 2	B6H	P2M2.7	P2M2.6	P2M2.5	P2M2.4	P2M2.3	P2M2.2	P2M2.1	P2M2.0	0000 0000b
P2M1	PORT 2 OUTPUT MODE 1	B5H	P2M1.7	P2M1.6	P2M1.5	P2M1.4	P2M1.3	P2M1.2	P2M1.1	P2M1.0	0000 0000b
P1M2	PORT 1 OUTPUT MODE 2	B4H	P1M2.7	-	-	-	P1M2.3	P1M2.2	P1M2.1	P1M2.0	000X 0000b
P1M1	PORT 1 OUTPUT MODE 1	B3H	P1M1.7	-	-	-	P1M1.3	P1M1.2	P1M1.1	P1M1.0	000X 0000b
P0M2	PORT 0 OUTPUT MODE 2	B2H	P0M2.7	P0M2.6	P0M2.5	P0M2.4	P0M2.3	P0M2.2	P0M2.1	P0M2.0	0000 0000b
P0M1	PORT 0 OUTPUT MODE 1	B1H	P0M1.7	P0M1.6	P0M1.5	P0M1.4	P0M1.3	P0M1.2	P0M1.1	P0M1.0	0000 0000b
P3M1	PORT 3 OUTPUT MODE 1	9EH	P3M1.7	P3M1.6	P3M1.5	P3M1.4	P3M1.3	P3M1.2	P3M1.1	P3M1.0	0000 0000b

23 OSCILLATOR

N79E875 series provide three oscillator input options. These are configured at CONFIG register (CONFIG0) that include On-Chip RC Oscillator Option, External Clock Input Option and Crystal Oscillator Input Option. The Crystal Oscillator Input frequency may be supported from 4MHz to 40MHz, and optionally with capacitor or resister.

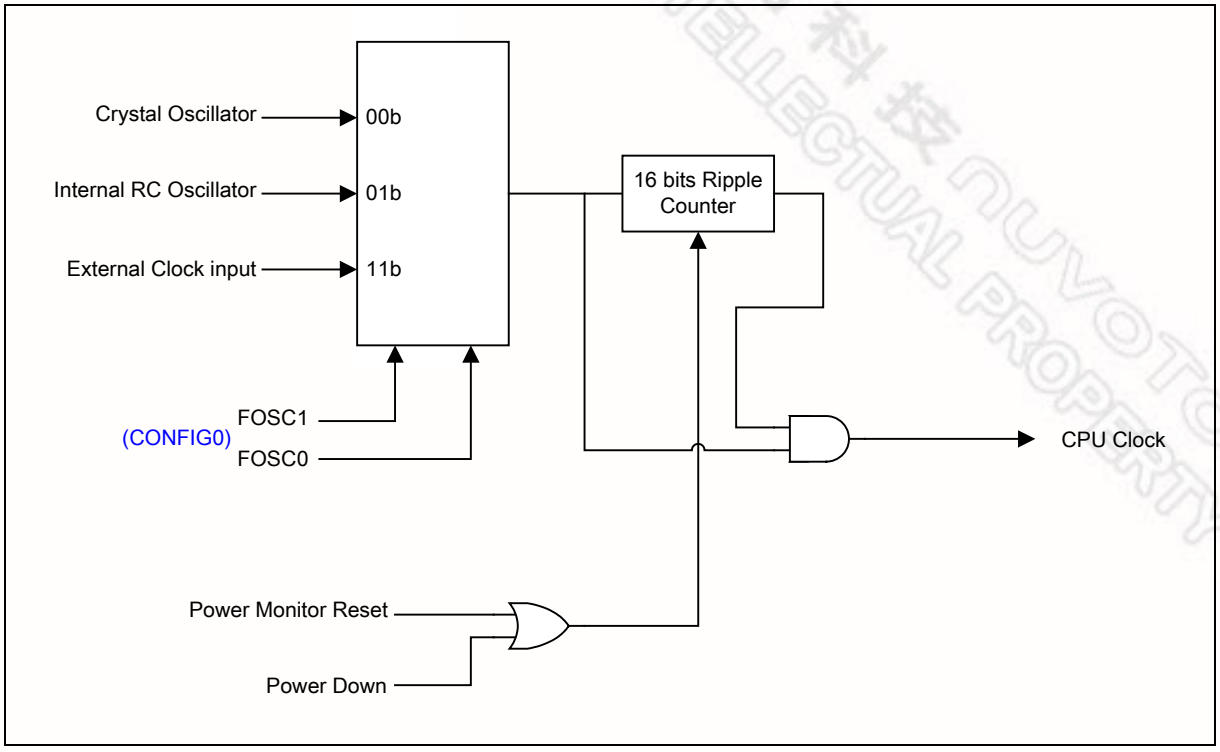

Figure 23-1: Oscillator

23.1 On-Chip RC Oscillator Option

The On-Chip RC Oscillator is programmable to 22.1184MHz/11.0592MHz +/- 2% (selectable by FS1 config bit) frequency to support clock source. When FOSC1, FOSC0 = 01b, the On-Chip RC Oscillator is enabled. A clock output on P1.0 (XTAL2) may be enabled when On-Chip RC oscillator is used.

23.2 External Clock Input Option

The clock source pin (XTAL1) is from External Clock Input by FOSC1, FOSC0 = 11b, and frequency range is form 0Hz up to 40MHz. A clock output on P1.0 (XTAL2) may be enabled when External Clock Input is used.

N79E875 series support a clock output function when either the on-chip RC oscillator or the external clock input options is selected. This allows external devices to synchronize to the device. When enabled, via the ENCLK bit in the AUXR2 register, the clock output appears on the XTAL2/CLKOUT pin whenever the on-chip oscillator is running, including in Idle Mode. The frequency of the clock output is 1/4 of the CPU clock rate. If the clock output is not needed in Idle Mode, it may be turned off prior to entering Idle mode, saving additional power. The clock output may also be enabled when the external clock input option is selected.

24 POWER MONITORING FUNCTION

Power-On Detect and Brownout are two additional power monitoring functions implemented in N79E875 series to prevent incorrect operation during power up and power drop or loss.

24.1 Power On Detect

The Power–On Detect function is a design to detect power up after power voltage reaches to a level where Brownout Detect can work. After power on detect, the POR (PCON.4) will be set to “1” to indicate an initial power up condition. The POR flag will be cleared by software.

24.2 Brownout Detect

The N79E875 has an on-chip Brown-out Detection (BOD) circuit for monitoring the V_{DD} level during operation by comparing it to a fixed trigger level. There are 3 trigger levels of BOD selected by 2 config0 bits BOV[1:0] suited for wide voltage use. The following table shows the brownout voltage levels supported;

BOV bits (CONFIG0.4-3)	Brownout voltage detect level
00	4.5V
01	3.8V
1x	2.6V (default)

Table 24-1: Brownout Voltage Detect Levels

When the Brownout voltage is drop to the select level, the brownout detector will detect and keeps this active until V_{DD} is returns to above brownout Detect voltage. The Brownout Detect block is as follow.

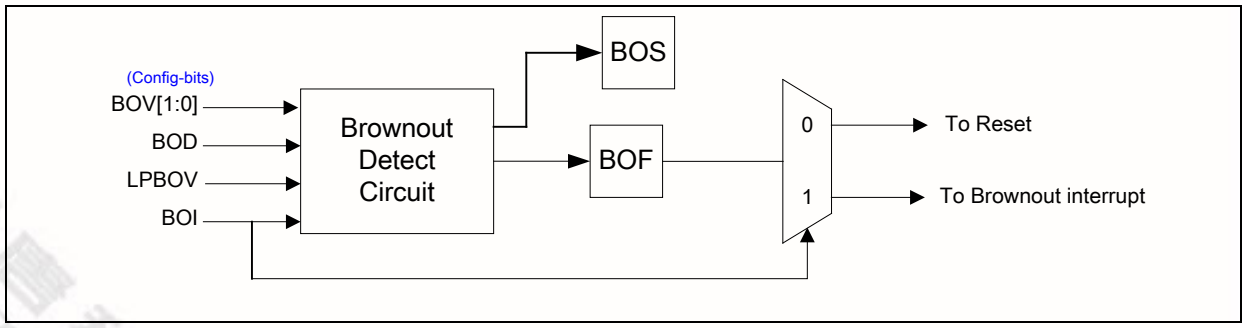

Figure 24-1: Brownout Detect Block

When Brownout Detect is enabled by BOD (AUXR1.6), the BOF (PCON.5) flag will be set that it causes brownout reset or interrupt, and BOF will be cleared by software. If BOI (AUXR1.5) is set to “1”, the brownout detect will cause interrupt via the EA (IE.7) and EBO (IE.5) bits is set.

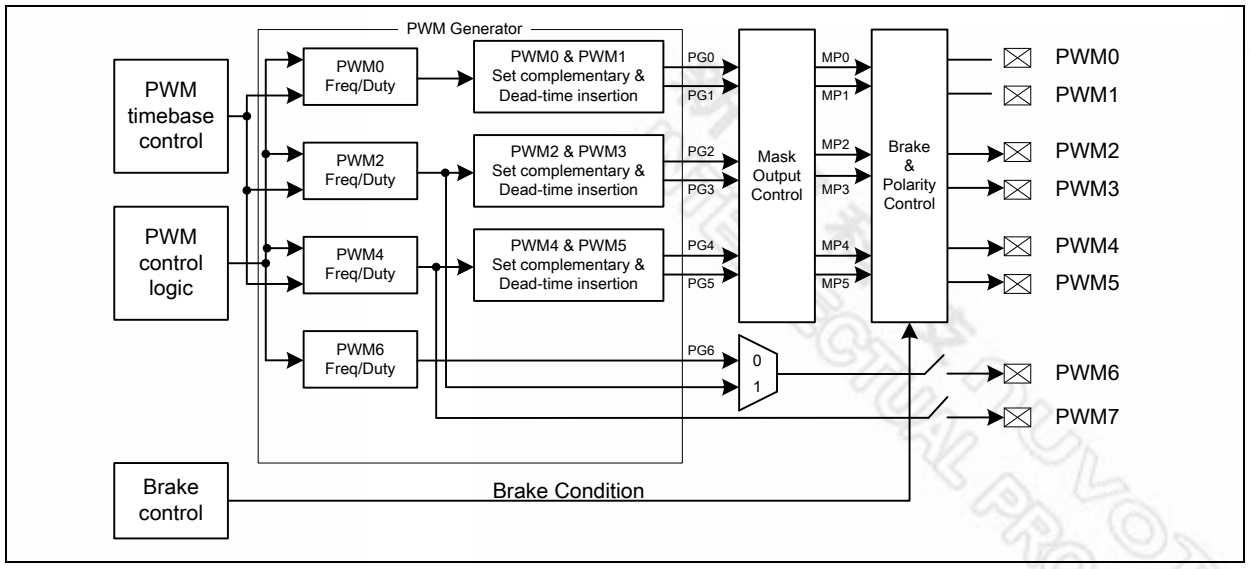

Figure 25-1: PWM Block Diagram

Note:

1. These values are for design guidance only and are not tested.

31.6.4 Typical Crystal Application Circuits

CRYSTAL	C1	C2	R
>24MHz	5p~15p	5p~15p	1.8k~2.2k
4MHz ~ 24 MHz	without	without	without

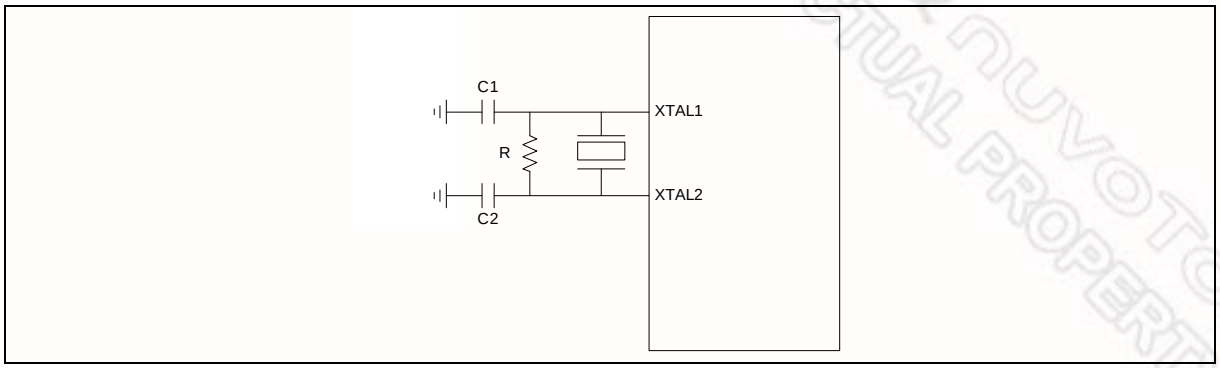

Figure 31-1 Typical Crystal Application Circuit