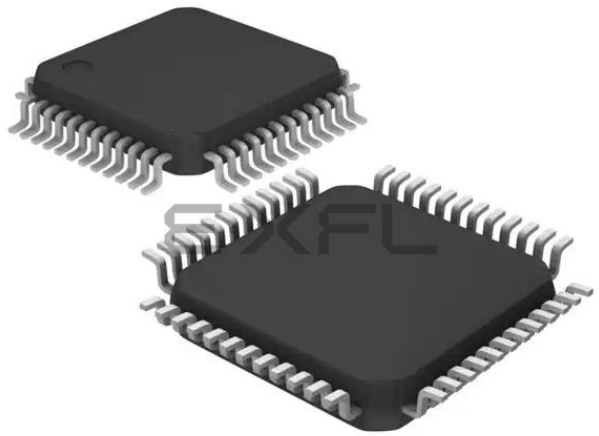
Nuvoton Technology Corporation - N79E875RALG Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/n79e875ralg

2 FEATURES

- Fully static design 8-bit Turbo 51 CMOS microcontroller;
  - V_{DD} = 4.5V to 5.5V @40MHz
  - V_{DD} = 3.0V to 5.5V @24MHz
  - V_{DD} = 2.4V to 5.5V @8MHz
- Operating temperature range
  - N79**E**875A/N79**E**875RA series: -40°C ~85°C
- Flexible CPU clock source configurable by config-bit and software:
  - High speed external oscillator: Up to 40MHz Crystal and resonator (enabled by config-bit).
  - Internal oscillator: Nominal 22MHz/11MHz (selected by config-bit)
    N79E875**A** series: 22MHz/11MHz with ±25% accuracy
    N79E875**RA** series: 22.1184MHz/11.0592MHz with ±2% accuracy, at 3.3V/25°C
- On-chip Memory
  - 16K bytes of Application Program Flash memory, with ICP and External Writer programmable mode.
  - 128 bytes (8 pages x 16 bytes) Data Flash for customer data storage used and 10K writer cycles; Data Flash program/erase V_{DD}=3.0V to 5.5V
  - 256 bytes of on-chip scratch-pad RAM.
  - 256 bytes of auxiliary RAM, software-selectable, accessed by MOVX instruction.
- Maximum 36 I/O pins.
  - Four outputs mode and TTL/Schmitt trigger selectable Port.
- 17 interrupts source with four levels of priority.
- Four timer/counters.
  - Two 16-bit timer/counters
  - One 16-bit timer supports 3 capture inputs capability for hall sensor feedback.
  - One 12-bit timer supports 12-bit auto reload timer, capture and compare mode.
- Three serial ports
  - One enhanced full duplex UART port with framing error detection and automatic address recognition.
  - One SPI with master/slave capability.
  - One I2C with master/slave capability.
- Four independent 12-bit PWM duty control units with maximum 8 port pins:
  - Six PWM output channels with mask control for BLDC application.
  - Three pairs complementary PWM with programmable dead-time insertion
  - Independent polarity setting for each channel
  - Two brake/fault input pins

7-0	DPL.[7:0]	This is the low byte of the standard 8052 16-bit data pointer.

DATA POINTER HIGH **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	DPH.7	DPH.6	DPH.5	DPH.4	DPH.3	DPH.2	DPH.1	DPH.0

Mnemonic: DPH Address: 83h

BIT	NAME	FUNCTION
7-0	DPH.[7:0]	This is the high byte of the standard 8052 16-bit data pointer. This is the high byte of the DPTR 16-bit data pointer.

DIVIDER **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	CCDIV.1	CCDIV.0	PWMDIV.1	PWMDIV.0	T3DIV.1	T3DIV.0	T0DIV.1	T0DIV.0

Mnemonic: DIV Address: 86h

BIT	NAME	FUNCTION
7~6	CCDIV.1~0	Timer 2 clock select: CCDIV.1 / CCDIV.0 0 / 0 : Timer 2 clock = Fcpu 0 / 1 : Timer 2 clock = Fcpu/4 1 / 0 : Timer 2 clock = Fcpu/16 1 / 1 : Timer 2 clock = Fcpu/32
5~4	PWMDIV.1~0	PWM clock select: PWMDIV.1 / PWMDIV.0 0 / 0 : PWM clock = Fcpu 0 / 1 : PWM clock = Fcpu/2 1 / 0 : PWM clock = Fcpu/4 1 / 1 : PWM clock = Fcpu/16
3~2	T3DIV.1~0	Timer 3 clock select: T3DIV.1 / T3DIV.0 0 / 0 : Timer 3 clock = Fcpu/4 0 / 1 : Timer 3 clock = Fcpu/16 1 / 0 : Timer 3 clock = Fcpu/32

RS.1-0: Register Bank Selection Bits:

RS1	RS0	REGISTER BANK	ADDRESS
0	0	0	00-07h
0	1	1	08-0Fh
1	0	2	10-17h
1	1	3	18-1Fh

PWM COUNTER HIGH BITS REGISTER **Initial=xxxx 0000b**

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	PWMP.11	PWMP.10	PWMP.9	PWMP.8

Mnemonic: PWMPH Address: D1h

BIT	NAME	FUNCTION
7-4	-	Reserved.
3-0	PWMP.[11:8]	The PWM Counter Register bits 11~8.

PWM 0 HIGH BITS REGISTER **Initial=xxxx 0000b**

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	PWM0.11	PWM0.10	PWM0.9	PWM0.8

Mnemonic: PWM0H Address: D2h

BIT	NAME	FUNCTION
7~4	-	Reserved.
3~0	PWM0.11~8	The PWM 0 Register bit 11~8.

EXTENDED INTERRUPT ENABLE 2 REGISTER **Initial=x0xx 0x00b**

Bit:	7	6	5	4	3	2	1	0
	-	ET2	-	-	ESPI	-	EADCP	ET3

Mnemonic: EIE2 Address: D4h

BIT	NAME	FUNCTION
7	-	Reserved.
6	ET2	Timer 2 interrupt enable: 0: Disable Timer 2 Interrupt. 1: Enable Timer 2 Interrupt.

5	GRP	Group bit 1: Unify the signals timing of PWM0, PWM2 and PWM4 in the same phase which is controlled by PWM0. 0: The signals timing of PWM0, PWM2 and PWM4 are independent.
4	PWMTYPE	PWM mode select bit: 0: Edge-aligned mode. 1: Centre-aligned mode.
3~2		Reserved
1	P6CTRL	PG6 output selection bit: 0: PWM6 output comes from PWM6 frequency/duty generator (if PIO.6 = 1). 1: PWM6 output comes from PWM2 frequency/duty generator (if PIO.6 = 1).
0	INT_TYPE	PWM interrupt type select bit: 0: PWMF will be set if PWM counter underflow. 1: PWMF will be set if PWM counter overflow. Note: This bit is effective when PWM in central align mode only.

WATCHDOG CONTROL **Initial= Refer to the table below**

Bit:	7	6	5	4	3	2	1	0
	WDRUN	-	WD1	WD0	WDIF	WTRF	EWRST	WDCLR

Mnemonic: WDCON Address: D8h

BIT	NAME	FUNCTION
7	WDRUN	0: The Watchdog is stopped. 1: The Watchdog is running.
6	-	Reserved.
5~4	WD1~WD0	Watchdog Timer Time-out values selected.
3	WDIF	Watchdog Timer Interrupt flag: 0: If the interrupt is not enabled, then this bit indicates that the time-out period has elapsed. This bit must be cleared by software. 1: If the watchdog interrupt is enabled, hardware will set this bit to indicate that the watchdog interrupt has occurred.

WD1	WD0	WATCHDOG INTERVAL
0	0	2^{12}
0	1	2^{16}
1	0	2^{18}
1	1	2^{20}

Mnemonic: PORTS Address: ECh

BIT	NAME	FUNCTION
7~5	-	Reserved.
4	P4S	1: Enables Schmitt trigger inputs on Port 4.
3	P3S	1: Enables Schmitt trigger inputs on Port 3.
2	P2S	1: Enables Schmitt trigger inputs on Port 2.
1	P1S	1: Enables Schmitt trigger inputs on Port 1.
0	P0S	1: Enables Schmitt trigger inputs on Port 0.

PWM MASK ENABLE REGISTER **Initial=xx00 0000b**

Bit:	7	6	5	4	3	2	1	0
	-	-	PME.5	PME.4	PME.3	PME.2	PME.1	PME.0

Mnemonic: PME Address: EDh

BIT	NAME	FUNCTION
7~6	-	Reserved.
5~0	PME.n	PWM Mask Enable bit: The PWM generator signal will be masked when this bit is enabled. The corresponding PWMn channel will be output with PMD.n data. 0: PWM generator signal is output to next stage. 1: PWM generator signal is masked and PMD.n is output to next stage. (Note: n = 0~5).

PWM MASK DATA REGISTER **Initial=xx00 0000b**

Bit:	7	6	5	4	3	2	1	0
	-	-	PMD.5	PMD.4	PMD.3	PMD.2	PMD.1	PMD.0

Mnemonic: PMD Address: EEh

BIT	NAME	FUNCTION
7~6	-	Reserved.
5~0	PMD.n	PWM Mask Data bit: This data bit control the state of PWMn output pin, if corresponding PME.n = 1. 0: Output logic low to PWMn. 1: Output logic high to PWMn. (Note: n = 0~5).

INTERRUPT HIGH PRIORITY 2 **Initial=x0xx 0xx0b**

Bit:	7	6	5	4	3	2	1	0

Op-code	HEX Code	Bytes	N79E875 series Machine Cycle	N79E875 series Clock cycles	8032 Clock cycles	N79E875 series vs. 8032 Speed Ratio
INC R7	0F	1	1	4	12	3
INC @R0	06	1	1	4	12	3
INC @R1	07	1	1	4	12	3
INC direct	05	2	2	8	12	1.5
INC DPTR	A3	1	2	8	24	3
DEC A	14	1	1	4	12	3
DEC R0	18	1	1	4	12	3
DEC R1	19	1	1	4	12	3
DEC R2	1A	1	1	4	12	3
DEC R3	1B	1	1	4	12	3
DEC R4	1C	1	1	4	12	3
DEC R5	1D	1	1	4	12	3
DEC R6	1E	1	1	4	12	3
DEC R7	1F	1	1	4	12	3
DEC @R0	16	1	1	4	12	3
DEC @R1	17	1	1	4	12	3
DEC direct	15	2	2	8	12	1.5
MUL AB	A4	1	5	20	48	2.4
DIV AB	84	1	5	20	48	2.4
DA A	D4	1	1	4	12	3
ANL A, R0	58	1	1	4	12	3
ANL A, R1	59	1	1	4	12	3
ANL A, R2	5A	1	1	4	12	3
ANL A, R3	5B	1	1	4	12	3
ANL A, R4	5C	1	1	4	12	3
ANL A, R5	5D	1	1	4	12	3
ANL A, R6	5E	1	1	4	12	3

Most of the SFRs and registers on the device will go to the same condition in the reset state. The Program Counter is forced to 0000h and is held there as long as the reset condition is applied. However, the reset state does not affect the on-chip RAM. The data in the RAM will be preserved during the reset. However, the stack pointer is reset to 07h, and therefore the stack contents will be lost. The RAM contents will be lost if the V_{DD} falls below approximately 2V, as this is the minimum voltage level required for the RAM data retention. Therefore after a first time power on reset the RAM contents will be indeterminate. During a power fail condition, if the power falls below 2V, the RAM contents are lost.

The WDCON SFR bits are set/cleared in reset condition depending on the source of the reset. The WDCON SFR is set to a 0x00 0000B on the reset. WTRF (WDCON.2) is set to a 1 on a Watchdog timer reset, but to a 0 on power on/down resets. WTRF (WDCON.2) is not altered by external reset. EWRST (WDCON.1) is cleared by any reset. Software or any reset will clear WDIF (WDCON.3) bit.

Some of the bits in the WDCON SFR (WDRUN, WDCLR, EWRST, WDIF, WD0 and WD1) have unrestricted read access which required Timed Access procedure to write. The remaining bits have unrestricted write accesses. Please refer TA register description.

The WDCON SFR bits are set or cleared in reset condition depending on the source of the reset.

WDCON	Watch-Dog control	D8H	(DF) WDRUN	(DE) -	(DD) WD1	(DC) WD0	(DB) WDIF	(DA) WTRF	(D9) EWRST	(D8) WDCLR	External reset: 0x00 0x00b Watchdog reset: 0x00 0100b Power on reset 0x00 0000b

Interrupt 1			(IE.2)	Software	IP0.2		
KBI	KBF	003BH	EKB (EIE1.1)	Software	IP1H.1, IP1.1	9	Yes
Comparator 1 & 2	CMF1+ CMF2	0063H	ECI (EIE1.2)	Software	IP1H.2, IP1.2	10	Yes
Timer 1 Overflow	TF1	001BH	ET1 (IE.3)	Hardware, Software	IP0H.3, IP0.3	11	No
Serial Port	RI + TI	0023H	ES (IE.4)	Software	IP0H.4, IP0.4	12	No
Timer 2 Overflow/ Match	TF2	007BH	ET2 (EIE2.6)	Software	IP2H.6, IP2.6	13	No
PWM brake	FBK0, FBK1	0083H	EBRK (EIE1.5)	Software	IP1H.2, IP1.2	14	No
Capture	CPTF0-2	006BH	ECPTF (EIE1.7)	Software	IP1H.7, IP1.7	15	No
Timer 3 Overflow/ Match/ Capture	TF3	008BH	ET3 (EIE2.0)	Software	IP2H.0, IP2.0	16	No
PWM match/ underflow	PWMF	0073H	EPWM (EIE1.6)	Software	IP1H.5, IP1.5	17 (lowest)	No

Table 11-2 Summary of interrupt sources

Note:

The Watchdog Timer can wake up Power Down Mode when its clock source is used internal RC.

ADC Converter interrupt source, ADCI, can wake up Power Down Mode when its clock source is used internal RC. However, ADC compare interrupt source, ADCPI, is not able to wake up from Power Down Mode.

11.3 Interrupt Response Time

The response time for each interrupt source depends on several factors, such as the nature of the interrupt and the instruction underway. In the case of external interrupts $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$, they are sampled at C3 of every machine cycle and then their corresponding interrupt flags IEx will be set or reset. The Timer 0 and 1 overflow flags are set at C3 of the machine cycle in which overflow has occurred. These flag values are polled only in the next machine cycle. If a request is active and all three conditions are met, then the hardware generated LCALL is executed. This LCALL itself takes four machine cycles to be completed. Thus there is a minimum time of five machine cycles between the interrupt flag being set and the interrupt service routine being executed.

Capture blocks can be triggered by the following pins/bit;

- IC0 (P2.4) or ADC compare result bit, ADCPO.
- IC1 (P2.5)
- IC2 (P2.6)

If ICENx is enabled, each time the external pin trigger, the content of the free running 16 bits counter, TL2 & TH2 (from Timer 2 block) will be captured/transferred into the capture registers, CCLx and CCHx, depending which external pin trigger. This action also causes the CPTFx flag bit in CAPCON1 to be set, which will also generate an interrupt (if enabled by ECPTF bit in SFR EIE1.7). The CPTF0-2 flags are logical “OR” to the interrupt module. Flag is set by hardware and clear by software. Software will have to resolve on the priority of the interrupt flags.

Setting the T2CR bit (T2MOD.3), will allow hardware to reset timer 2 automatically after the value of TL2 and TH2 have been captured. Priority is given to T2CR to reset counter after capture the timer value into the capture register.

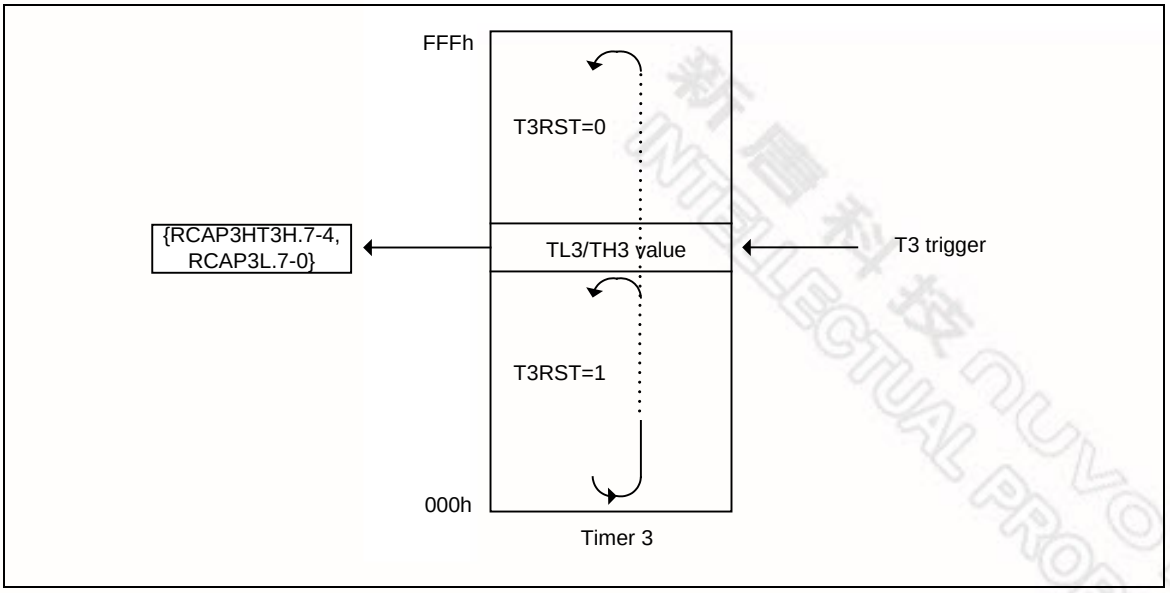


Figure 16-2: Timer 3 – capture function

16.3 Compare Mode

In this mode, RCAP3L and RCAP3HT3H.7-4 serve as compare registers. As timer 3 counting up, upon matching the compare registers, EXF3 flag will also be set. Similarly, an interrupt will be generated if enabled by ET3 bit (EIE2.0). If T3RST = 0, the timer 3 will continue count up, until overflow follow by count up again from zero. Setting T3RST bit, will allow hardware to reset timer 3 automatically after there is compare matched.

When enable T3OE, T3 pin is toggled whenever compare matched occurs (or timer 3 overflows).

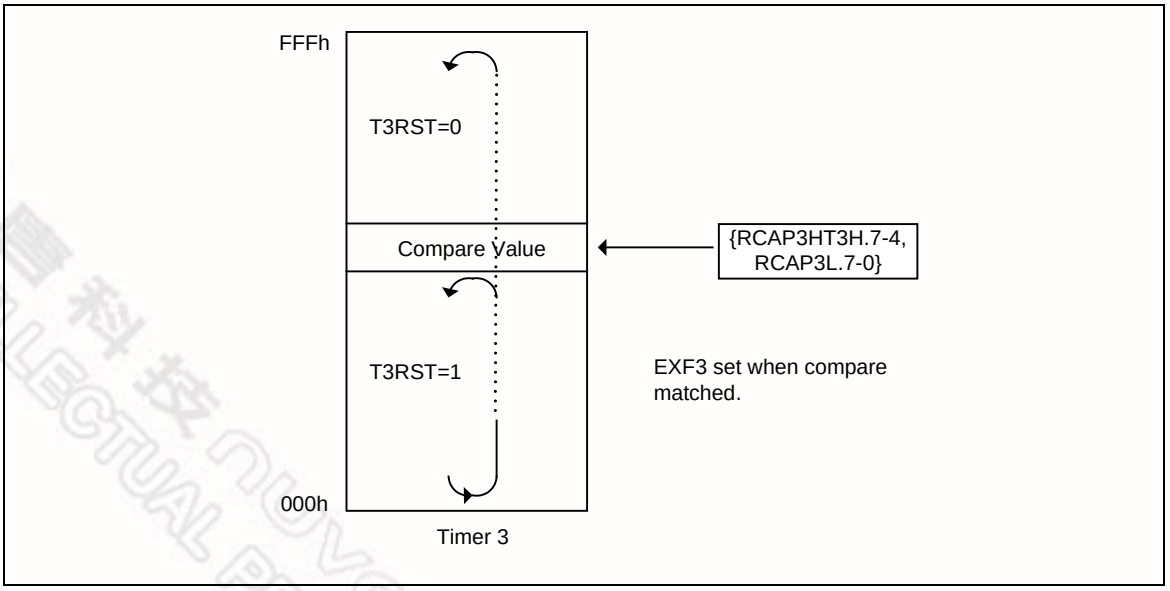


Figure 16-3: Timer 3 – compare function

16.4 Auto-reload Mode

In this mode, RCAP3L and RCAP3HT3H.7-4 serve as reload registers. When timer 3 overflows, a reload is generated that causes the content of RCAP3L and RCAP3HT3H.7-4 reloaded to T3L and RCAP3HT3H.3-0. TF3 flag is set, and interrupt request is generated if ET3 bit is enabled.

slave mode immediately and can detect its own slave address in the same serial transfer.

18.3.1 Master Transmitter Mode

Serial data output through SDA while SCL outputs the serial clock. The first byte transmitted contains the slave address of the receiving device (7 bits) and the data direction bit. In this case the data direction bit (R/W) will be logic 0, and it is represented by “W” in the flow diagrams. Thus the first byte transmitted is SLA+W. Serial data is transmitted 8 bits at a time. After each byte is transmitted, an acknowledge bit is received. START and STOP conditions are output to indicate the beginning and the end of a serial transfer.

18.3.2 Master Receiver Mode

In this case the data direction bit (R/W) will be logic 1, and it is represented by “R” in the flow diagrams. Thus the first byte transmitted is SLA+R. Serial data is received via SDA while SCL outputs the serial clock. Serial data is received 8 bits at a time. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are output to indicate the beginning and end of a serial transfer.

18.3.3 Slave Receiver Mode

Serial data and the serial clock are received through SDA and SCL. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit.

18.3.4 Slave Transmitter Mode

The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit will indicate that the transfer direction is reversed. Serial data is transmitted via SDA while the serial clock is input through SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer.

18.4 Data Transfer Flow in Five Operating Modes

The five operating modes are: Master/Transmitter, Master/Receiver, Slave/Transmitter, Slave/Receiver and GC Call. Bits STA, STO and AA in I2CON register will determine the next state of the SIO hardware after SI flag is cleared. Upon complexion of the new action, a new status code will be updated and the SI flag will be set. If the I2C interrupt control bits (EA and EI2C) are enable, appropriate action or software branch of the new status code can be performed in the Interrupt service routine.

Data transfers in each mode are shown in the following figures.

*** Legend for the following five figures:

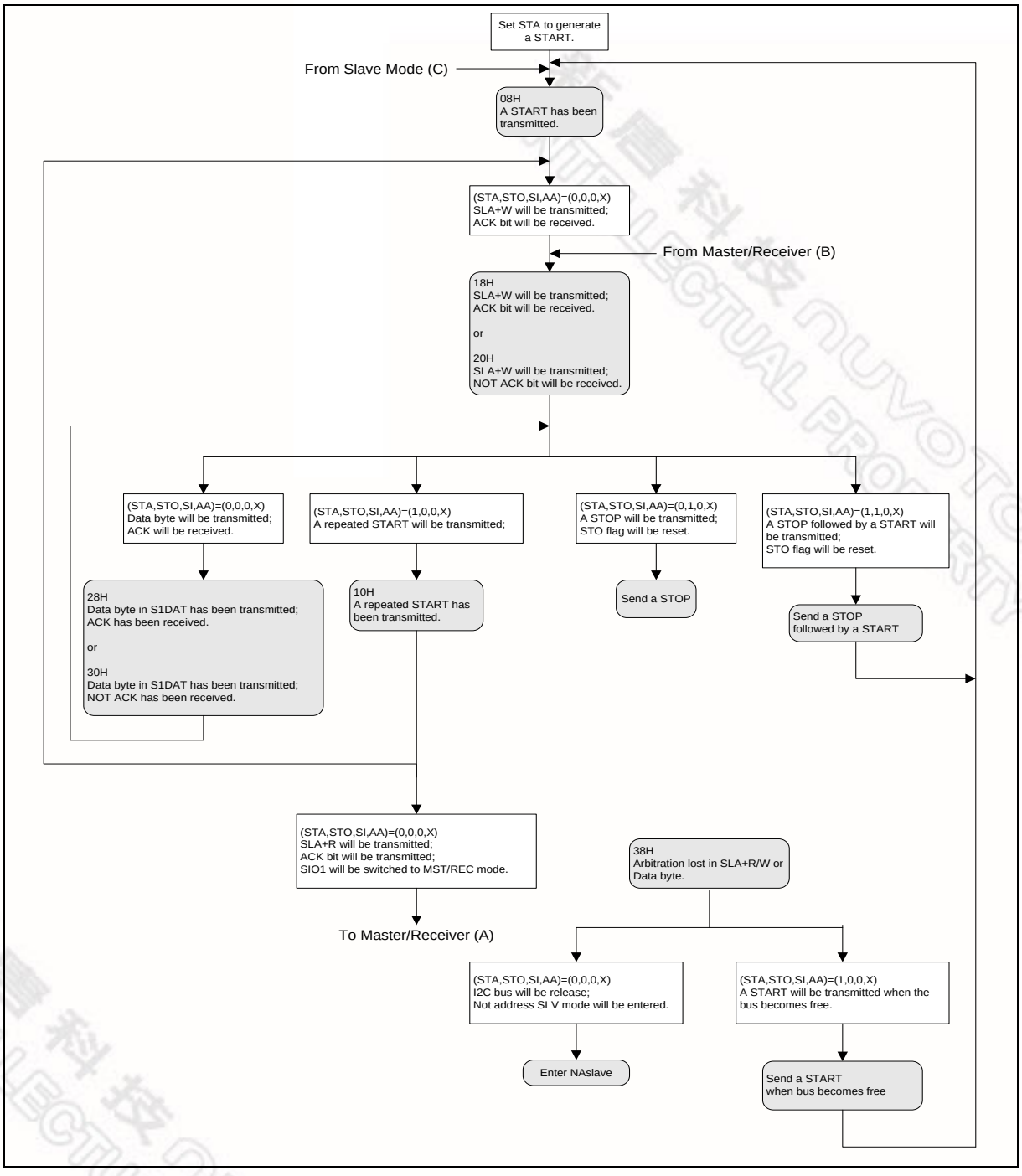


Figure 18-5 Master Transmitter Mode

25.2 PWM Operation

The following diagram shows PWM time-base generator.

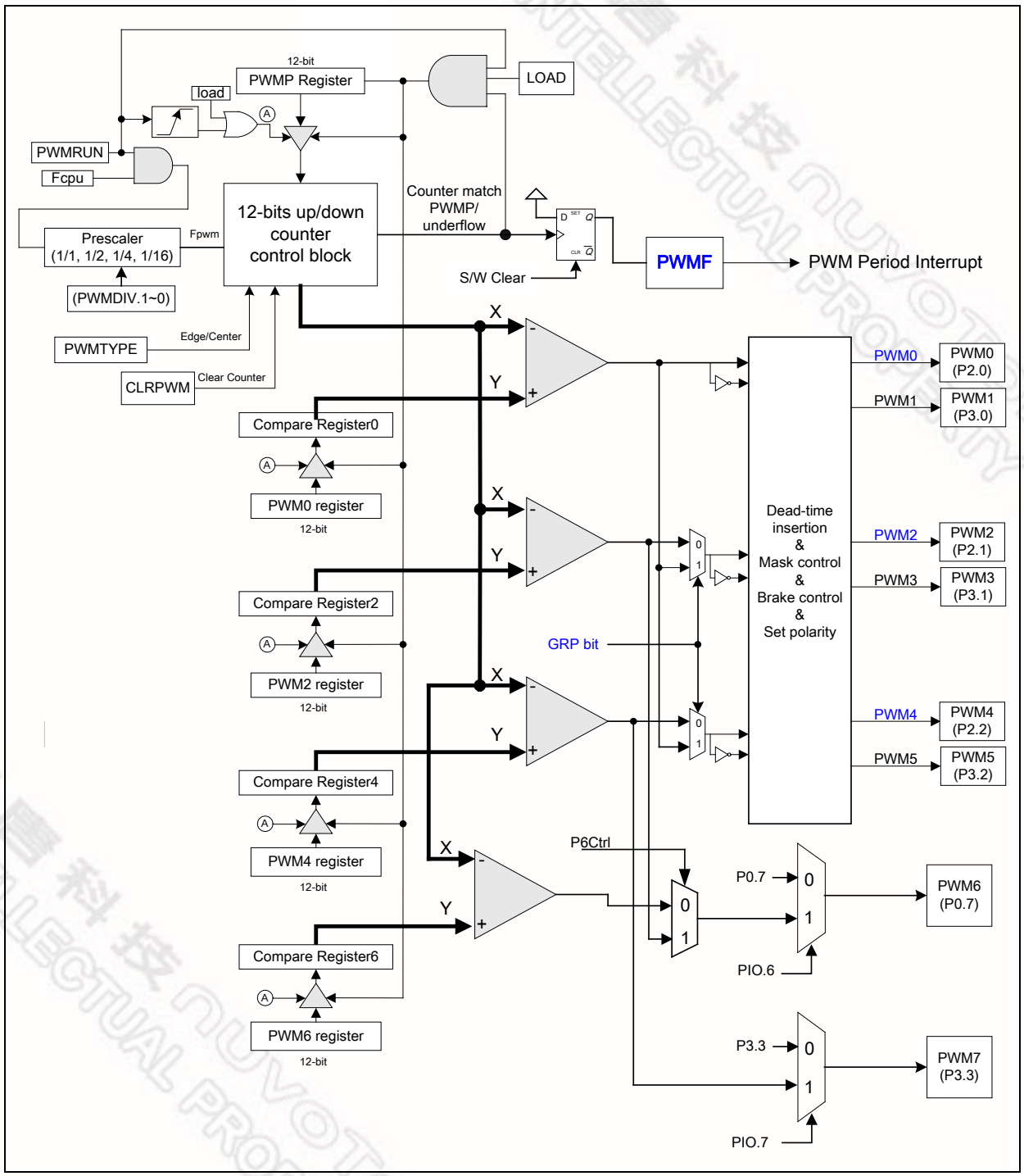


Figure 25-2: PWM Time-base Generator

program can poll these brake flag bits or enable PWM's brake interrupt to determine which condition causes a brake to occur.

25.4 PWM Output Driving Control

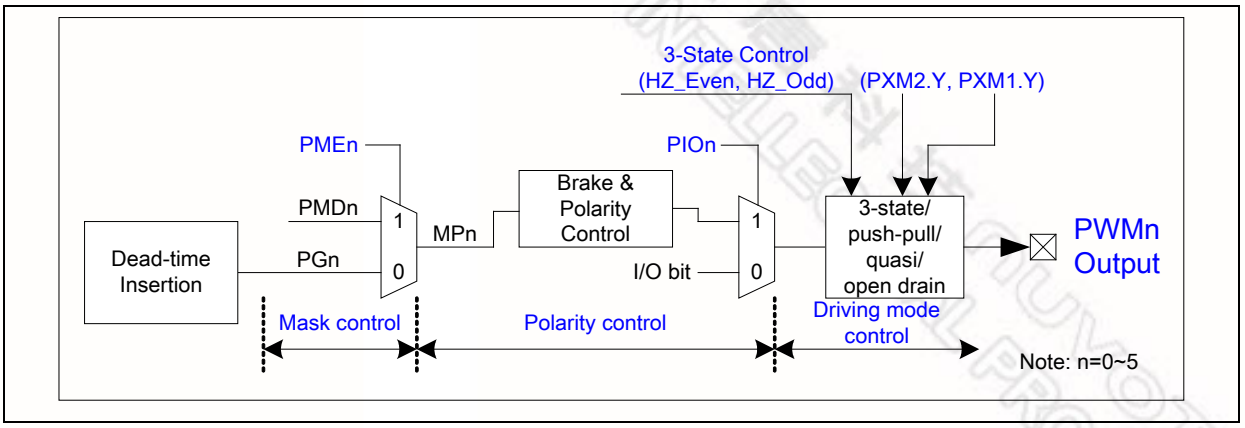


Figure 25-12: PWM Output Driving Control

The driving type of PWM output ports can be initialized as Tri-state type or other type dependent with SFR PxMy setting after any reset. As show in the above diagram, PWM output structures are controllable through option bits (config1.0-1), SFR (PWMCON3.HZ_Even,HZ_Odd) bits and SFR PxMy mode registers.

HZ_Even/HZ_Odd (SFR PWMCON3 BITS)	PWM Output Drive mode
0	Depend on PxMy SFR.
1	Driving mode = Hi-Z.

Note: SFR bits for HZ_Even and HZ_Odd are latched from config1.0 and config1.1, respectively, during all reset.

25.5 PWM modes

This powerful PWM unit supports Independent mode which may be applied to DC and BLDC motor system, Complementary mode with dead-time insertion which may be used in the application of AC induction motor and synchronous motor, Synchronous mode that makes both pins of each pair are in phase. Besides, the Group mode, forces the PWM0, PWM2 and PWM4 synchronous with PWM0 generator, may simplify updating duty control in DC and BLDC motor applications.

25.5.1 Independent mode

Independent mode is enabled when PMOD.1-0 = 00b.

On default, the PWM is operating in independent mode, with four PWM even channels outputs: PWM0, PWM2, PWM4 and PWM6. Each channel is running off its own duty-cycle generator module.

PWM6 can be user controllable to output from PWM2 generator if P6CTRL = 1.

PWM7 is taking output from PWM4 generator.

This device support Group Mode control. This control allows all even PWM channels output to be duty controllable by PWM0 duty register.

If GRP = 1, both (PG2, PG3) and (PG4, PG5) pairs will follow (PG0, PG1), which imply;

PG4 = PG2 = PG0;

PG5 = PG3 = PG1 = invert (PG0) if Complementary mode is enabled (PMOD.1-0=01b)

25.6 Polarity Control

Each PWM port of from PWM0 to PWM5 has independent polarity control to configure the polarity of active state of PWM output. At default, the PWM output is active high. This implies the PWM OFF state is low and ON state is high. This is controllable through SFR PNP on each individual PWM channel.

The following diagram show the initial state before PWM starts with different polarity settings.

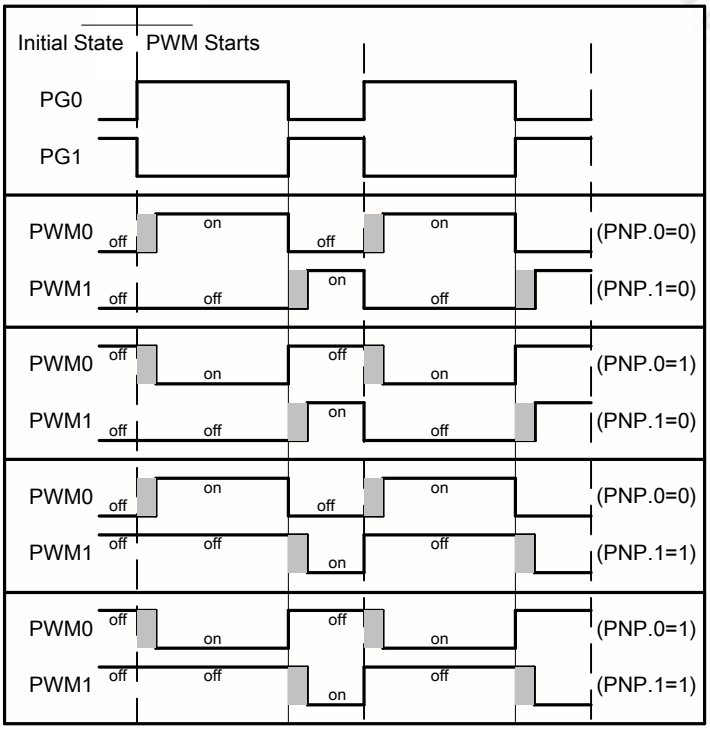


Figure 25-14: Initial state and polarity control with rising edge dead time insertion

25.7 PWM Mask Output

Each of the PWM output channels can be manually overridden by using the appropriate bits in the SFR PME and PMD registers to drive the PWM I/O pins to specified logic states independent of the duty cycle comparison units. The PWM mask bits are useful when controlling various types of Electrically Commutated Motor (ECM) like a BLDC motor. The PMD register contains six bits, PMD[5:0] determine which PWM I/O pins will be overridden. On reset PMD is 00H.

26 ANALOG-TO-DIGITAL CONVERTER (ADC)

N79E875 series support a 10-bit analog-to-digital converter (ADC) which contains a DAC which converts the contents of a successive approximation register to a voltage (V_{DAC}) which is compared to the analog input voltage (Vin). The output of the comparator is fed to the successive approximation control logic which controls the successive approximation register. This is illustrated in the figure below.

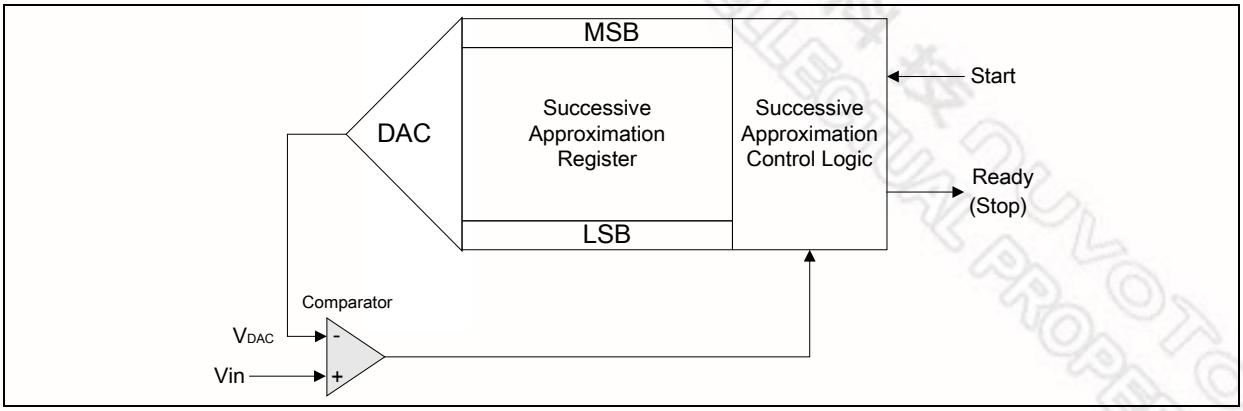


Figure 26-1: Successive Approximation ADC

26.1 Operation of ADC

26.1.1 Normal Operation of ADC

A conversion can be initiated by software only or by either hardware or software. The software only start mode is selected when control bit ADCCON.5 (ADCEX)=0. A conversion is then started by setting control bit ADCCON.3 (ADCS) The hardware or software start mode is selected when ADCEX =1, and a conversion may be started by setting ADCS as above or by applying a rising edge to external pin STADC(P1.7) or by a trigger signal synchronous with PWM unit. When a conversion is started by applying a rising edge, a low level must be applied to STADC for at least one machine cycle followed by a high level for at least one machine cycle. When ADCCON.5 (ADCEX) is set by external pin to start ADC conversion, after N79E875 series have entered idle mode, STADC/P1.7 can start ADC conversion at least 1 machine cycle.

The end of the 10-bit conversion is flagged by control bit ADCCON.4 (ADCI). The upper 8 bits of the result are held in special function register ADCH, and the two remaining bits are held in ADCCON.7 (ADC.1) and ADCCON.6 (ADC.0). The user may ignore the two least significant bits in ADCCON and use the ADC as an 8-bit converter (8 upper bits in ADCH). In any event, the total actual conversion time is 34 ADC clock cycles. ADCI flag is set at end of ADC conversion. ADCS will be hardware cleared when ADCI is set.

Control bits ADCCON.0, ADCCON.1 and ADCCON.2 are used to control an analog multiplexer which selects one of eight analog channels. An ADC conversion in progress is unaffected by an external or software ADC start. The result of a completed conversion remains unaffected provided ADCI = logic 1.

30 CONFIG BITS

The N79E875 series has two CONFIG bits (CONFIG0 located at FB00h, CONFIG1 located at FB01h) that must be defined at power up and can not be set the program after start of execution. Those features are configured through the use of two flash EPROM bytes, and the flash EPROM can be programmed and verified repeatedly. Until the code inside the Flash EPROM is confirmed OK, the code can be protected. The protection of flash EPROM (CONFIG1) and those operations on it are described below. The data of these bytes may be read by the MOVX instruction at the addresses.

30.1 CONFIG0

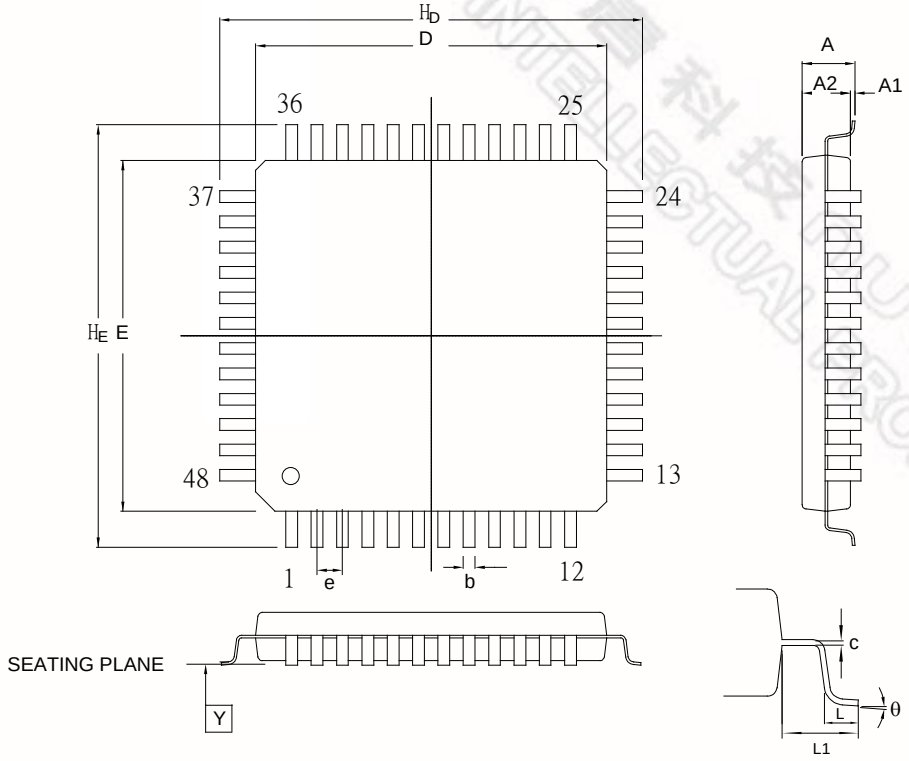
CONFIG0

Bit:	7	6	5	4	3	2	1	0
	WDTCK	RPD	PRHI	CBOV1	CBOV0	BPFR	Fosc1	Fosc0

BIT	NAME	FUNCTION
7	WDTCK	Clock source of Watchdog Timer select bit: 0: The internal 500KHz RC oscillator clock is for Watchdog Timer clock used. 1: The uC clock is for Watchdog Timer clock used.
6	RPD	Reset Pin Disable bit: 0: Enable Reset function of Pin 1.4. 1: Disable Reset function of Pin 1.4, and it to be used as an input port pin.
5	PRHI	Port Reset High or Low bit: 0: Port reset to low state. 1: Port reset to high state.
4-3	CBOV.1-0	Brownout Voltage Select bits: 00: Brownout detect voltage is 4.5V. 01: Brownout detect voltage is 3.8V. 1x: Brownout detect voltage is 2.6V (default).
2	BPFR	Bypass Clock Filter of Crystal Oscillator bit: 0: Disable Clock Filter. 1: Enable Clock Filter. (default)

32 PACKAGE DIMENSIONS

32.1 48L LQFP (7x7x1.4mm footprint 2.0mm)



Controlling dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	—	—	—	—
A_1	0.002	0.004	0.006	0.05	0.10	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.006	0.008	0.010	0.15	0.20	0.25
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.272	0.276	0.280	6.90	7.00	7.10
E	0.272	0.276	0.280	6.90	7.00	7.10
e	0.014	0.020	0.026	0.35	0.50	0.65
H_D	0.350	0.354	0.358	8.90	9.00	9.10
H_E	0.350	0.354	0.358	8.90	9.00	9.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	—
Y	—	—	0.004	—	—	0.10
θ	0°	—	7°	0°	—	7°

33 REVISION HISTORY

VERSION	DATE	PAGE/ CHAP.	DESCRIPTION
A01	December 30, 2008	-	Initial Issued
A02	April 13, 2009	All All Ch7 101 Ch7	a. Remove N79M8xx, 874 & 873 series and change 125°C to 85°C. b. Revise typos in the document. c. Rename PDTC1(ABh) to DTCNT d. Revise typo in Figure 15-2. (Change P4S to P2S) e. Remove “BOD = inverse (CBOD) config bit”

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