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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (1)
SATA	SATA 3Gbps (1)
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-20°C ~ 105°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	569-LFBGA
Supplier Device Package	569-MAPBGA (12x12)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcimx6d5ezk08ad

4.1.3 Operating Ranges

Table 6 provides the operating ranges of the i.MX 6Dual/6Quad processors.

Table 6. Operating Ranges

Parameter Description	Symbol	Min	Typ	Max[1]	Unit	Comment[2]
Run mode: LDO enabled	VDD_ARM_IN VDD_ARM23_IN[3]	1.275[4]	—	1.5	V	LDO Output Set Point (VDD_ARM_CAP[5]) of 1.150 V minimum for operation up to 792 MHz.
		1.05[4]	—	1.5	V	LDO Output Set Point (VDD_ARM_CAP) of 0.925 V minimum for operation up to 396 MHz.
	VDD_SOC_IN[6]	1.350[4]	—	1.5	V	264 MHz < VPU ≤ 352 MHz; VDDSOC and VDDPU LDO outputs (VDD_SOC_CAP and VDD_PU_CAP) require 1.225 V minimum.
		1.275[4,7]	—	1.5	V	VPU ≤ 264 MHz; VDDSOC and VDDPU LDO outputs (VDD_SOC_CAP and VDD_PU_CAP) require 1.15 V minimum.
Run mode: LDO bypassed[8]	VDD_ARM_IN VDD_ARM23_IN[3]	1.150	—	1.3	V	LDO bypassed for operation up to 792 MHz.
		0.925	—	1.3	V	LDO bypassed for operation up to 396 MHz.
	VDD_SOC_IN	1.225	—	1.3	V	264 MHz < VPU ≤ 352 MHz.
		1.15	—	1.3	V	VPU ≤ 264 MHz.
Standby/DSM Mode	VDD_ARM_IN VDD_ARM23_IN[3]	0.9	—	1.3	V	See Table 9, “Stop Mode Current and Power Consumption,” on page 27.
	VDD_SOC_IN	0.9	—	1.3	V	
VDD_HIGH internal Regulator	VDD_HIGH_IN[9]	2.8	—	3.3	V	Must match the range of voltages that the rechargeable backup battery supports.
Backup battery supply range	VDD_SNVS_IN[9]	2.8	—	3.3	V	Should be supplied from the same supply as VDD_HIGH_IN, if the system does not require keeping real time and other data on OFF state.
USB supply voltages	USB_OTG_VBUS	4.4	—	5.25	V	—
	USB_H1_VBUS	4.4	—	5.25	V	—
DDR I/O supply	NVCC_DRAM	1.14	1.2	1.3	V	LPDDR2
Supply for RGMII I/O power group[10]	NVCC_RGMII	1.15	—	2.625	V	• 1.15 V – 1.30 V in HSIC 1.2 V mode • 1.43 V – 1.58 V in RGMII 1.5 V mode • 1.70 V – 1.90 V in RGMII 1.8 V mode • 2.25 V – 2.625 V in RGMII 2.5 V mode

Table 6. Operating Ranges (continued)

Parameter Description	Symbol	Min	Typ	Max[1]	Unit	Comment[2]
GPIO supplies[10]	NVCC_CSI, NVCC_EIM0, NVCC_EIM1, NVCC_EIM2, NVCC_ENET, NVCC_GPIO, NVCC_LCD, NVCC_NANDF, NVCC_SD1, NVCC_SD2, NVCC_SD3, NVCC_JTAG	1.65	1.8, 2.8, 3.3	3.6	V	Isolation between the NVCC_EIMx and NVCC_SDx different supplies allow them to operate at different voltages within the specified range. Example: NVCC_EIM1 can operate at 1.8 V while NVCC_EIM2 operates at 3.3 V.
	NVCC_LVDS_2P5[11] NVCC_MIPI	2.25	2.5	2.75	V	—
HDMI supply voltages	HDMI_VP	0.99	1.1	1.3	V	—
	HDMI_VPH	2.25	2.5	2.75	V	—
PCIe supply voltages	PCIE_VP	1.023	1.1	1.3	V	—
	PCIE_VPH	2.325	2.5	2.75	V	—
	PCIE_VPTX	1.023	1.1	1.3	V	—
SATA Supply voltages	SATA_VP	0.99	1.1	1.3	V	—
	SATA_VPH	2.25	2.5	2.75	V	—
Junction temperature Extended Commercial	T_J	-20	—	105	°C	See *i.MX 6Dual/6Quad Product Lifetime Usage Estimates Application Note*, AN4724, for information on product lifetime (power-on years) for this processor.
Junction temperature Industrial	T_J	-40	—	105	°C	See *i.MX 6Dual/6Quad Product Usage Lifetime Estimates Application Note*, AN4724, for information on product lifetime (power-on years) for this processor.

1 Applying the maximum voltage results in maximum power consumption and heat generation. NXP recommends a voltage set point = (Vmin + the supply tolerance). This results in an optimized power/speed ratio.

2 See the Hardware Development Guide for i.MX 6Quad, 6Dual, 6DualLite, 6Solo Families of Applications Processors (IMX6DQ6SDLHDG) for bypass capacitors requirements for each of the *_CAP supply outputs.

3 For Quad core system, connect to VDD_ARM_IN. For Dual core system, may be shorted to GND together with VDD_ARM23_CAP to reduce leakage.

4 VDD_ARM_IN and VDD_SOC_IN must be at least 125 mV higher than the LDO Output Set Point for correct voltage regulation.

5 VDD_ARM_CAP must not exceed VDD_CACHE_CAP by more than +50 mV. VDD_CACHE_CAP must not exceed VDD_ARM_CAP by more than 200 mV.

6 VDD_SOC_CAP and VDD_PU_CAP must be equal.

7 In LDO enabled mode, the internal LDO output set points must be configured such that the:

VDD_ARM LDO output set point does not exceed the VDD_SOC LDO output set point by more than 100 mV.

VDD_SOC LDO output set point is equal to the VDD_PU LDO output set point.

The VDD_ARM LDO output set point can be lower than the VDD_SOC LDO output set point, however, the minimum output set points shown in this table must be maintained.

4.7.1 General Purpose I/O AC Parameters

The I/O AC parameters for GPIO in slow and fast modes are presented in the Table 25 and Table 26, respectively. Note that the fast or slow I/O behavior is determined by the appropriate control bits in the IOMUXC control registers.

Table 25. General Purpose I/O AC Parameters 1.8 V Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times, rise/fall (Max Drive, DSE=111)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	2.72/2.79 1.51/1.54	ns
Output Pad Transition Times, rise/fall (High Drive, DSE=101)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.20/3.36 1.96/2.07	
Output Pad Transition Times, rise/fall (Medium Drive, DSE=100)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.64/3.88 2.27/2.53	
Output Pad Transition Times, rise/fall (Low Drive. DSE=011)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	4.32/4.50 3.16/3.17	
Input Transition Times[1]	trm	—	—	—	25	ns

1 Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

Table 26. General Purpose I/O AC Parameters 3.3 V Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times, rise/fall (Max Drive, DSE=101)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	1.70/1.79 1.06/1.15	ns
Output Pad Transition Times, rise/fall (High Drive, DSE=011)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	2.35/2.43 1.74/1.77	
Output Pad Transition Times, rise/fall (Medium Drive, DSE=010)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.13/3.29 2.46/2.60	
Output Pad Transition Times, rise/fall (Low Drive. DSE=001)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	5.14/5.57 4.77/5.15	
Input Transition Times[1]	trm	—	—	—	25	ns

1 Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

4.8.1 GPIO Output Buffer Impedance

Table 29 shows the GPIO output buffer impedance (OVDD 1.8 V).

Table 29. GPIO Output Buffer Average Impedance (OVDD 1.8 V)

Parameter	Symbol	Drive Strength (DSE)	Typ Value	Unit
Output Driver Impedance	Rdrv	001 010 011 100 101 110 111	260 130 90 60 50 40 33	Ω

Table 30 shows the GPIO output buffer impedance (OVDD 3.3 V).

Table 30. GPIO Output Buffer Average Impedance (OVDD 3.3 V)

Parameter	Symbol	Drive Strength (DSE)	Typ Value	Unit
Output Driver Impedance	Rdrv	001 010 011 100 101 110 111	150 75 50 37 30 25 20	Ω

Table 38. Asynchronous Mode Timing Parameters[1] (continued)

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min	Max	
NF16	Data setup on read	tDSR	—	(DS × T -0.67)/18.38 [see [5,6]]	ns
NF17	Data hold on read	tDHR	0.82/11.83 [see [5,6]]	—	ns

1 The GPMI asynchronous mode output timing can be controlled by the module's internal registers HW_GPMI_TIMING0_ADDRESS_SETUP, HW_GPMI_TIMING0_DATA_SETUP, and HW_GPMI_TIMING0_DATA_HOLD. This AC timing depends on these registers settings. In the table, AS/DS/DH represents each of these settings.

2 AS minimum value can be 0, while DS/DH minimum value is 1.

3 T = GPMI clock period -0.075ns (half of maximum p-p jitter).

4 NF12 is met automatically by the design.

5 Non-EDO mode.

6 EDO mode, GPMI clock ≈ 100 MHz
(AS=DS=DH=1, GPMI_CTL1 [RDN_DELAY] = 8, GPMI_CTL1 [HALF_PERIOD] = 0).

In EDO mode (Figure 26), NF16/NF17 are different from the definition in non-EDO mode (Figure 25). They are called tREA/tRHOH (NAND_RE_B access time/NAND_RE_B HIGH to output hold). The typical value for them are 16 ns (max for tREA)/15 ns (min for tRHOH) at 50 MB/s EDO mode. In EDO mode, GPMI will sample NAND_DATAxx at rising edge of delayed NAND_RE_B provided by an internal DPLL. The delay value can be controlled by GPMI_CTRL1.RDN_DELAY (see the GPMI chapter of the i.MX 6Dual/6Quad reference manual (IMX6DQRM)). The typical value of this control register is 0x8 at 50 MT/s EDO mode. However, if the board delay is large enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

4.11.2 Source Synchronous Mode AC Timing (ONFI 2.x Compatible)

Figure 27 shows the write and read timing of Source Synchronous mode.

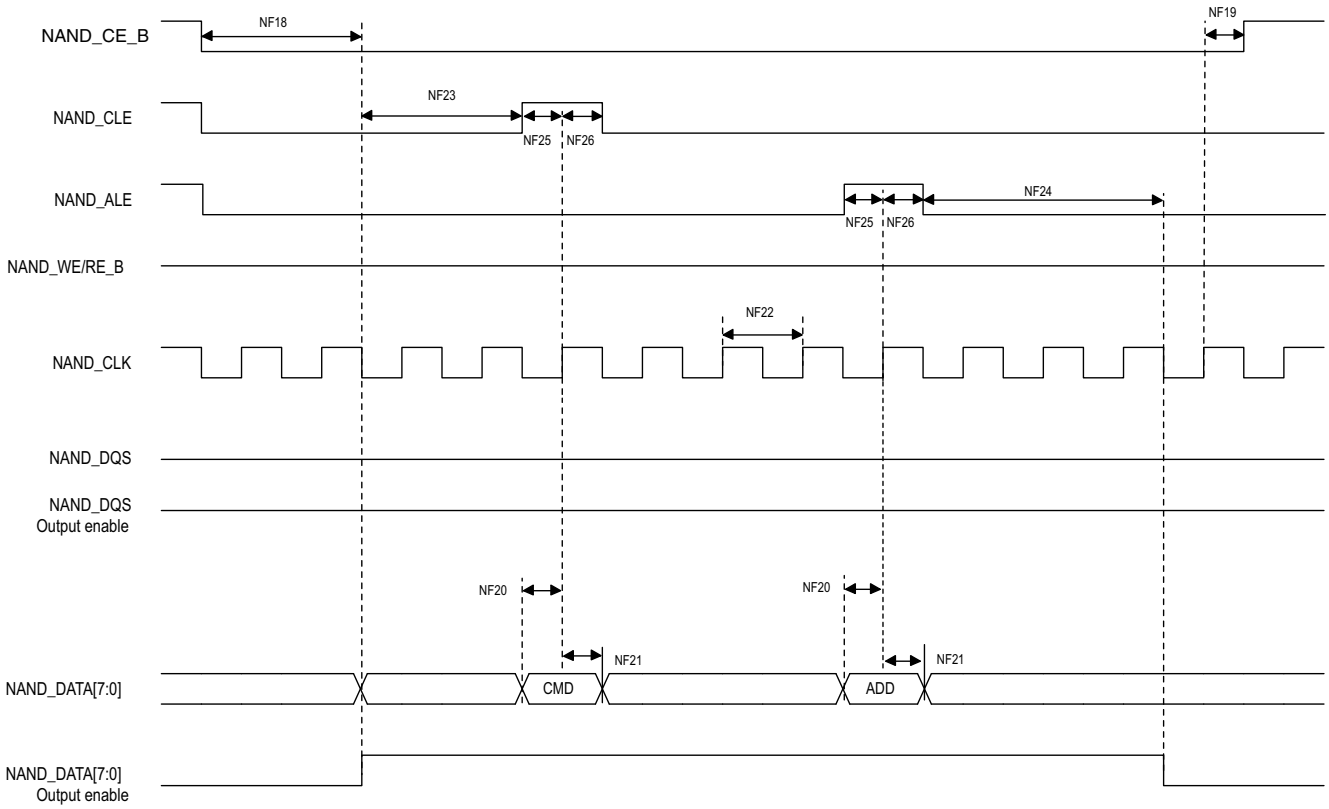


Figure 27. Source Synchronous Mode Command and Address Timing Diagram

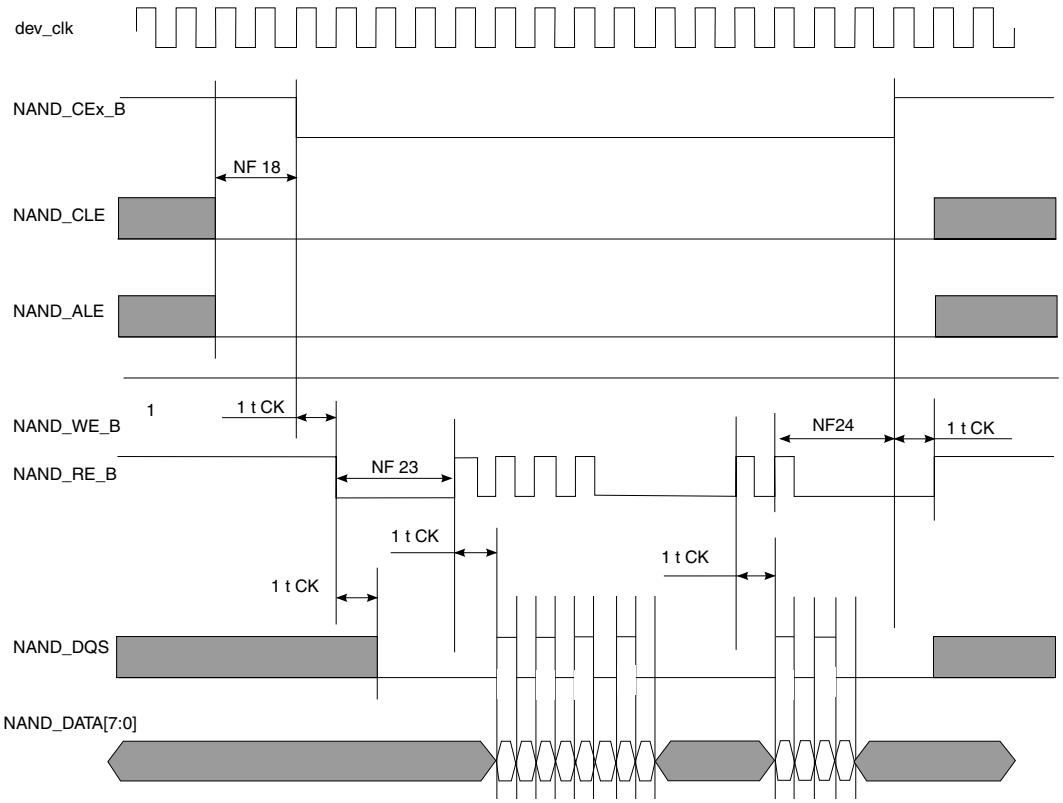


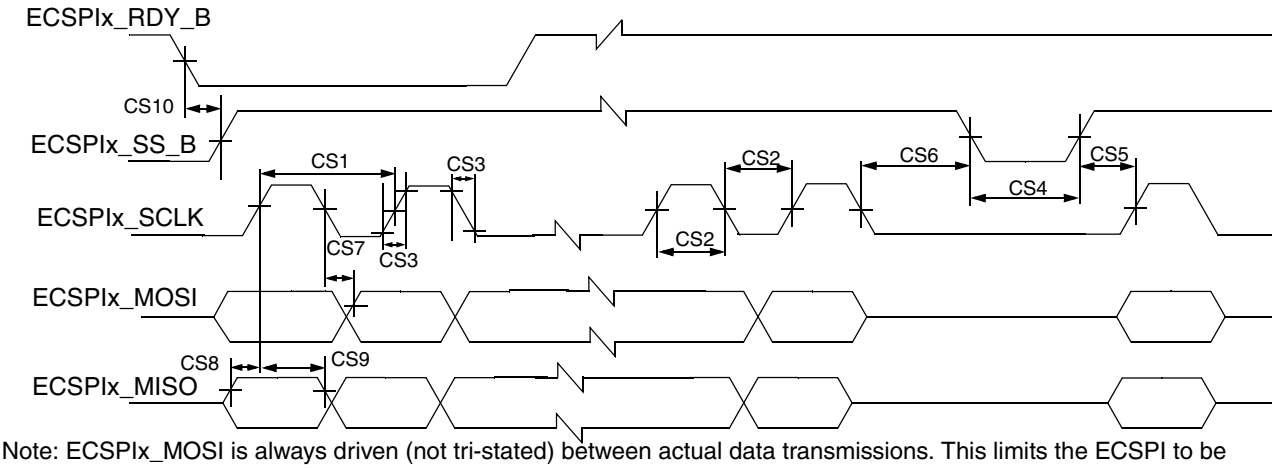
Figure 32. Samsung Toggle Mode Data Read Timing

Table 40. Samsung Toggle Mode Timing Parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min	Max	
NF1	NAND_CLE setup time	tCLS	(AS + DS) × T - 0.12 [see 2,3]		—
NF2	NAND_CLE hold time	tCLH	DH × T - 0.72 [see 2]		—
NF3	NAND_CEx_B setup time	tCS	(AS + DS) × T - 0.58 [see 3,2]		—
NF4	NAND_CEx_B hold time	tCH	DH × T - 1 [see 2]		—
NF5	NAND_WE_B pulse width	tWP	DS × T [see 2]		—
NF6	NAND_ALE setup time	tALS	(AS + DS) × T - 0.49 [see 3,2]		—
NF7	NAND_ALE hold time	tALH	DH × T - 0.42 [see 2]		—
NF8	Command/address NAND_DATAxx setup time	tCAS	DS × T - 0.26 [see 2]		—
NF9	Command/address NAND_DATAxx hold time	tCAH	DH × T - 1.37 [see 2]		—
NF18	NAND_CEx_B access time	tCE	CE_DELAY × T [see 4,2]	—	ns
NF22	clock period	tCK	—	—	ns
NF23	preamble delay	tPRE	PRE_DELAY × T [see 5,2]	—	ns
NF24	postamble delay	tPOST	POST_DELAY × T +0.43 [see 2]	—	ns

4.12.2.1 ECSPI Master Mode Timing

Figure 33 depicts the timing of ECSPI in master mode and Table 41 lists the ECSPI master mode timing characteristics.



Note: ECSPIx_MOSI is always driven (not tri-stated) between actual data transmissions. This limits the ECSPI to be connected between a single master and a single slave.

Figure 33. ECSPI Master Mode Timing Diagram

Table 41. ECSPI Master Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	ECSPIx_SCLK Cycle Time–Read • Slow group[1] • Fast group[2] ECSPIx_SCLK Cycle Time–Write	t_{clk}	 55 40 15	—	ns
CS2	ECSPIx_SCLK High or Low Time–Read • Slow group[1] • Fast group[2] ECSPIx_SCLK High or Low Time–Write	t_{SW}	 26 20 7	—	ns
CS3	ECSPIx_SCLK Rise or Fall[3]	$t_{RISE/FALL}$	—	—	ns
CS4	ECSPIx_SSx pulse width	t_{CSLH}	Half ECSPIx_SCLK period	—	ns
CS5	ECSPIx_SSx Lead Time (CS setup time)	t_{SCS}	Half ECSPIx_SCLK period - 4	—	ns
CS6	ECSPIx_SSx Lag Time (CS hold time)	t_{HCS}	Half ECSPIx_SCLK period - 2	—	ns
CS7	ECSPIx_MOSI Propagation Delay (C_{LOAD} = 20 pF)	t_{PDmosi}	-1	1	ns
CS8	ECSPIx_MISO Setup Time • Slow group[1] • Fast group[2]	t_{Smiso}	 21.5 16	—	ns
CS9	ECSPIx_MISO Hold Time	t_{Hmiso}	0	—	ns
CS10	ECSPIx_RDY to ECSPIx_SSx Time[4]	t_{SDRY}	5	—	ns

1 ECSPI slow includes:

ECSPI1/DISP0_DAT22, ECSPI1/KEY_COL1, ECSPI1/CSI0_DAT6, ECSPI2/EIM_OE, ECSPI2/ ECSPI2/CSI0_DAT10, ECSPI3/DISP0_DAT2

2 ECSPI fast includes:

ECSPI1/EIM_D17, ECSPI4/EIM_D22, ECSPI5/SD2_DAT0, ECSPI5/SD1_DAT0

3 See specific I/O AC parameters Section 4.7, “I/O AC Parameters.”

4 ECSPI_RDY is sampled internally by ipg_clk and is asynchronous to all other CSPI signals.

4.12.3 Enhanced Serial Audio Interface (ESAI) Timing Parameters

The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. Table 43 shows the interface timing values. The number field in the table refers to timing signals found in Figure 35 and Figure 36.

Table 43. Enhanced Serial Audio Interface (ESAI) Timing

ID	Parameter[1,2]	Symbol	Expression[2]	Min	Max	Condition[3]	Unit
62	Clock cycle[4]	t_{SSICC}	$4 \times T_C$ $4 \times T_C$	30.0 30.0	— —	i ck i ck	ns
63	Clock high period: • For internal clock • For external clock	— —	$2 \times T_C - 9.0$ $2 \times T_C$	6 15	— —	— —	ns
64	Clock low period: • For internal clock • For external clock	— —	$2 \times T_C - 9.0$ $2 \times T_C$	6 15	— —	— —	ns
65	ESAI_RX_CLK rising edge to ESAI_RX_FS out (bl) high	— —	— —	— —	19.0 7.0	x ck i ck a	ns
66	ESAI_RX_CLK rising edge to ESAI_RX_FS out (bl) low	— —	— —	— —	19.0 7.0	x ck i ck a	ns
67	ESAI_RX_CLK rising edge to ESAI_RX_FS out (wr) high[5]	— —	— —	— —	19.0 9.0	x ck i ck a	ns
68	ESAI_RX_CLK rising edge to ESAI_RX_FS out (wr) low[5]	— —	— —	— —	19.0 9.0	x ck i ck a	ns
69	ESAI_RX_CLK rising edge to ESAI_RX_FS out (wl) high	— —	— —	— —	19.0 6.0	x ck i ck a	ns
70	ESAI_RX_CLK rising edge to ESAI_RX_FSout (wl) low	— —	— —	— —	17.0 7.0	x ck i ck a	ns
71	Data in setup time before ESAI_RX_CLK (serial clock in synchronous mode) falling edge	— —	— —	12.0 19.0	— —	x ck i ck	ns
72	Data in hold time after ESAI_RX_CLK falling edge	— —	— —	3.5 9.0	— —	x ck i ck	ns
73	ESAI_RX_FS input (bl, wr) high before ESAI_RX_CLK falling edge[5]	— —	— —	2.0 19.0	— —	x ck i ck a	ns
74	ESAI_RX_FS input (wl) high before ESAI_RX_CLK falling edge	— —	— —	2.0 19.0	— —	x ck i ck a	ns
75	ESAI_RX_FS input hold time after ESAI_RX_CLK falling edge	— —	— —	2.5 8.5	— —	x ck i ck a	ns
78	ESAI_TX_CLK rising edge to ESAI_TX_FS out (bl) high	— —	— —	— —	19.0 8.0	x ck i ck	ns
79	ESAI_TX_CLK rising edge to ESAI_TX_FS out (bl) low	— —	— —	— —	20.0 10.0	x ck i ck	ns
80	ESAI_TX_CLK rising edge to ESAI_TX_FS out (wr) high[5]	— —	— —	— —	20.0 10.0	x ck i ck	ns

2 The MSB bits are duplicated on LSB bits implementing color extension.
3 The two MSB bits are duplicated on LSB bits implementing color extension.
4 YCbCr, 8 bits—Supported within the BT.656 protocol (sync embedded within the data stream).
5 RGB, 16 bits—Supported in two ways: (1) As a “generic data” input—with no on-the-fly processing; (2) With on-the-fly processing, but only under some restrictions on the control protocol.
6 YCbCr, 16 bits—Supported as a “generic-data” input—with no on-the-fly processing.
7 YCbCr, 16 bits—Supported as a sub-case of the YCbCr, 20 bits, under the same conditions (BT.1120 protocol).
8 YCbCr, 20 bits—Supported only within the BT.1120 protocol (syncs embedded within the data stream).

4.12.10.2 Sensor Interface Timings

There are three camera timing modes supported by the IPU.

4.12.10.2.1 BT.656 and BT.1120 Video Mode

Smart camera sensors, which include imaging processing, usually support video mode transfer. They use an embedded timing syntax to replace the IPU2_CSIx_VSYNC and IPU2_CSIx_HSYNC signals. The timing syntax is defined by the BT.656/BT.1120 standards.

This operation mode follows the recommendations of ITU BT.656/ ITU BT.1120 specifications. The only control signal used is IPU2_CSIx_PIX_CLK. Start-of-frame and active-line signals are embedded in the data stream. An active line starts with a SAV code and ends with a EAV code. In some cases, digital blanking is inserted in between EAV and SAV code. The CSI decodes and filters out the timing-coding from the data stream, thus recovering IPU2_CSIx_VSYNC and IPU2_CSIx_HSYNC signals for internal use. On BT.656 one component per cycle is received over the IPU2_CSIx_DATA_EN bus. On BT.1120 two components per cycle are received over the IPU2_CSIx_DATA_EN bus.

4.12.10.2.2 Gated Clock Mode

The IPU2_CSIx_VSYNC, IPU2_CSIx_HSYNC, and IPU2_CSIx_PIX_CLK signals are used in this mode. See Figure 57.

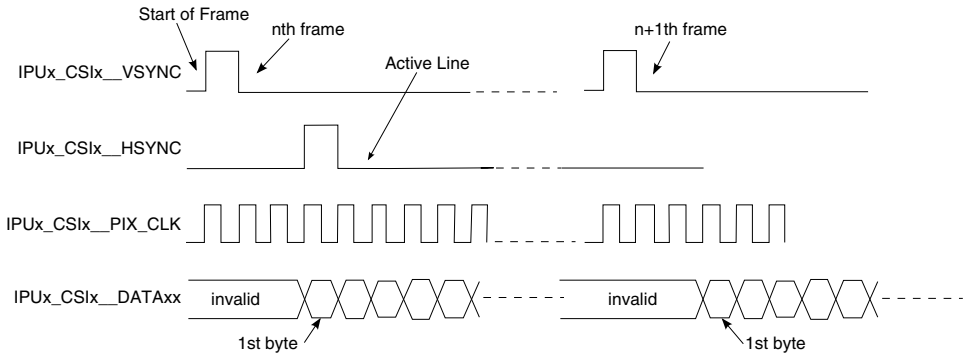


Figure 57. Gated Clock Mode Timing Diagram

A frame starts with a rising edge on IPU2_CSIx_VSYNC (all the timings correspond to straight polarity of the corresponding signals). Then IPU2_CSIx_HSYNC goes to high and hold for the entire line. Pixel clock is valid as long as IPU2_CSIx_HSYNC is high. Data is latched at the rising edge of the valid pixel clocks. IPU2_CSIx_HSYNC goes to low at the end of line. Pixel clocks then become invalid and the CSI

There are special physical outputs to provide synchronous controls:

- The ipp_disp_clk is a dedicated base synchronous signal that is used to generate a base display (component, pixel) clock for a display.
- The ipp_pin_1– ipp_pin_7 are general purpose synchronous pins, that can be used to provide HSYNC, VSYNC, DRDY or any else independent signal to a display.

The IPU has a system of internal binding counters for internal events (such as, HSYNC/VSYNC) calculation. The internal event (local start point) is synchronized with internal DI_CLK. A suitable control starts from the local start point with predefined UP and DOWN values to calculate control's changing points with half DI_CLK resolution. A full description of the counter system can be found in the IPU chapter of the i.MX 6Dual/6Quad reference manual (IMX6DQRM).

4.12.10.5.2 Asynchronous Controls

The asynchronous control is a data-oriented signal that changes its value with an output data according to additional internal flags coming with the data.

There are special physical outputs to provide asynchronous controls, as follows:

- The ipp_d0_cs and ipp_d1_cs pins are dedicated to provide chip select signals to two displays.
- The ipp_pin_11– ipp_pin_17 are general purpose asynchronous pins, that can be used to provide WR. RD, RS or any other data-oriented signal to display.

NOTE

The IPU has independent signal generators for asynchronous signals toggling. When a DI decides to put a new asynchronous data on the bus, a new internal start (local start point) is generated. The signal generators calculate predefined UP and DOWN values to change pins states with half DI_CLK resolution.

4.12.10.6 Synchronous Interfaces to Standard Active Matrix TFT LCD Panels

4.12.10.6.1 IPU Display Operating Signals

The IPU uses four control signals and data to operate a standard synchronous interface:

- IPP_DISP_CLK—Clock to display
- HSYNC—Horizontal synchronization
- VSYNC—Vertical synchronization
- DRDY—Active data

All synchronous display controls are generated on the base of an internally generated "local start point". The synchronous display controls can be placed on time axis with DI's offset, up and down parameters. The display access can be whole number of DI clock (Tdiclk) only. The IPP_DATA can not be moved relative to the local start point. The data bus of the synchronous interface is output direction only.

Table 59. Synchronous Display Interface Timing Characteristics (Pixel Level) (continued)

ID	Parameter	Symbol	Value	Description	Unit
IP5o	Offset of IPP_DISP_CLK	Todicp	DISP_CLK_OFFSET × Tdiclk	DISP_CLK_OFFSET—offset of IPP_DISP_CLK edges from local start point, in DI_CLK×2 (0.5 DI_CLK Resolution). Defined by DISP_CLK counter.	ns
IP13o	Offset of VSYNC	Tovs	VSYNC_OFFSET × Tdiclk	VSYNC_OFFSET—offset of Vsync edges from a local start point, when a Vsync should be active, in DI_CLK×2 (0.5 DI_CLK Resolution). The VSYNC_OFFSET should be built by suitable DI's counter.	ns
IP8o	Offset of HSYNC	Tohs	HSYNC_OFFSET × Tdiclk	HSYNC_OFFSET—offset of Hsync edges from a local start point, when a Hsync should be active, in DI_CLK×2 (0.5 DI_CLK Resolution). The HSYNC_OFFSET should be built by suitable DI's counter.	ns
IP9o	Offset of DRDY	Todrdy	DRDY_OFFSET × Tdiclk	DRDY_OFFSET—offset of DRDY edges from a suitable local start point, when a corresponding data has been set on the bus, in DI_CLK×2 (0.5 DI_CLK Resolution). The DRDY_OFFSET should be built by suitable DI's counter.	ns

[1] Display interface clock period immediate value.

$$Tdicp = \begin{cases} T_{diclk} \times \frac{DISP\_CLK\_PERIOD}{DI\_CLK\_PERIOD}, & \text{for integer } \frac{DISP\_CLK\_PERIOD}{DI\_CLK\_PERIOD} \\ T_{diclk}\left(floor\left[\frac{DISP\_CLK\_PERIOD}{DI\_CLK\_PERIOD}\right] + 0.5 \pm 0.5\right), & \text{for fractional } \frac{DISP\_CLK\_PERIOD}{DI\_CLK\_PERIOD} \end{cases}$$

DISP_CLK_PERIOD—number of DI_CLK per one Tdicp. Resolution 1/16 of DI_CLK.
DI_CLK_PERIOD—relation of between programing clock frequency and current system clock frequency
Display interface clock period average value.

$$\overline{T}dicp = T_{diclk} \times \frac{DISP\_CLK\_PERIOD}{DI\_CLK\_PERIOD}$$

[2] DI's counter can define offset, period and UP/DOWN characteristic of output signal according to programed parameters of the counter. Same of parameters in the table are not defined by DI's registers directly (by name), but can be generated by corresponding DI's counter. The SCREEN_WIDTH is an input value for DI's HSYNC generation counter. The distance between HSYNCs is a SCREEN_WIDTH.

The maximum accuracy of UP/DOWN edge of controls is:

$$Accuracy = (0.5 \times T_{diclk}) \pm 0.62ns$$

The maximum accuracy of UP/DOWN edge of IPP_DISP_DATA is:

$$Accuracy = T_{diclk} \pm 0.62ns$$

The DISP_CLK_PERIOD, DI_CLK_PERIOD parameters are register-controlled.

6 Package Information and Contact Assignments

This section includes the contact assignment information and mechanical package drawing.

6.1 Signal Naming Convention

The signal names of the i.MX6 series of products are standardized to align the signal names within the family and across the documentation. Benefits of this standardization are as follows:

- Signal names are unique within the scope of an SoC and within the series of products
- Searches will return all occurrences of the named signal
- Signal names are consistent between i.MX 6 series products implementing the same modules
- The module instance is incorporated into the signal name

This standardization applies only to signal names. The ball names are preserved to prevent the need to change schematics, BSDL models, IBIS models, and so on.

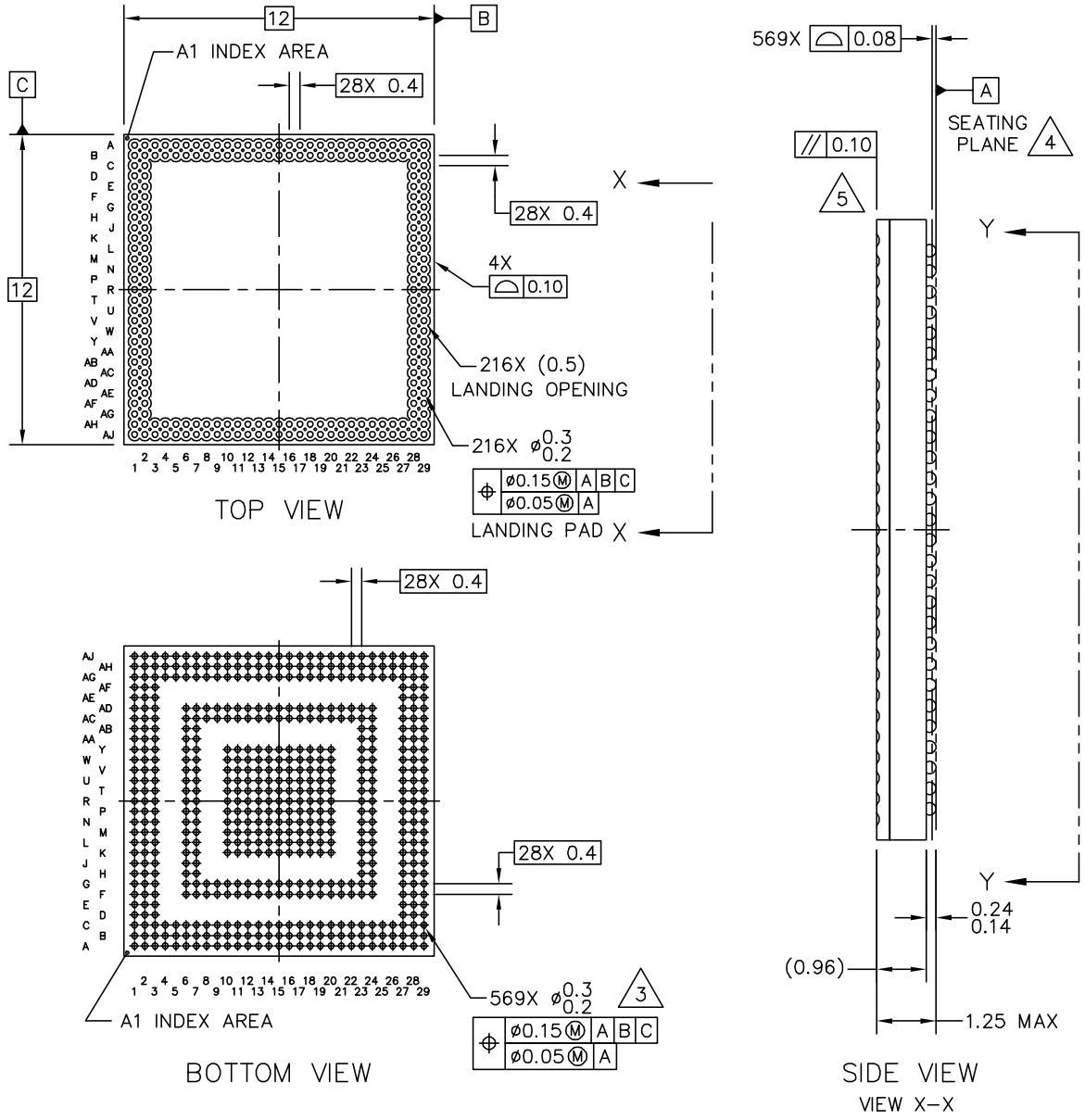
Throughout this document, the signal names are used except where referenced as a ball name (such as the Functional Contact Assignments table, Ball Map table, and so on). A master list of signal names is in the document, *IMX 6 Series Standardized Signal Name Map* (EB792). This list can be used to map the signal names used in older documentation to the standardized naming conventions.

6.2 12 x 12 mm Package on Package (PoP) Information

This section contains the outline drawing, signal assignment map, ground/power reference ID (by ball grid location) for the 12 x 12 mm, 0.4 mm pitch PoP package.

6.2.1 Case PoP, 0.4 mm Pitch, 12 x 12 Ball Matrix

Figure 97 and Figure 97 show the top, bottom, and side views of the 12 x 12 mm PoP package.



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TITLE: FCMAPBGA STACKABLE, 12 X 12 X 1.15 PKG, 0.4 MM PITCH, 569 I/O	DOCUMENT NO: 98ASA00383D	REV: A
	STANDARD: NON–JEDEC	
	SOT1644–1	29 FEB 2016

Figure 96. 12 x 12 mm PoP Package Top, Bottom, and Side Views (Sheet 1 of 2)

Table 85. 12 x 12 mm Functional Contact Assignments (continued)

Ball Name	PoP Bottom Ball	PoP Top Ball	Power Group	Ball Type	Out of Reset Condition[1]			
					Default Mode	Default Function	Input/ Output	Value[2]
CSI_D3M	G2	—	NVCC_MIPI	—	—	CSI_DATA3_N	—	—
CSI_D3P	G1	—	NVCC_MIPI	—	—	CSI_DATA3_P	—	—
CSI0_DAT4	U6	—	NVCC_CSI	GPIO	ALT5	GPIO5_IO22	Input	PU (100k)
CSI0_DAT5	U7	—	NVCC_CSI	GPIO	ALT5	GPIO5_IO23	Input	PU (100k)
CSI0_DAT6	Y1	—	NVCC_CSI	GPIO	ALT5	GPIO5_IO24	Input	PU (100k)
CSI0_DAT7	Y2	—	NVCC_CSI	GPIO	ALT5	GPIO5_IO25	Input	PU (100k)
CSI0_DAT8	W2	—	NVCC_CSI	GPIO	ALT5	GPIO5_IO26	Input	PU (100k)
CSI0_DAT9	W1	—	NVCC_CSI	GPIO	ALT5	GPIO5_IO27	Input	PU (100k)
CSI0_DAT10	W3	—	NVCC_CSI	GPIO	ALT5	GPIO5_IO28	Input	PU (100k)
CSI0_DAT11	V1	—	NVCC_CSI	GPIO	ALT5	GPIO5_IO29	Input	PU (100k)
CSI0_DAT12	V3	—	NVCC_CSI	GPIO	ALT5	GPIO5_IO30	Input	PU (100k)
CSI0_DAT13	T6	—	NVCC_CSI	GPIO	ALT5	GPIO5_IO31	Input	PU (100k)
CSI0_DAT14	U2	—	NVCC_CSI	GPIO	ALT5	GPIO6_IO00	Input	PU (100k)
CSI0_DAT15	V2	—	NVCC_CSI	GPIO	ALT5	GPIO6_IO01	Input	PU (100k)
CSI0_DAT16	T2	—	NVCC_CSI	GPIO	ALT5	GPIO6_IO02	Input	PU (100k)
CSI0_DAT17	U1	—	NVCC_CSI	GPIO	ALT5	GPIO6_IO03	Input	PU (100k)
CSI0_DAT18	T1	—	NVCC_CSI	GPIO	ALT5	GPIO6_IO04	Input	PU (100k)
CSI0_DAT19	R3	—	NVCC_CSI	GPIO	ALT5	GPIO6_IO05	Input	PU (100k)
CSI0_DATA_EN	V6	—	NVCC_CSI	GPIO	ALT5	GPIO5_IO20	Input	PU (100k)
CSI0_MCLK	AA2	—	NVCC_CSI	GPIO	ALT5	GPIO5_IO19	Input	PU (100k)
CSI0_PIXCLK	AD1	—	NVCC_CSI	GPIO	ALT5	GPIO5_IO18	Input	PU (100k)
CSI0_VSYNC	AA1	—	NVCC_CSI	GPIO	ALT5	GPIO5_IO21	Input	PU (100k)
DI0_DISP_CLK	AF29	—	NVCC_LCD	GPIO	ALT5	GPIO4_IO16	Input	PU (100k)
DI0_PIN2	AD29	—	NVCC_LCD	GPIO	ALT5	GPIO4_IO18	Input	PU (100k)
DI0_PIN3	W24	—	NVCC_LCD	GPIO	ALT5	GPIO4_IO19	Input	PU (100k)
DI0_PIN4	U24	—	NVCC_LCD	GPIO	ALT5	GPIO4_IO20	Input	PU (100k)
DI0_PIN15	AD28	—	NVCC_LCD	GPIO	ALT5	GPIO4_IO17	Input	PU (100k)
DISP0_DAT0	AH29	—	NVCC_LCD	GPIO	ALT5	GPIO4_IO21	Input	PU (100k)
DISP0_DAT1	AD27	—	NVCC_LCD	GPIO	ALT5	GPIO4_IO22	Input	PU (100k)
DISP0_DAT2	AB27	—	NVCC_LCD	GPIO	ALT5	GPIO4_IO23	Input	PU (100k)
DISP0_DAT3	V23	—	NVCC_LCD	GPIO	ALT5	GPIO4_IO24	Input	PU (100k)
DISP0_DAT4	V24	—	NVCC_LCD	GPIO	ALT5	GPIO4_IO25	Input	PU (100k)
DISP0_DAT5	AH27	—	NVCC_LCD	GPIO	ALT5	GPIO4_IO26	Input	PU (100k)
DISP0_DAT6	U23	—	NVCC_LCD	GPIO	ALT5	GPIO4_IO27	Input	PU (100k)
DISP0_DAT7	AE28	—	NVCC_LCD	GPIO	ALT5	GPIO4_IO28	Input	PU (100k)
DISP0_DAT8	AJ26	—	NVCC_LCD	GPIO	ALT5	GPIO4_IO29	Input	PU (100k)
DISP0_DAT9	AG28	—	NVCC_LCD	GPIO	ALT5	GPIO4_IO30	Input	PU (100k)
DISP0_DAT10	AH26	—	NVCC_LCD	GPIO	ALT5	GPIO4_IO31	Input	PU (100k)
DISP0_DAT11	AJ27	—	NVCC_LCD	GPIO	ALT5	GPIO5_IO05	Input	PU (100k)
DISP0_DAT12	AF28	—	NVCC_LCD	GPIO	ALT5	GPIO5_IO06	Input	PU (100k)

Table 85. 12 x 12 mm Functional Contact Assignments (continued)

Ball Name	PoP Bottom Ball	PoP Top Ball	Power Group	Ball Type	Out of Reset Condition[1]			
					Default Mode	Default Function	Input/ Output	Value[2]
DISP0_DAT13	AJ25	—	NVCC_LCD	GPIO	ALT5	GPIO5_IO07	Input	PU (100k)
DISP0_DAT14	AJ28	—	NVCC_LCD	GPIO	ALT5	GPIO5_IO08	Input	PU (100k)
DISP0_DAT15	AH25	—	NVCC_LCD	GPIO	ALT5	GPIO5_IO09	Input	PU (100k)
DISP0_DAT16	AB24	—	NVCC_LCD	GPIO	ALT5	GPIO5_IO10	Input	PU (100k)
DISP0_DAT17	AH28	—	NVCC_LCD	GPIO	ALT5	GPIO5_IO11	Input	PU (100k)
DISP0_DAT18	AH24	—	NVCC_LCD	GPIO	ALT5	GPIO5_IO12	Input	PU (100k)
DISP0_DAT19	AA24	—	NVCC_LCD	GPIO	ALT5	GPIO5_IO13	Input	PU (100k)
DISP0_DAT20	AD24	—	NVCC_LCD	GPIO	ALT5	GPIO5_IO14	Input	PU (100k)
DISP0_DAT21	AC24	—	NVCC_LCD	GPIO	ALT5	GPIO5_IO15	Input	PU (100k)
DISP0_DAT22	Y24	—	NVCC_LCD	GPIO	ALT5	GPIO5_IO16	Input	PU (100k)
DISP0_DAT23	AJ24	—	NVCC_LCD	GPIO	ALT5	GPIO5_IO17	Input	PU (100k)
DRAM_CA0P0	—	R29	NVCC_DRAM	DDR	ALT0	LPDDR2_CA0_P0	Output	0
DRAM_CA0P1	—	AJ27	NVCC_DRAM	DDR	ALT0	LPDDR2_CA0_P1	Output	0
DRAM_CA1P0	—	T29	NVCC_DRAM	DDR	ALT0	LPDDR2_CA1_P0	Output	0
DRAM_CA1P1	—	AH27	NVCC_DRAM	DDR	ALT0	LPDDR2_CA1_P1	Output	0
DRAM_CA2P0	—	U29	NVCC_DRAM	DDR	ALT0	LPDDR2_CA2_P0	Output	0
DRAM_CA2P1	—	AH26	NVCC_DRAM	DDR	ALT0	LPDDR2_CA2_P1	Output	0
DRAM_CA3P0	—	V29	NVCC_DRAM	DDR	ALT0	LPDDR2_CA3_P0	Output	0
DRAM_CA3P1	—	AH25	NVCC_DRAM	DDR	ALT0	LPDDR2_CA3_P1	Output	0
DRAM_CA4P0	—	W28	NVCC_DRAM	DDR	ALT0	LPDDR2_CA4_P0	Output	0
DRAM_CA4P1	—	AJ25	NVCC_DRAM	DDR	ALT0	LPDDR2_CA4_P1	Output	0
DRAM_CA5P0	—	AC29	NVCC_DRAM	DDR	ALT0	LPDDR2_CA5_P0	Output	0
DRAM_CA5P1	—	AJ20	NVCC_DRAM	DDR	ALT0	LPDDR2_CA5_P1	Output	0
DRAM_CA6P0	—	AD29	NVCC_DRAM	DDR	ALT0	LPDDR2_CA6_P0	Output	0
DRAM_CA6P1	—	AH20	NVCC_DRAM	DDR	ALT0	LPDDR2_CA6_P1	Output	0
DRAM_CA7P0	—	AD28	NVCC_DRAM	DDR	ALT0	LPDDR2_CA7_P0	Output	0
DRAM_CA7P1	—	AH19	NVCC_DRAM	DDR	ALT0	LPDDR2_CA7_P1	Output	0
DRAM_CA8P0	—	AE28	NVCC_DRAM	DDR	ALT0	LPDDR2_CA8_P0	Output	0
DRAM_CA8P1	—	AJ18	NVCC_DRAM	DDR	ALT0	LPDDR2_CA8_P1	Output	0
DRAM_CA9P0	—	AF29	NVCC_DRAM	DDR	ALT0	LPDDR2_CA9_P0	Output	0
DRAM_CA9P1	—	AH17	NVCC_DRAM	DDR	ALT0	LPDDR2_CA9_P1	Output	0
DRAM_CKE0P0	AA29	AA29	NVCC_DRAM	DDR	ALT0	LPDDR2_CKE0_P0	Output	Bottom side signals: DRAM_CKE0P0, DRAM_CKE0P1, DRAM_CKE1P0 & DRAM_1CKE1P0 must connect to ground through a 10 kohm resistor.
DRAM_CKE0P1	AH23	AH23	NVCC_DRAM	DDR	ALT0	LPDDR2_CKE0_P1	Output	
DRAM_CKE1P0	Y29	Y29	NVCC_DRAM	DDR	ALT0	LPDDR2_CKE1_P0	Output	
DRAM_CKE1P1	AJ23	AJ23	NVCC_DRAM	DDR	ALT0	LPDDR2_CKE1_P1	Output	
DRAM_CLKP0	—	AB28	NVCC_DRAM	DDRCLK	ALT0	LPDDR2_CK_P0	Input	Hi-Z
DRAM_CLKP0_B	—	AB29	NVCC_DRAM	—	—	LPDDR2_CK_P0_B	—	—
DRAM_CLKP1	—	AJ21	NVCC_DRAM	DDRCLK	ALT0	LPDDR2_CK_P1	Input	Hi-Z

Table 85. 12 x 12 mm Functional Contact Assignments (continued)

Ball Name	PoP Bottom Ball	PoP Top Ball	Power Group	Ball Type	Out of Reset Condition[1]			
					Default Mode	Default Function	Input/ Output	Value[2]
ENET_TXD0	AD23	—	NVCC_ENET	GPIO	ALT5	GPIO1_IO30	Input	PU (100k)
ENET_TXD1	AG21	—	NVCC_ENET	GPIO	ALT5	GPIO1_IO29	Input	PU (100k)
GPIO_0	AE2	—	NVCC_GPIO	GPIO	ALT5	GPIO1_IO00	Input	PD (100k)
GPIO_1	AA6	—	NVCC_GPIO	GPIO	ALT5	GPIO1_IO01	Input	PU (100k)
GPIO_2	W6	—	NVCC_GPIO	GPIO	ALT5	GPIO1_IO02	Input	PU (100k)
GPIO_3	AE1	—	NVCC_GPIO	GPIO	ALT5	GPIO1_IO03	Input	PU (100k)
GPIO_4	Y6	—	NVCC_GPIO	GPIO	ALT5	GPIO1_IO04	Input	PU (100k)
GPIO_5	AB3	—	NVCC_GPIO	GPIO	ALT5	GPIO1_IO05	Input	PU (100k)
GPIO_6	AC6	—	NVCC_GPIO	GPIO	ALT5	GPIO1_IO06	Input	PU (100k)
GPIO_7	AC1	—	NVCC_GPIO	GPIO	ALT5	GPIO1_IO07	Input	PU (100k)
GPIO_8	V7	—	NVCC_GPIO	GPIO	ALT5	GPIO1_IO08	Input	PU (100k)
GPIO_9	AD2	—	NVCC_GPIO	GPIO	ALT5	GPIO1_IO09	Input	PU (100k)
GPIO_16	AB2	—	NVCC_GPIO	GPIO	ALT5	GPIO7_IO11	Input	PU (100k)
GPIO_17	AC2	—	NVCC_GPIO	GPIO	ALT5	GPIO7_IO12	Input	PU (100k)
GPIO_18	AA3	—	NVCC_GPIO	GPIO	ALT5	GPIO7_IO13	Input	PU (100k)
GPIO_19	AB1	—	NVCC_GPIO	GPIO	ALT5	GPIO4_IO05	Input	PU (100k)
HDMI_CLKM	L1	—	HDMI_VPH	—	—	HDMI_TX_CLK_N	—	—
HDMI_CLKP	L2	—	HDMI_VPH	—	—	HDMI_TX_CLK_P	—	—
HDMI_D0M	M1	—	HDMI_VPH	—	—	HDMI_TX_DATA0_N	—	—
HDMI_D0P	M2	—	HDMI_VPH	—	—	HDMI_TX_DATA0_P	—	—
HDMI_D1M	N1	—	HDMI_VPH	—	—	HDMI_TX_DATA1_N	—	—
HDMI_D1P	N2	—	HDMI_VPH	—	—	HDMI_TX_DATA1_P	—	—
HDMI_D2M	P1	—	HDMI_VPH	—	—	HDMI_TX_DATA2_N	—	—
HDMI_D2P	P2	—	HDMI_VPH	—	—	HDMI_TX_DATA2_P	—	—
HDMI_HPD	R1	—	HDMI_VPH	—	—	HDMI_TX_HPD	—	—
JTAG_MOD	F3	—	NVCC_JTAG	GPIO	ALT0	JTAG_MODE	Input	PU (100k)
JTAG_TCK	B1	—	NVCC_JTAG	GPIO	ALT0	JTAG_TCK	Input	PU (47k)
JTAG_TDI	L7	—	NVCC_JTAG	GPIO	ALT0	JTAG_TDI	Input	PU (47k)
JTAG_TDO	B2	—	NVCC_JTAG	GPIO	ALT0	JTAG_TDO	Output	Keeper
JTAG_TMS	A2	—	NVCC_JTAG	GPIO	ALT0	JTAG_TMS	Input	PU (47k)
JTAG_TRSTB	K3	—	NVCC_JTAG	GPIO	ALT0	JTAG_TRST_B	Input	PU (47k)
KEY_COL0	AB6	—	NVCC_GPIO	GPIO	ALT5	GPIO4_IO06	Input	PU (100k)
KEY_COL1	Y7	—	NVCC_GPIO	GPIO	ALT5	GPIO4_IO08	Input	PU (100k)
KEY_COL2	AD7	—	NVCC_GPIO	GPIO	ALT5	GPIO4_IO10	Input	PU (100k)
KEY_COL3	AD6	—	NVCC_GPIO	GPIO	ALT5	GPIO4_IO12	Input	PU (100k)
KEY_COL4	AF1	—	NVCC_GPIO	GPIO	ALT5	GPIO4_IO14	Input	PU (100k)
KEY_ROW0	AB7	—	NVCC_GPIO	GPIO	ALT5	GPIO4_IO07	Input	PU (100k)
KEY_ROW1	AD3	—	NVCC_GPIO	GPIO	ALT5	GPIO4_IO09	Input	PU (100k)
KEY_ROW2	AF2	—	NVCC_GPIO	GPIO	ALT5	GPIO4_IO11	Input	PU (100k)
KEY_ROW3	AE3	—	NVCC_GPIO	GPIO	ALT5	GPIO4_IO13	Input	PU (100k)

Table 87. PoP 12 x 12 mm, 0.4 mm Pitch Top Ball Map (continued)

AG	AF	AE	AD	AC	AB	AA
DRAM_D10P0	DRAM_D14P0	DRAM_D12P0	DRAM_DQS1P0_B	POP_VDDQ	DRAM_DM0P0	DRAM_DQS0P0
DRAM_D13P0	POP_VDDQ	GND	DRAM_DQS1P0	DRAM_DM1P0	GND	DRAM_DQS0P0_B
POP_VDD2__8	GND	DRAM_CA8P0	DRAM_CA7P0	POP_VDDCA	DRAM_CLKP0	GND
POP_ZQP0	DRAM_CA9P0	POP_VDDCA	DRAM_CA6P0	DRAM_CA5P0	DRAM_CLKP0_B	DRAM_CKE0P0

Table 88. PoP 12 x 12 mm, 0.4 mm Pitch Bottom Ball Map (continued)

AJ	AH	AG	AF	AE	AD	AC	AB
GND	LVDS0_TX1_P	LVDS0_TX0_P	KEY_COL4	GPIO_3	CSI0_PIXCLK	GPIO_7	GPIO_19
GND	LVDS0_TX1_N	LVDS0_TX0_N	KEY_ROW2	GPIO_0	GPIO_9	GPIO_17	GPIO_16
LVDS0_TX2_P	LVDS0_TX2_N	POP_VDD1__6	POP_VDDQ	KEY_ROW3	KEY_ROW1	POP_VDDQ	GPIO_5
LVDS0_CLK_P	LVDS0_CLK_N	POP_VDD2__6					
LVDS0_TX3_P	LVDS0_TX3_N	GND					
LVDS1_TX0_N	LVDS1_TX0_P	POP_VDDQ			KEY_COL3	GPIO_6	KEY_COL0
LVDS1_TX1_P	LVDS1_TX1_N	GND			KEY_COL2	KEY_ROW4	KEY_ROW0
LVDS1_CLK_N	LVDS1_CLK_P	GND			NVCC_DRAM	NVCC_DRAM	
LVDS1_TX2_N	LVDS1_TX2_P	POP_VDDQ			NVCC_DRAM	NVCC_DRAM	
LVDS1_TX3_N	LVDS1_TX3_P	DRAM_VREF			NVCC_DRAM	NVCC_DRAM	
GND	GND	GND			NVCC_DRAM	NVCC_DRAM	
GND	GND	POP_VDDQ			NVCC_DRAM	NVCC_DRAM	
GND	GND	GND			NVCC_DRAM	NVCC_DRAM	
GND	GND	NVCC_LVDS2P5			NVCC_DRAM	NVCC_DRAM	
GND	GND	POP_VDD2__7			NVCC_DRAM	NVCC_DRAM	
GND	GND	POP_VDD1__7			NVCC_DRAM	NVCC_DRAM	
GND	GND	POP_ZQP1			NVCC_DRAM	NVCC_DRAM	
GND	GND	NVCC_LVDS2P5			NVCC_DRAM	NVCC_DRAM	
ZQPAD	GND	POP_VDDCA			NVCC_DRAM	NVCC_DRAM	
GND	ENET_RXD1	NVCC_LVDS2P5			NVCC_DRAM	NVCC_DRAM	
ENET_MDC	ENET_REF_CLK	ENET_TXD1			NVCC_DRAM	NVCC_DRAM	
ENET_MDIO	ENET_RXD0	POP_VDDCA			ENET_RX_ER	NVCC_DRAM	
DRAM_CKE1P1	DRAM_CKE0P1	ENET_CRS_DV			ENET_TXD0	NVCC_DRAM	NVCC_DRAM
DISP0_DAT23	DISP0_DAT18	ENET_TX_EN			DISP0_DAT20	DISP0_DAT21	DISP0_DAT16
DISP0_DAT13	DISP0_DAT15	POP_VDDCA					
DISP0_DAT8	DISP0_DAT10	POP_VDD1__8					
DISP0_DAT11	DISP0_DAT5	POP_VDD2__8	POP_ZQP0	POP_VDDCA	DISP0_DAT1	POP_VDDCA	DISP0_DAT2
DISP0_DAT14	DISP0_DAT17	DISP0_DAT9	DISP0_DAT12	DISP0_DAT7	DI0_PIN15	EIM_DA14	EIM_DA8
GND	DISP0_DAT0	EIM_WAIT	DI0_DISP_CLK	EIM_DA11	DI0_PIN2	EIM_DA9	EIM_DA3

7 Revision History

Table 89 provides a revision history for the i.MX 6Dual Pop and i.MX 6Quad Pop data sheet.

Table 89. Data Sheet Document Revision History

Rev. Number	Date	Substantive Change(s)
1	09/2017	Rev. 1 changes include the following: • Changed throughout: – Changed terminology from “floating” to “not connected”. • Section 1, “Introduction” on page 1: Changed ARM Cortex-A9 operating speed from “up to 1 GHz” to “up to 800 MHz.” • Figure 1, "Part Number Nomenclature—i.MX 6Dual PoP and 6Quad PoP," on page 4: – Removed from Temperature block: Automotive temperature row. • Table 2, “i.MX 6Dual/6Quad Modules List,” on page 10: – Added bullet to uSDHC row: “Conforms to the SD Host Controller Standard Specification v3.0” • Table 4, “Absolute Maximum Ratings,” on page 20: Extensive changes: – Separated rows Core supply voltage by LDO enable/bypass — Maximum LDO enabled value change from 1.5 to 1.6 V — Maximum LDO bypass value added, 1.4 V – Renamed Internal supply voltages to Core supply output voltage (LDO enabled) and changed maximum value from 1.3 to 1.4V. Added symbol NVCC_PLL_OUT. – Reordered VDD_HIGH_IN row and changed maximum value from 3.6 to 3.7V. – DDR I/O supply voltage row changes: — Changed Symbols from “Supplies denoted as I/O supply” to: “NVCC_DRAM” — Added footnote to maximum value regarding “The absolute maximum voltage includes an allowance for 400 mV …”. – Change row GPIO I/O supply voltage: — Changed Symbols from “Supplies denoted as I/O supply” to: multiple values — Maximum value change from 3.6 to 3.7 V – Added rows: HDMI, PCIe, and SATA PHY high (VPH) and low (VP) supply voltage and values – Change row “LVDS I/O supply voltage” to “LVDS and MIPI I/O supply voltage (2.5V supply)” — Changed Symbols from “Supplies denoted as I/O supply” to: multiple values — Maximum value change from 2.8 to 2.85 V – Added row: PCI PHY supply voltage and values – Added row: RGMII I/O supply voltage and values – Added row: SNVS IN supply voltage and values – Added row: USB_OTG_CHD_B and values – Changed row: “Input voltage on USB_OTG_DP…” to “USB I/O supply voltage” — Changed Symbols from “USB_DP/USB_DN” to: multiple values — Maximum value change from 3.63 to 3.73 V – Separated row: “Input/output voltage range” by non-DDR/DDR pins, and added Vin/Vout to row name — Maximum value added for Vin/Vout DDR pins: OVDD + 0.4 V and added footnote – Separated and renamed row: “ESD damage immunity” by HBM/CDM and changed Symbol names — Maximum value added for Vin/Vout DDR pins: OVDD + 0.4 V and added footnote *(Revision History table continues on next page.)*