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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (1)
SATA	SATA 3Gbps (1)
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	569-LFBGA
Supplier Device Package	569-MAPBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6d7czk08ae

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
CSI	MIPI CSI-2 Interface	Multimedia Peripherals	The CSI IP provides MIPI CSI-2 standard camera interface port. The CSI-2 interface supports up to 1 Gbps for up to 3 data lanes and up to 800 Mbps for 4 data lanes.
CSU	Central Security Unit	Security	The Central Security Unit (CSU) is responsible for setting comprehensive security policy within the i.MX 6Dual/6Quad platform. The Security Control Registers (SCR) of the CSU are set during boot time by the HAB and are locked to prevent further writing.
CTI-0 CTI-1 CTI-2 CTI-3 CTI-4	Cross Trigger Interfaces	Debug / Trace	Cross Trigger Interfaces allows cross-triggering based on inputs from masters attached to CTIs. The CTI module is internal to the Cortex-A9 Core Platform.
CTM	Cross Trigger Matrix	Debug / Trace	Cross Trigger Matrix IP is used to route triggering events between CTIs. The CTM module is internal to the Cortex-A9 Core Platform.
DAP	Debug Access Port	System Control Peripherals	The DAP provides real-time access for the debugger without halting the core to: • System memory and peripheral registers • All debug configuration registers The DAP also provides debugger access to JTAG scan chains. The DAP module is internal to the Cortex-A9 Core Platform.
DCIC-0 DCIC-1	Display Content Integrity Checker	Automotive IP	The DCIC provides integrity check on portion(s) of the display. Each i.MX 6Dual/6Quad processor has two such modules, one for each IPU.
DSI	MIPI DSI interface	Multimedia Peripherals	The MIPI DSI IP provides DSI standard display port interface. The DSI interface support 80 Mbps to 1 Gbps speed per data lane.
eCSPI1-5	Configurable SPI	Connectivity Peripherals	Full-duplex enhanced Synchronous Serial Interface. It is configurable to support Master/Slave modes, four chip selects to support multiple peripherals.
ENET	Ethernet Controller	Connectivity Peripherals	The Ethernet Media Access Controller (MAC) is designed to support 10/100/1000 Mbps Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The i.MX 6Dual/6Quad processors also consist of hardware assist for IEEE 1588 standard. For details, see the ENET chapter of the i.MX 6Dual/6Quad reference manual (IMX6DQRM). **Note:** The theoretical maximum performance of 1 Gbps ENET is limited to 470 Mbps (total for Tx and Rx) due to internal bus throughput limitations. The actual measured performance in optimized environment is up to 400 Mbps. For details, see the ERR004512 erratum in the i.MX 6Dual/6Quad errata document (IMX6DQCE).
EPIT-1 EPIT-2	Enhanced Periodic Interrupt Timer	Timer Peripherals	Each EPIT is a 32-bit “set and forget” timer that starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler for division of input clock frequency to get the required time setting for the interrupts to occur, and counter value can be programmed on the fly.

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
TEMPMON	Temperature Monitor	System Control Peripherals	The temperature monitor/sensor IP module for detecting high temperature conditions. The temperature read out does not reflect case or ambient temperature. It reflects the temperature in proximity of the sensor location on the die. Temperature distribution may not be uniformly distributed; therefore, the read out value may not be the reflection of the temperature value for the entire die.
TZASC	Trust-Zone Address Space Controller	Security	The TZASC (TZC-380 by ARM) provides security address region control functions required for intended application. It is used on the path to the DRAM controller.
UART-1 UART-2 UART-3 UART-4 UART-5	UART Interface	Connectivity Peripherals	Each of the UARTv2 modules support the following serial data transmit/receive protocols and configurations: • 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none) • Programmable baud rates up to 5 MHz • 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud • IrDA 1.0 support (up to SIR speed of 115200 bps) • Option to operate as 8-pins full UART, DCE, or DTE
USBOH3A	USB 2.0 High Speed OTG and 3x HS Hosts	Connectivity Peripherals	USBOH3 contains: • One high-speed OTG module with integrated HS USB PHY • One high-speed Host module with integrated HS USB PHY • Two identical high-speed Host modules connected to HSIC USB ports.

4.1.3 Operating Ranges

Table 6 provides the operating ranges of the i.MX 6Dual/6Quad processors.

Table 6. Operating Ranges

Parameter Description	Symbol	Min	Typ	Max[1]	Unit	Comment[2]
Run mode: LDO enabled	VDD_ARM_IN VDD_ARM23_IN[3]	1.275[4]	—	1.5	V	LDO Output Set Point (VDD_ARM_CAP[5]) of 1.150 V minimum for operation up to 792 MHz.
		1.05[4]	—	1.5	V	LDO Output Set Point (VDD_ARM_CAP) of 0.925 V minimum for operation up to 396 MHz.
	VDD_SOC_IN[6]	1.350[4]	—	1.5	V	264 MHz < VPU ≤ 352 MHz; VDDSOC and VDDPU LDO outputs (VDD_SOC_CAP and VDD_PU_CAP) require 1.225 V minimum.
		1.275[4,7]	—	1.5	V	VPU ≤ 264 MHz; VDDSOC and VDDPU LDO outputs (VDD_SOC_CAP and VDD_PU_CAP) require 1.15 V minimum.
Run mode: LDO bypassed[8]	VDD_ARM_IN VDD_ARM23_IN[3]	1.150	—	1.3	V	LDO bypassed for operation up to 792 MHz.
		0.925	—	1.3	V	LDO bypassed for operation up to 396 MHz.
	VDD_SOC_IN	1.225	—	1.3	V	264 MHz < VPU ≤ 352 MHz.
		1.15	—	1.3	V	VPU ≤ 264 MHz.
Standby/DSM Mode	VDD_ARM_IN VDD_ARM23_IN[3]	0.9	—	1.3	V	See Table 9, “Stop Mode Current and Power Consumption,” on page 27.
	VDD_SOC_IN	0.9	—	1.3	V	
VDD_HIGH internal Regulator	VDD_HIGH_IN[9]	2.8	—	3.3	V	Must match the range of voltages that the rechargeable backup battery supports.
Backup battery supply range	VDD_SNVS_IN[9]	2.8	—	3.3	V	Should be supplied from the same supply as VDD_HIGH_IN, if the system does not require keeping real time and other data on OFF state.
USB supply voltages	USB_OTG_VBUS	4.4	—	5.25	V	—
	USB_H1_VBUS	4.4	—	5.25	V	—
DDR I/O supply	NVCC_DRAM	1.14	1.2	1.3	V	LPDDR2
Supply for RGMII I/O power group[10]	NVCC_RGMII	1.15	—	2.625	V	• 1.15 V – 1.30 V in HSIC 1.2 V mode • 1.43 V – 1.58 V in RGMII 1.5 V mode • 1.70 V – 1.90 V in RGMII 1.8 V mode • 2.25 V – 2.625 V in RGMII 2.5 V mode

  - No external component required
  - Starts up quicker than 32 kHz crystal oscillator
- External crystal oscillator with on-chip support circuit
  - At power up, an internal ring oscillator is used. After crystal oscillator is stable, the clock circuit switches over to the crystal oscillator automatically.
  - Higher accuracy than ring oscillator.
  - If no external crystal is present, then the ring oscillator is used.

The decision to choose a clock source should be based on real-time clock use and precision timeout.

4.1.5 Maximum Measured Supply Currents

Power consumption is highly dependent on the application. Estimating the maximum supply currents required for power supply design is difficult because the use case that requires maximum supply current is not a realistic use case.

To help illustrate the effect of the application on power consumption, data was collected while running industry standard benchmarks that are designed to be compute and graphic intensive. The results provided are intended to be used as guidelines for power supply design.

Description of test conditions:

- The Power Virus data shown in Table 8 represent a use case designed specifically to show the maximum current consumption possible for the ARM core complex. All cores are running at the defined maximum frequency and are limited to L1 cache accesses only to ensure no pipeline stalls. Although a valid condition, it would have a very limited, if any, practical use case, and be limited to an extremely low duty cycle unless the intention was to specifically cause the worst case power consumption.
- EEMBC CoreMark: Benchmark designed specifically for the purpose of measuring the performance of a CPU core. More information available at www.eembc.org/coremark. Note that this benchmark is designed as a core performance benchmark, not a power benchmark. This use case is provided as an example of power consumption that would be typical in a computationally-intensive application rather than the Power Virus.
- 3DMark Mobile 2011: Suite of benchmarks designed for the purpose of measuring graphics and overall system performance. More information available at www.rightware.com/benchmarks. Note that this benchmark is designed as a graphics performance benchmark, not a power benchmark. This use case is provided as an example of power consumption that would be typical in a very graphics-intensive application.
- Devices used for the tests were from the high current end of the expected process variation.

The NXP power management IC, MMPF0100xxxx, which is targeted for the i.MX 6 series processor family, supports the power consumption shown in Table 8, however a robust thermal design is required for the increased system power dissipation.

See the *i.MX 6Dual/6Quad Power Consumption Measurement Application Note* (AN4509) for more details on typical power consumption under various use case definitions.

4.6.1 XTALI and RTC_XTALI (Clock Inputs) DC Parameters

Table 20 shows the DC parameters for the clock inputs.

Table 20. XTALI and RTC_XTALI DC Parameters

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
XTALI high-level DC input voltage	Vih	—	0.8 x NVCC_PLL_OUT	—	NVCC_PLL_ OUT	V
XTALI low-level DC input voltage	Vil	—	0	—	0.2	V
RTC_XTALI high-level DC input voltage	Vih	—	0.8	—	1.1 (See note 1)	V
RTC_XTALI low-level DC input voltage	Vil	—	0	—	0.2	V
Input capacitance	C_{IN}	Simulated data	—	5	—	pF
XTALI input leakage current at startup	$I_{XTALI\_STARTUP}$	Power-on startup for 0.15 msec with a driven 32 KHz RTC clock @ 1.1 V. [2]	—	—	600	µA
DC input current	I_{XTALI_DC}	—	—	—	2.5	µA

[1] This voltage specification must not be exceeded and, as such, is an absolute maximum specification.

[2] This current draw is present even if an external clock source directly drives XTALI.

NOTE

The Vil and Vih specifications only apply when an external clock source is used. If a crystal is used, Vil and Vih do not apply.

4.6.2 General Purpose I/O (GPIO) DC Parameters

Table 21 shows DC parameters for GPIO pads. The parameters in Table 21 are guaranteed per the operating ranges in Table 6, unless otherwise noted.

Table 21. GPIO I/O DC Parameters

Parameter	Symbol	Test Conditions	Min	Max	Unit
High-level output voltage[1]	Voh	Ioh = -0.1 mA (DSE[2] = 001, 010) Ioh = -1 mA (DSE = 011, 100, 101, 110, 111)	OVDD – 0.15	—	V
Low-level output voltage[1]	Vol	Iol = 0.1 mA (DSE[2] = 001, 010) Iol = 1mA (DSE = 011, 100, 101, 110, 111)	—	0.15	V
High-Level DC input voltage[1, 3]	Vih	—	0.7 × OVDD	OVDD	V
Low-Level DC input voltage[1, 3]	Vil	—	0	0.3 × OVDD	V
Input Hysteresis	Vhys	OVDD = 1.8 V OVDD = 3.3 V	0.25	—	V
Schmitt trigger VT+[3, 4]	VT+	—	0.5 × OVDD	—	V
Schmitt trigger VT–[3, 4]	VT–	—	—	0.5 × OVDD	V

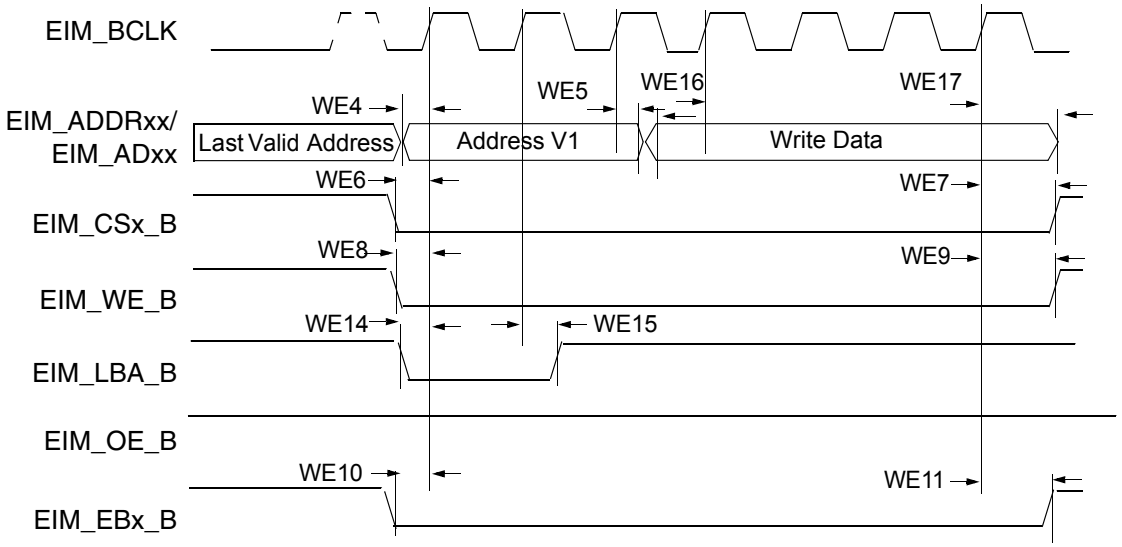

Figure 14. Muxed Address/Data (A/D) Mode, Synchronous Write Access, WSC=6,ADVA=0, ADVN=1, and ADH=1

NOTE

In 32-bit muxed address/data (A/D) mode the 16 MSBs are driven on the data bus.

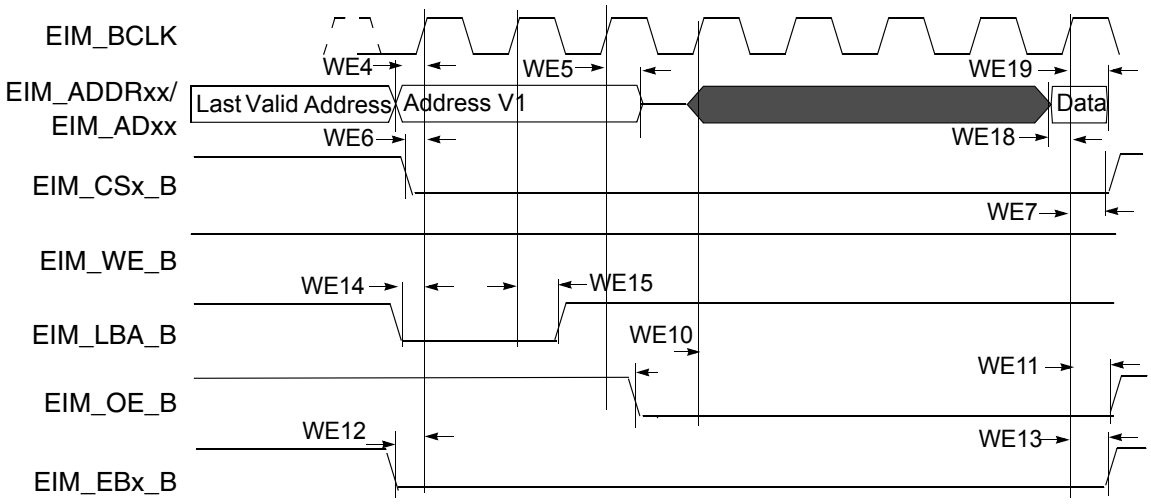

Figure 15. 16-Bit Muxed A/D Mode, Synchronous Read Access, WSC=7, RADVN=1, ADH=1, OEA=0

4.12.3 Enhanced Serial Audio Interface (ESAI) Timing Parameters

The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. Table 43 shows the interface timing values. The number field in the table refers to timing signals found in Figure 35 and Figure 36.

Table 43. Enhanced Serial Audio Interface (ESAI) Timing

ID	Parameter[1,2]	Symbol	Expression[2]	Min	Max	Condition[3]	Unit
62	Clock cycle[4]	t_{SSICC}	$4 \times T_C$ $4 \times T_C$	30.0 30.0	— —	i ck i ck	ns
63	Clock high period: • For internal clock • For external clock	— —	$2 \times T_C - 9.0$ $2 \times T_C$	6 15	— —	— —	ns
64	Clock low period: • For internal clock • For external clock	— —	$2 \times T_C - 9.0$ $2 \times T_C$	6 15	— —	— —	ns
65	ESAI_RX_CLK rising edge to ESAI_RX_FS out (bl) high	— —	— —	— —	19.0 7.0	x ck i ck a	ns
66	ESAI_RX_CLK rising edge to ESAI_RX_FS out (bl) low	— —	— —	— —	19.0 7.0	x ck i ck a	ns
67	ESAI_RX_CLK rising edge to ESAI_RX_FS out (wr) high[5]	— —	— —	— —	19.0 9.0	x ck i ck a	ns
68	ESAI_RX_CLK rising edge to ESAI_RX_FS out (wr) low[5]	— —	— —	— —	19.0 9.0	x ck i ck a	ns
69	ESAI_RX_CLK rising edge to ESAI_RX_FS out (wl) high	— —	— —	— —	19.0 6.0	x ck i ck a	ns
70	ESAI_RX_CLK rising edge to ESAI_RX_FSout (wl) low	— —	— —	— —	17.0 7.0	x ck i ck a	ns
71	Data in setup time before ESAI_RX_CLK (serial clock in synchronous mode) falling edge	— —	— —	12.0 19.0	— —	x ck i ck	ns
72	Data in hold time after ESAI_RX_CLK falling edge	— —	— —	3.5 9.0	— —	x ck i ck	ns
73	ESAI_RX_FS input (bl, wr) high before ESAI_RX_CLK falling edge[5]	— —	— —	2.0 19.0	— —	x ck i ck a	ns
74	ESAI_RX_FS input (wl) high before ESAI_RX_CLK falling edge	— —	— —	2.0 19.0	— —	x ck i ck a	ns
75	ESAI_RX_FS input hold time after ESAI_RX_CLK falling edge	— —	— —	2.5 8.5	— —	x ck i ck a	ns
78	ESAI_TX_CLK rising edge to ESAI_TX_FS out (bl) high	— —	— —	— —	19.0 8.0	x ck i ck	ns
79	ESAI_TX_CLK rising edge to ESAI_TX_FS out (bl) low	— —	— —	— —	20.0 10.0	x ck i ck	ns
80	ESAI_TX_CLK rising edge to ESAI_TX_FS out (wr) high[5]	— —	— —	— —	20.0 10.0	x ck i ck	ns

4.12.4.3 SDR50/SDR104 AC Timing

Figure 39 depicts the timing of SDR50/SDR104, and Table 46 lists the SDR50/SDR104 timing characteristics.

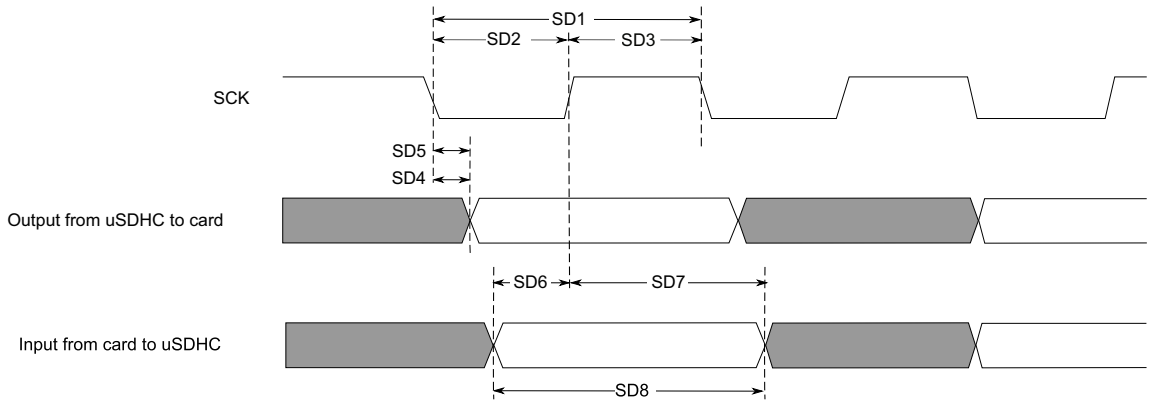

Figure 39. SDR50/SDR104 Timing

Table 46. SDR50/SDR104 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency Period	t_{CLK}	4.8	—	ns
SD2	Clock Low Time	t_{CL}	$0.46 \times t_{CLK}$	$0.54 \times t_{CLK}$	ns
SD3	Clock High Time	t_{CH}	$0.46 \times t_{CLK}$	$0.54 \times t_{CLK}$	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR50 (Reference to SDx_CLK)					
SD4	uSDHC Output Delay	t_{OD}	–3	1	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR104 (Reference to SDx_CLK)					
SD5	uSDHC Output Delay	t_{OD}	–1.6	0.74	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR50 (Reference to SDx_CLK)					
SD6	uSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD7	uSDHC Input Hold Time	t_{IH}	1.5	—	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR104 (Reference to SDx_CLK)[1]					
SD8	Card Output Data Window	t_{ODW}	$0.5 \times t_{CLK}$	—	ns

[1]Data window in SDR100 mode is variable.

4.12.4.4 Bus Operation Condition for 3.3 V and 1.8 V Signaling

Signalling level of SD/eMMC4.3 and eMMC4.4/4.41 modes is 3.3 V. Signalling level of SDR104/SDR50 mode is 1.8 V. The DC parameters for the NVCC_SD1, NVCC_SD2, and NVCC_SD3 supplies are identical to those shown in Table 21, “GPIO I/O DC Parameters,” on page 38.

4.12.5 Ethernet Controller (ENET) AC Electrical Specifications

4.12.5.1 ENET MII Mode Timing

This subsection describes MII receive, transmit, asynchronous inputs, and serial management signal timings.

4.12.5.1.1 MII Receive Signal Timing (ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER, and ENET_RX_CLK)

The receiver functions correctly up to an ENET_RX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. Additionally, the processor clock frequency must exceed twice the ENET_RX_CLK frequency.

Figure 40 shows MII receive signal timings. Table 47 describes the timing parameters (M1–M4) shown in the figure.

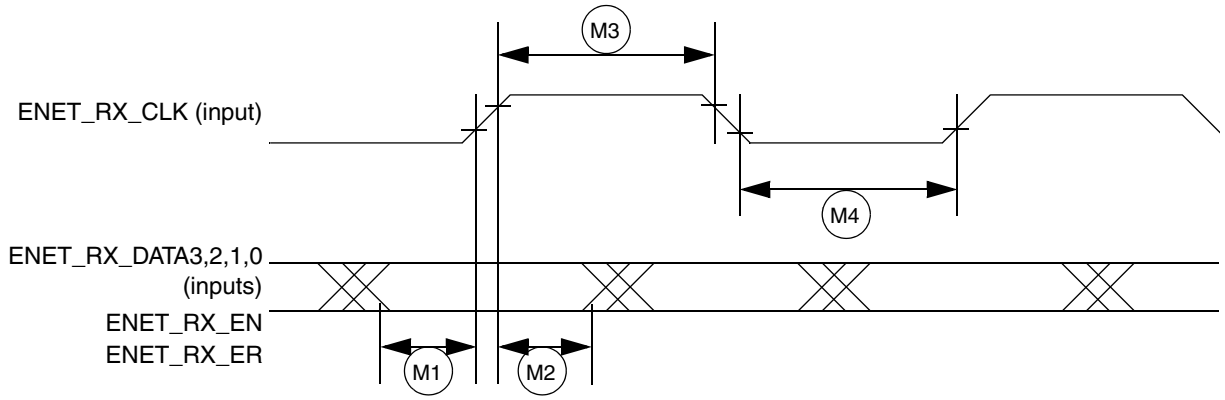

Figure 40. MII Receive Signal Timing Diagram

Table 47. MII Receive Signal Timing

ID	Characteristic[1]	Min	Max	Unit
M1	ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER to ENET_RX_CLK setup	5	—	ns
M2	ENET_RX_CLK to ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER hold	5	—	ns
M3	ENET_RX_CLK pulse width high	35%	65%	ENET_RX_CLK period
M4	ENET_RX_CLK pulse width low	35%	65%	ENET_RX_CLK period

[1] ENET_RX_EN, ENET_RX_CLK, and ENET0_RXD0 have the same timing in 10 Mbps 7-wire interface mode.

Table 54. Switching Characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_F	Differential output signal fall time	20–80% RL = 50 Ω See Figure 55.	75	—	0.4 UI	ps
—	Differential signal overshoot	Referred to 2x V_{SWING}	—	—	15	%
—	Differential signal undershoot	Referred to 2x V_{SWING}	—	—	25	%
Data and Control Interface Specifications						
$t_{Power-up}$[2]	HDMI 3D Tx PHY power-up time	From power-down to HSI_TX_READY assertion	—	—	3.35	ms

1 Relative to ideal recovery clock, as specified in the HDMI specification, version 1.4a, section 4.2.3.

2 For information about latencies and associated timings, see Section 4.12.7.1, "Latencies and Timing Information."

4.12.9 I²C Module Timing Parameters

This section describes the timing parameters of the I²C module. Figure 56 depicts the timing of I²C module, and Table 55 lists the I²C module timing characteristics.

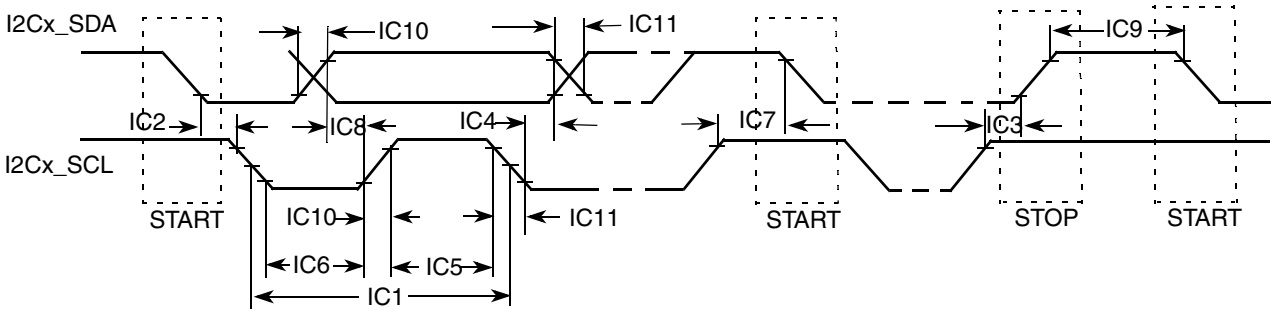

Figure 56. I²C Bus Timing

Table 55. I²C Module Timing Parameters

ID	Parameter	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
IC1	I2Cx_SCL cycle time	10	—	2.5	—	µs
IC2	Hold time (repeated) START condition	4.0	—	0.6	—	µs
IC3	Set-up time for STOP condition	4.0	—	0.6	—	µs
IC4	Data hold time	0[1]	3.45[2]	0[1]	0.9[2]	µs
IC5	HIGH Period of I2Cx_SCL Clock	4.0	—	0.6	—	µs
IC6	LOW Period of the I2Cx_SCL Clock	4.7	—	1.3	—	µs
IC7	Set-up time for a repeated START condition	4.7	—	0.6	—	µs
IC8	Data set-up time	250	—	100[3]	—	ns

There are special physical outputs to provide synchronous controls:

- The ipp_disp_clk is a dedicated base synchronous signal that is used to generate a base display (component, pixel) clock for a display.
- The ipp_pin_1– ipp_pin_7 are general purpose synchronous pins, that can be used to provide HSYNC, VSYNC, DRDY or any else independent signal to a display.

The IPU has a system of internal binding counters for internal events (such as, HSYNC/VSYNC) calculation. The internal event (local start point) is synchronized with internal DI_CLK. A suitable control starts from the local start point with predefined UP and DOWN values to calculate control's changing points with half DI_CLK resolution. A full description of the counter system can be found in the IPU chapter of the i.MX 6Dual/6Quad reference manual (IMX6DQRM).

4.12.10.5.2 Asynchronous Controls

The asynchronous control is a data-oriented signal that changes its value with an output data according to additional internal flags coming with the data.

There are special physical outputs to provide asynchronous controls, as follows:

- The ipp_d0_cs and ipp_d1_cs pins are dedicated to provide chip select signals to two displays.
- The ipp_pin_11– ipp_pin_17 are general purpose asynchronous pins, that can be used to provide WR. RD, RS or any other data-oriented signal to display.

NOTE

The IPU has independent signal generators for asynchronous signals toggling. When a DI decides to put a new asynchronous data on the bus, a new internal start (local start point) is generated. The signal generators calculate predefined UP and DOWN values to change pins states with half DI_CLK resolution.

4.12.10.6 Synchronous Interfaces to Standard Active Matrix TFT LCD Panels

4.12.10.6.1 IPU Display Operating Signals

The IPU uses four control signals and data to operate a standard synchronous interface:

- IPP_DISP_CLK—Clock to display
- HSYNC—Horizontal synchronization
- VSYNC—Vertical synchronization
- DRDY—Active data

All synchronous display controls are generated on the base of an internally generated "local start point". The synchronous display controls can be placed on time axis with DI's offset, up and down parameters. The display access can be whole number of DI clock (Tdiclk) only. The IPP_DATA can not be moved relative to the local start point. The data bus of the synchronous interface is output direction only.

Table 71. SSI Transmitter Timing with Internal Clock (continued)

ID	Parameter	Min	Max	Unit
Synchronous Internal Clock Operation				
SS42	AUDx_RXD setup before AUDx_TXC falling	10.0	—	ns
SS43	AUDx_RXD hold after AUDx_TXC falling	0.0	—	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal AUDx_TXC/AUDx_RXC and/or the frame sync AUDx_TXFS/AUDx_RXFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- The terms, WL and BL, refer to Word Length(WL) and Bit Length(BL).
- For internal Frame Sync operation using external clock, the frame sync timing is the same as that of transmit data (for example, during AC97 mode of operation).

4.12.20.2.3 UART IrDA Mode Timing

The following subsections give the UART transmit and receive timings in IrDA mode.

UART IrDA Mode Transmitter

Figure 92 depicts the UART IrDA mode transmit timing, with 8 data bit/1 stop bit format. Table 78 lists the transmit timing characteristics.

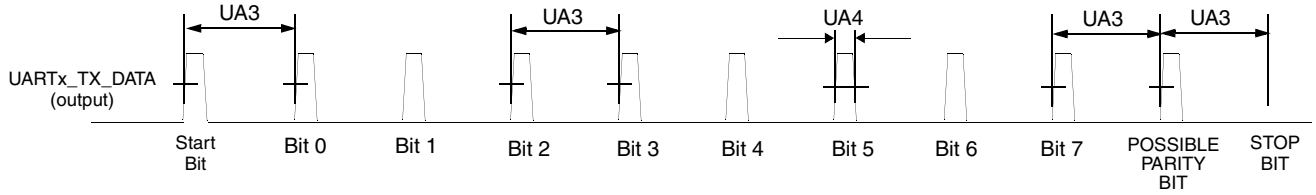

Figure 92. UART IrDA Mode Transmit Timing Diagram

Table 78. IrDA Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA3	Transmit Bit Time in IrDA mode	t_{TIRbit}	$1/F_{baud\_rate}$ [1] – T_{ref_clk} [2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—
UA4	Transmit IR Pulse Duration	$t_{TIRpulse}$	$(3/16) \times (1/F_{baud\_rate}) - T_{ref\_clk}$	$(3/16) \times (1/F_{baud\_rate}) + T_{ref\_clk}$	—

1 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

2 T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

UART IrDA Mode Receiver

Figure 93 depicts the UART IrDA mode receive timing, with 8 data bit/1 stop bit format. Table 79 lists the receive timing characteristics.

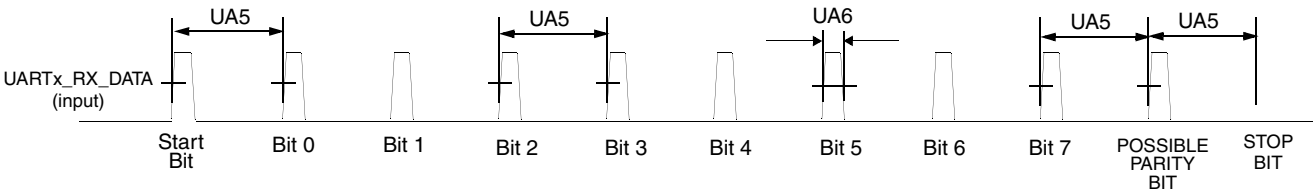

Figure 93. UART IrDA Mode Receive Timing Diagram

Table 79. IrDA Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA5	Receive Bit Time[1] in IrDA mode	t_{RIRbit}	$1/F_{baud\_rate}$ [2] – $1/(16 \times F_{baud\_rate})$	$1/F_{baud\_rate} + 1/(16 \times F_{baud\_rate})$	—
UA6	Receive IR Pulse Duration	$t_{RIRpulse}$	1.41 µs	$(5/16) \times (1/F_{baud\_rate})$	—

1 The UART receiver can tolerate $1/(16 \times F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud\_rate})$.

2 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

4.12.21 USB HSIC Timings

This section describes the electrical information of the USB HSIC port.

NOTE

HSIC is a DDR signal. The following timing specification is for both rising and falling edges.

4.12.21.1 Transmit Timing

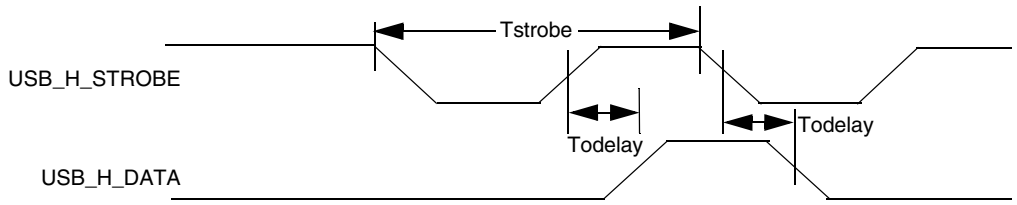

Figure 94. USB HSIC Transmit Waveform

Table 80. USB HSIC Transmit Parameters

Name	Parameter	Min	Max	Unit	Comment
Tstrobe	strobe period	4.166	4.167	ns	—
Todelay	data output delay time	550	1350	ps	Measured at 50% point
Tslew	strobe/data rising/falling time	0.7	2	V/ns	Averaged from 30% – 70% points

4.12.21.2 Receive Timing

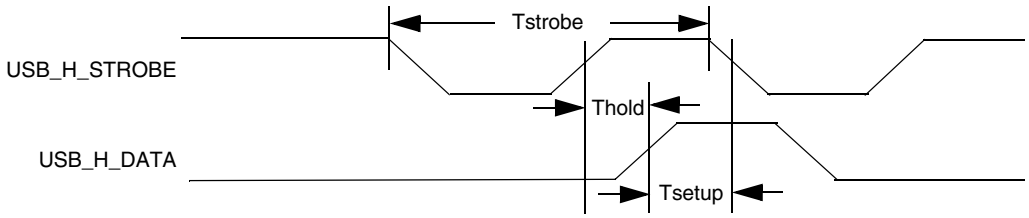

Figure 95. USB HSIC Receive Waveform

Table 81. USB HSIC Receive Parameters[1]

Name	Parameter	Min	Max	Unit	Comment
Tstrobe	strobe period	4.166	4.167	ns	—
Thold	data hold time	300	—	ps	Measured at 50% point
Tsetup	data setup time	365	—	ps	Measured at 50% point
Tslew	strobe/data rising/falling time	0.7	2	V/ns	Averaged from 30% – 70% points

[1] The timings in the table are guaranteed when:
—AC I/O voltage is between 0.9x to 1x of the I/O supply
—DDR_SEL configuration bits of the I/O are set to (10)b

4.12.22 USB PHY Parameters

This section describes the USB-OTG PHY and the USB Host port PHY parameters.

The USB PHY meets the electrical compliance requirements defined in the Universal Serial Bus Revision 2.0 OTG, USB Host with the amendments below (On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification is not applicable to Host port).

- USB ENGINEERING CHANGE NOTICE
  - Title: 5V Short Circuit Withstand Requirement Change
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- Errata for USB Revision 2.0 April 27, 2000 as of 12/7/2000
- USB ENGINEERING CHANGE NOTICE
  - Title: Pull-up/Pull-down resistors
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: Suspend Current Limit Changes
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: USB 2.0 Phase Locked SOFs
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification
  - Revision 2.0 plus errata and ecn June 4, 2010
- Battery Charging Specification (available from USB-IF)
  - Revision 1.2, December 7, 2010
  - Portable device only

Table 85. 12 x 12 mm Functional Contact Assignments (continued)

Ball Name	PoP Bottom Ball	PoP Top Ball	Power Group	Ball Type	Out of Reset Condition[1]			
					Default Mode	Default Function	Input/ Output	Value[2]
DRAM_DQS1P0_B	—	AD1	NVCC_DRAM	DDRCLK	—	DRAM_SDQS1_N	—	—
DRAM_DQS2P0	—	K2	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS2_P	Input	Hi-Z
DRAM_DQS2P0_B	—	K1	NVCC_DRAM	DDRCLK	—	DRAM_SDQS2_N	—	—
DRAM_DQS3P0	—	AH8	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS3_P	Input	Hi-Z
DRAM_DQS3P0_B	—	AJ8	NVCC_DRAM	DDRCLK	—	DRAM_SDQS3_N	—	—
DRAM_DQS0P1	—	B10	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS4_P	Input	Hi-Z
DRAM_DQS0P1_B	—	A10	NVCC_DRAM	DDRCLK	—	DRAM_SDQS4_N	—	—
DRAM_DQS1P1	—	A20	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS5_P	Input	Hi-Z
DRAM_DQS1P1_B	—	B20	NVCC_DRAM	DDRCLK	—	DRAM_SDQS5_N	—	—
DRAM_DQS2P1	—	A23	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS6_P	Input	Hi-Z
DRAM_DQS2P1_B	—	B23	NVCC_DRAM	DDRCLK	—	DRAM_SDQS6_N	—	—
DRAM_DQS3P1	—	G28	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS7_P	Input	Hi-Z
DRAM_DQS3P1_B	—	G29	NVCC_DRAM	DDRCLK	—	DRAM_SDQS7_N	—	—
DSI_CLK0M	J1	—	NVCC_MIPI	—	—	DSI_CLK_N	—	—
DSI_CLK0P	J2	—	NVCC_MIPI	—	—	DSI_CLK_P	—	—
DSI_D0M	H2	—	NVCC_MIPI	—	—	DSI_DATA0_N	—	—
DSI_D0P	H1	—	NVCC_MIPI	—	—	DSI_DATA0_P	—	—
DSI_D1M	K2	—	NVCC_MIPI	—	—	DSI_DATA1_N	—	—
DSI_D1P	K1	—	NVCC_MIPI	—	—	DSI_DATA1_P	—	—
EIM_A16	T29	—	NVCC_EIM1	GPIO	ALT0	EIM_ADDR16	Output	0
EIM_A17	N24	—	NVCC_EIM1	GPIO	ALT0	EIM_ADDR17	Output	0
EIM_A18	M24	—	NVCC_EIM1	GPIO	ALT0	EIM_ADDR18	Output	0
EIM_A19	R28	—	NVCC_EIM1	GPIO	ALT0	EIM_ADDR19	Output	0
EIM_A20	R29	—	NVCC_EIM1	GPIO	ALT0	EIM_ADDR20	Output	0
EIM_A21	P29	—	NVCC_EIM1	GPIO	ALT0	EIM_ADDR21	Output	0
EIM_A22	P28	—	NVCC_EIM1	GPIO	ALT0	EIM_ADDR22	Output	0
EIM_A23	N28	—	NVCC_EIM1	GPIO	ALT0	EIM_ADDR23	Output	0
EIM_A24	N27	—	NVCC_EIM1	GPIO	ALT0	EIM_ADDR24	Output	0
EIM_A25	H28	—	NVCC_EIM0	GPIO	ALT0	EIM_ADDR25	Output	0
EIM_BCLK	AA27	—	NVCC_EIM2	GPIO	ALT0	EIM_BCLK	Output	0
EIM_CS0	U29	—	NVCC_EIM1	GPIO	ALT0	EIM_CS0_B	Output	1
EIM_CS1	U28	—	NVCC_EIM1	GPIO	ALT0	EIM_CS1_B	Output	1
EIM_D16	J24	—	NVCC_EIM0	GPIO	ALT5	GPIO3_IO16	Input	PU (100k)
EIM_D17	H29	—	NVCC_EIM0	GPIO	ALT5	GPIO3_IO17	Input	PU (100k)
EIM_D18	J28	—	NVCC_EIM0	GPIO	ALT5	GPIO3_IO18	Input	PU (100k)
EIM_D19	J29	—	NVCC_EIM0	GPIO	ALT5	GPIO3_IO19	Input	PU (100k)
EIM_D20	J23	—	NVCC_EIM0	GPIO	ALT5	GPIO3_IO20	Input	PU (100k)
EIM_D21	K29	—	NVCC_EIM0	GPIO	ALT5	GPIO3_IO21	Input	PU (100k)
EIM_D22	K28	—	NVCC_EIM0	GPIO	ALT5	GPIO3_IO22	Input	PU (100k)
EIM_D23	K24	—	NVCC_EIM0	GPIO	ALT5	GPIO3_IO23	Input	PU (100k)

Table 85. 12 x 12 mm Functional Contact Assignments (continued)

Ball Name	PoP Bottom Ball	PoP Top Ball	Power Group	Ball Type	Out of Reset Condition[1]			
					Default Mode	Default Function	Input/ Output	Value[2]
PCIE_TXM	A5	—	PCIE_VPH	—	—	PCIE_TX_N	—	—
PCIE_TXP	B5	—	PCIE_VPH	—	—	PCIE_TX_P	—	—
PMIC_ON_REQ	A12	—	VDD_SNVS_IN	GPIO	ALT0	SNVS_PMIC_ON_REQ	Output	Open Drain with PU(100k)
PMIC_STBY_REQ	C12	—	VDD_SNVS_IN	GPIO	ALT0	CCM_PMIC_STBY_REQ	Output	0
POR_B	F13	—	VDD_SNVS_IN	GPIO	ALT0	SRC_POR_B	Input	PU (100k)
RGMII_RD0	G27	—	NVCC_RGMII	DDR	ALT5	GPIO6_IO25	Input	PU (100k)
RGMII_RD1	F29	—	NVCC_RGMII	DDR	ALT5	GPIO6_IO27	Input	PU (100k)
RGMII_RD2	H23	—	NVCC_RGMII	DDR	ALT5	GPIO6_IO28	Input	PU (100k)
RGMII_RD3	G29	—	NVCC_RGMII	DDR	ALT5	GPIO6_IO29	Input	PU (100k)
RGMII_RX_CTL	F28	—	NVCC_RGMII	DDR	ALT5	GPIO6_IO24	Input	PD (100k)
RGMII_RXC	H24	—	NVCC_RGMII	DDR	ALT5	GPIO6_IO30	Input	PD (100k)
RGMII_TD0	C28	—	NVCC_RGMII	DDR	ALT5	GPIO6_IO20	Input	PU (100k)
RGMII_TD1	E29	—	NVCC_RGMII	DDR	ALT5	GPIO6_IO21	Input	PU (100k)
RGMII_TD2	G24	—	NVCC_RGMII	DDR	ALT5	GPIO6_IO22	Input	PU (100k)
RGMII_TD3	F27	—	NVCC_RGMII	DDR	ALT5	GPIO6_IO23	Input	PU (100k)
RGMII_TX_CTL	G28	—	NVCC_RGMII	DDR	ALT5	GPIO6_IO26	Input	PD (100k)
RGMII_TXC	C29	—	NVCC_RGMII	DDR	ALT5	GPIO6_IO19	Input	PD (100k)
RTC_XTALI	B10	—	VDD_SNVS_CAP	—	—	RTC_XTALI	—	—
RTC_XTALO	A10	—	VDD_SNVS_CAP	—	—	RTC_XTALO	—	—
SATA_RXM	A16	—	SATA_VPH	—	—	SATA_PHY_RX_N	—	—
SATA_RXP	B16	—	SATA_VPH	—	—	SATA_PHY_RX_P	—	—
SATA_TXM	A14	—	SATA_VPH	—	—	SATA_PHY_TX_N	—	—
SATA_TXP	B14	—	SATA_VPH	—	—	SATA_PHY_TX_P	—	—
SD1_CLK	C26	—	NVCC_SD1	GPIO	ALT5	GPIO1_IO20	Input	PU (100k)
SD1_CMD	D28	—	NVCC_SD1	GPIO	ALT5	GPIO1_IO18	Input	PU (100k)
SD1_DAT0	A27	—	NVCC_SD1	GPIO	ALT5	GPIO1_IO16	Input	PU (100k)
SD1_DAT1	B27	—	NVCC_SD1	GPIO	ALT5	GPIO1_IO17	Input	PU (100k)
SD1_DAT2	F22	—	NVCC_SD1	GPIO	ALT5	GPIO1_IO19	Input	PU (100k)
SD1_DAT3	A28	—	NVCC_SD1	GPIO	ALT5	GPIO1_IO21	Input	PU (100k)
SD2_CLK	E28	—	NVCC_SD2	GPIO	ALT5	GPIO1_IO10	Input	PU (100k)
SD2_CMD	D29	—	NVCC_SD2	GPIO	ALT5	GPIO1_IO11	Input	PU (100k)
SD2_DAT0	B29	—	NVCC_SD2	GPIO	ALT5	GPIO1_IO15	Input	PU (100k)
SD2_DAT1	F24	—	NVCC_SD2	GPIO	ALT5	GPIO1_IO14	Input	PU (100k)
SD2_DAT2	B28	—	NVCC_SD2	GPIO	ALT5	GPIO1_IO13	Input	PU (100k)
SD2_DAT3	F23	—	NVCC_SD2	GPIO	ALT5	GPIO1_IO12	Input	PU (100k)
SD3_CLK	C17	—	NVCC_SD3	GPIO	ALT5	GPIO7_IO03	Input	PU (100k)
SD3_CMD	F16	—	NVCC_SD3	GPIO	ALT5	GPIO7_IO02	Input	PU (100k)
SD3_DAT0	A18	—	NVCC_SD3	GPIO	ALT5	GPIO7_IO04	Input	PU (100k)
SD3_DAT1	B18	—	NVCC_SD3	GPIO	ALT5	GPIO7_IO05	Input	PU (100k)
SD3_DAT2	A19	—	NVCC_SD3	GPIO	ALT5	GPIO7_IO06	Input	PU (100k)

Table 86. Signals with Differing Before Reset and After Reset States (continued)

Ball Name	Before Reset State	
	Input/Output	Value
GPIO_19	Output	Drive state unknown (x)
KEY_COL0	Output	Drive state unknown (x)

6.2.5 12 x 12 mm PoP, 0.4 mm Pitch Ball Maps

Table 87 shows the 12 x 12 mm, 0.4 mm pitch top ball map. Table 88 shows the 12 x 12 mm, 0.4 mm pitch bottom ball map.

NOTE

On the top of the package, the data and control signals associated with each byte have been swizzled relative to the ball map of the associated LPDDR2 memory. This does not affect the operation of the i.MX 6Dual/6Quad SoC with the LPDDR2 memory.

Table 87. PoP 12 x 12 mm, 0.4 mm Pitch Top Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
A	DNU	GND	POP_VDD2__1	DRAM_D2P1	DRAM_D4P1	GND	DRAM_D1P1	DRAM_D5P1	GND	DRAM_DQS0P1_B	GND	DRAM_D11P1	DRAM_D9P1	GND	POP_VDD1__2	POP_VDD2__2	DRAM_D13P1	DRAM_D8P1	DRAM_D12P1	DRAM_DQS1P1	DRAM_DM1P1	POP_VDDQ	DRAM_DQS2P1	DRAM_D17P1	DRAM_D23P1	DRAM_D19P1	DRAM_D18P1	GND	DNU
B	GND	POP_VDD1__1	DRAM_D0P1	POP_VDDQ	DRAM_D3P1	DRAM_D7P1	POP_VDDQ	DRAM_D6P1	POP_VDDQ	DRAM_DQS0P1	DRAM_DM0P1	DRAM_D14P1	POP_VDDQ	GND	DRAM_VREF	POP_VDD2__2	DRAM_D15P1	POP_VDDQ	DRAM_D10P1	DRAM_DQS1P1_B	GND	DRAM_DM2P1	DRAM_DQS2P1_B	GND	POP_VDDQ	DRAM_D22P1	DRAM_D20P1	POP_VDD1__3	GND
C	POP_VDD1__1	DRAM_D18P0																										POP_VDD1__3	POP_VDD2__3
D	DRAM_D23P0	POP_VDDQ																										DRAM_D21P1	POP_VDDQ

Table 87. PoP 12 x 12 mm, 0.4 mm Pitch Top Ball Map (continued)

Y	W	V	U	T	R	P	N
POP_VDDQ	DRAM_D5P0	DRAM_D4P0	POP_VDDQ	POP_VDD2__5	POP_VDD1__4	GND	DRAM_D1P0
DRAM_D3P0	DRAM_D6P0	GND	DRAM_D0P0	POP_VDD2__5	DRAM_VREF	GND	POP_VDD1__4
DRAM_CS0P0	DRAM_CA4P0	GND	DRAM_VREF	POP_VDDCA	GND	POP_VDD2__4	DRAM_D29P1
DRAM_CKE1P0	DRAM_CS1P0	DRAM_CA3P0	DRAM_CA2P0	DRAM_CA1P0	DRAM_CA0P0	POP_VDD1__5	DRAM_D25P1

Table 88. PoP 12 x 12 mm, 0.4 mm Pitch Bottom Ball Map (continued)

N	M	L	K	J	H	G	F
HDMI_D1M	HDMI_D0M	HDMI_CLKM	DSI_D1P	DSI_CLK0M	DSI_D0P	CSI_D3P	CSI_D2M
HDMI_D1P	HDMI_D0P	HDMI_CLKP	DSI_D1M	DSI_CLK0P	DSI_D0M	CSI_D3M	CSI_D2P
GND	GND	GND	JTAG_TRSTB	POP_VDDQ	GND	POP_VDDQ	JTAG_MOD
GND	GND	GND	DSI_REXT	VDD_FA	CSI_REXT	NVCC_JTAG	GND
HDMI_VPH	HDMI_VP	JTAG_TDI	NVCC_MIPI	FA_ANA	PCIE_VP	PCIE_VPH	GND
						PCIE_VPTX	VDDHIGH_IN
						VDD_SNVS_CAP	VDDHIGH_IN
VDDARM23_IN	VDDARM23_IN	VDDARM23_IN	VDDARM23_IN			VDDUSB_CAP	VDDHIGH_CAP
VDDARM23_IN	VDDARM23_IN	VDDARM23_IN	VDDARM23_IN			USB_OTG_VBUS	VDDHIGH_CAP
VDDARM23_IN	VDDARM23_IN	VDDARM23_IN	VDDARM23_IN			VDD_SNVS_IN	USB_OTG_CHD_B
GND	GND	GND	GND			BOOT_MODE1	POR_B
GND	GND	GND	GND			SATA_VPH	SD3_DAT4
GND	GND	GND	GND			SATA_VP	SATA_REXT
VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN			NVCC_SD3	SD3_CMD
VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN			NANDF_CLE	SD3_DAT3
VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN			NVCC_NANDF	NANDF_CS1
VDDPU_CAP	VDDSOC_IN	VDDSOC_IN	VDDSOC_CAP			NANDF_D4	NANDF_D0
VDDPU_CAP	VDDSOC_IN	VDDSOC_IN	VDDSOC_CAP			SD4_DAT2	NANDF_D7
						NVCC_SD1	SD4_DAT4
						NVCC_SD2	SD1_DAT2
EIM_EB0	NVCC_EIM1	EIM_D31	NVCC_EIM0	EIM_D20	RGMII_RD2	NVCC_RGMII	SD2_DAT3
EIM_A17	EIM_A18	EIM_D29	EIM_D23	EIM_D16	RGMII_RXC	RGMII_TD2	SD2_DAT1
EIM_A24	POP_VDDQ	EIM_D26	EIM_EB3	POP_VDDQ	EIM_EB2	RGMII_RD0	RGMII_TD3
EIM_A23	EIM_D27	EIM_D25	EIM_D22	EIM_D18	EIM_A25	RGMII_TX_CTL	RGMII_RX_CTL
EIM_D30	EIM_D28	EIM_D24	EIM_D21	EIM_D19	EIM_D17	RGMII_RD3	RGMII_RD1