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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	4 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (1)
SATA	SATA 3Gbps (1)
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-20°C ~ 105°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	569-LFBGA
Supplier Device Package	569-MAPBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6q5ezk08ad

3 Modules List

The i.MX 6Dual/6Quad processors contain a variety of digital and analog modules. Table 2 describes these modules in alphabetical order.

Table 2. i.MX 6Dual/6Quad Modules List

Block Mnemonic	Block Name	Subsystem	Brief Description
512 x 8 Fuse Box	Electrical Fuse Array	Security	Electrical Fuse Array. Enables to setup Boot Modes, Security Levels, Security Keys, and many other system parameters. The i.MX 6Dual/6Quad processors consist of 512x8-bit fuse box accessible through OCOTP_CTRL interface.
APBH-DMA	NAND Flash and BCH ECC DMA Controller	System Control Peripherals	DMA controller used for GPMI2 operation.
ARM	ARM Platform	ARM	The ARM Cortex-A9 platform consists of 4x (four) Cortex-A9 cores version r2p10 and associated sub-blocks, including Level 2 Cache Controller, SCU (Snoop Control Unit), GIC (General Interrupt Controller), private timers, Watchdog, and CoreSight debug modules.
ASRC	Asynchronous Sample Rate Converter	Multimedia Peripherals	The Asynchronous Sample Rate Converter (ASRC) converts the sampling rate of a signal associated to an input clock into a signal associated to a different output clock. The ASRC supports concurrent sample rate conversion of up to 10 channels of about -120dB THD+N. The sample rate conversion of each channel is associated to a pair of incoming and outgoing sampling rates. The ASRC supports up to three sampling rate pairs.
AUDMUX	Digital Audio Mux	Multimedia Peripherals	The AUDMUX is a programmable interconnect for voice, audio, and synchronous data routing between host serial interfaces (for example, SSI1, SSI2, and SSI3) and peripheral serial interfaces (audio and voice codecs). The AUDMUX has seven ports with identical functionality and programming models. A desired connectivity is achieved by configuring two or more AUDMUX ports.
BCH40	Binary-BCH ECC Processor	System Control Peripherals	The BCH40 module provides up to 40-bit ECC error correction for NAND Flash controller (GPMI).
CAAM	Cryptographic Accelerator and Assurance Module	Security	CAAM is a cryptographic accelerator and assurance module. CAAM implements several encryption and hashing functions, a run-time integrity checker, and a Pseudo Random Number Generator (PRNG). The pseudo random number generator is certified by Cryptographic Algorithm Validation Program (CAVP) of National Institute of Standards and Technology (NIST). Its DRBG validation number is 94 and its SHS validation number is 1455. CAAM also implements a Secure Memory mechanism. In i.MX 6Dual/6Quad processors, the security memory provided is 16 KB.
CCM GPC SRC	Clock Control Module, General Power Controller, System Reset Controller	Clocks, Resets, and Power Control	These modules are responsible for clock and reset distribution in the system, and also for the system power management.

  - No external component required
  - Starts up quicker than 32 kHz crystal oscillator
- External crystal oscillator with on-chip support circuit
  - At power up, an internal ring oscillator is used. After crystal oscillator is stable, the clock circuit switches over to the crystal oscillator automatically.
  - Higher accuracy than ring oscillator.
  - If no external crystal is present, then the ring oscillator is used.

The decision to choose a clock source should be based on real-time clock use and precision timeout.

4.1.5 Maximum Measured Supply Currents

Power consumption is highly dependent on the application. Estimating the maximum supply currents required for power supply design is difficult because the use case that requires maximum supply current is not a realistic use case.

To help illustrate the effect of the application on power consumption, data was collected while running industry standard benchmarks that are designed to be compute and graphic intensive. The results provided are intended to be used as guidelines for power supply design.

Description of test conditions:

- The Power Virus data shown in Table 8 represent a use case designed specifically to show the maximum current consumption possible for the ARM core complex. All cores are running at the defined maximum frequency and are limited to L1 cache accesses only to ensure no pipeline stalls. Although a valid condition, it would have a very limited, if any, practical use case, and be limited to an extremely low duty cycle unless the intention was to specifically cause the worst case power consumption.
- EEMBC CoreMark: Benchmark designed specifically for the purpose of measuring the performance of a CPU core. More information available at www.eembc.org/coremark. Note that this benchmark is designed as a core performance benchmark, not a power benchmark. This use case is provided as an example of power consumption that would be typical in a computationally-intensive application rather than the Power Virus.
- 3DMark Mobile 2011: Suite of benchmarks designed for the purpose of measuring graphics and overall system performance. More information available at www.rightware.com/benchmarks. Note that this benchmark is designed as a graphics performance benchmark, not a power benchmark. This use case is provided as an example of power consumption that would be typical in a very graphics-intensive application.
- Devices used for the tests were from the high current end of the expected process variation.

The NXP power management IC, MMPF0100xxxx, which is targeted for the i.MX 6 series processor family, supports the power consumption shown in Table 8, however a robust thermal design is required for the increased system power dissipation.

See the *i.MX 6Dual/6Quad Power Consumption Measurement Application Note* (AN4509) for more details on typical power consumption under various use case definitions.

Table 12. PCIe PHY Current Drain (continued)

Mode	Test Conditions	Supply	Max Current	Unit
P1: Longer Recovery Time Latency, Lower Power State	—	PCIE_VP (1.1 V)	12	mA
		PCIE_VPTX (1.1 V)	2.4	
		PCIE_VPH (2.5 V)	12	
Power Down	—	PCIE_VP (1.1 V)	1.3	mA
		PCIE_VPTX (1.1 V)	0.18	
		PCIE_VPH (2.5 V)	0.36	

4.1.10 HDMI Maximum Power Consumption

Table 13 provides HDMI PHY currents for both Active 3D Tx with LFSR15 data pattern and Power-down modes.

Table 13. HDMI PHY Current Drain

Mode	Test Conditions	Supply	Max Current	Unit
Active	Bit rate 251.75 Mbps	HDMI_VPH	14	mA
		HDMI_VP	4.1	mA
	Bit rate 279.27 Mbps	HDMI_VPH	14	mA
		HDMI_VP	4.2	mA
	Bit rate 742.5 Mbps	HDMI_VPH	17	mA
		HDMI_VP	7.5	mA
	Bit rate 1.485 Gbps	HDMI_VPH	17	mA
		HDMI_VP	12	mA
	Bit rate 2.275 Gbps	HDMI_VPH	16	mA
		HDMI_VP	17	mA
	Bit rate 2.97 Gbps	HDMI_VPH	19	mA
		HDMI_VP	22	mA
Power-down	—	HDMI_VPH	49	µA
		HDMI_VP	1100	µA

- When the PCIE interface is not used, the PCIE_VP, PCIE_VPH, and PCIE_VPTX supplies should be grounded. The input and output supplies for rest of the ports (PCIE_REXT, PCIE_RX_N, PCIE_RX_P, PCIE_TX_N, and PCIE_TX_P) can remain unconnected. It is recommended not to turn the PCIE_VPH supply OFF while the PCIE_VP supply is ON, as it may lead to excessive power consumption. If boundary scan test is used, PCIE_VP, PCIE_VPH, and PCIE_VPTX must remain powered.

4.3 Integrated LDO Voltage Regulator Parameters

Various internal supplies can be powered ON from internal LDO voltage regulators. All the supply pins named *_CAP must be connected to external capacitors. The onboard LDOs are intended for internal use only and should not be used to power any external circuitry. See the i.MX 6Dual/6Quad reference manual (IMX6DQRM) for details on the power tree scheme recommended operation.

NOTE

The *_CAP signals should not be powered externally. These signals are intended for internal LDO or LDO bypass operation only.

4.3.1 Digital Regulators (LDO_ARM, LDO_PU, LDO_SOC)

There are three digital LDO regulators (“Digital”, because of the logic loads that they drive, not because of their construction). The advantages of the regulators are to reduce the input supply variation because of their input supply ripple rejection and their on die trimming. This translates into more voltage for the die producing higher operating frequencies. These regulators have three basic modes.

- Bypass. The regulation FET is switched fully on passing the external voltage, DCDC_LOW, to the load unaltered. The analog part of the regulator is powered down in this state, removing any loss other than the IR drop through the power grid and FET.
- Power Gate. The regulation FET is switched fully off limiting the current draw from the supply. The analog part of the regulator is powered down here limiting the power consumption.
- Analog regulation mode. The regulation FET is controlled such that the output voltage of the regulator equals the programmed target voltage. The target voltage is fully programmable in 25 mV steps.

Optionally LDO_SOC/VDD_SOC_CAP can be used to power the HDMI, PCIe, and SATA PHY's through external connections.

For additional information, see the i.MX 6Dual/6Quad reference manual (IMX6DQRM).

4.3.2 Regulators for Analog Modules

4.3.2.1 LDO_1P1 / NVCC_PLL_OUT

The LDO_1P1 regulator implements a programmable linear-regulator function from VDD_HIGH_IN (see Table 6 for minimum and maximum input requirements). Typical Programming Operating Range is 1.0 V to 1.2 V with the nominal default setting as 1.1 V. The LDO_1P1 supplies the 24 MHz oscillator, PLLs, and USB PHY. A programmable brown-out detector is included in the regulator that can be used by the

4.6.1 XTALI and RTC_XTALI (Clock Inputs) DC Parameters

Table 20 shows the DC parameters for the clock inputs.

Table 20. XTALI and RTC_XTALI DC Parameters

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
XTALI high-level DC input voltage	Vih	—	0.8 x NVCC_PLL_OUT	—	NVCC_PLL_ OUT	V
XTALI low-level DC input voltage	Vil	—	0	—	0.2	V
RTC_XTALI high-level DC input voltage	Vih	—	0.8	—	1.1 (See note 1)	V
RTC_XTALI low-level DC input voltage	Vil	—	0	—	0.2	V
Input capacitance	C_{IN}	Simulated data	—	5	—	pF
XTALI input leakage current at startup	$I_{XTALI\_STARTUP}$	Power-on startup for 0.15 msec with a driven 32 KHz RTC clock @ 1.1 V. [2]	—	—	600	µA
DC input current	I_{XTALI_DC}	—	—	—	2.5	µA

[1] This voltage specification must not be exceeded and, as such, is an absolute maximum specification.

[2] This current draw is present even if an external clock source directly drives XTALI.

NOTE

The Vil and Vih specifications only apply when an external clock source is used. If a crystal is used, Vil and Vih do not apply.

4.6.2 General Purpose I/O (GPIO) DC Parameters

Table 21 shows DC parameters for GPIO pads. The parameters in Table 21 are guaranteed per the operating ranges in Table 6, unless otherwise noted.

Table 21. GPIO I/O DC Parameters

Parameter	Symbol	Test Conditions	Min	Max	Unit
High-level output voltage[1]	Voh	Ioh = -0.1 mA (DSE[2] = 001, 010) Ioh = -1 mA (DSE = 011, 100, 101, 110, 111)	OVDD – 0.15	—	V
Low-level output voltage[1]	Vol	Iol = 0.1 mA (DSE[2] = 001, 010) Iol = 1mA (DSE = 011, 100, 101, 110, 111)	—	0.15	V
High-Level DC input voltage[1, 3]	Vih	—	0.7 × OVDD	OVDD	V
Low-Level DC input voltage[1, 3]	Vil	—	0	0.3 × OVDD	V
Input Hysteresis	Vhys	OVDD = 1.8 V OVDD = 3.3 V	0.25	—	V
Schmitt trigger VT+[3, 4]	VT+	—	0.5 × OVDD	—	V
Schmitt trigger VT–[3, 4]	VT–	—	—	0.5 × OVDD	V

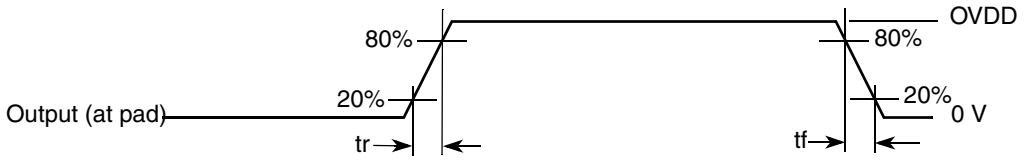


Figure 5. Output Transition Time Waveform

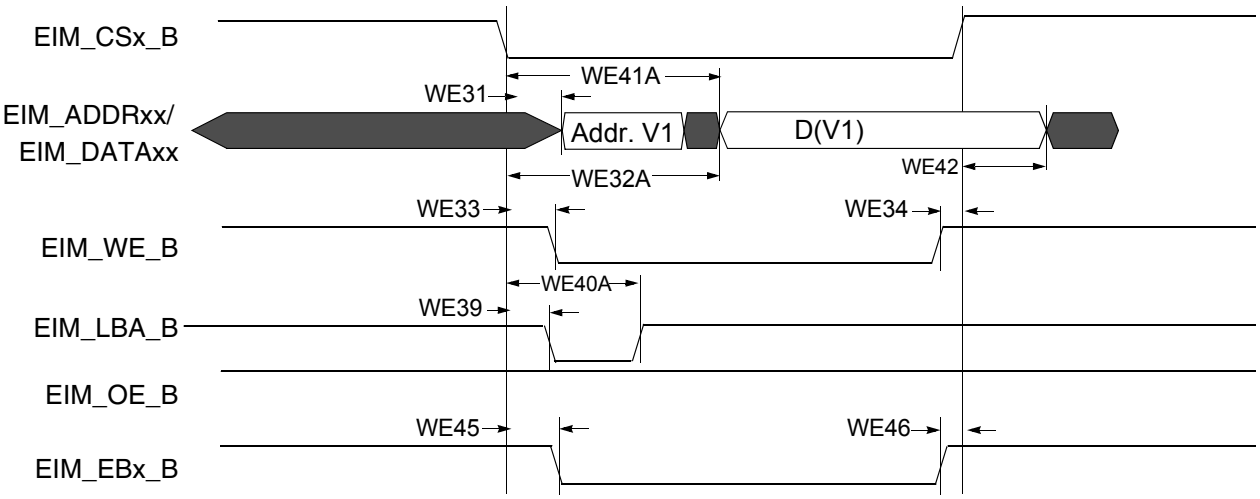


Figure 19. Asynchronous A/D Muxed Write Access

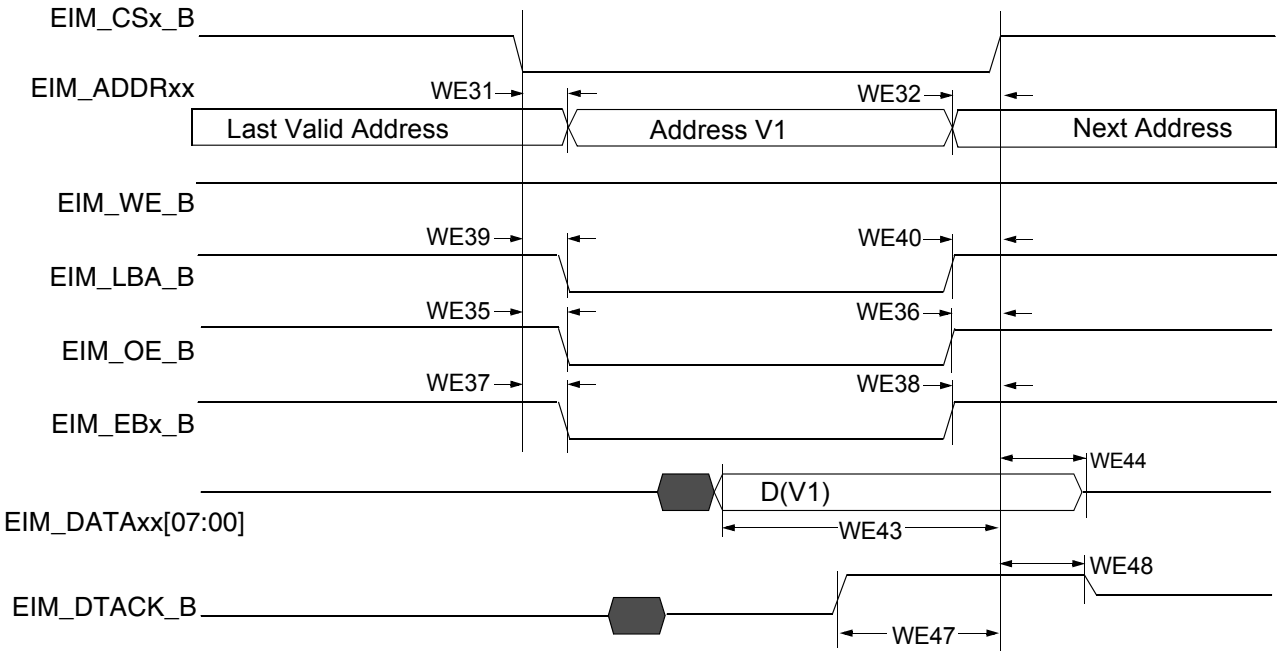


Figure 20. DTACK Mode Read Access (DAP=0)

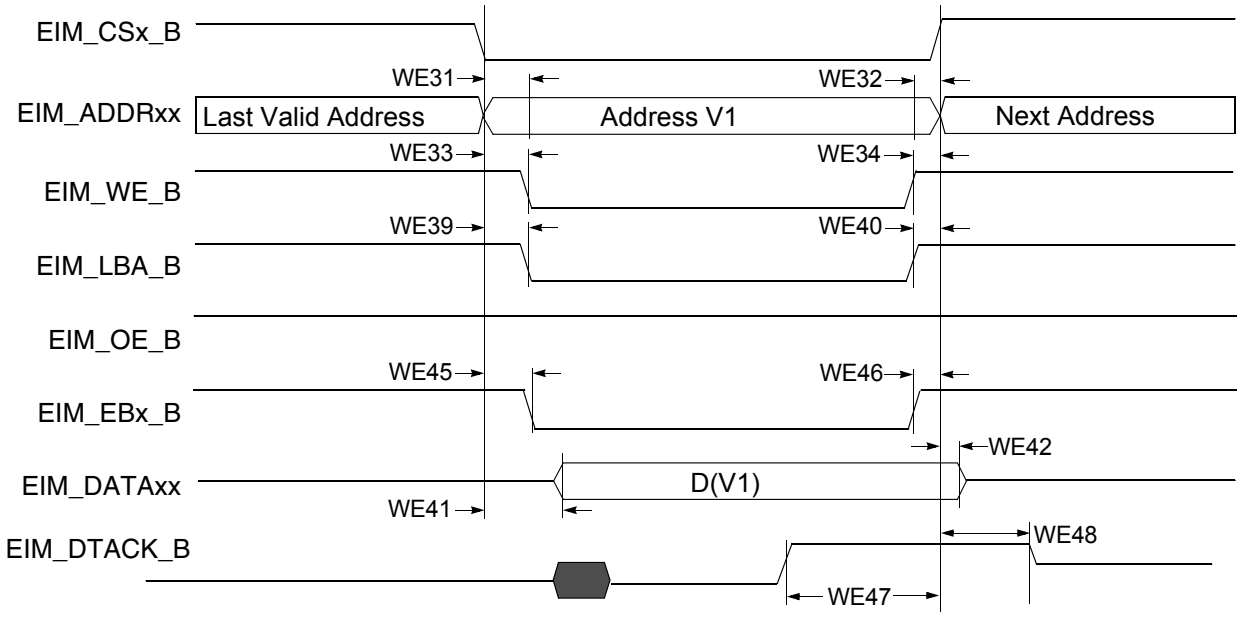


Figure 21. DTACK Mode Write Access (DAP=0)

Table 36. EIM Asynchronous Timing Parameters Relative to Chip Select[1, 2]

Ref No.	Parameter	Determination by Synchronous measured parameters	Min	Max	Unit
WE31	EIM_CSx_B valid to Address Valid	WE4-WE6-CSA×t	-3.5-CSA×t	3.5-CSA×t	ns
WE32	Address Invalid to EIM_CSx_B Invalid	WE7-WE5-CSN×t	-3.5-CSN×t	3.5-CSN×t	ns
WE32A (muxed A/D)	EIM_CSx_B valid to Address Invalid	t+WE4-WE7+ (ADVN+ADVA+1-CSA)×t	t - 3.5+(ADVN+ADVA+1-CSA)×t	t + 3.5+(ADVN+ADVA+1-CSA)×t	ns
WE33	EIM_CSx_B Valid to EIM_WE_B Valid	WE8-WE6+(WEA-WCSA)×t	-3.5+(WEA-WCSA)×t	3.5+(WEA-WCSA)×t	ns
WE34	EIM_WE_B Invalid to EIM_CSx_B Invalid	WE7-WE9+(WEN-WCSN)×t	-3.5+(WEN-WCSN)×t	3.5+(WEN-WCSN)×t	ns
WE35	EIM_CSx_B Valid to EIM_OE_B Valid	WE10- WE6+(OEA-RCSA)×t	-3.5+(OEA-RCSA)×t	3.5+(OEA-RCSA)×t	ns
WE35A (muxed A/D)	EIM_CSx_B Valid to EIM_OE_B Valid	WE10-WE6+(OEA+RADVN+RADVA+ADH+1-RCSA)×t	-3.5+(OEA+RADVN+RADVA+ADH+1-RCSA)×t	3.5+(OEA+RADVN+RADVA+ADH+1-RCSA)×t	ns
WE36	EIM_OE_B Invalid to EIM_CSx_B Invalid	WE7-WE11+(OEN-RCSN)×t	-3.5+(OEN-RCSN)×t	3.5+(OEN-RCSN)×t	ns
WE37	EIM_CSx_B Valid to EIM_EBx_B Valid (Read access)	WE12-WE6+(RBEA-RCSA)× t	-3.5+(RBEA- RCSA)×t	3.5+(RBEA - RCSA)×t	ns
WE38	EIM_EBx_B Invalid to EIM_CSx_B Invalid (Read access)	WE7-WE13+(RBEN-RCSN)×t	-3.5+ (RBEN-RCSN)×t	3.5+(RBEN-RCSN)×t	ns
WE39	EIM_CSx_B Valid to EIM_LBA_B Valid	WE14-WE6+(ADVA-CSA)×t	-3.5+ (ADVA-CSA)×t	3.5+(ADVA-CSA)×t	ns

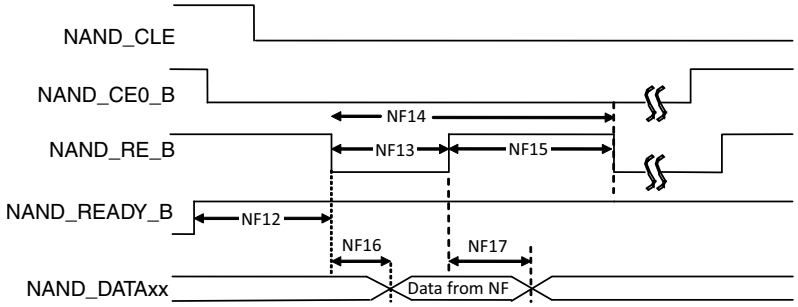


Figure 25. Read Data Latch Cycle Timing Diagram (Non-EDO Mode)

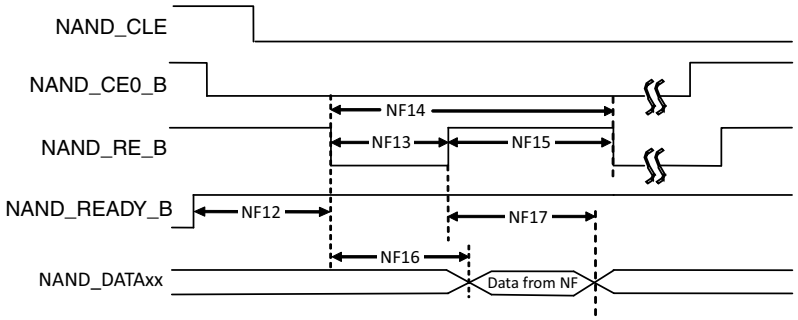


Figure 26. Read Data Latch Cycle Timing Diagram (EDO Mode)

Table 38. Asynchronous Mode Timing Parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min	Max	
NF1	NAND_CLE setup time	tCLS	(AS + DS) × T - 0.12 [see [2,3]]		ns
NF2	NAND_CLE hold time	tCLH	DH × T - 0.72 [see [2]]		ns
NF3	NAND_CEx_B setup time	tCS	(AS + DS + 1) × T [see [3,2]]		ns
NF4	NAND_CEx_B hold time	tCH	(DH+1) × T - 1 [see [2]]		ns
NF5	NAND_WE_B pulse width	tWP	DS × T [see [2]]		ns
NF6	NAND_ALE setup time	tALS	(AS + DS) × T - 0.49 [see [3,2]]		ns
NF7	NAND_ALE hold time	tALH	(DH × T - 0.42 [see [2]]		ns
NF8	Data setup time	tDS	DS × T - 0.26 [see [2]]		ns
NF9	Data hold time	tDH	DH × T - 1.37 [see [2]]		ns
NF10	Write cycle time	tWC	(DS + DH) × T [see [2]]		ns
NF11	NAND_WE_B hold time	tWH	DH × T [see [2]]		ns
NF12	Ready to NAND_RE_B low	tRR[4]	(AS + 2) × T [see [3,2]]	—	ns
NF13	NAND_RE_B pulse width	tRP	DS × T [see [2]]		ns
NF14	READ cycle time	tRC	(DS + DH) × T [see [2]]		ns
NF15	NAND_RE_B high hold time	tREH	DH × T [see [2]]		ns

Table 40. Samsung Toggle Mode Timing Parameters[1] (continued)

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min	Max	
NF28	Data write setup	tDS[6]	0.25 × tCK - 0.32	—	ns
NF29	Data write hold	tDH[6]	0.25 × tCK - 0.79	—	ns
NF30	NAND_DQS/NAND_DQ read setup skew	tDQSQ[7]	—	3.18	—
NF31	NAND_DQS/NAND_DQ read hold skew	tQHS[7]	—	3.27	—

1 The GPMI toggle mode output timing can be controlled by the module's internal registers HW_GPMI_TIMING0_ADDRESS_SETUP, HW_GPMI_TIMING0_DATA_SETUP, and HW_GPMI_TIMING0_DATA_HOLD. This AC timing depends on these registers settings. In the table, AS/DS/DH represents each of these settings.

2 AS minimum value can be 0, while DS/DH minimum value is 1.

3 T = tCK (GPMI clock period) -0.075ns (half of maximum p-p jitter).

4 CE_DELAY represents HW_GPMI_TIMING2[CE_DELAY]. NF18 is met automatically by the design. Read/Write operation is started with enough time of ALE/CLE assertion to low level.

5 PRE_DELAY+1) ≥ (AS+DS)

6 Shown in Figure 28.

7 Shown in Figure 29.

Figure 30 shows the timing diagram of NAND_DQS/NAND_DATAxx read valid window. For DDR Toggle mode, the typical value of tDQSQ is 1.4 ns (max) and 1.4 ns (max) for tQHS at 133 MB/s. GPMI will sample NAND_DATA[7:0] at both rising and falling edge of a delayed NAND_DQS signal, which is provided by an internal DPLL. The delay value of this register can be controlled by GPMI register GPMI_READ_DDR_DLL_CTRL.SLV_DLY_TARGET (see the GPMI chapter of the i.MX 6Dual/6Quad reference manual (IMX6DQRM)). Generally, the typical delay value is equal to 0x7 which means 1/4 clock cycle delay expected. However, if the board delay is large enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

4.12 External Peripheral Interface Parameters

The following subsections provide information on external peripheral interfaces.

4.12.1 AUDMUX Timing Parameters

The AUDMUX provides a programmable interconnect logic for voice, audio, and data routing between internal serial interfaces (SSIs) and external serial interfaces (audio and voice codecs). The AC timing of AUDMUX external pins is governed by the SSI module. For more information, see the respective SSI electrical specifications found within this document.

4.12.2 ECSPI Timing Parameters

This section describes the timing parameters of the ECSPI block. The ECSPI has separate timing parameters for master and slave modes.

4.12.3 Enhanced Serial Audio Interface (ESAI) Timing Parameters

The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. Table 43 shows the interface timing values. The number field in the table refers to timing signals found in Figure 35 and Figure 36.

Table 43. Enhanced Serial Audio Interface (ESAI) Timing

ID	Parameter[1,2]	Symbol	Expression[2]	Min	Max	Condition[3]	Unit
62	Clock cycle[4]	t_{SSICC}	$4 \times T_C$ $4 \times T_C$	30.0 30.0	— —	i ck i ck	ns
63	Clock high period: • For internal clock • For external clock	— —	$2 \times T_C - 9.0$ $2 \times T_C$	6 15	— —	— —	ns
64	Clock low period: • For internal clock • For external clock	— —	$2 \times T_C - 9.0$ $2 \times T_C$	6 15	— —	— —	ns
65	ESAI_RX_CLK rising edge to ESAI_RX_FS out (bl) high	— —	— —	— —	19.0 7.0	x ck i ck a	ns
66	ESAI_RX_CLK rising edge to ESAI_RX_FS out (bl) low	— —	— —	— —	19.0 7.0	x ck i ck a	ns
67	ESAI_RX_CLK rising edge to ESAI_RX_FS out (wr) high[5]	— —	— —	— —	19.0 9.0	x ck i ck a	ns
68	ESAI_RX_CLK rising edge to ESAI_RX_FS out (wr) low[5]	— —	— —	— —	19.0 9.0	x ck i ck a	ns
69	ESAI_RX_CLK rising edge to ESAI_RX_FS out (wl) high	— —	— —	— —	19.0 6.0	x ck i ck a	ns
70	ESAI_RX_CLK rising edge to ESAI_RX_FSout (wl) low	— —	— —	— —	17.0 7.0	x ck i ck a	ns
71	Data in setup time before ESAI_RX_CLK (serial clock in synchronous mode) falling edge	— —	— —	12.0 19.0	— —	x ck i ck	ns
72	Data in hold time after ESAI_RX_CLK falling edge	— —	— —	3.5 9.0	— —	x ck i ck	ns
73	ESAI_RX_FS input (bl, wr) high before ESAI_RX_CLK falling edge[5]	— —	— —	2.0 19.0	— —	x ck i ck a	ns
74	ESAI_RX_FS input (wl) high before ESAI_RX_CLK falling edge	— —	— —	2.0 19.0	— —	x ck i ck a	ns
75	ESAI_RX_FS input hold time after ESAI_RX_CLK falling edge	— —	— —	2.5 8.5	— —	x ck i ck a	ns
78	ESAI_TX_CLK rising edge to ESAI_TX_FS out (bl) high	— —	— —	— —	19.0 8.0	x ck i ck	ns
79	ESAI_TX_CLK rising edge to ESAI_TX_FS out (bl) low	— —	— —	— —	20.0 10.0	x ck i ck	ns
80	ESAI_TX_CLK rising edge to ESAI_TX_FS out (wr) high[5]	— —	— —	— —	20.0 10.0	x ck i ck	ns

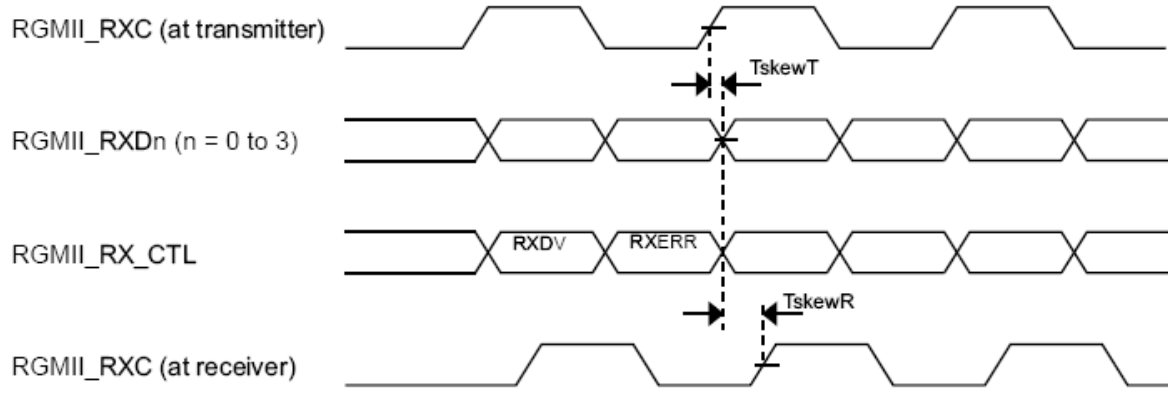


Figure 46. RGMII Receive Signal Timing Diagram Original

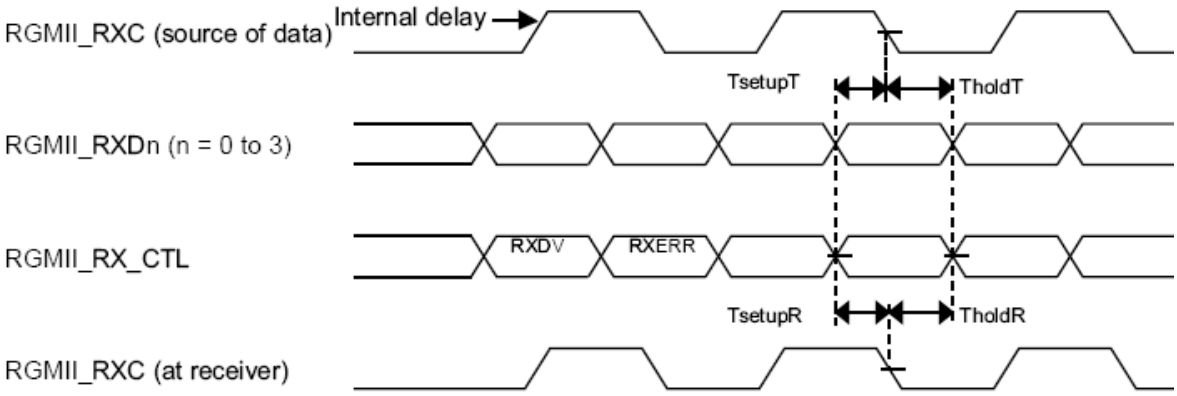


Figure 47. RGMII Receive Signal Timing Diagram with Internal Delay

4.12.6 Flexible Controller Area Network (FlexCAN) AC Electrical Specifications

The Flexible Controller Area Network (FlexCAN) module is a communication controller implementing the CAN protocol according to the CAN 2.0B protocol specification.The processor has two CAN modules available for systems design. Tx and Rx ports for both modules are multiplexed with other I/O pins. See the IOMUXC chapter of the i.MX 6Dual/6Quad reference manual (IMX6DQRM) to see which pins expose Tx and Rx pins; these ports are named FLEXCAN_TX and FLEXCAN_RX, respectively.

4.12.7 HDMI Module Timing Parameters

4.12.7.1 Latencies and Timing Information

Power-up time (time between TX_PWRON assertion and TX_READY assertion) for the HDMI 3D Tx PHY while operating with the slowest input reference clock supported (13.5 MHz) is 3.35 ms.

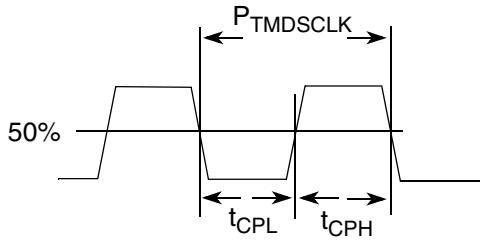


Figure 51. TMDS Clock Signal Definitions

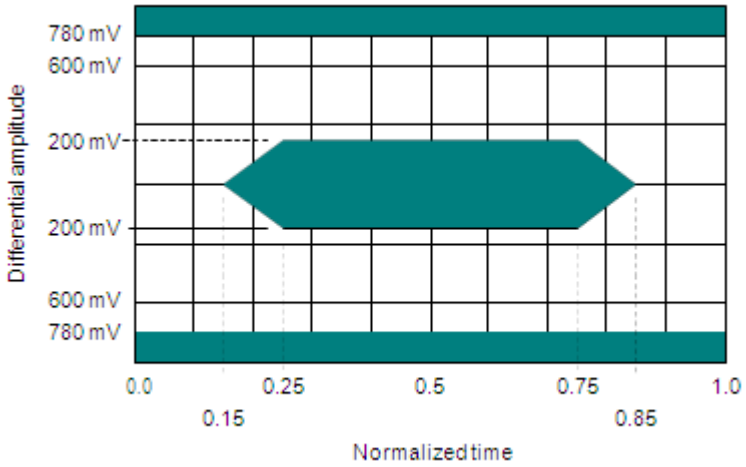


Figure 52. Eye Diagram Mask Definition for HDMI Driver Signal Specification at TP1

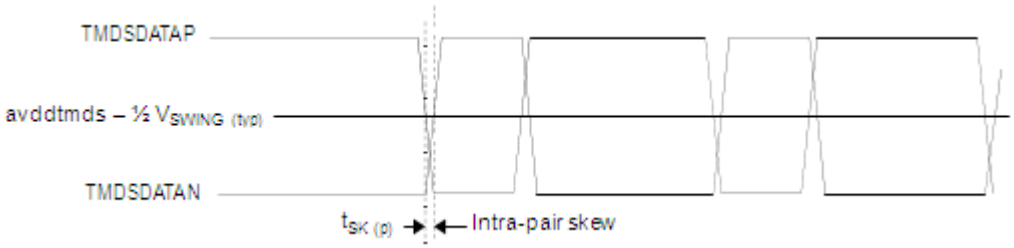


Figure 53. Intra-Pair Skew Definition

4.12.10.3 Electrical Characteristics

Figure 59 depicts the sensor interface timing. IPU2_CSIx_PIX_CLK signal described here is not generated by the IPU. Table 57 lists the sensor interface timing characteristics.

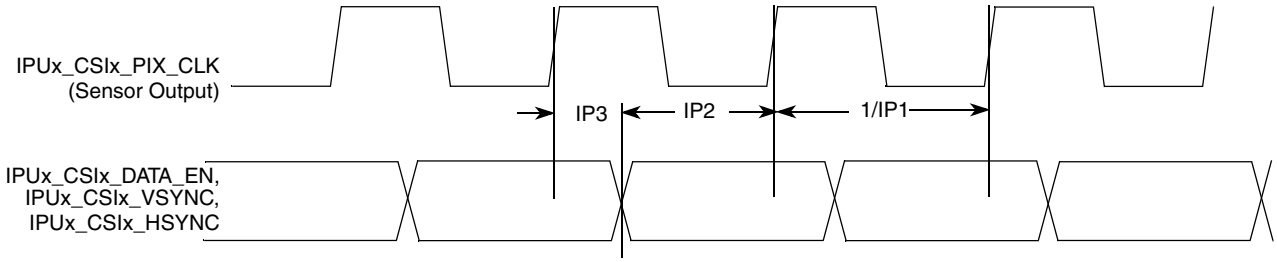


Figure 59. Sensor Interface Timing Diagram

Table 57. Sensor Interface Timing Characteristics

ID	Parameter	Symbol	Min	Max	Unit
IP1	Sensor output (pixel) clock frequency	Fpck	0.01	180	MHz
IP2	Data and control setup time	Tsu	2	—	ns
IP3	Data and control holdup time	Thd	1	—	ns
—	Vsync to Hsync	Tv-h	1/Fpck	—	ns
—	Vsync and Hsync pulse width	Tpulse	1/Fpck	—	ns
—	Vsync to first data	Tv-d	1/Fpck	—	ns

4.12.10.4 IPU Display Interface Signal Mapping

The IPU supports a number of display output video formats. Table 58 defines the mapping of the Display Interface Pins used during various supported video interface formats.

Table 58. Video Signal Cross-Reference

i.MX 6Dual/6Quad	LCD							Comment[1,2]
Port Name (x = 0, 1)	RGB, Signal Name (General)	RGB/TV Signal Allocation (Example)						
		16-bit RGB	18-bit RGB	24 Bit RGB	8-bit YCrCb[3]	16-bit YCrCb	20-bit YCrCb	
IPUx_DISPx_DAT00	DAT[0]	B[0]	B[0]	B[0]	Y/C[0]	C[0]	C[0]	—
IPUx_DISPx_DAT01	DAT[1]	B[1]	B[1]	B[1]	Y/C[1]	C[1]	C[1]	—
IPUx_DISPx_DAT02	DAT[2]	B[2]	B[2]	B[2]	Y/C[2]	C[2]	C[2]	—
IPUx_DISPx_DAT03	DAT[3]	B[3]	B[3]	B[3]	Y/C[3]	C[3]	C[3]	—
IPUx_DISPx_DAT04	DAT[4]	B[4]	B[4]	B[4]	Y/C[4]	C[4]	C[4]	—

Table 58. Video Signal Cross-Reference (continued)

i.MX 6Dual/6Quad	LCD							Comment[1,2]
Port Name (x = 0, 1)	RGB, Signal Name (General)	RGB/TV Signal Allocation (Example)						
		16-bit RGB	18-bit RGB	24 Bit RGB	8-bit YCrCb[3]	16-bit YCrCb	20-bit YCrCb	
IPUx_DISPx_DAT05	DAT[5]	G[0]	B[5]	B[5]	Y/C[5]	C[5]	C[5]	—
IPUx_DISPx_DAT06	DAT[6]	G[1]	G[0]	B[6]	Y/C[6]	C[6]	C[6]	—
IPUx_DISPx_DAT07	DAT[7]	G[2]	G[1]	B[7]	Y/C[7]	C[7]	C[7]	—
IPUx_DISPx_DAT08	DAT[8]	G[3]	G[2]	G[0]	—	Y[0]	C[8]	—
IPUx_DISPx_DAT09	DAT[9]	G[4]	G[3]	G[1]	—	Y[1]	C[9]	—
IPUx_DISPx_DAT10	DAT[10]	G[5]	G[4]	G[2]	—	Y[2]	Y[0]	—
IPUx_DISPx_DAT11	DAT[11]	R[0]	G[5]	G[3]	—	Y[3]	Y[1]	—
IPUx_DISPx_DAT12	DAT[12]	R[1]	R[0]	G[4]	—	Y[4]	Y[2]	—
IPUx_DISPx_DAT13	DAT[13]	R[2]	R[1]	G[5]	—	Y[5]	Y[3]	—
IPUx_DISPx_DAT14	DAT[14]	R[3]	R[2]	G[6]	—	Y[6]	Y[4]	—
IPUx_DISPx_DAT15	DAT[15]	R[4]	R[3]	G[7]	—	Y[7]	Y[5]	—
IPUx_DISPx_DAT16	DAT[16]	—	R[4]	R[0]	—	—	Y[6]	—
IPUx_DISPx_DAT17	DAT[17]	—	R[5]	R[1]	—	—	Y[7]	—
IPUx_DISPx_DAT18	DAT[18]	—	—	R[2]	—	—	Y[8]	—
IPUx_DISPx_DAT19	DAT[19]	—	—	R[3]	—	—	Y[9]	—
IPUx_DISPx_DAT20	DAT[20]	—	—	R[4]	—	—	—	—
IPUx_DISPx_DAT21	DAT[21]	—	—	R[5]	—	—	—	—
IPUx_DISPx_DAT22	DAT[22]	—	—	R[6]	—	—	—	—
IPUx_DISPx_DAT23	DAT[23]	—	—	R[7]	—	—	—	—
IPUx_DIx_DISP_CLK	PixCLK							—
IPUx_DIx_PIN01	—							May be required for anti-tearing
IPUx_DIx_PIN02	HSYNC							—
IPUx_DIx_PIN03	VSYNC							VSYNC out

Table 62. Electrical and Timing Information (continued)

Symbol	Parameters	Test Conditions	Min	Typ	Max	Unit
LP Line Receiver DC Specifications						
V_{IL}	Input low voltage	—	—	—	550	mV
V_{IH}	Input high voltage	—	920	—	—	mV
V_{HYST}	Input hysteresis	—	25	—	—	mV
Contention Line Receiver DC Specifications						
V_{ILF}	Input low fault threshold	—	200	—	450	mV

4.12.12.2 D-PHY Signaling Levels

The signal levels are different for differential HS mode and single-ended LP mode. Figure 64 shows both the HS and LP signal levels on the left and right sides, respectively. The HS signalling levels are below the LP low-level input threshold such that LP receiver always detects low on HS signals.

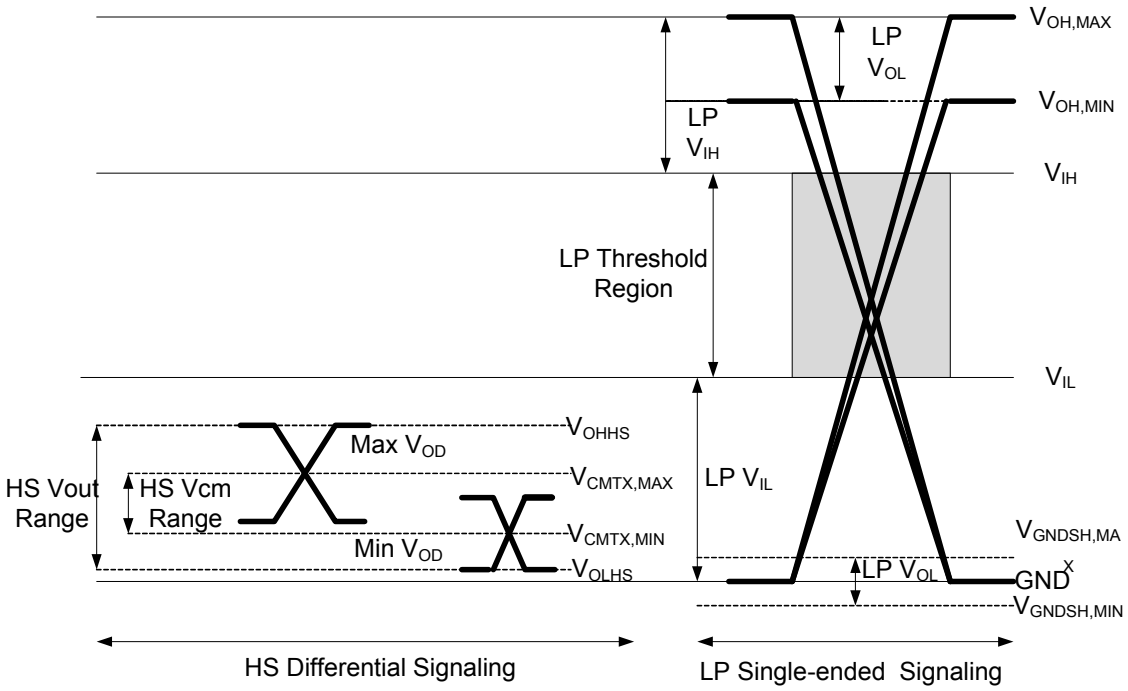


Figure 64. D-PHY Signaling Levels

Table 71. SSI Transmitter Timing with Internal Clock (continued)

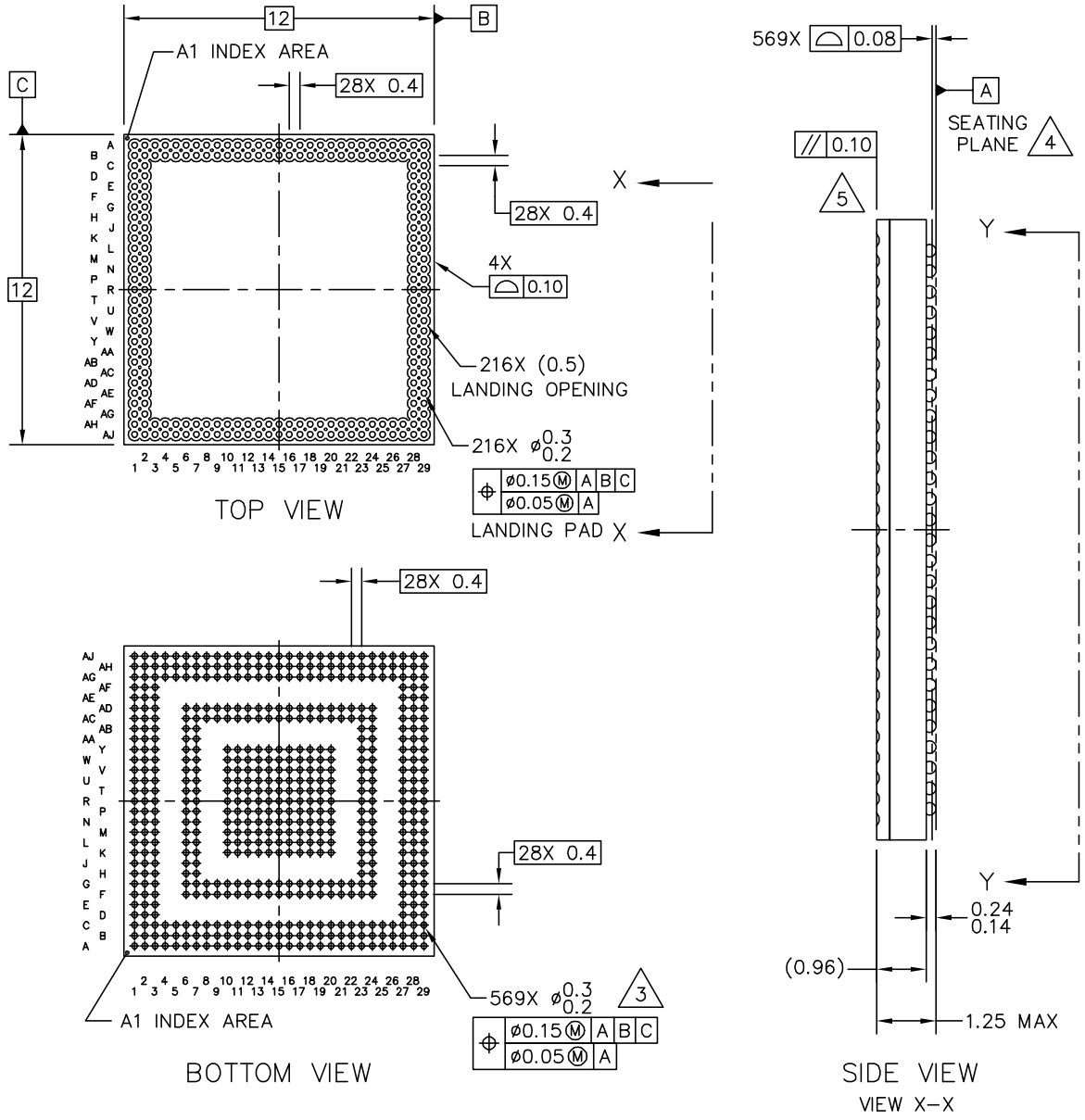
ID	Parameter	Min	Max	Unit
Synchronous Internal Clock Operation				
SS42	AUDx_RXD setup before AUDx_TXC falling	10.0	—	ns
SS43	AUDx_RXD hold after AUDx_TXC falling	0.0	—	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal AUDx_TXC/AUDx_RXC and/or the frame sync AUDx_TXFS/AUDx_RXFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- The terms, WL and BL, refer to Word Length(WL) and Bit Length(BL).
- For internal Frame Sync operation using external clock, the frame sync timing is the same as that of transmit data (for example, during AC97 mode of operation).

6.2.1 Case PoP, 0.4 mm Pitch, 12 x 12 Ball Matrix

Figure 97 and Figure 97 show the top, bottom, and side views of the 12 x 12 mm PoP package.



© NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: FCMAPBGA STACKABLE, 12 X 12 X 1.15 PKG, 0.4 MM PITCH, 569 I/O	DOCUMENT NO: 98ASA00383D	REV: A
	STANDARD: NON–JEDEC	
	SOT1644–1	29 FEB 2016

Figure 96. 12 x 12 mm PoP Package Top, Bottom, and Side Views (Sheet 1 of 2)

Table 84. 12 x 12 mm PoP Ground, Power, Sense, and Reference Contact Assignments (continued)

Ball Name	PoP Bottom Ball Position	PoP Top Ball Position	Remark
VDDHIGH_CAP	F10, F11	—	Secondary supply for the 2.5 V domain (internal regulator output—requires capacitor if internal regulator is used)
VDDHIGH_IN	F8, F9	—	Primary supply for the 2.5 V regulator
VDDPU_CAP	N19, N20, P19, P20, U19, U20, V19, V20	—	Secondary supply for the VPU and GPU (internal regulator output—requires capacitor if internal regulator is used)
VDDSOC_CAP	K19, K20, R6, R7, W10, W11, W12, W15, W16, Y10, Y11, Y12, Y15, Y16	—	Secondary supply for the SoC and PU (internal regulator output—requires capacitor if internal regulator is used)
VDDSOC_IN	L19, L20, M19, M20, W19, W20, Y19, Y20	—	Primary supply for the SoC and PU regulators
VDDUSB_CAP	G10	—	Secondary supply for the 3 V domain (internal regulator output—requires capacitor if internal regulator is used)
ZQPAD	AJ19	—	Connect ZQPAD to an external 240Ω 1% resistor to GND. This is a reference used during DRAM output buffer driver calibration.

6.2.3 12 x 12 mm Functional Contact Assignments

Table 85 displays an alpha-sorted list of the signal assignments including power rails. The table also includes out of reset pad state.

Table 85. 12 x 12 mm Functional Contact Assignments

Ball Name	PoP Bottom Ball	PoP Top Ball	Power Group	Ball Type	Out of Reset Condition[1]			
					Default Mode	Default Function	Input/ Output	Value[2]
BOOT_MODE0	C14	—	VDD_SNVS_IN	GPIO	ALT0	SRC_BOOT_MODE0	Input	PD (100k)
BOOT_MODE1	G13	—	VDD_SNVS_IN	GPIO	ALT0	SRC_BOOT_MODE1	Input	PD (100k)
CLK1_N	A7	—	VDD_HIGH_CAP	—	—	CLK1_N	—	—
CLK1_P	B7	—	VDD_HIGH_CAP	—	—	CLK1_P	—	—
CLK2_N	A6	—	VDD_HIGH_CAP	—	—	CLK2_N	—	—
CLK2_P	B6	—	VDD_HIGH_CAP	—	—	CLK2_P	—	—
CSI_CLK0M	E2	—	NVCC_MIPI	—	—	CSI_CLK_N	—	—
CSI_CLK0P	E1	—	NVCC_MIPI	—	—	CSI_CLK_P	—	—
CSI_D0M	C2	—	NVCC_MIPI	—	—	CSI_DATA0_N	—	—
CSI_D0P	C1	—	NVCC_MIPI	—	—	CSI_DATA0_P	—	—
CSI_D1M	D1	—	NVCC_MIPI	—	—	CSI_DATA1_N	—	—
CSI_D1P	D2	—	NVCC_MIPI	—	—	CSI_DATA1_P	—	—
CSI_D2M	F1	—	NVCC_MIPI	—	—	CSI_DATA2_N	—	—
CSI_D2P	F2	—	NVCC_MIPI	—	—	CSI_DATA2_P	—	—

Table 88. PoP 12 x 12 mm, 0.4 mm Pitch Bottom Ball Map (continued)

N	M	L	K	J	H	G	F
HDMI_D1M	HDMI_D0M	HDMI_CLKM	DSI_D1P	DSI_CLK0M	DSI_D0P	CSI_D3P	CSI_D2M
HDMI_D1P	HDMI_D0P	HDMI_CLKP	DSI_D1M	DSI_CLK0P	DSI_D0M	CSI_D3M	CSI_D2P
GND	GND	GND	JTAG_TRSTB	POP_VDDQ	GND	POP_VDDQ	JTAG_MOD
GND	GND	GND	DSI_REXT	VDD_FA	CSI_REXT	NVCC_JTAG	GND
HDMI_VPH	HDMI_VP	JTAG_TDI	NVCC_MIPI	FA_ANA	PCIE_VP	PCIE_VPH	GND
						PCIE_VPTX	VDDHIGH_IN
						VDD_SNVS_CAP	VDDHIGH_IN
VDDARM23_IN	VDDARM23_IN	VDDARM23_IN	VDDARM23_IN			VDDUSB_CAP	VDDHIGH_CAP
VDDARM23_IN	VDDARM23_IN	VDDARM23_IN	VDDARM23_IN			USB_OTG_VBUS	VDDHIGH_CAP
VDDARM23_IN	VDDARM23_IN	VDDARM23_IN	VDDARM23_IN			VDD_SNVS_IN	USB_OTG_CHD_B
GND	GND	GND	GND			BOOT_MODE1	POR_B
GND	GND	GND	GND			SATA_VPH	SD3_DAT4
GND	GND	GND	GND			SATA_VP	SATA_REXT
VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN			NVCC_SD3	SD3_CMD
VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN			NANDF_CLE	SD3_DAT3
VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN			NVCC_NANDF	NANDF_CS1
VDDPU_CAP	VDDSOC_IN	VDDSOC_IN	VDDSOC_CAP			NANDF_D4	NANDF_D0
VDDPU_CAP	VDDSOC_IN	VDDSOC_IN	VDDSOC_CAP			SD4_DAT2	NANDF_D7
						NVCC_SD1	SD4_DAT4
						NVCC_SD2	SD1_DAT2
EIM_EB0	NVCC_EIM1	EIM_D31	NVCC_EIM0	EIM_D20	RGMII_RD2	NVCC_RGMII	SD2_DAT3
EIM_A17	EIM_A18	EIM_D29	EIM_D23	EIM_D16	RGMII_RXC	RGMII_TD2	SD2_DAT1
EIM_A24	POP_VDDQ	EIM_D26	EIM_EB3	POP_VDDQ	EIM_EB2	RGMII_RD0	RGMII_TD3
EIM_A23	EIM_D27	EIM_D25	EIM_D22	EIM_D18	EIM_A25	RGMII_TX_CTL	RGMII_RX_CTL
EIM_D30	EIM_D28	EIM_D24	EIM_D21	EIM_D19	EIM_D17	RGMII_RD3	RGMII_RD1