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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	4 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (1)
SATA	SATA 3Gbps (1)
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-20°C ~ 105°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	569-LFBGA
Supplier Device Package	569-MAPBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6q5ezk08ae

1.1 Ordering Information

Table 1 shows examples of orderable part numbers covered by this data sheet. This table does not include all possible orderable part numbers. The latest part numbers are available on nxp.com/imx6series. If your desired part number is not listed in the table, or you have questions about available parts, see nxp.com/imx6series or contact your NXP representative.

Table 1. Orderable Part Numbers

Part Number	Quad/Dual CPU	Options	Speed Grade	Temperature Grade	Package
MCIMX6Q5EZK08AD	i.MX 6Quad	MLB not supported	800 MHz	Extended Commercial	12 mm x 12 mm, 0.4 mm pitch, FCPBGA, Package on Package (PoP)
MCIMX6Q5EZK08AE	i.MX 6Quad	MLB not supported	800 MHz	Extended Commercial	12 mm x 12 mm, 0.4 mm pitch, FCPBGA, Package on Package (PoP)
MCIMX6Q7CZK08AD	i.MX 6Quad	MLB not supported	800 MHz	Industrial	12 mm x 12 mm, 0.4 mm pitch, FCPBGA, Package on Package (PoP)
MCIMX6Q7CZK08AE	i.MX 6Quad	MLB not supported	800 MHz	Industrial	12 mm x 12 mm, 0.4 mm pitch, FCPBGA, Package on Package (PoP)
MCIMX6D5EZK08AD	i.MX 6Dual	MLB not supported	800 MHz	Extended Commercial	12 mm x 12 mm, 0.4 mm pitch, FCPBGA, Package on Package (PoP)
MCIMX6D5EZK08AE	i.MX 6Dual	MLB not supported	800 MHz	Extended Commercial	12 mm x 12 mm, 0.4 mm pitch, FCPBGA, Package on Package (PoP)
MCIMX6D7CZK08AD	i.MX 6Dual	MLB not supported	800 MHz	Industrial	12 mm x 12 mm, 0.4 mm pitch, FCPBGA, Package on Package (PoP)
MCIMX6D7CZK08AE	i.MX 6Dual	MLB not supported	800 MHz	Industrial	12 mm x 12 mm, 0.4 mm pitch, FCPBGA, Package on Package (PoP)

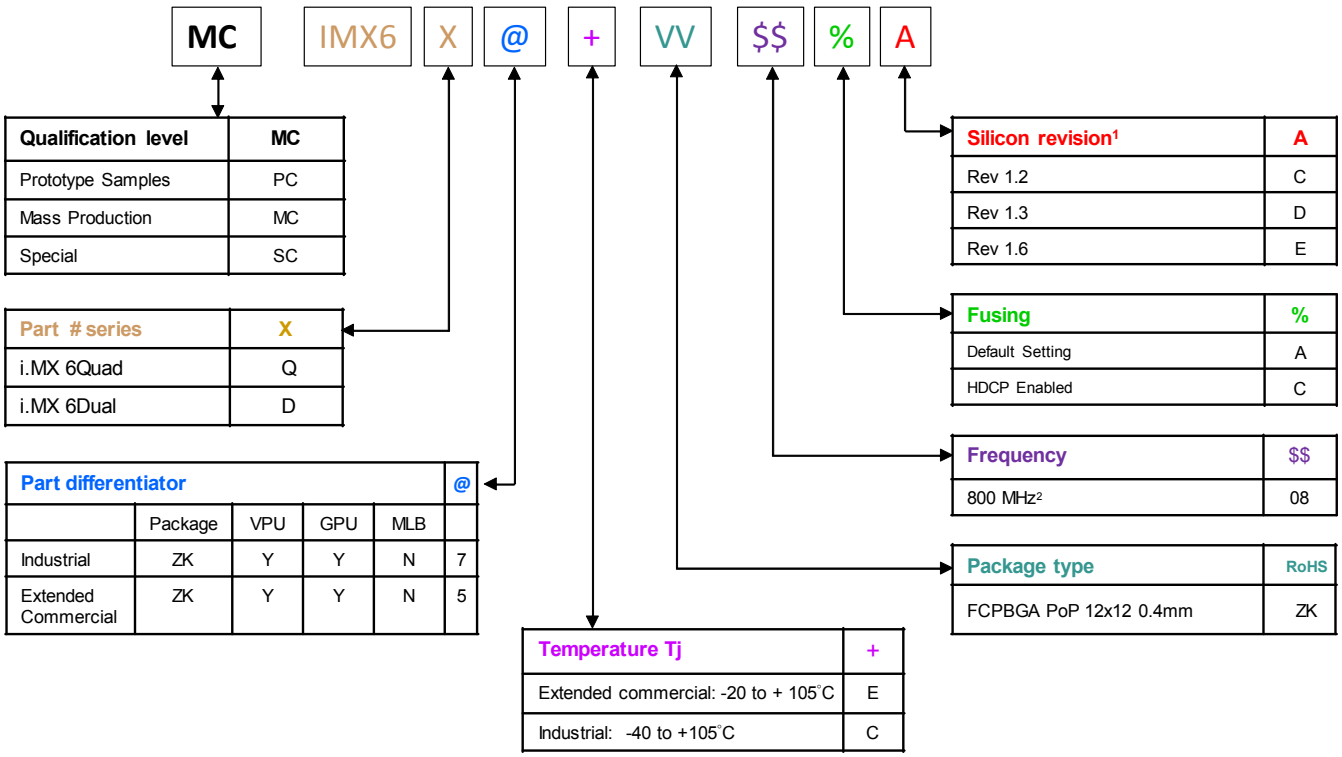
Figure 1 describes the part number nomenclature to identify the characteristics of the specific part number you have (for example, cores, frequency, temperature grade, fuse options, silicon revision). Figure 1 applies to the i.MX 6Dual/6Quad.

The two characteristics that identify which data sheet a specific part applies to are the part number series field and the temperature grade (junction) field:

- The i.MX 6Dual/6Quad Automotive and Infotainment Applications Processors data sheet (IMX6DQAEC) covers parts listed with “A (Automotive temp)”
- The i.MX 6Dual/6Quad Applications Processors for Consumer Products data sheet (IMX6DQCEC) covers parts listed with “D (Commercial temp)” or “E (Extended Commercial temp)”

- The i.MX 6Dual/6Quad Applications Processors for Consumer Products data sheet (IMX6DQCPOPEC) covers parts listed with “D (Commercial temp)” or “E (Extended Commercial temp)” and that uses the Package-on-Package.
- The i.MX 6Dual/6Quad Applications Processors for Industrial Products data sheet (IMX6DQIEC) covers parts listed with “C (Industrial temp)”

Ensure that you have the right data sheet for your specific part by checking the temperature grade (junction) field and matching it to the right data sheet. If you have questions, see nxp.com/imx6series or contact your NXP representative.



1. See the nxp.com\imx6series Web page for latest information on the available silicon revision.
2. If a 24 MHz input clock is used (required for USB), the maximum SoC speed is limited to 792 MHz.

Figure 1. Part Number Nomenclature—i.MX 6Dual PoP and 6Quad PoP

1.2 Features

The i.MX 6Dual/6Quad processors are based on ARM Cortex-A9 MPCore platform, which has the following features:

- ARM Cortex-A9 MPCore 4xCPU processor (with TrustZone®)
- The core configuration is symmetric, where each core includes:

2 Architectural Overview

The following subsections provide an architectural overview of the i.MX 6Dual/6Quad processor system.

2.1 Block Diagram

Figure 2 shows the functional modules in the i.MX 6Dual/6Quad processor system.

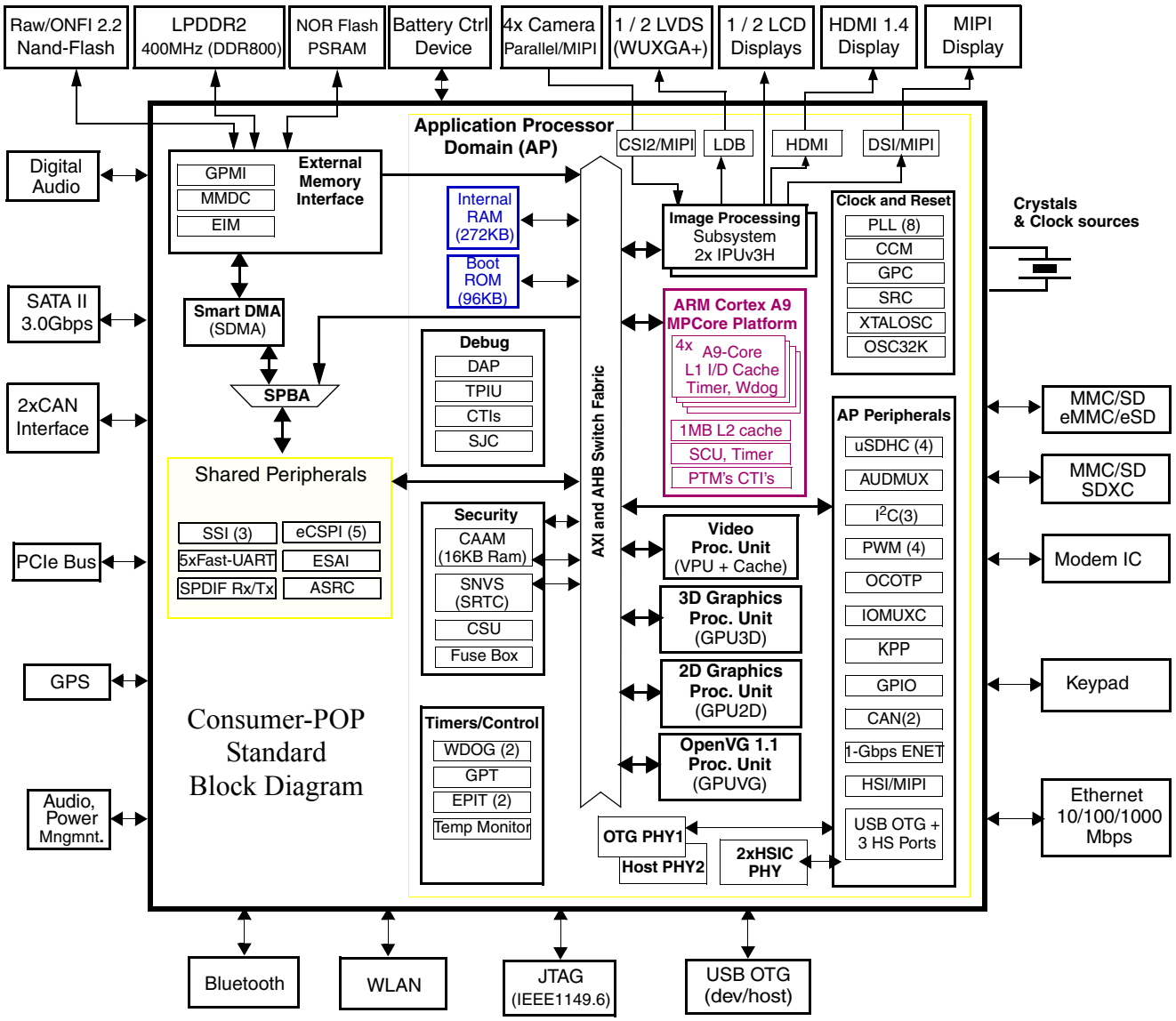


Figure 2. i.MX 6Dual/6QuadConsumer Grade System Block Diagram

NOTE

The numbers in brackets indicate number of module instances. For example, PWM (4) indicates four separate PWM peripherals.

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
ESAI	Enhanced Serial Audio Interface	Connectivity Peripherals	The Enhanced Serial Audio Interface (ESAI) provides a full-duplex serial port for serial communication with a variety of serial devices, including industry-standard codecs, SPDIF transceivers, and other processors. The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. All serial transfers are synchronized to a clock. Additional synchronization signals are used to delineate the word frames. The normal mode of operation is used to transfer data at a periodic rate, one word per period. The network mode is also intended for periodic transfers; however, it supports up to 32 words (time slots) per period. This mode can be used to build time division multiplexed (TDM) networks. In contrast, the on-demand mode is intended for non-periodic transfers of data and to transfer data serially at high speed when the data becomes available. The ESAI has 12 pins for data and clocking connection to external devices.
FlexCAN-1 FlexCAN-2	Flexible Controller Area Network	Connectivity Peripherals	The CAN protocol was primarily, but not only, designed to be used as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the Electromagnetic interference (EMI) environment of a vehicle, cost-effectiveness and required bandwidth. The FlexCAN module is a full implementation of the CAN protocol specification, Version 2.0 B, which supports both standard and extended message frames.
GPIO-1 GPIO-2 GPIO-3 GPIO-4 GPIO-5 GPIO-6 GPIO-7	General Purpose I/O Modules	System Control Peripherals	Used for general purpose input/output to external devices. Each GPIO module supports 32 bits of I/O.
GPMI	General Purpose Media Interface	Connectivity Peripherals	The GPMI module supports up to 8x NAND devices. 40-bit ECC error correction for NAND Flash controller (GPMI2). The GPMI supports separate DMA channels per NAND device.
GPT	General Purpose Timer	Timer Peripherals	Each GPT is a 32-bit “free-running” or “set and forget” mode timer with programmable prescaler and compare and capture register. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in “set and forget” mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.
GPU2Dv2	Graphics Processing Unit-2D, ver. 2	Multimedia Peripherals	The GPU2Dv2 provides hardware acceleration for 2D graphics algorithms, such as Bit BLT, stretch BLT, and many other 2D functions.
GPU3Dv4	Graphics Processing Unit-3D, ver. 4	Multimedia Peripherals	The GPU2Dv4 provides hardware acceleration for 3D graphics algorithms with sufficient processor power to run desktop quality interactive graphics applications on displays up to HD1080 resolution. The GPU3D provides OpenGL ES 2.0, including extensions, OpenGL ES 1.1, and OpenVG 1.1

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
GPUVGv2	Vector Graphics Processing Unit, ver. 2	Multimedia Peripherals	OpenVG graphics accelerator provides OpenVG 1.1 support as well as other accelerations, including Real-time hardware curve tesselation of lines, quadratic and cubic Bezier curves, 16x Line Anti-aliasing, and various Vector Drawing functions.
HDMI Tx	HDMI Tx interface	Multimedia Peripherals	The HDMI module provides HDMI standard interface port to an HDMI 1.4 compliant display.
HSI	MIPI HSI interface	Connectivity Peripherals	The MIPI HSI provides a standard MIPI interface to the applications processor.
I^2C-1 I^2C-2 I^2C-3	I^2C Interface	Connectivity Peripherals	I^2C provide serial interface for external devices. Data rates of up to 400 kbps are supported.
IOMUXC	IOMUX Control	System Control Peripherals	This module enables flexible IO multiplexing. Each IO pad has default and several alternate functions. The alternate functions are software configurable.
IPUv3H-1 IPUv3H-2	Image Processing Unit, ver. 3H	Multimedia Peripherals	IPUv3H enables connectivity to displays and video sources, relevant processing and synchronization and control capabilities, allowing autonomous operation. The IPUv3H supports concurrent output to two display ports and concurrent input from two camera ports, through the following interfaces: • Parallel Interfaces for both display and camera • Single/dual channel LVDS display interface • HDMI transmitter • MIPI/DSI transmitter • MIPI/CSI-2 receiver The processing includes: • Image conversions: resizing, rotation, inversion, and color space conversion • A high-quality de-interlacing filter • Video/graphics combining • Image enhancement: color adjustment and gamut mapping, gamma correction, and contrast enhancement • Support for display backlight reduction
KPP	Key Pad Port	Connectivity Peripherals	KPP Supports 8 x 8 external key pad matrix. KPP features are: • Open drain design • Glitch suppression circuit design • Multiple keys detection • Standby key press detection
LDB	LVDS Display Bridge	Connectivity Peripherals	LVDS Display Bridge is used to connect the IPU (Image Processing Unit) to External LVDS Display Interface. LDB supports two channels; each channel has following signals: • One clock pair • Four data pairs Each signal pair contains LVDS special differential pad (PadP, PadM).
MMDC	Multi-Mode DDR Controller	Connectivity Peripherals	DDR Controller has the following features: • Supports dual x32 for LPDDR2-800 • Supports up to 4 GByte DDR memory space

Table 6. Operating Ranges (continued)

Parameter Description	Symbol	Min	Typ	Max[1]	Unit	Comment[2]
GPIO supplies[10]	NVCC_CSI, NVCC_EIM0, NVCC_EIM1, NVCC_EIM2, NVCC_ENET, NVCC_GPIO, NVCC_LCD, NVCC_NANDF, NVCC_SD1, NVCC_SD2, NVCC_SD3, NVCC_JTAG	1.65	1.8, 2.8, 3.3	3.6	V	Isolation between the NVCC_EIMx and NVCC_SDx different supplies allow them to operate at different voltages within the specified range. Example: NVCC_EIM1 can operate at 1.8 V while NVCC_EIM2 operates at 3.3 V.
	NVCC_LVDS_2P5[11] NVCC_MIPI	2.25	2.5	2.75	V	—
HDMI supply voltages	HDMI_VP	0.99	1.1	1.3	V	—
	HDMI_VPH	2.25	2.5	2.75	V	—
PCIe supply voltages	PCIE_VP	1.023	1.1	1.3	V	—
	PCIE_VPH	2.325	2.5	2.75	V	—
	PCIE_VPTX	1.023	1.1	1.3	V	—
SATA Supply voltages	SATA_VP	0.99	1.1	1.3	V	—
	SATA_VPH	2.25	2.5	2.75	V	—
Junction temperature Extended Commercial	T_J	-20	—	105	°C	See *i.MX 6Dual/6Quad Product Lifetime Usage Estimates Application Note*, AN4724, for information on product lifetime (power-on years) for this processor.
Junction temperature Industrial	T_J	-40	—	105	°C	See *i.MX 6Dual/6Quad Product Usage Lifetime Estimates Application Note*, AN4724, for information on product lifetime (power-on years) for this processor.

1 Applying the maximum voltage results in maximum power consumption and heat generation. NXP recommends a voltage set point = (Vmin + the supply tolerance). This results in an optimized power/speed ratio.

2 See the Hardware Development Guide for i.MX 6Quad, 6Dual, 6DualLite, 6Solo Families of Applications Processors (IMX6DQ6SDLHDG) for bypass capacitors requirements for each of the *_CAP supply outputs.

3 For Quad core system, connect to VDD_ARM_IN. For Dual core system, may be shorted to GND together with VDD_ARM23_CAP to reduce leakage.

4 VDD_ARM_IN and VDD_SOC_IN must be at least 125 mV higher than the LDO Output Set Point for correct voltage regulation.

5 VDD_ARM_CAP must not exceed VDD_CACHE_CAP by more than +50 mV. VDD_CACHE_CAP must not exceed VDD_ARM_CAP by more than 200 mV.

6 VDD_SOC_CAP and VDD_PU_CAP must be equal.

7 In LDO enabled mode, the internal LDO output set points must be configured such that the:

VDD_ARM LDO output set point does not exceed the VDD_SOC LDO output set point by more than 100 mV.

VDD_SOC LDO output set point is equal to the VDD_PU LDO output set point.

The VDD_ARM LDO output set point can be lower than the VDD_SOC LDO output set point, however, the minimum output set points shown in this table must be maintained.

4.9.3.2 General EIM Timing-Synchronous Mode

Figure 10, Figure 11, and Table 35 specify the timings related to the EIM module. All EIM output control signals may be asserted and deasserted by an internal clock synchronized to the EIM_BCLK rising edge according to corresponding assertion/negation control fields.

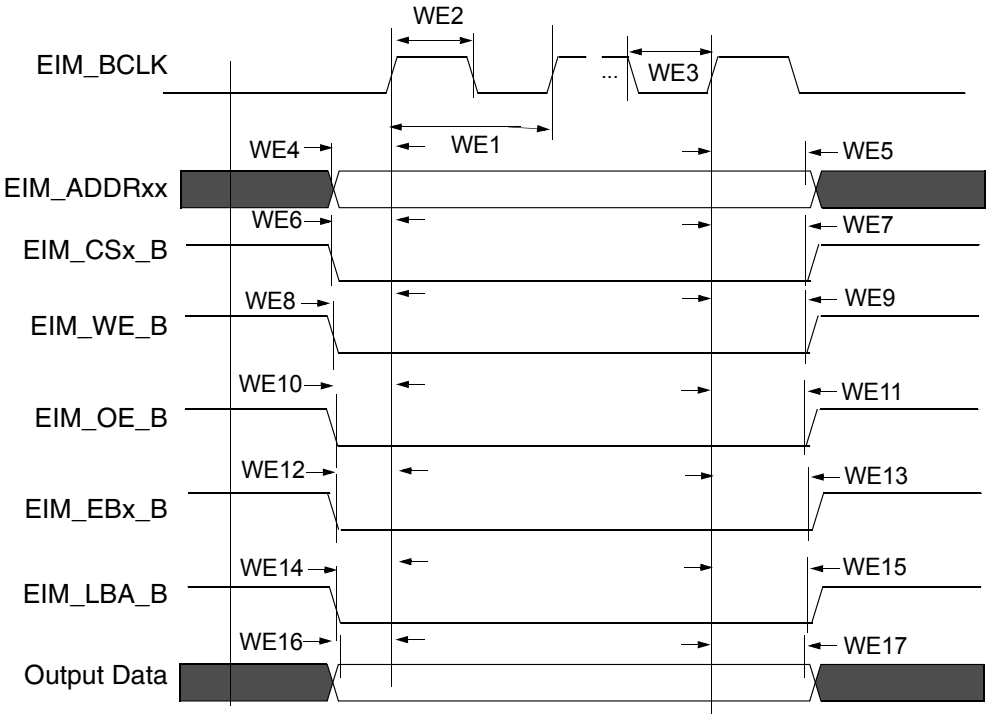


Figure 10. EIM Output Timing Diagram

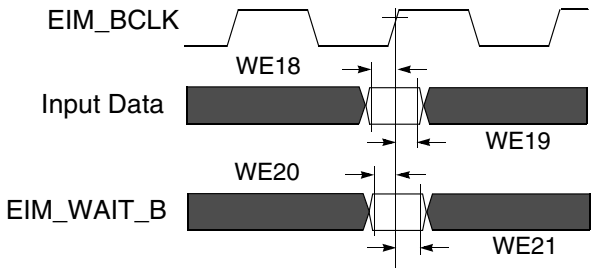


Figure 11. EIM Input Timing Diagram

4.9.3.3 Examples of EIM Synchronous Accesses

Table 35. EIM Bus Timing Parameters

ID	Parameter	Min[1]	Max[1]	Unit
WE1	EIM_BCLK cycle time[2]	t × (k+1)	—	ns
WE2	EIM_BCLK high level width	0.4 × t × (k+1)	—	ns
WE3	EIM_BCLK low level width	0.4 × t × (k+1)	—	ns

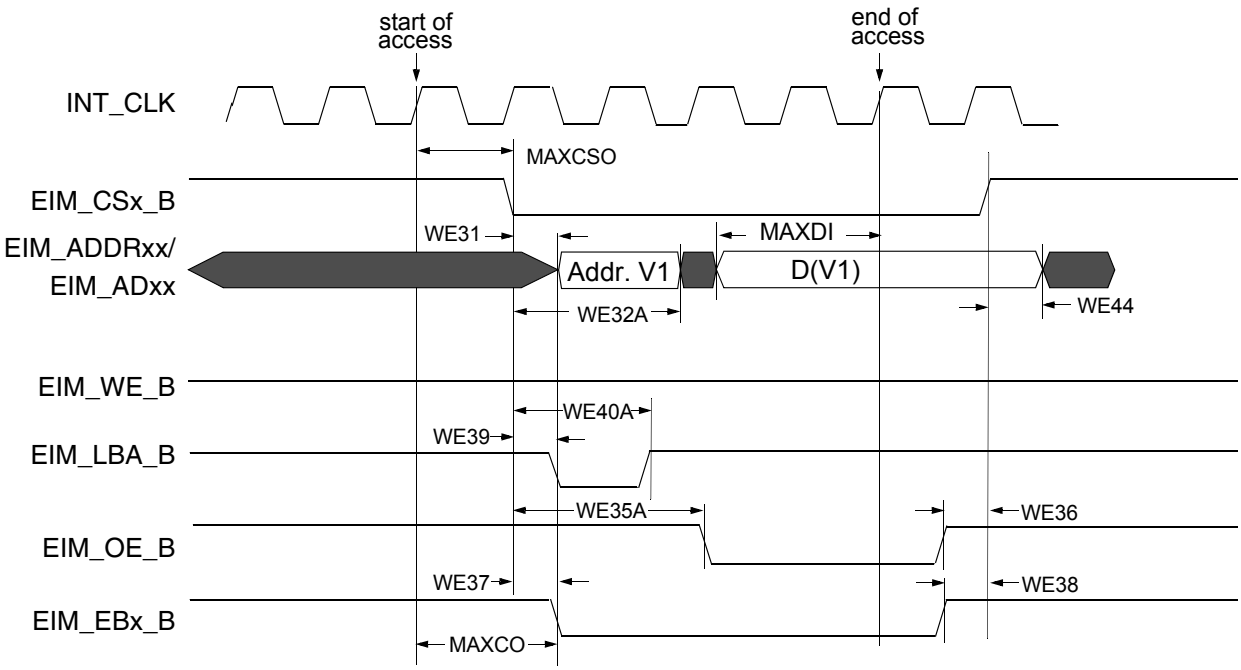


Figure 17. Asynchronous A/D Muxed Read Access (RWSC = 5)

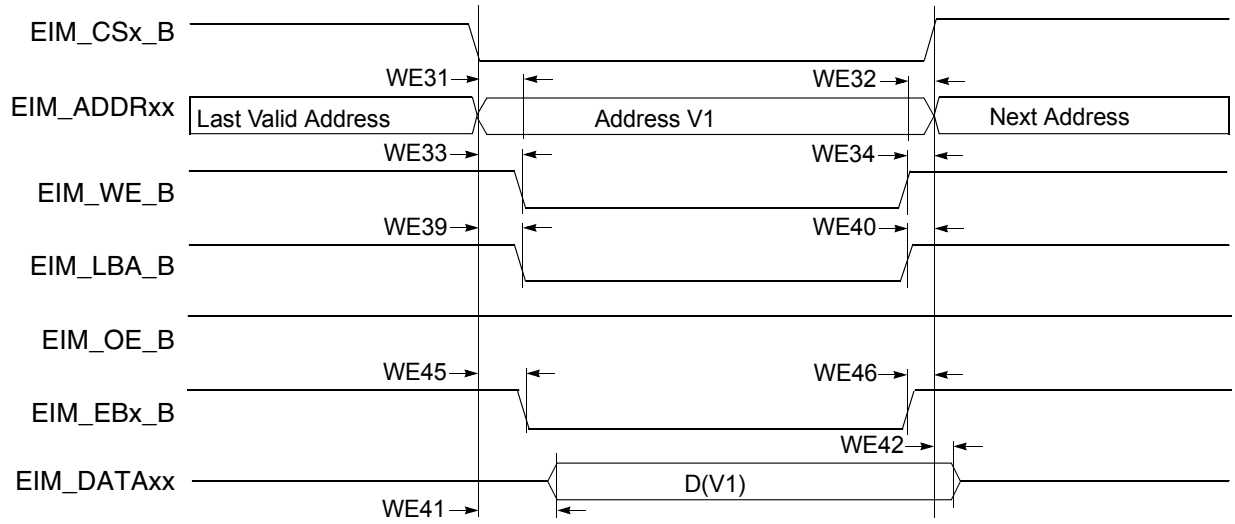


Figure 18. Asynchronous Memory Write Access

4.12.3 Enhanced Serial Audio Interface (ESAI) Timing Parameters

The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. Table 43 shows the interface timing values. The number field in the table refers to timing signals found in Figure 35 and Figure 36.

Table 43. Enhanced Serial Audio Interface (ESAI) Timing

ID	Parameter[1,2]	Symbol	Expression[2]	Min	Max	Condition[3]	Unit
62	Clock cycle[4]	t_{SSICC}	$4 \times T_C$ $4 \times T_C$	30.0 30.0	— —	i ck i ck	ns
63	Clock high period: • For internal clock • For external clock	— —	$2 \times T_C - 9.0$ $2 \times T_C$	6 15	— —	— —	ns
64	Clock low period: • For internal clock • For external clock	— —	$2 \times T_C - 9.0$ $2 \times T_C$	6 15	— —	— —	ns
65	ESAI_RX_CLK rising edge to ESAI_RX_FS out (bl) high	— —	— —	— —	19.0 7.0	x ck i ck a	ns
66	ESAI_RX_CLK rising edge to ESAI_RX_FS out (bl) low	— —	— —	— —	19.0 7.0	x ck i ck a	ns
67	ESAI_RX_CLK rising edge to ESAI_RX_FS out (wr) high[5]	— —	— —	— —	19.0 9.0	x ck i ck a	ns
68	ESAI_RX_CLK rising edge to ESAI_RX_FS out (wr) low[5]	— —	— —	— —	19.0 9.0	x ck i ck a	ns
69	ESAI_RX_CLK rising edge to ESAI_RX_FS out (wl) high	— —	— —	— —	19.0 6.0	x ck i ck a	ns
70	ESAI_RX_CLK rising edge to ESAI_RX_FSout (wl) low	— —	— —	— —	17.0 7.0	x ck i ck a	ns
71	Data in setup time before ESAI_RX_CLK (serial clock in synchronous mode) falling edge	— —	— —	12.0 19.0	— —	x ck i ck	ns
72	Data in hold time after ESAI_RX_CLK falling edge	— —	— —	3.5 9.0	— —	x ck i ck	ns
73	ESAI_RX_FS input (bl, wr) high before ESAI_RX_CLK falling edge[5]	— —	— —	2.0 19.0	— —	x ck i ck a	ns
74	ESAI_RX_FS input (wl) high before ESAI_RX_CLK falling edge	— —	— —	2.0 19.0	— —	x ck i ck a	ns
75	ESAI_RX_FS input hold time after ESAI_RX_CLK falling edge	— —	— —	2.5 8.5	— —	x ck i ck a	ns
78	ESAI_TX_CLK rising edge to ESAI_TX_FS out (bl) high	— —	— —	— —	19.0 8.0	x ck i ck	ns
79	ESAI_TX_CLK rising edge to ESAI_TX_FS out (bl) low	— —	— —	— —	20.0 10.0	x ck i ck	ns
80	ESAI_TX_CLK rising edge to ESAI_TX_FS out (wr) high[5]	— —	— —	— —	20.0 10.0	x ck i ck	ns

Table 43. Enhanced Serial Audio Interface (ESAI) Timing (continued)

ID	Parameter[1,2]	Symbol	Expression[2]	Min	Max	Condition[3]	Unit
81	ESAI_TX_CLK rising edge to ESAI_TX_FS out (wr) low[5]	— —	— —	— —	22.0 12.0	x ck i ck	ns
82	ESAI_TX_CLK rising edge to ESAI_TX_FS out (wl) high	— —	— —	— —	19.0 9.0	x ck i ck	ns
83	ESAI_TX_CLK rising edge to ESAI_TX_FS out (wl) low	— —	— —	— —	20.0 10.0	x ck i ck	ns
84	ESAI_TX_CLK rising edge to data out enable from high impedance	— —	— —	— —	22.0 17.0	x ck i ck	ns
86	ESAI_TX_CLK rising edge to data out valid	— —	— —	— —	19.0 13.0	x ck i ck	ns
87	ESAI_TX_CLK rising edge to data out high impedance [67]	— —	— —	— —	21.0 16.0	x ck i ck	ns
89	ESAI_TX_FS input (bl, wr) setup time before ESAI_TX_CLK falling edge[5]	— —	— —	2.0 18.0	— —	x ck i ck	ns
90	ESAI_TX_FS input (wl) setup time before ESAI_TX_CLK falling edge	— —	— —	2.0 18.0	— —	x ck i ck	ns
91	ESAI_TX_FS input hold time after ESAI_TX_CLK falling edge	— —	— —	4.0 5.0	— —	x ck i ck	ns
95	ESAI_RX_HF_CLK/ESAI_TX_HF_CLK clock cycle	—	$2 \times T_C$	15	—	—	ns
96	ESAI_TX_HF_CLK input rising edge to ESAI_TX_CLK output	—	—	—	18.0	—	ns
97	ESAI_RX_HF_CLK input rising edge to ESAI_RX_CLK output	—	—	—	18.0	—	ns

1 i ck = internal clock
x ck = external clock
i ck a = internal clock, asynchronous mode
(asynchronous implies that ESAI_TX_CLK and ESAI_RX_CLK are two different clocks)
i ck s = internal clock, synchronous mode
(synchronous implies that ESAI_TX_CLK and ESAI_RX_CLK are the same clock)

2 bl = bit length
wl = word length
wr = word length relative

3 ESAI_TX_CLK(ESAI_TX_CLK pin) = transmit clock
ESAI_RX_CLK(ESAI_RX_CLK pin) = receive clock
ESAI_TX_FS(ESAI_TX_FS pin) = transmit frame sync
ESAI_RX_FS(ESAI_RX_FS pin) = receive frame sync
ESAI_TX_HF_CLK(ESAI_TX_HF_CLK pin) = transmit high frequency clock
ESAI_RX_HF_CLK(ESAI_RX_HF_CLK pin) = receive high frequency clock

4 For the internal clock, the external clock cycle is defined by Icyc and the ESAI control register.

5 The word-relative frame sync signal waveform relative to the clock operates in the same manner as the bit-length frame sync signal waveform, but it spreads from one serial clock before the first bit clock (like the bit length frame sync signal), until the second-to-last bit clock of the first word in the frame.

6 Periodically sampled and not 100% tested.

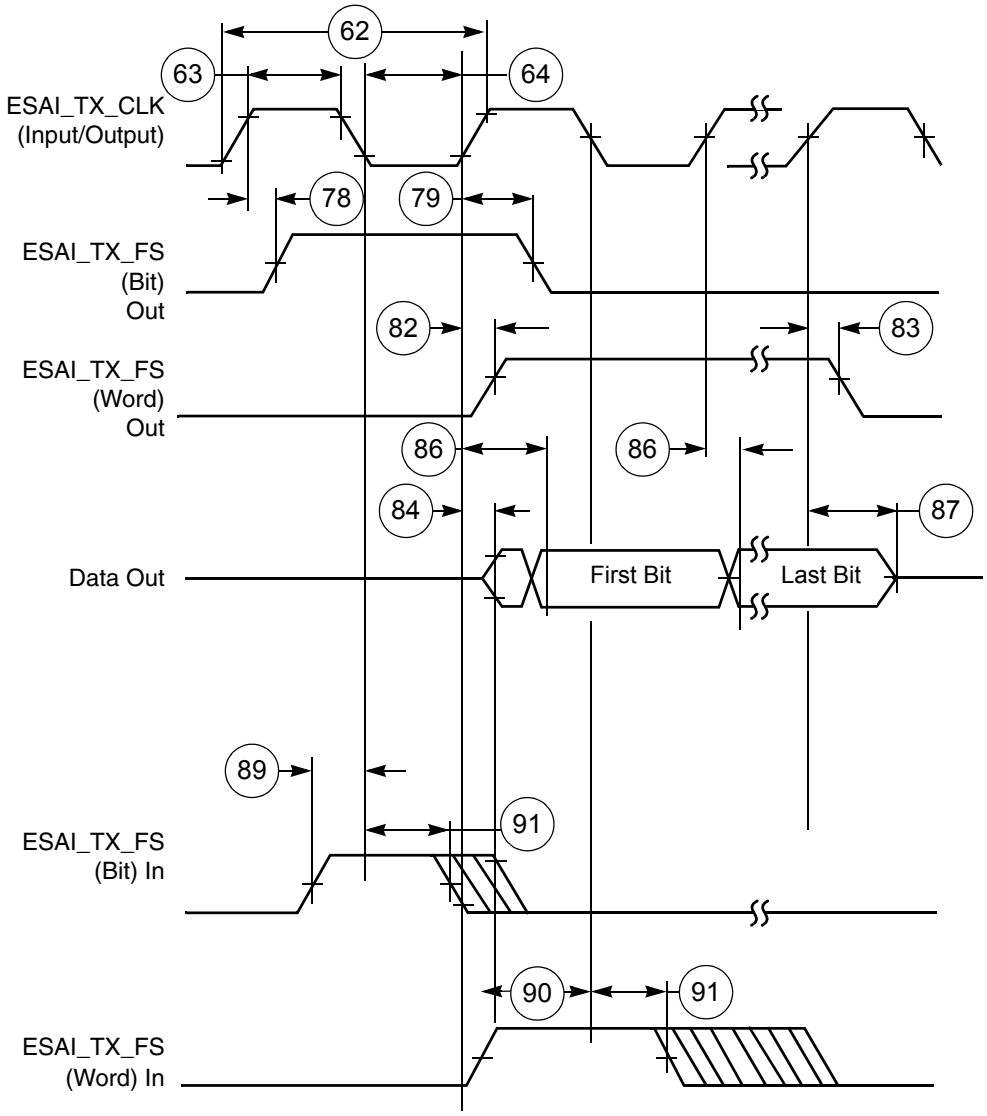


Figure 35. ESAI Transmitter Timing

Table 44. SD/eMMC4.3 Interface Timing Specification (continued)

ID	Parameter	Symbols	Min	Max	Unit
eSDHC Input/Card Outputs SD_CMD, SD_DATAx (Reference to SDx_CLK)					
SD7	eSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD8	eSDHC Input Hold Time[4]	t_{IH}	1.5	—	ns

1 In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

2 In normal (full) speed mode for SD/SDIO card, clock frequency can be any value between 0—25 MHz. In high-speed mode, clock frequency can be any value between 0—50 MHz.

3 In normal (full) speed mode for MMC card, clock frequency can be any value between 0—20 MHz. In high-speed mode, clock frequency can be any value between 0—52 MHz.

4 To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

4.12.4.2 eMMC4.4/4.41 (Dual Data Rate) eSDHCv3 AC Timing

Figure 38 depicts the timing of eMMC4.4/4.41. Table 45 lists the eMMC4.4/4.41 timing characteristics. Be aware that only SDx_DATAx is sampled on both edges of the clock (not applicable to SD_CMD).

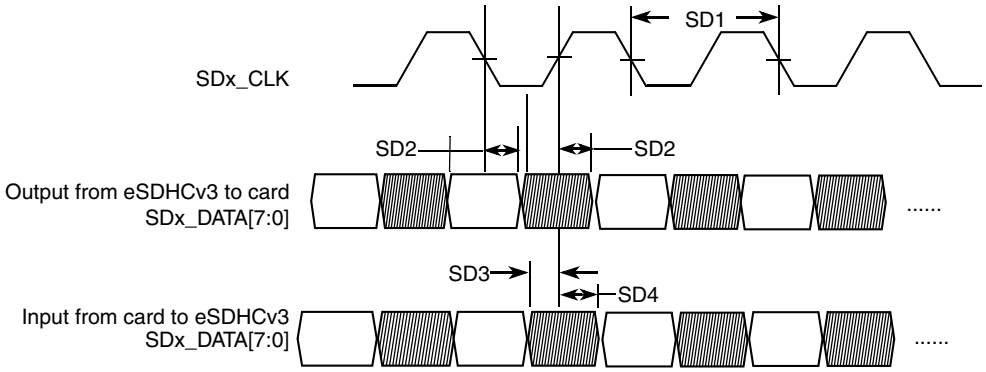


Figure 38. eMMC4.4/4.41 Timing

Table 45. eMMC4.4/4.41 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock[1]					
SD1	Clock Frequency (EMMC4.4 DDR)	f_{PP}	0	52	MHz
SD1	Clock Frequency (SD3.0 DDR)	f_{PP}	0	50	MHz
uSDHC Output / Card Inputs SD_CMD, SD_DATAx (Reference to SD_CLK)					
SD2	uSDHC Output Delay	t_{OD}	2.5	7.1	ns
uSDHC Input / Card Outputs SD_CMD, SD_DATAx (Reference to SD_CLK)					
SD3	uSDHC Input Setup Time	t_{ISU}	1.7	—	ns
SD4	uSDHC Input Hold Time	t_{IH}	1.5	—	ns

1 Clock duty cycle will be in the range of 47% to 53%.

4.12.10.3 Electrical Characteristics

Figure 59 depicts the sensor interface timing. IPU2_CSIx_PIX_CLK signal described here is not generated by the IPU. Table 57 lists the sensor interface timing characteristics.

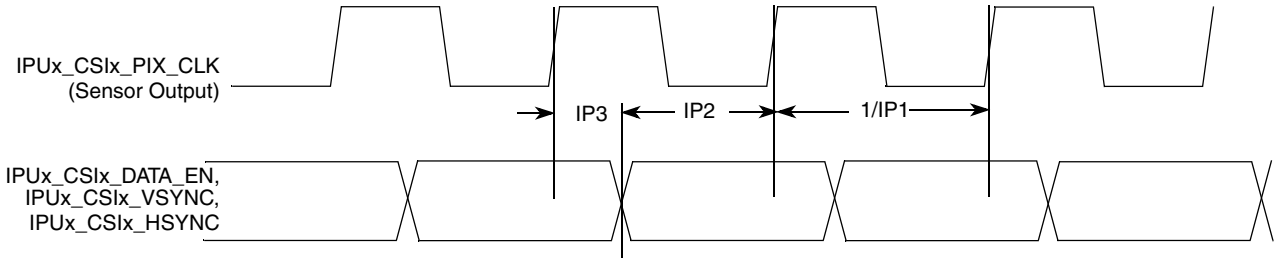


Figure 59. Sensor Interface Timing Diagram

Table 57. Sensor Interface Timing Characteristics

ID	Parameter	Symbol	Min	Max	Unit
IP1	Sensor output (pixel) clock frequency	Fpck	0.01	180	MHz
IP2	Data and control setup time	Tsu	2	—	ns
IP3	Data and control holdup time	Thd	1	—	ns
—	Vsync to Hsync	Tv-h	1/Fpck	—	ns
—	Vsync and Hsync pulse width	Tpulse	1/Fpck	—	ns
—	Vsync to first data	Tv-d	1/Fpck	—	ns

4.12.10.4 IPU Display Interface Signal Mapping

The IPU supports a number of display output video formats. Table 58 defines the mapping of the Display Interface Pins used during various supported video interface formats.

Table 58. Video Signal Cross-Reference

i.MX 6Dual/6Quad	LCD							Comment[1,2]
Port Name (x = 0, 1)	RGB, Signal Name (General)	RGB/TV Signal Allocation (Example)						
		16-bit RGB	18-bit RGB	24 Bit RGB	8-bit YCrCb[3]	16-bit YCrCb	20-bit YCrCb	
IPUx_DISPx_DAT00	DAT[0]	B[0]	B[0]	B[0]	Y/C[0]	C[0]	C[0]	—
IPUx_DISPx_DAT01	DAT[1]	B[1]	B[1]	B[1]	Y/C[1]	C[1]	C[1]	—
IPUx_DISPx_DAT02	DAT[2]	B[2]	B[2]	B[2]	Y/C[2]	C[2]	C[2]	—
IPUx_DISPx_DAT03	DAT[3]	B[3]	B[3]	B[3]	Y/C[3]	C[3]	C[3]	—
IPUx_DISPx_DAT04	DAT[4]	B[4]	B[4]	B[4]	Y/C[4]	C[4]	C[4]	—

4.12.10.6.2 LCD Interface Functional Description

Figure 60 depicts the LCD interface timing for a generic active matrix color TFT panel. In this figure, signals are shown with negative polarity. The sequence of events for active matrix interface timing is:

- DI_CLK internal DI clock is used for calculation of other controls.
- IPP_DISP_CLK latches data into the panel on its negative edge (when positive polarity is selected). In active mode, IPP_DISP_CLK runs continuously.
- HSYNC causes the panel to start a new line. (Usually IPUx_DIx_PIN02 is used as HSYNC.)
- VSYNC causes the panel to start a new frame. It always encompasses at least one HSYNC pulse. (Usually IPUx_DIx_PIN03 is used as VSYNC.)
- DRDY acts like an output enable signal to the CRT display. This output enables the data to be shifted onto the display. When disabled, the data is invalid and the trace is off.
  (DRDY can be used either synchronous or asynchronous generic purpose pin as well.)

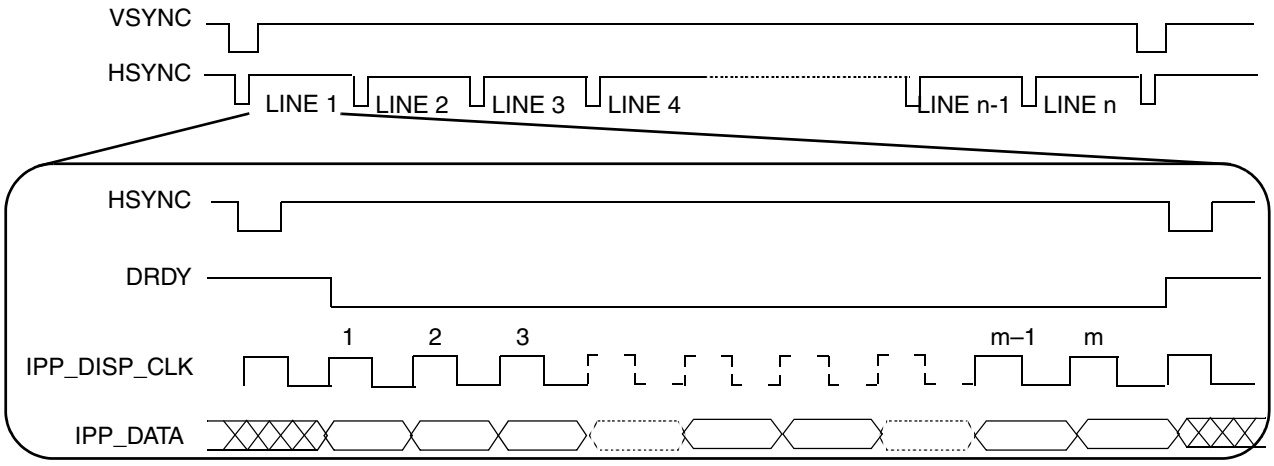


Figure 60. Interface Timing Diagram for TFT (Active Matrix) Panels

4.12.10.6.3 TFT Panel Sync Pulse Timing Diagrams

Figure 61 depicts the horizontal timing (timing of one line), including both the horizontal sync pulse and the data. All the parameters shown in the figure are programmable. All controls are started by corresponding internal events—local start points. The timing diagrams correspond to inverse polarity of the IPP_DISP_CLK signal and active-low polarity of the HSYNC, VSYNC, and DRDY signals.

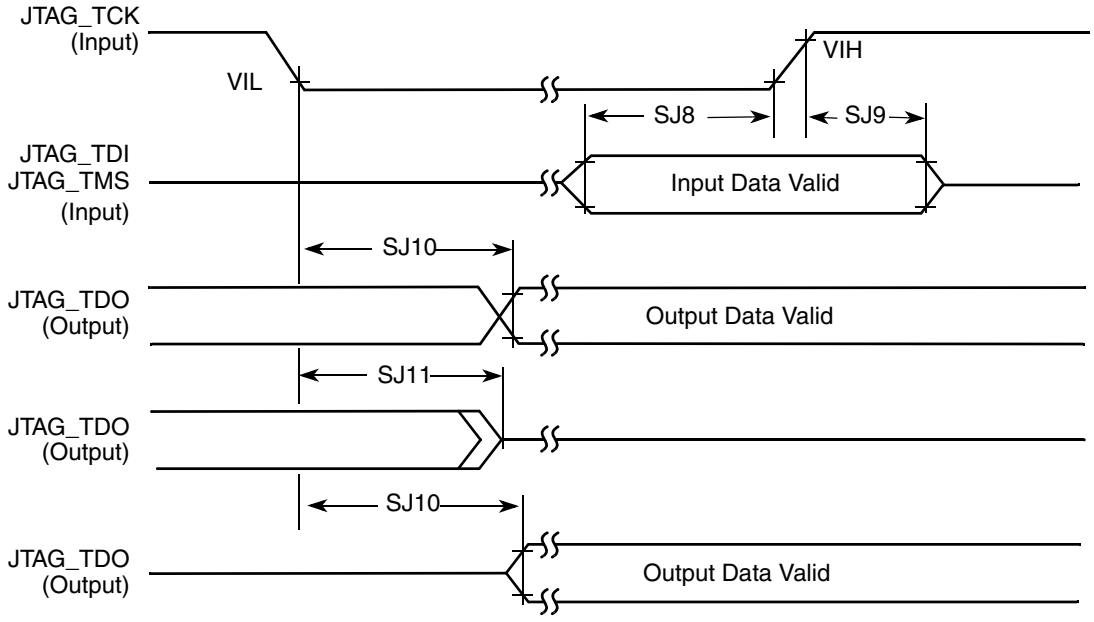


Figure 82. Test Access Port Timing Diagram

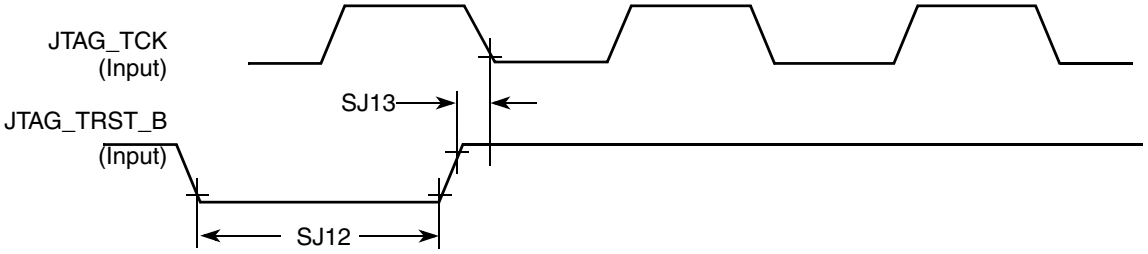


Figure 83. JTAG_TRST_B Timing Diagram

Table 68. JTAG Timing

ID	Parameter[1,2]	All Frequencies		Unit
		Min	Max	
SJ0	JTAG_TCK frequency of operation $1/(3xT_{DC})$[1]	0.001	22	MHz
SJ1	JTAG_TCK cycle time in crystal mode	45	—	ns
SJ2	JTAG_TCK clock pulse width measured at V_M[2]	22.5	—	ns
SJ3	JTAG_TCK rise and fall times	—	3	ns
SJ4	Boundary scan input data set-up time	5	—	ns
SJ5	Boundary scan input data hold time	24	—	ns
SJ6	JTAG_TCK low to output data valid	—	40	ns
SJ7	JTAG_TCK low to output high impedance	—	40	ns
SJ8	JTAG_TMS, JTAG_TDI data set-up time	5	—	ns

Table 72. SSI Receiver Timing with Internal Clock (continued)

ID	Parameter	Min	Max	Unit
Oversampling Clock Operation				
SS47	Oversampling clock period	15.04	—	ns
SS48	Oversampling clock high period	6.0	—	ns
SS49	Oversampling clock rise time	—	3.0	ns
SS50	Oversampling clock low period	6.0	—	ns
SS51	Oversampling clock fall time	—	3.0	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal AUDx_TXC/AUDx_RXC and/or the frame sync AUDx_TXFS/AUDx_RXFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- AUDx_TXC and AUDx_RXC refer to the Transmit and Receive sections of the SSI.
- The terms, WL and BL, refer to Word Length (WL) and Bit Length(BL).
- For internal Frame Sync operation using external clock, the frame sync timing is same as that of transmit data (for example, during AC97 mode of operation).

4.12.20.2 UART RS-232 Serial Mode Timing

The following sections describe the electrical information of the UART module in the RS-232 mode.

4.12.20.2.1 UART Transmitter

Figure 90 depicts the transmit timing of UART in the RS-232 serial mode, with 8 data bit/1 stop bit format. Table 76 lists the UART RS-232 serial mode transmit timing characteristics.

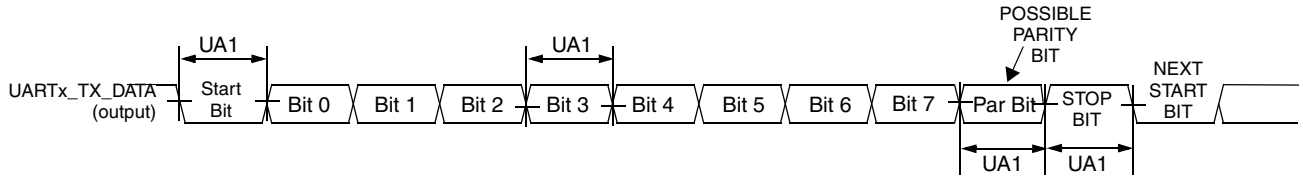


Figure 90. UART RS-232 Serial Mode Transmit Timing Diagram

Table 76. RS-232 Serial Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA1	Transmit Bit Time	t_{Tbit}	$1/F_{baud\_rate}$ [1] – T_{ref_clk} [2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—

[1] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

[2] T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

4.12.20.2.2 UART Receiver

Figure 91 depicts the RS-232 serial mode receive timing with 8 data bit/1 stop bit format. Table 77 lists serial mode receive timing characteristics.

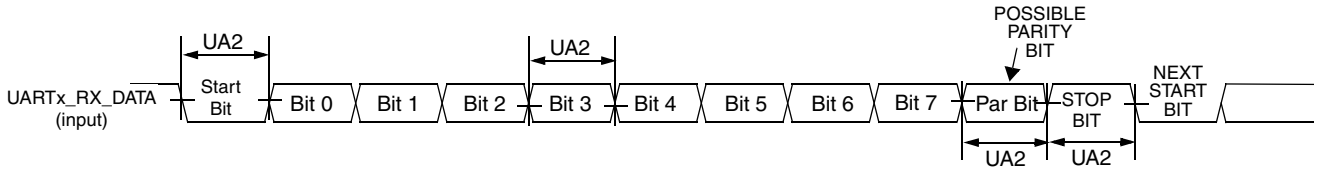


Figure 91. UART RS-232 Serial Mode Receive Timing Diagram

Table 77. RS-232 Serial Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA2	Receive Bit Time[1]	t_{Rbit}	$1/F_{baud\_rate}$ [2] – $1/(16 \times F_{baud\_rate})$	$1/F_{baud\_rate} + 1/(16 \times F_{baud\_rate})$	—

[1] The UART receiver can tolerate $1/(16 \times F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud\_rate})$.

[2] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK AND LANDING PADS ON TOP SURFACE OF PACKAGE.

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	STANDARD: NON–JEDEC	
	SOT1644–1	29 FEB 2016

Figure 97. 12 x 12 mm PoP Package Top, Bottom, and Side Views (Sheet 2 of 2)

Table 85. 12 x 12 mm Functional Contact Assignments (continued)

Ball Name	PoP Bottom Ball	PoP Top Ball	Power Group	Ball Type	Out of Reset Condition[1]			
					Default Mode	Default Function	Input/ Output	Value[2]
DRAM_CLKP1_B	—	AH21	NVCC_DRAM	—	—	LPDDR2_CK_P1_B	—	—
DRAM_CS0P0	—	Y28	NVCC_DRAM	DDR	ALT0	LPDDR2_CS_B0_P0	Output	0
DRAM_CS1P0	—	W29	NVCC_DRAM	DDR	ALT0	LPDDR2_CS_B1_P0	Output	0
DRAM_CS0P1	—	AH24	NVCC_DRAM	DDR	ALT0	LPDDR2_CS_B0_P1	Output	0
DRAM_CS1P1	—	AJ24	NVCC_DRAM	DDR	ALT0	LPDDR2_CS_B1_P1	Output	0
DRAM_D0P0	—	U2	NVCC_DRAM	DDR	ALT0	DRAM_DATA00	Input	PU (100k)
DRAM_D1P0	—	N1	NVCC_DRAM	DDR	ALT0	DRAM_DATA01	Input	PU (100k)
DRAM_D2P0	—	M1	NVCC_DRAM	DDR	ALT0	DRAM_DATA02	Input	PU (100k)
DRAM_D3P0	—	Y2	NVCC_DRAM	DDR	ALT0	DRAM_DATA03	Input	PU (100k)
DRAM_D4P0	—	V1	NVCC_DRAM	DDR	ALT0	DRAM_DATA04	Input	PU (100k)
DRAM_D5P0	—	W1	NVCC_DRAM	DDR	ALT0	DRAM_DATA05	Input	PU (100k)
DRAM_D6P0	—	W2	NVCC_DRAM	DDR	ALT0	DRAM_DATA06	Input	PU (100k)
DRAM_D7P0	—	L2	NVCC_DRAM	DDR	ALT0	DRAM_DATA07	Input	PU (100k)
DRAM_D8P0	—	AJ3	NVCC_DRAM	DDR	ALT0	DRAM_DATA08	Input	PU (100k)
DRAM_D9P0	—	AH4	NVCC_DRAM	DDR	ALT0	DRAM_DATA09	Input	PU (100k)
DRAM_D10P0	—	AG1	NVCC_DRAM	DDR	ALT0	DRAM_DATA10	Input	PU (100k)
DRAM_D11P0	—	AH6	NVCC_DRAM	DDR	ALT0	DRAM_DATA11	Input	PU (100k)
DRAM_D12P0	—	AE1	NVCC_DRAM	DDR	ALT0	DRAM_DATA12	Input	PU (100k)
DRAM_D13P0	—	AG2	NVCC_DRAM	DDR	ALT0	DRAM_DATA13	Input	PU (100k)
DRAM_D14P0	—	AF1	NVCC_DRAM	DDR	ALT0	DRAM_DATA14	Input	PU (100k)
DRAM_D15P0	—	AJ5	NVCC_DRAM	DDR	ALT0	DRAM_DATA15	Input	PU (100k)
DRAM_D16P0	—	H2	NVCC_DRAM	DDR	ALT0	DRAM_DATA16	Input	PU (100k)
DRAM_D17P0	—	F2	NVCC_DRAM	DDR	ALT0	DRAM_DATA17	Input	PU (100k)
DRAM_D18P0	—	C2	NVCC_DRAM	DDR	ALT0	DRAM_DATA18	Input	PU (100k)
DRAM_D19P0	—	E1	NVCC_DRAM	DDR	ALT0	DRAM_DATA19	Input	PU (100k)
DRAM_D20P0	—	H1	NVCC_DRAM	DDR	ALT0	DRAM_DATA20	Input	PU (100k)
DRAM_D21P0	—	G1	NVCC_DRAM	DDR	ALT0	DRAM_DATA21	Input	PU (100k)
DRAM_D22P0	—	E2	NVCC_DRAM	DDR	ALT0	DRAM_DATA22	Input	PU (100k)
DRAM_D23P0	—	D1	NVCC_DRAM	DDR	ALT0	DRAM_DATA23	Input	PU (100k)
DRAM_D24P0	—	AH11	NVCC_DRAM	DDR	ALT0	DRAM_DATA24	Input	PU (100k)
DRAM_D25P0	—	AJ9	NVCC_DRAM	DDR	ALT0	DRAM_DATA25	Input	PU (100k)
DRAM_D26P0	—	AJ14	NVCC_DRAM	DDR	ALT0	DRAM_DATA26	Input	PU (100k)
DRAM_D27P0	—	AJ12	NVCC_DRAM	DDR	ALT0	DRAM_DATA27	Input	PU (100k)
DRAM_D28P0	—	AH10	NVCC_DRAM	DDR	ALT0	DRAM_DATA28	Input	PU (100k)
DRAM_D29P0	—	AJ10	NVCC_DRAM	DDR	ALT0	DRAM_DATA29	Input	PU (100k)
DRAM_D30P0	—	AJ13	NVCC_DRAM	DDR	ALT0	DRAM_DATA30	Input	PU (100k)
DRAM_D31P0	—	AH13	NVCC_DRAM	DDR	ALT0	DRAM_DATA31	Input	PU (100k)
DRAM_D0P1	—	B3	NVCC_DRAM	DDR	ALT0	DRAM_DATA32	Input	PU (100k)
DRAM_D1P1	—	A7	NVCC_DRAM	DDR	ALT0	DRAM_DATA33	Input	PU (100k)
DRAM_D2P1	—	A4	NVCC_DRAM	DDR	ALT0	DRAM_DATA34	Input	PU (100k)

Table 85. 12 x 12 mm Functional Contact Assignments (continued)

Ball Name	PoP Bottom Ball	PoP Top Ball	Power Group	Ball Type	Out of Reset Condition[1]			
					Default Mode	Default Function	Input/ Output	Value[2]
DRAM_DQS1P0_B	—	AD1	NVCC_DRAM	DDRCLK	—	DRAM_SDQS1_N	—	—
DRAM_DQS2P0	—	K2	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS2_P	Input	Hi-Z
DRAM_DQS2P0_B	—	K1	NVCC_DRAM	DDRCLK	—	DRAM_SDQS2_N	—	—
DRAM_DQS3P0	—	AH8	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS3_P	Input	Hi-Z
DRAM_DQS3P0_B	—	AJ8	NVCC_DRAM	DDRCLK	—	DRAM_SDQS3_N	—	—
DRAM_DQS0P1	—	B10	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS4_P	Input	Hi-Z
DRAM_DQS0P1_B	—	A10	NVCC_DRAM	DDRCLK	—	DRAM_SDQS4_N	—	—
DRAM_DQS1P1	—	A20	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS5_P	Input	Hi-Z
DRAM_DQS1P1_B	—	B20	NVCC_DRAM	DDRCLK	—	DRAM_SDQS5_N	—	—
DRAM_DQS2P1	—	A23	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS6_P	Input	Hi-Z
DRAM_DQS2P1_B	—	B23	NVCC_DRAM	DDRCLK	—	DRAM_SDQS6_N	—	—
DRAM_DQS3P1	—	G28	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS7_P	Input	Hi-Z
DRAM_DQS3P1_B	—	G29	NVCC_DRAM	DDRCLK	—	DRAM_SDQS7_N	—	—
DSI_CLK0M	J1	—	NVCC_MIPI	—	—	DSI_CLK_N	—	—
DSI_CLK0P	J2	—	NVCC_MIPI	—	—	DSI_CLK_P	—	—
DSI_D0M	H2	—	NVCC_MIPI	—	—	DSI_DATA0_N	—	—
DSI_D0P	H1	—	NVCC_MIPI	—	—	DSI_DATA0_P	—	—
DSI_D1M	K2	—	NVCC_MIPI	—	—	DSI_DATA1_N	—	—
DSI_D1P	K1	—	NVCC_MIPI	—	—	DSI_DATA1_P	—	—
EIM_A16	T29	—	NVCC_EIM1	GPIO	ALT0	EIM_ADDR16	Output	0
EIM_A17	N24	—	NVCC_EIM1	GPIO	ALT0	EIM_ADDR17	Output	0
EIM_A18	M24	—	NVCC_EIM1	GPIO	ALT0	EIM_ADDR18	Output	0
EIM_A19	R28	—	NVCC_EIM1	GPIO	ALT0	EIM_ADDR19	Output	0
EIM_A20	R29	—	NVCC_EIM1	GPIO	ALT0	EIM_ADDR20	Output	0
EIM_A21	P29	—	NVCC_EIM1	GPIO	ALT0	EIM_ADDR21	Output	0
EIM_A22	P28	—	NVCC_EIM1	GPIO	ALT0	EIM_ADDR22	Output	0
EIM_A23	N28	—	NVCC_EIM1	GPIO	ALT0	EIM_ADDR23	Output	0
EIM_A24	N27	—	NVCC_EIM1	GPIO	ALT0	EIM_ADDR24	Output	0
EIM_A25	H28	—	NVCC_EIM0	GPIO	ALT0	EIM_ADDR25	Output	0
EIM_BCLK	AA27	—	NVCC_EIM2	GPIO	ALT0	EIM_BCLK	Output	0
EIM_CS0	U29	—	NVCC_EIM1	GPIO	ALT0	EIM_CS0_B	Output	1
EIM_CS1	U28	—	NVCC_EIM1	GPIO	ALT0	EIM_CS1_B	Output	1
EIM_D16	J24	—	NVCC_EIM0	GPIO	ALT5	GPIO3_IO16	Input	PU (100k)
EIM_D17	H29	—	NVCC_EIM0	GPIO	ALT5	GPIO3_IO17	Input	PU (100k)
EIM_D18	J28	—	NVCC_EIM0	GPIO	ALT5	GPIO3_IO18	Input	PU (100k)
EIM_D19	J29	—	NVCC_EIM0	GPIO	ALT5	GPIO3_IO19	Input	PU (100k)
EIM_D20	J23	—	NVCC_EIM0	GPIO	ALT5	GPIO3_IO20	Input	PU (100k)
EIM_D21	K29	—	NVCC_EIM0	GPIO	ALT5	GPIO3_IO21	Input	PU (100k)
EIM_D22	K28	—	NVCC_EIM0	GPIO	ALT5	GPIO3_IO22	Input	PU (100k)
EIM_D23	K24	—	NVCC_EIM0	GPIO	ALT5	GPIO3_IO23	Input	PU (100k)