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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	4 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (1)
SATA	SATA 3Gbps (1)
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	569-LFBGA
Supplier Device Package	569-MAPBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6q7czk08ad

Table 8. Maximum Supply Currents (continued)

Power Supply	Conditions	Maximum Current		Unit
		Power Virus	CoreMark	
MISC				
DRAM_VREF	—	1		mA

1 The actual maximum current drawn from VDD_HIGH_IN will be as shown plus any additional current drawn from the VDD_HIGH_CAP outputs, depending upon actual application configuration (for example, NVCC_LVDS_2P5, NVCC_MIPI, or HDMI, PCIe, and SATA VPH supplies).

2 Under normal operating conditions, the maximum current on VDD_SNVS_IN is shown Table 8. The maximum VDD_SNVS_IN current may be higher depending on specific operating configurations, such as BOOT_MODE[1:0] not equal to 00, or use of the Tamper feature. During initial power on, VDD_SNVS_IN can draw up to 1 mA if the supply is capable of sourcing that current. If less than 1 mA is available, the VDD_SNVS_CAP charge time will increase.

3 This is the maximum current per active USB physical interface.

4 The DRAM power consumption is dependent on several factors such as external signal termination. DRAM power calculators are typically available from memory vendors which take into account factors such as signal termination.
See the *i.MX 6Dual/6Quad Power Consumption Measurement Application Note* (AN4509) for examples of DRAM power consumption during specific use case scenarios.

5 General equation for estimated, maximum power consumption of an IO power supply:
Imax = N x C x V x (0.5 x F)
Where:
N—Number of IO pins supplied by the power line
C—Equivalent external capacitive load
V—IO voltage
(0.5 xF)—Data change rate. Up to 0.5 of the clock rate (F)
In this equation, Imax is in Amps, C in Farads, V in Volts, and F in Hertz.

4.1.6 Low Power Mode Supply Currents

Table 9 shows the current core consumption (not including I/O) of the i.MX 6Dual/6Quad processors in selected low power modes.

Table 9. Stop Mode Current and Power Consumption

Mode	Test Conditions	Supply	Typical[1]	Unit
WAIT	• ARM, SoC, and PU LDOs are set to 1.225 V • HIGH LDO set to 2.5 V • Clocks are gated • DDR is in self refresh • PLLs are active in bypass (24 MHz) • Supply voltages remain ON	VDD_ARM_IN (1.4 V)	6	mA
		VDD_SOC_IN (1.4 V)	23	mA
		VDD_HIGH_IN (3.0 V)	3.7	mA
		Total	52	mW
STOP_ON	• ARM LDO set to 0.9 V • SoC and PU LDOs set to 1.225 V • HIGH LDO set to 2.5 V • PLLs disabled • DDR is in self refresh	VDD_ARM_IN (1.4 V)	7.5	mA
		VDD_SOC_IN (1.4 V)	22	mA
		VDD_HIGH_IN (3.0 V)	3.7	mA
		Total	52	mW

Table 9. Stop Mode Current and Power Consumption (continued)

Mode	Test Conditions	Supply	Typical[1]	Unit
STOP_OFF	• ARM LDO set to 0.9 V • SoC LDO set to 1.225 V • PU LDO is power gated • HIGH LDO set to 2.5 V • PLLs disabled • DDR is in self refresh	VDD_ARM_IN (1.4 V)	7.5	mA
		VDD_SOC_IN (1.4 V)	13.5	mA
		VDD_HIGH_IN (3.0 V)	3.7	mA
		Total	41	mW
STANDBY	• ARM and PU LDOs are power gated • SoC LDO is in bypass • HIGH LDO is set to 2.5 V • PLLs are disabled • Low voltage • Well Bias ON • Crystal oscillator is enabled	VDD_ARM_IN (0.9 V)	0.1	mA
		VDD_SOC_IN (0.9 V)	13	mA
		VDD_HIGH_IN (3.0 V)	3.7	mA
		Total	22	mW
Deep Sleep Mode (DSM)	• ARM and PU LDOs are power gated • SoC LDO is in bypass • HIGH LDO is set to 2.5 V • PLLs are disabled • Low voltage • Well Bias ON • Crystal oscillator and bandgap are disabled	VDD_ARM_IN (0.9 V)	0.1	mA
		VDD_SOC_IN (0.9 V)	2	mA
		VDD_HIGH_IN (3.0 V)	0.5	mA
		Total	3.4	mW
SNVS Only	• VDD_SNVS_IN powered • All other supplies off • SRTC running	VDD_SNVS_IN (2.8V)	41	µA
		Total	115	µW

[1] The typical values shown here are for information only and are not guaranteed. These values are average values measured on a worst-case wafer at 25°C.

4.7.2 DDR I/O AC Parameters

For details on supported DDR memory configurations, see Section 4.10.2, "MMDC Supported LPDDR2 Configurations."

Table 27 shows the AC parameters for DDR I/O operating in LPDDR2 mode.

Table 27. DDR I/O LPDDR2 Mode AC Parameters[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AC input logic high	Vih(ac)	—	Vref + 0.22	—	OVDD	V
AC input logic low	Vil(ac)	—	0	—	Vref – 0.22	V
AC differential input high voltage[2]	Vidh(ac)	—	0.44	—	—	V
AC differential input low voltage	Vidl(ac)	—	—	—	0.44	V
Input AC differential cross point voltage[3]	Vix(ac)	Relative to Vref	-0.12	—	0.12	V
Over/undershoot peak	Vpeak	—	—	—	0.35	V
Over/undershoot area (above OVDD or below OVSS)	Varea	400 MHz	—	—	0.2	V-ns
Single output slew rate, measured between Vol(ac) and Voh(ac)	tsr	50 Ω to Vref. 5 pF load. Drive impedance = 4 0 Ω ±30%	1.5	—	3.5	V/ns
		50 Ω to Vref. 5pF load. Drive impedance = 60 Ω ±30%	1	—	2.5	
Skew between pad rise/fall asymmetry + skew caused by SSN	t_{SKD}	clk = 400 MHz	—	—	0.1	ns

1 Note that the JEDEC LPDDR2 specification (JESD209_2B) supersedes any specification in this document.

2 Vid(ac) specifies the input differential voltage |Vtr – Vcp| required for switching, where Vtr is the "true" input signal and Vcp is the "complementary" input signal. The Minimum value is equal to Vih(ac) – Vil(ac).

3 The typical value of Vix(ac) is expected to be about 0.5 × OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

4.7.3 LVDS I/O AC Parameters

The differential output transition time waveform is shown in Figure 6.

4.9.3.4 General EIM Timing-Asynchronous Mode

Figure 16 through Figure 20 and Table 36 provide timing parameters relative to the chip select (CS) state for asynchronous and DTACK EIM accesses with corresponding EIM bit fields and the timing parameters mentioned above.

Asynchronous read and write access length in cycles may vary from what is shown in Figure 16 through Figure 19 as RWSC, OEN & CSN is configured differently. See the i.MX 6Dual/6Quad reference manual (IMX6DQRM) for the EIM programming model.

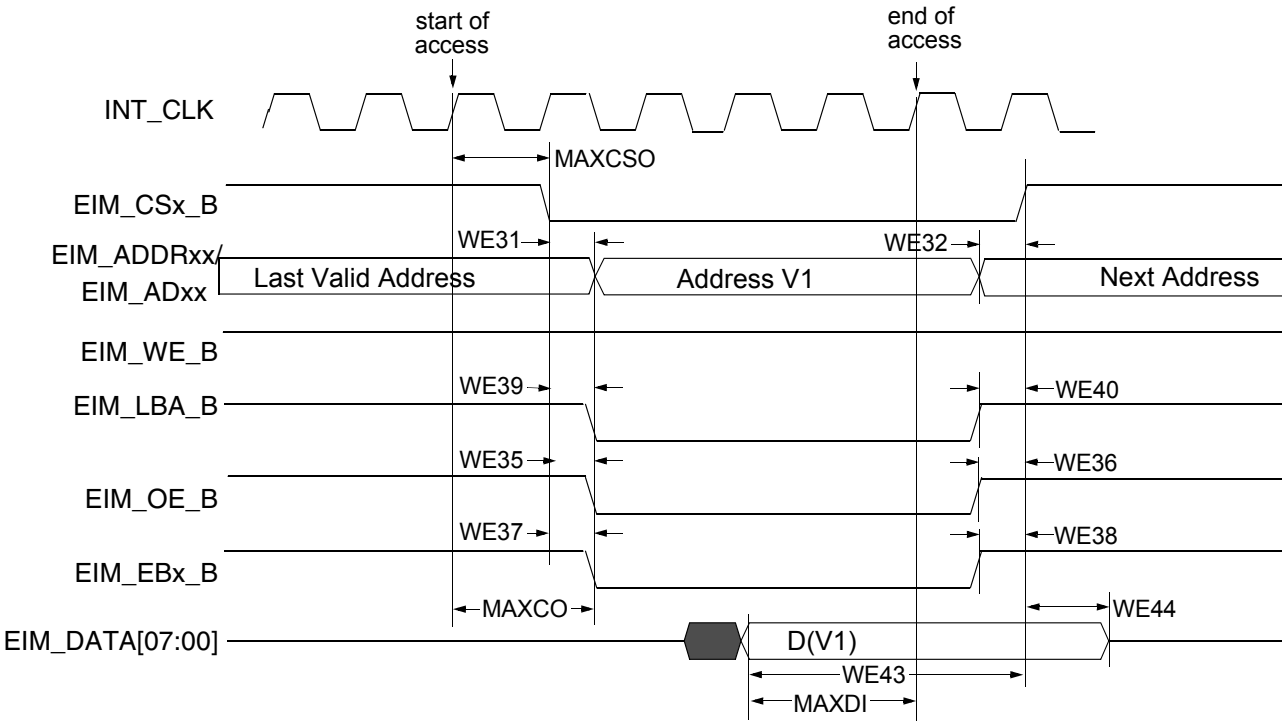

Figure 16. Asynchronous Memory Read Access (RWSC = 5)

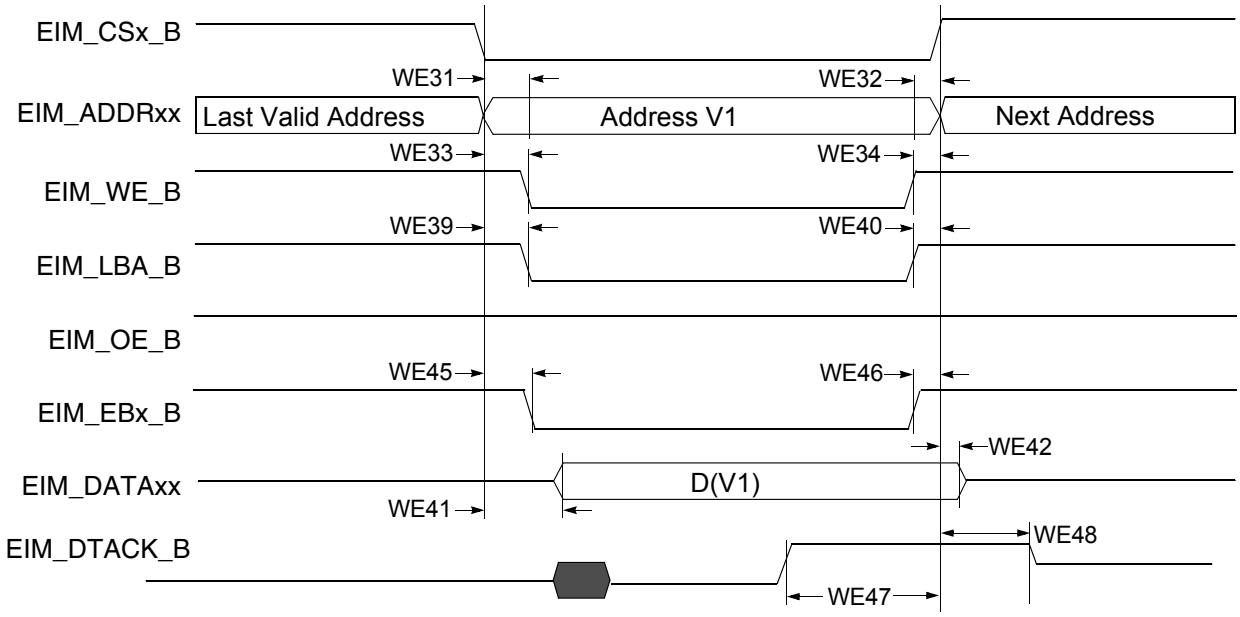

Figure 21. DTACK Mode Write Access (DAP=0)

Table 36. EIM Asynchronous Timing Parameters Relative to Chip Select[1, 2]

Ref No.	Parameter	Determination by Synchronous measured parameters	Min	Max	Unit
WE31	EIM_CSx_B valid to Address Valid	WE4-WE6-CSA×t	-3.5-CSA×t	3.5-CSA×t	ns
WE32	Address Invalid to EIM_CSx_B Invalid	WE7-WE5-CSN×t	-3.5-CSN×t	3.5-CSN×t	ns
WE32A (muxed A/D)	EIM_CSx_B valid to Address Invalid	t+WE4-WE7+ (ADVN+ADVA+1-CSA)×t	t - 3.5+(ADVN+ADVA+1-CSA)×t	t + 3.5+(ADVN+ADVA+1-CSA)×t	ns
WE33	EIM_CSx_B Valid to EIM_WE_B Valid	WE8-WE6+(WEA-WCSA)×t	-3.5+(WEA-WCSA)×t	3.5+(WEA-WCSA)×t	ns
WE34	EIM_WE_B Invalid to EIM_CSx_B Invalid	WE7-WE9+(WEN-WCSN)×t	-3.5+(WEN-WCSN)×t	3.5+(WEN-WCSN)×t	ns
WE35	EIM_CSx_B Valid to EIM_OE_B Valid	WE10- WE6+(OEA-RCSA)×t	-3.5+(OEA-RCSA)×t	3.5+(OEA-RCSA)×t	ns
WE35A (muxed A/D)	EIM_CSx_B Valid to EIM_OE_B Valid	WE10-WE6+(OEA+RADVN+RADVA+ADH+1-RCSA)×t	-3.5+(OEA+RADVN+RADVA+ADH+1-RCSA)×t	3.5+(OEA+RADVN+RADVA+ADH+1-RCSA)×t	ns
WE36	EIM_OE_B Invalid to EIM_CSx_B Invalid	WE7-WE11+(OEN-RCSN)×t	-3.5+(OEN-RCSN)×t	3.5+(OEN-RCSN)×t	ns
WE37	EIM_CSx_B Valid to EIM_EBx_B Valid (Read access)	WE12-WE6+(RBEA-RCSA)× t	-3.5+(RBEA- RCSA)×t	3.5+(RBEA - RCSA)×t	ns
WE38	EIM_EBx_B Invalid to EIM_CSx_B Invalid (Read access)	WE7-WE13+(RBEN-RCSN)×t	-3.5+ (RBEN-RCSN)×t	3.5+(RBEN-RCSN)×t	ns
WE39	EIM_CSx_B Valid to EIM_LBA_B Valid	WE14-WE6+(ADVA-CSA)×t	-3.5+ (ADVA-CSA)×t	3.5+(ADVA-CSA)×t	ns

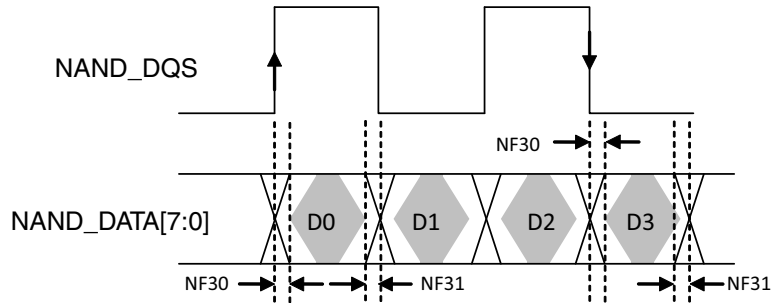

Figure 30. NAND_DQS/NAND_DQ Read Valid Window

Table 39. Source Synchronous Mode Timing Parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min	Max	
NF18	NAND_CEx_B access time	tCE	CE_DELAY × T - 0.79 [see 2]		ns
NF19	NAND_CEx_B hold time	tCH	0.5 × tCK - 0.63 [see 2]		ns
NF20	Command/address NAND_DATAxx setup time	tCAS	0.5 × tCK - 0.05		ns
NF21	Command/address NAND_DATAxx hold time	tCAH	0.5 × tCK - 1.23		ns
NF22	clock period	tCK	—		ns
NF23	preamble delay	tPRE	PRE_DELAY × T - 0.29 [see 2]		ns
NF24	postamble delay	tPOST	POST_DELAY × T - 0.78 [see 2]		ns
NF25	NAND_CLE and NAND_ALE setup time	tCALS	0.5 × tCK - 0.86		ns
NF26	NAND_CLE and NAND_ALE hold time	tCALH	0.5 × tCK - 0.37		ns
NF27	NAND_CLK to first NAND_DQS latching transition	tDQSS	T - 0.41 [see 2]		ns
NF28	Data write setup	tDS	0.25 × tCK - 0.35		—
NF29	Data write hold	tDH	0.25 × tCK - 0.85		—
NF30	NAND_DQS/NAND_DQ read setup skew	tDQSQ	—	2.06	—
NF31	NAND_DQS/NAND_DQ read hold skew	tQHS	—	1.95	—

1 The GPMI source synchronous mode output timing can be controlled by the module's internal registers GPMI_TIMING2_CE_DELAY, GPMI_TIMING_PREAMBLE_DELAY, GPMI_TIMING2_POST_DELAY. This AC timing depends on these registers settings. In the table, CE_DELAY/PRE_DELAY/POST_DELAY represents each of these settings.

2 T = tCK (GPMI clock period) -0.075ns (half of maximum p-p jitter).

Figure 30 shows the timing diagram of NAND_DQS/NAND_DATAxx read valid window. For Source Synchronous mode, the typical value of tDQSQ is 0.85 ns (max) and 1 ns (max) for tQHS at 200MB/s. GPMI will sample NAND_DATA[7:0] at both rising and falling edge of a delayed NAND_DQS signal, which can be provided by an internal DPLL. The delay value can be controlled by GPMI register GPMI_READ_DDR_DLL_CTRL.SLV_DLY_TARGET (see the GPMI chapter of the i.MX 6Dual/6Quad reference manual (IMX6DQRM)). Generally, the typical delay value of this register is equal to 0x7 which means 1/4 clock cycle delay expected. However, if the board delay is large enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

4.11.3 Samsung Toggle Mode AC Timing

4.11.3.1 Command and Address Timing

Samsung Toggle mode command and address timing is the same as ONFI 1.0 compatible Async mode AC timing. See Section 4.11.1, “Asynchronous Mode AC Timing (ONFI 1.0 Compatible)” for details.

4.11.3.2 Read and Write Timing

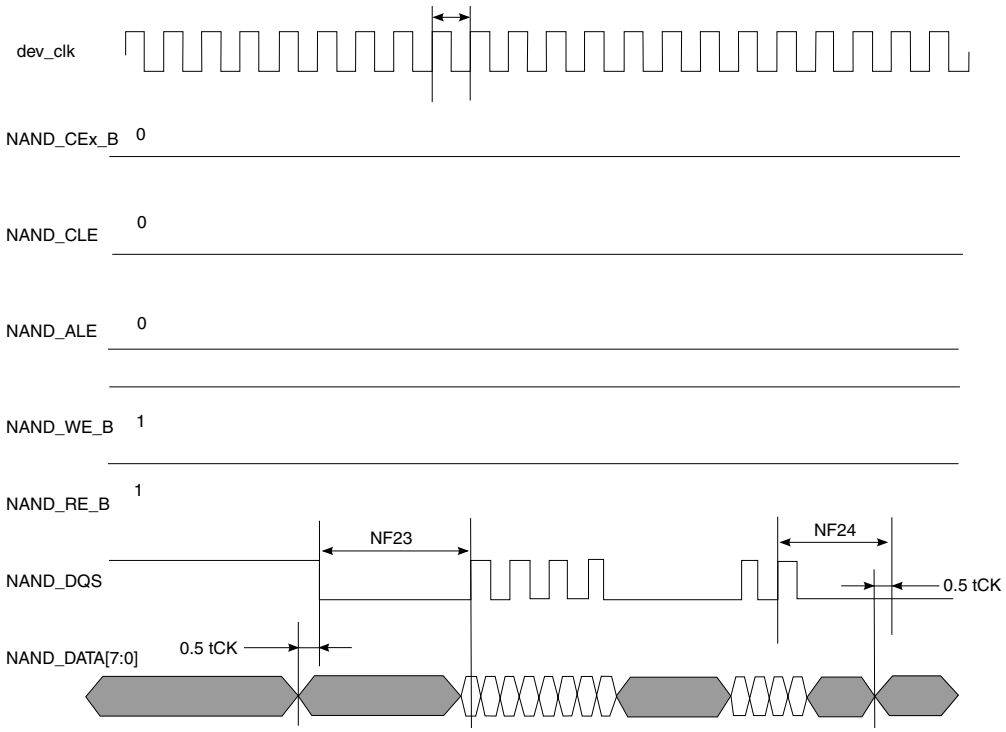

Figure 31. Samsung Toggle Mode Data Write Timing

4.12.4 Ultra High Speed SD/SDIO/MMC Host Interface (uSDHC) AC Timing

This section describes the electrical information of the uSDHC, which includes SD/eMMC4.3 (Single Data Rate) timing and eMMC4.4/4.1 (Dual Date Rate) timing.

4.12.4.1 SD/eMMC4.3 (Single Data Rate) AC Timing

Figure 37 depicts the timing of SD/eMMC4.3, and Table 44 lists the SD/eMMC4.3 timing characteristics.

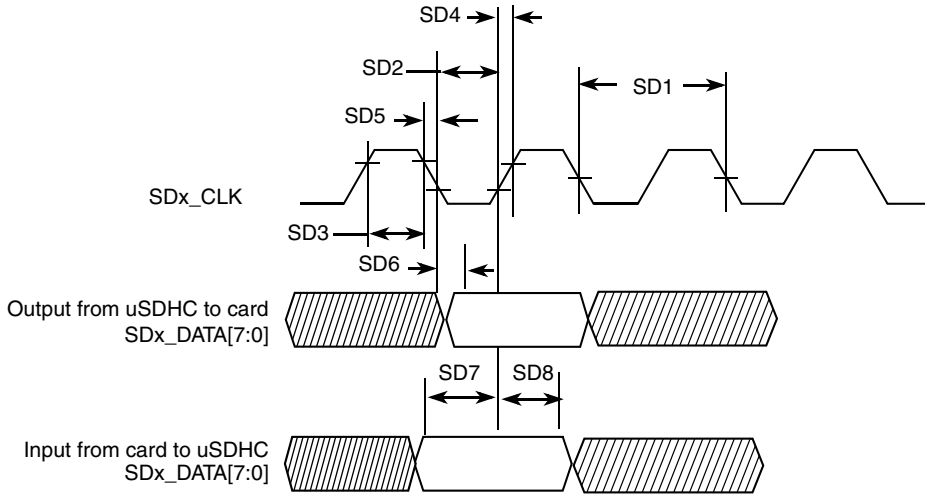

Figure 37. SD/eMMC4.3 Timing

Table 44. SD/eMMC4.3 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (Low Speed)	f_{PP}[1]	0	400	kHz
	Clock Frequency (SD/SDIO Full Speed/High Speed)	f_{PP}[2]	0	25/50	MHz
	Clock Frequency (MMC Full Speed/High Speed)	f_{PP}[3]	0	20/52	MHz
	Clock Frequency (Identification Mode)	f_{OD}	100	400	kHz
SD2	Clock Low Time	t_{WL}	7	—	ns
SD3	Clock High Time	t_{WH}	7	—	ns
SD4	Clock Rise Time	t_{TLH}	—	3	ns
SD5	Clock Fall Time	t_{THL}	—	3	ns
eSDHC Output/Card Inputs SD_CMD, SD_DATAx (Reference to SDx_CLK)					
SD6	eSDHC Output Delay	t_{OD}	–6.6	3.6	ns

Table 44. SD/eMMC4.3 Interface Timing Specification (continued)

ID	Parameter	Symbols	Min	Max	Unit
eSDHC Input/Card Outputs SD_CMD, SD_DATAx (Reference to SDx_CLK)					
SD7	eSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD8	eSDHC Input Hold Time[4]	t_{IH}	1.5	—	ns

1 In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

2 In normal (full) speed mode for SD/SDIO card, clock frequency can be any value between 0—25 MHz. In high-speed mode, clock frequency can be any value between 0—50 MHz.

3 In normal (full) speed mode for MMC card, clock frequency can be any value between 0—20 MHz. In high-speed mode, clock frequency can be any value between 0—52 MHz.

4 To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

4.12.4.2 eMMC4.4/4.41 (Dual Data Rate) eSDHCv3 AC Timing

Figure 38 depicts the timing of eMMC4.4/4.41. Table 45 lists the eMMC4.4/4.41 timing characteristics. Be aware that only SDx_DATAx is sampled on both edges of the clock (not applicable to SD_CMD).

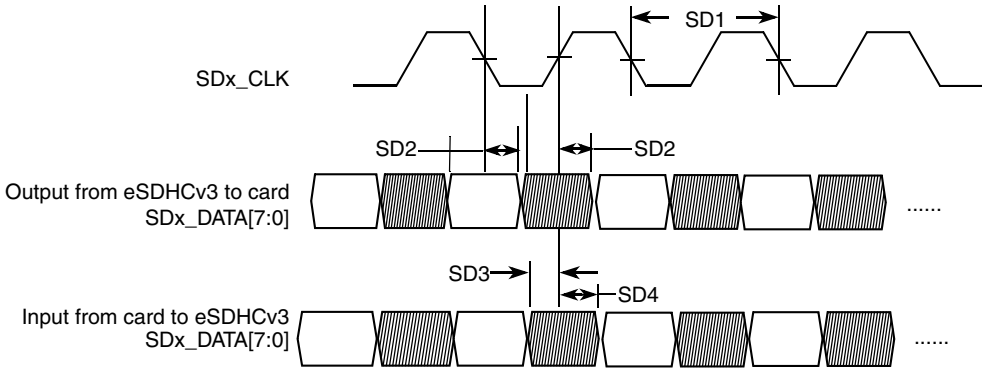

Figure 38. eMMC4.4/4.41 Timing

Table 45. eMMC4.4/4.41 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock[1]					
SD1	Clock Frequency (EMMC4.4 DDR)	f_{PP}	0	52	MHz
SD1	Clock Frequency (SD3.0 DDR)	f_{PP}	0	50	MHz
uSDHC Output / Card Inputs SD_CMD, SD_DATAx (Reference to SD_CLK)					
SD2	uSDHC Output Delay	t_{OD}	2.5	7.1	ns
uSDHC Input / Card Outputs SD_CMD, SD_DATAx (Reference to SD_CLK)					
SD3	uSDHC Input Setup Time	t_{ISU}	1.7	—	ns
SD4	uSDHC Input Hold Time	t_{IH}	1.5	—	ns

1 Clock duty cycle will be in the range of 47% to 53%.

2 The MSB bits are duplicated on LSB bits implementing color extension.
3 The two MSB bits are duplicated on LSB bits implementing color extension.
4 YCbCr, 8 bits—Supported within the BT.656 protocol (sync embedded within the data stream).
5 RGB, 16 bits—Supported in two ways: (1) As a “generic data” input—with no on-the-fly processing; (2) With on-the-fly processing, but only under some restrictions on the control protocol.
6 YCbCr, 16 bits—Supported as a “generic-data” input—with no on-the-fly processing.
7 YCbCr, 16 bits—Supported as a sub-case of the YCbCr, 20 bits, under the same conditions (BT.1120 protocol).
8 YCbCr, 20 bits—Supported only within the BT.1120 protocol (syncs embedded within the data stream).

4.12.10.2 Sensor Interface Timings

There are three camera timing modes supported by the IPU.

4.12.10.2.1 BT.656 and BT.1120 Video Mode

Smart camera sensors, which include imaging processing, usually support video mode transfer. They use an embedded timing syntax to replace the IPU2_CSIx_VSYNC and IPU2_CSIx_HSYNC signals. The timing syntax is defined by the BT.656/BT.1120 standards.

This operation mode follows the recommendations of ITU BT.656/ ITU BT.1120 specifications. The only control signal used is IPU2_CSIx_PIX_CLK. Start-of-frame and active-line signals are embedded in the data stream. An active line starts with a SAV code and ends with a EAV code. In some cases, digital blanking is inserted in between EAV and SAV code. The CSI decodes and filters out the timing-coding from the data stream, thus recovering IPU2_CSIx_VSYNC and IPU2_CSIx_HSYNC signals for internal use. On BT.656 one component per cycle is received over the IPU2_CSIx_DATA_EN bus. On BT.1120 two components per cycle are received over the IPU2_CSIx_DATA_EN bus.

4.12.10.2.2 Gated Clock Mode

The IPU2_CSIx_VSYNC, IPU2_CSIx_HSYNC, and IPU2_CSIx_PIX_CLK signals are used in this mode. See Figure 57.

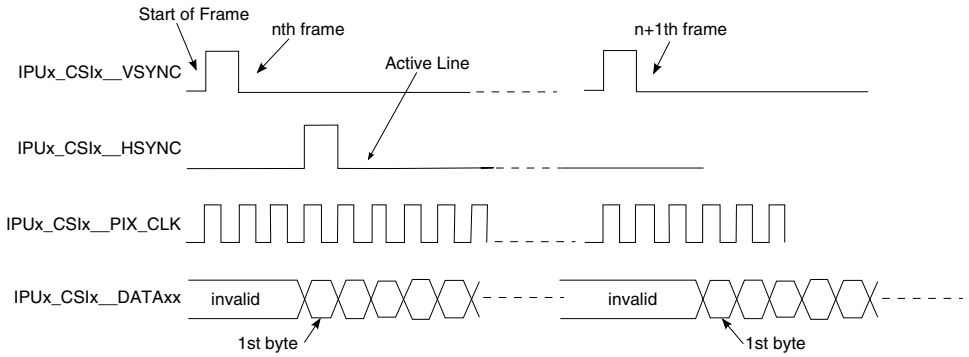

Figure 57. Gated Clock Mode Timing Diagram

A frame starts with a rising edge on IPU2_CSIx_VSYNC (all the timings correspond to straight polarity of the corresponding signals). Then IPU2_CSIx_HSYNC goes to high and hold for the entire line. Pixel clock is valid as long as IPU2_CSIx_HSYNC is high. Data is latched at the rising edge of the valid pixel clocks. IPU2_CSIx_HSYNC goes to low at the end of line. Pixel clocks then become invalid and the CSI

Figure 63 depicts the synchronous display interface timing for access level. The DISP_CLK_DOWN and DISP_CLK_UP parameters are register-controlled. Table 60 lists the synchronous display interface timing characteristics.

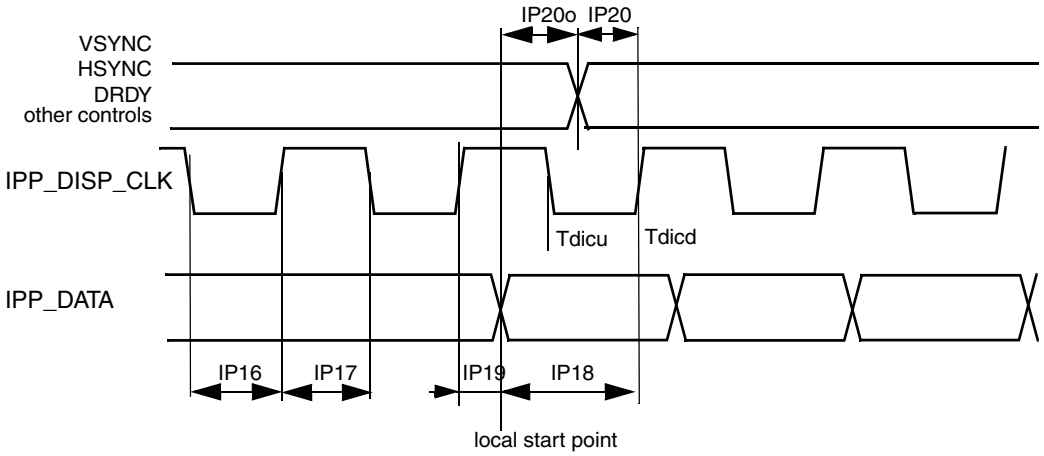

Figure 63. Synchronous Display Interface Timing Diagram—Access Level

Table 60. Synchronous Display Interface Timing Characteristics (Access Level)

ID	Parameter	Symbol	Min	Typ[1]	Max	Unit
IP16	Display interface clock low time	Tckl	Tdicd-Tdicu-1.24	Tdicd[2]-Tdicu[3]	Tdicd-Tdicu+1.24	ns
IP17	Display interface clock high time	Tckh	Tdicp-Tdicd+Tdicu-1.24	Tdicp-Tdicd+Tdicu	Tdicp-Tdicd+Tdicu+1.2	ns
IP18	Data setup time	Tdsu	Tdicd-1.24	Tdicu	—	ns
IP19	Data holdup time	Tdhd	Tdicp-Tdicd-1.24	Tdicp-Tdicu	—	ns
IP20o	Control signals offset times (defined for each pin)	Tocsu	Tocsu-1.24	Tocsu	Tocsu+1.24	ns
IP20	Control signals setup time to display interface clock (defined for each pin)	Tcsu	Tdicd-1.24-Tocsu%Tdicp	Tdicu	—	ns

[1]The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be chip specific.

[2] Display interface clock down time

$$\mathrm{Tdicd} = \frac{1}{2}\left(\mathrm{T_{diclk}} \times \mathrm{ceil}\left[\frac{2 \times \mathrm{DISP\_CLK\_DOWN}}{\mathrm{DI\_CLK\_PERIOD}}\right]\right)$$

[3] Display interface clock up time where CEIL(X) rounds the elements of X to the nearest integers towards infinity.

$$\mathrm{Tdicu} = \frac{1}{2}\left(\mathrm{T_{diclk}} \times \mathrm{ceil}\left[\frac{2 \times \mathrm{DISP\_CLK\_UP}}{\mathrm{DI\_CLK\_PERIOD}}\right]\right)$$

Table 62. Electrical and Timing Information (continued)

Symbol	Parameters	Test Conditions	Min	Typ	Max	Unit
LP Line Receiver DC Specifications						
V_{IL}	Input low voltage	—	—	—	550	mV
V_{IH}	Input high voltage	—	920	—	—	mV
V_{HYST}	Input hysteresis	—	25	—	—	mV
Contention Line Receiver DC Specifications						
V_{ILF}	Input low fault threshold	—	200	—	450	mV

4.12.12.2 D-PHY Signaling Levels

The signal levels are different for differential HS mode and single-ended LP mode. Figure 64 shows both the HS and LP signal levels on the left and right sides, respectively. The HS signalling levels are below the LP low-level input threshold such that LP receiver always detects low on HS signals.

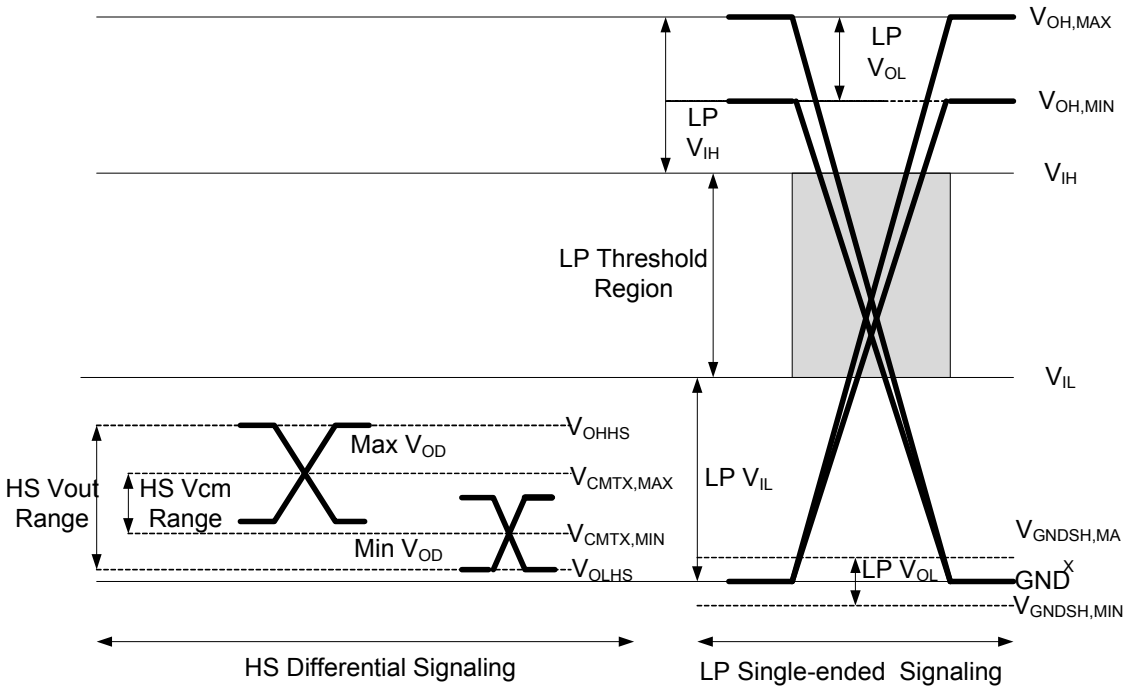

Figure 64. D-PHY Signaling Levels

4.12.12.9 Low-Power Receiver Timing

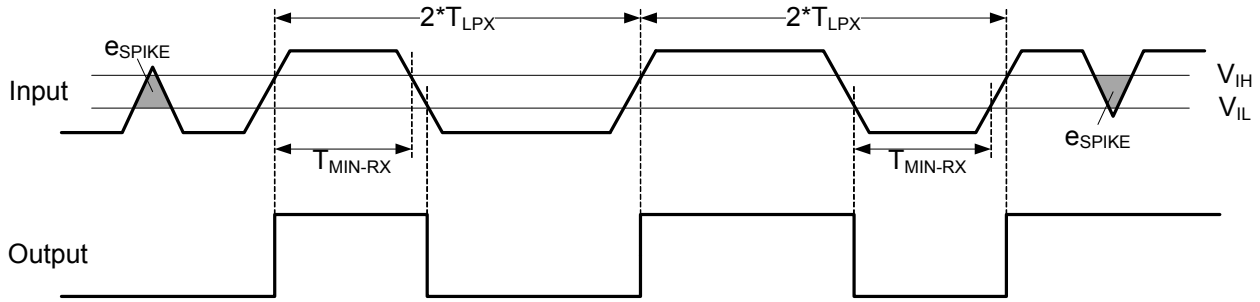

Figure 70. Input Glitch Rejection of Low-Power Receivers

4.12.13 HSI Host Controller Timing Parameters

This section describes the timing parameters of the HSI Host Controller which are compliant with High-Speed Synchronous Serial Interface (HSI) Physical Layer specification version 1.01.

4.12.13.1 Synchronous Data Flow

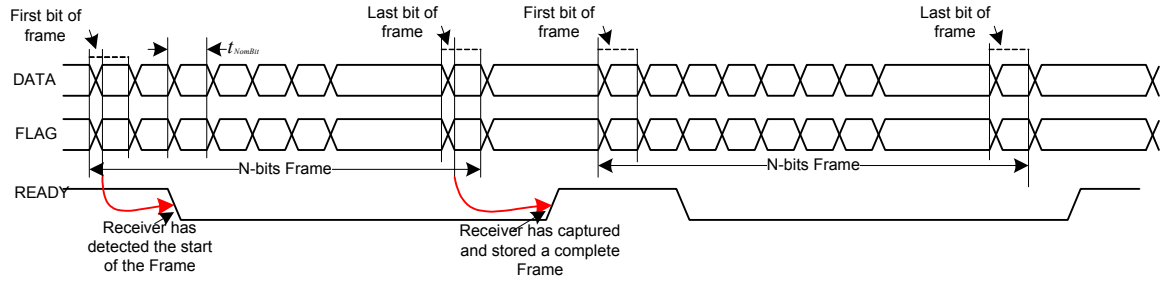

Figure 71. Synchronized Data Flow READY Signal Timing (Frame and Stream Transmission)

4.12.13.2 Pipelined Data Flow

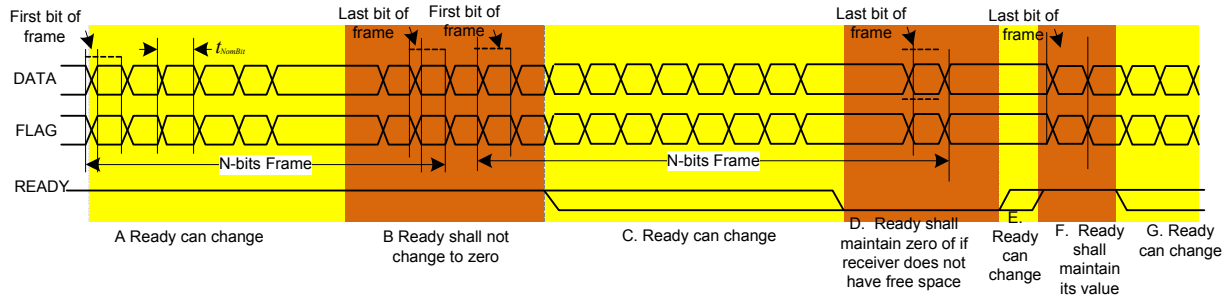

Figure 72. Pipelined Data Flow READY Signal Timing (Frame Transmission Mode)

4.12.16 SATA PHY Parameters

This section describes SATA PHY electrical specifications.

4.12.16.1 Transmitter and Receiver Characteristics

The SATA PHY meets or exceeds the electrical compliance requirements defined in the SATA specifications.

NOTE

The tables in the following sections indicate any exceptions to the SATA specification or aspects of the SATA PHY that exceed the standard, as well as provide information about parameters not defined in the standard.

The following subsections provide values obtained from a combination of simulations and silicon characterization.

4.12.16.1.1 SATA PHY Transmitter Characteristics

Table 66 provides specifications for SATA PHY transmitter characteristics.

Table 66. SATA PHY Transmitter Characteristics

Parameters	Symbol	Min	Typ	Max	Unit
Transmit common mode voltage	V_{CTM}	0.4	—	0.6	V
Transmitter pre-emphasis accuracy (measured change in de-emphasized bit)	—	–0.5	—	0.5	dB

4.12.16.1.2 SATA PHY Receiver Characteristics

Table 67 provides specifications for SATA PHY receiver characteristics.

Table 67. SATA PHY Receiver Characteristics

Parameters	Symbol	Min	Typ	Max	Unit
Minimum Rx eye height (differential peak-to-peak)	$V_{MIN\_RX\_EYE\_HEIGHT}$	175	—	—	mV
Tolerance	PPM	–400	—	400	ppm

4.12.16.2 SATA_REXT Reference Resistor Connection

The impedance calibration process requires connection of reference resistor 191 Ω 1% precision resistor on SATA_REXT pad to ground.

Resistor calibration consists of learning which state of the internal Resistor Calibration register causes an internal, digitally trimmed calibration resistor to best match the impedance applied to the SATA_REXT pin. The calibration register value is then supplied to all Tx and Rx termination resistors.

During the calibration process (for a few tens of microseconds), up to 0.3 mW can be dissipated in the external SATA_REXT resistor. At other times, no power is dissipated by the SATA_REXT resistor.

Table 68. JTAG Timing (continued)

ID	Parameter[1,2]	All Frequencies		Unit
		Min	Max	
SJ9	JTAG_TMS, JTAG_TDI data hold time	25	—	ns
SJ10	JTAG_TCK low to JTAG_TDO data valid	—	44	ns
SJ11	JTAG_TCK low to JTAG_TDO high impedance	—	44	ns
SJ12	JTAG_TRST_B assert time	100	—	ns
SJ13	JTAG_TRST_B set-up time to JTAG_TCK low	40	—	ns

1 T_{DC} = target frequency of SJC

2 V_M = mid-point voltage

4.12.18 SPDIF Timing Parameters

The Sony/Philips Digital Interconnect Format (SPDIF) data is sent using the bi-phase marking code. When encoding, the SPDIF data signal is modulated by a clock that is twice the bit rate of the data signal.

Table 69 and Figure 84 and Figure 85 show SPDIF timing parameters for the Sony/Philips Digital Interconnect Format (SPDIF), including the timing of the modulating Rx clock (SPDIF_SR_CLK) for SPDIF in Rx mode and the timing of the modulating Tx clock (SPDIF_ST_CLK) for SPDIF in Tx mode.

Table 69. SPDIF Timing Parameters

Parameter	Symbol	Timing Parameter Range		Unit
		Min	Max	
SPDIF_IN Skew: asynchronous inputs, no specs apply	—	—	0.7	ns
SPDIF_OUT output (Load = 50pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 24.2 31.3	ns
SPDIF_OUT output (Load = 30pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 13.6 18.0	ns
Modulating Rx clock (SPDIF_SR_CLK) period	srckp	40.0	—	ns
SPDIF_SR_CLK high period	srckph	16.0	—	ns
SPDIF_SR_CLK low period	srckpl	16.0	—	ns
Modulating Tx clock (SPDIF_ST_CLK) period	stclkp	40.0	—	ns
SPDIF_ST_CLK high period	stclkph	16.0	—	ns
SPDIF_ST_CLK low period	stclkpl	16.0	—	ns

4.12.20.2.3 UART IrDA Mode Timing

The following subsections give the UART transmit and receive timings in IrDA mode.

UART IrDA Mode Transmitter

Figure 92 depicts the UART IrDA mode transmit timing, with 8 data bit/1 stop bit format. Table 78 lists the transmit timing characteristics.

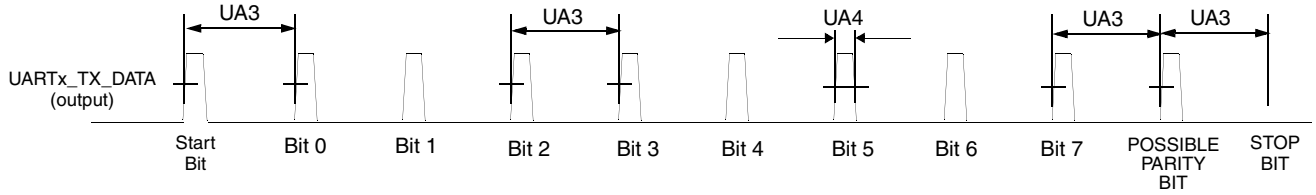

Figure 92. UART IrDA Mode Transmit Timing Diagram

Table 78. IrDA Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA3	Transmit Bit Time in IrDA mode	t_{TIRbit}	$1/F_{baud\_rate}$ [1] – T_{ref_clk} [2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—
UA4	Transmit IR Pulse Duration	$t_{TIRpulse}$	$(3/16) \times (1/F_{baud\_rate}) - T_{ref\_clk}$	$(3/16) \times (1/F_{baud\_rate}) + T_{ref\_clk}$	—

1 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

2 T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

UART IrDA Mode Receiver

Figure 93 depicts the UART IrDA mode receive timing, with 8 data bit/1 stop bit format. Table 79 lists the receive timing characteristics.

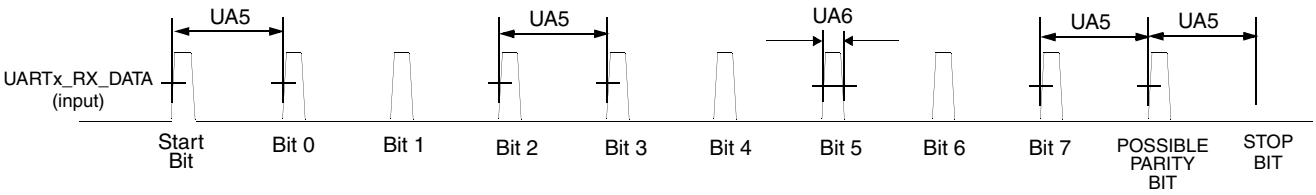

Figure 93. UART IrDA Mode Receive Timing Diagram

Table 79. IrDA Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA5	Receive Bit Time[1] in IrDA mode	t_{RIRbit}	$1/F_{baud\_rate}$ [2] – $1/(16 \times F_{baud\_rate})$	$1/F_{baud\_rate} + 1/(16 \times F_{baud\_rate})$	—
UA6	Receive IR Pulse Duration	$t_{RIRpulse}$	1.41 µs	$(5/16) \times (1/F_{baud\_rate})$	—

1 The UART receiver can tolerate $1/(16 \times F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud\_rate})$.

2 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

Table 84. 12 x 12 mm PoP Ground, Power, Sense, and Reference Contact Assignments (continued)

Ball Name	PoP Bottom Ball Position	PoP Top Ball Position	Remark
VDDHIGH_CAP	F10, F11	—	Secondary supply for the 2.5 V domain (internal regulator output—requires capacitor if internal regulator is used)
VDDHIGH_IN	F8, F9	—	Primary supply for the 2.5 V regulator
VDDPU_CAP	N19, N20, P19, P20, U19, U20, V19, V20	—	Secondary supply for the VPU and GPU (internal regulator output—requires capacitor if internal regulator is used)
VDDSOC_CAP	K19, K20, R6, R7, W10, W11, W12, W15, W16, Y10, Y11, Y12, Y15, Y16	—	Secondary supply for the SoC and PU (internal regulator output—requires capacitor if internal regulator is used)
VDDSOC_IN	L19, L20, M19, M20, W19, W20, Y19, Y20	—	Primary supply for the SoC and PU regulators
VDDUSB_CAP	G10	—	Secondary supply for the 3 V domain (internal regulator output—requires capacitor if internal regulator is used)
ZQPAD	AJ19	—	Connect ZQPAD to an external 240Ω 1% resistor to GND. This is a reference used during DRAM output buffer driver calibration.

6.2.3 12 x 12 mm Functional Contact Assignments

Table 85 displays an alpha-sorted list of the signal assignments including power rails. The table also includes out of reset pad state.

Table 85. 12 x 12 mm Functional Contact Assignments

Ball Name	PoP Bottom Ball	PoP Top Ball	Power Group	Ball Type	Out of Reset Condition[1]			
					Default Mode	Default Function	Input/ Output	Value[2]
BOOT_MODE0	C14	—	VDD_SNVS_IN	GPIO	ALT0	SRC_BOOT_MODE0	Input	PD (100k)
BOOT_MODE1	G13	—	VDD_SNVS_IN	GPIO	ALT0	SRC_BOOT_MODE1	Input	PD (100k)
CLK1_N	A7	—	VDD_HIGH_CAP	—	—	CLK1_N	—	—
CLK1_P	B7	—	VDD_HIGH_CAP	—	—	CLK1_P	—	—
CLK2_N	A6	—	VDD_HIGH_CAP	—	—	CLK2_N	—	—
CLK2_P	B6	—	VDD_HIGH_CAP	—	—	CLK2_P	—	—
CSI_CLK0M	E2	—	NVCC_MIPI	—	—	CSI_CLK_N	—	—
CSI_CLK0P	E1	—	NVCC_MIPI	—	—	CSI_CLK_P	—	—
CSI_D0M	C2	—	NVCC_MIPI	—	—	CSI_DATA0_N	—	—
CSI_D0P	C1	—	NVCC_MIPI	—	—	CSI_DATA0_P	—	—
CSI_D1M	D1	—	NVCC_MIPI	—	—	CSI_DATA1_N	—	—
CSI_D1P	D2	—	NVCC_MIPI	—	—	CSI_DATA1_P	—	—
CSI_D2M	F1	—	NVCC_MIPI	—	—	CSI_DATA2_N	—	—
CSI_D2P	F2	—	NVCC_MIPI	—	—	CSI_DATA2_P	—	—

Table 85. 12 x 12 mm Functional Contact Assignments (continued)

Ball Name	PoP Bottom Ball	PoP Top Ball	Power Group	Ball Type	Out of Reset Condition[1]			
					Default Mode	Default Function	Input/ Output	Value[2]
DRAM_D3P1	—	B5	NVCC_DRAM	DDR	ALT0	DRAM_DATA35	Input	PU (100k)
DRAM_D4P1	—	A5	NVCC_DRAM	DDR	ALT0	DRAM_DATA36	Input	PU (100k)
DRAM_D5P1	—	A8	NVCC_DRAM	DDR	ALT0	DRAM_DATA37	Input	PU (100k)
DRAM_D6P1	—	B8	NVCC_DRAM	DDR	ALT0	DRAM_DATA38	Input	PU (100k)
DRAM_D7P1	—	B6	NVCC_DRAM	DDR	ALT0	DRAM_DATA39	Input	PU (100k)
DRAM_D8P1	—	A18	NVCC_DRAM	DDR	ALT0	DRAM_DATA40	Input	PU (100k)
DRAM_D9P1	—	A13	NVCC_DRAM	DDR	ALT0	DRAM_DATA41	Input	PU (100k)
DRAM_D10P1	—	B19	NVCC_DRAM	DDR	ALT0	DRAM_DATA42	Input	PU (100k)
DRAM_D11P1	—	A12	NVCC_DRAM	DDR	ALT0	DRAM_DATA43	Input	PU (100k)
DRAM_D12P1	—	A19	NVCC_DRAM	DDR	ALT0	DRAM_DATA44	Input	PU (100k)
DRAM_D13P1	—	A17	NVCC_DRAM	DDR	ALT0	DRAM_DATA45	Input	PU (100k)
DRAM_D14P1	—	B12	NVCC_DRAM	DDR	ALT0	DRAM_DATA46	Input	PU (100k)
DRAM_D15P1	—	B17	NVCC_DRAM	DDR	ALT0	DRAM_DATA47	Input	PU (100k)
DRAM_D16P1	—	E29	NVCC_DRAM	DDR	ALT0	DRAM_DATA48	Input	PU (100k)
DRAM_D17P1	—	A24	NVCC_DRAM	DDR	ALT0	DRAM_DATA49	Input	PU (100k)
DRAM_D18P1	—	A27	NVCC_DRAM	DDR	ALT0	DRAM_DATA50	Input	PU (100k)
DRAM_D19P1	—	A26	NVCC_DRAM	DDR	ALT0	DRAM_DATA51	Input	PU (100k)
DRAM_D20P1	—	B27	NVCC_DRAM	DDR	ALT0	DRAM_DATA52	Input	PU (100k)
DRAM_D21P1	—	D28	NVCC_DRAM	DDR	ALT0	DRAM_DATA53	Input	PU (100k)
DRAM_D22P1	—	B26	NVCC_DRAM	DDR	ALT0	DRAM_DATA54	Input	PU (100k)
DRAM_D23P1	—	A25	NVCC_DRAM	DDR	ALT0	DRAM_DATA55	Input	PU (100k)
DRAM_D24P1	—	K28	NVCC_DRAM	DDR	ALT0	DRAM_DATA56	Input	PU (100k)
DRAM_D25P1	—	N29	NVCC_DRAM	DDR	ALT0	DRAM_DATA57	Input	PU (100k)
DRAM_D26P1	—	H29	NVCC_DRAM	DDR	ALT0	DRAM_DATA58	Input	PU (100k)
DRAM_D27P1	—	L28	NVCC_DRAM	DDR	ALT0	DRAM_DATA59	Input	PU (100k)
DRAM_D28P1	—	M29	NVCC_DRAM	DDR	ALT0	DRAM_DATA60	Input	PU (100k)
DRAM_D29P1	—	N28	NVCC_DRAM	DDR	ALT0	DRAM_DATA61	Input	PU (100k)
DRAM_D30P1	—	K29	NVCC_DRAM	DDR	ALT0	DRAM_DATA62	Input	PU (100k)
DRAM_D31P1	—	J29	NVCC_DRAM	DDR	ALT0	DRAM_DATA63	Input	PU (100k)
DRAM_DM0P0	—	AB1	NVCC_DRAM	DDR	ALT0	DRAM_DQM0	Output	0
DRAM_DM1P0	—	AC2	NVCC_DRAM	DDR	ALT0	DRAM_DQM1	Output	0
DRAM_DM2P0	—	L1	NVCC_DRAM	DDR	ALT0	DRAM_DQM2	Output	0
DRAM_DM3P0	—	AH7	NVCC_DRAM	DDR	ALT0	DRAM_DQM3	Output	0
DRAM_DM0P1	—	B11	NVCC_DRAM	DDR	ALT0	DRAM_DQM4	Output	0
DRAM_DM1P1	—	A21	NVCC_DRAM	DDR	ALT0	DRAM_DQM5	Output	0
DRAM_DM2P1	—	B22	NVCC_DRAM	DDR	ALT0	DRAM_DQM6	Output	0
DRAM_DM3P1	—	F28	NVCC_DRAM	DDR	ALT0	DRAM_DQM7	Output	0
DRAM_DQS0P0	—	AA1	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS0_P	Input	Hi-Z
DRAM_DQS0P0_B	—	AA2	NVCC_DRAM	DDRCLK	—	DRAM_SDQS0_N	—	—
DRAM_DQS1P0	—	AD2	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS1_P	Input	Hi-Z

Table 87. PoP 12 x 12 mm, 0.4 mm Pitch Top Ball Map (continued)

M	L	K	J	H	G	F	E
DRAM_D2P0	DRAM_DM2P0	DRAM_DQS2P0_B	GND	DRAM_D20P0	DRAM_D21P0	GND	DRAM_D19P0
GND	DRAM_D7P0	DRAM_DQS2P0	POP_VDDQ	DRAM_D16P0	POP_VDDQ	DRAM_D17P0	DRAM_D22P0
POP_VDDQ	DRAM_D27P1	DRAM_D24P1	POP_VDDQ	GND	DRAM_DQS3P1	DRAM_DM3P1	GND
DRAM_D28P1	GND	DRAM_D30P1	DRAM_D31P1	DRAM_D26P1	DRAM_DQS3P1_B	POP_VDDQ	DRAM_D16P1

Table 87. PoP 12 x 12 mm, 0.4 mm Pitch Top Ball Map (continued)

AG	AF	AE	AD	AC	AB	AA
DRAM_D10P0	DRAM_D14P0	DRAM_D12P0	DRAM_DQS1P0_B	POP_VDDQ	DRAM_DM0P0	DRAM_DQS0P0
DRAM_D13P0	POP_VDDQ	GND	DRAM_DQS1P0	DRAM_DM1P0	GND	DRAM_DQS0P0_B
POP_VDD2__8	GND	DRAM_CA8P0	DRAM_CA7P0	POP_VDDCA	DRAM_CLKP0	GND
POP_ZQP0	DRAM_CA9P0	POP_VDDCA	DRAM_CA6P0	DRAM_CA5P0	DRAM_CLKP0_B	DRAM_CKE0P0