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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	4 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (1)
SATA	SATA 3Gbps (1)
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	569-LFBGA
Supplier Device Package	569-MAPBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6q7czk08ae

- Gaming consoles
- Portable navigation devices (PND)

The i.MX 6Dual/6Quad processors offers numerous advanced features, such as:

- Applications processors—The processors enhance the capabilities of high-tier portable applications by fulfilling the ever increasing MIPS needs of operating systems and games. The Dynamic Voltage and Frequency Scaling (DVFS) provides significant power reduction, allowing the device to run at lower voltage and frequency with sufficient MIPS for tasks such as audio decode.
- Multilevel memory system—The multilevel memory system of each processor is based on the L1 instruction and data caches, L2 cache, and internal and external memory. The processors support many types of external memory devices, including LPDDR2, NOR Flash, PSRAM, cellular RAM, NAND Flash (MLC and SLC), OneNAND™, and managed NAND, including eMMC up to rev 4.4/4.41.
- Smart speed technology—The processors have power management throughout the device that enables the rich suite of multimedia features and peripherals to consume minimum power in both active and various low power modes. Smart speed technology enables the designer to deliver a feature-rich product, requiring levels of power far lower than industry expectations.
- Dynamic voltage and frequency scaling—The processors improve the power efficiency of devices by scaling the voltage and frequency to optimize performance.
- Multimedia powerhouse—The multimedia performance of each processor is enhanced by a multilevel cache system, Neon® MPE (Media Processor Engine) co-processor, a multi-standard hardware video codec, 2 autonomous and independent image processing units (IPU), and a programmable smart DMA (SDMA) controller.
- Powerful graphics acceleration—Each processor provides three independent, integrated graphics processing units: an OpenGL® ES .0 3D graphics accelerator with four shaders (up to MTri/s and OpenCL support), 2D graphics accelerator, and dedicated OpenVG™ 1.1 accelerator.
- Interface flexibility—Each processor supports connections to a variety of interfaces: LCD controller for up to four displays (including parallel display, HDMI1.4, MIPI display, and LVDS display), dual CMOS sensor interface (parallel or through MIPI), high-speed USB on-the-go with PHY, high-speed USB host with PHY, multiple expansion card ports (high-speed MMC/SDIO host and other), 10/100/1000 Mbps Gigabit Ethernet controller, and a variety of other popular interfaces (such as UART, I^2C, and I^2S serial audio, SATA-II, and PCIe-II).
- Advanced security—The processors deliver hardware-enabled security features that enable secure e-commerce, digital rights management (DRM), information encryption, secure boot, and secure software downloads. The security features are discussed in detail in the i.MX 6Dual/6Quad security reference manual (IMX6DQ6SDLSRM).
- Integrated power management—The processors integrate linear regulators and internally generate voltage levels for different domains. This significantly simplifies system power management structure.

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
ESAI	Enhanced Serial Audio Interface	Connectivity Peripherals	The Enhanced Serial Audio Interface (ESAI) provides a full-duplex serial port for serial communication with a variety of serial devices, including industry-standard codecs, SPDIF transceivers, and other processors. The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. All serial transfers are synchronized to a clock. Additional synchronization signals are used to delineate the word frames. The normal mode of operation is used to transfer data at a periodic rate, one word per period. The network mode is also intended for periodic transfers; however, it supports up to 32 words (time slots) per period. This mode can be used to build time division multiplexed (TDM) networks. In contrast, the on-demand mode is intended for non-periodic transfers of data and to transfer data serially at high speed when the data becomes available. The ESAI has 12 pins for data and clocking connection to external devices.
FlexCAN-1 FlexCAN-2	Flexible Controller Area Network	Connectivity Peripherals	The CAN protocol was primarily, but not only, designed to be used as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the Electromagnetic interference (EMI) environment of a vehicle, cost-effectiveness and required bandwidth. The FlexCAN module is a full implementation of the CAN protocol specification, Version 2.0 B, which supports both standard and extended message frames.
GPIO-1 GPIO-2 GPIO-3 GPIO-4 GPIO-5 GPIO-6 GPIO-7	General Purpose I/O Modules	System Control Peripherals	Used for general purpose input/output to external devices. Each GPIO module supports 32 bits of I/O.
GPMI	General Purpose Media Interface	Connectivity Peripherals	The GPMI module supports up to 8x NAND devices. 40-bit ECC error correction for NAND Flash controller (GPMI2). The GPMI supports separate DMA channels per NAND device.
GPT	General Purpose Timer	Timer Peripherals	Each GPT is a 32-bit “free-running” or “set and forget” mode timer with programmable prescaler and compare and capture register. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in “set and forget” mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.
GPU2Dv2	Graphics Processing Unit-2D, ver. 2	Multimedia Peripherals	The GPU2Dv2 provides hardware acceleration for 2D graphics algorithms, such as Bit BLT, stretch BLT, and many other 2D functions.
GPU3Dv4	Graphics Processing Unit-3D, ver. 4	Multimedia Peripherals	The GPU2Dv4 provides hardware acceleration for 3D graphics algorithms with sufficient processor power to run desktop quality interactive graphics applications on displays up to HD1080 resolution. The GPU3D provides OpenGL ES 2.0, including extensions, OpenGL ES 1.1, and OpenVG 1.1

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
GPUVGv2	Vector Graphics Processing Unit, ver. 2	Multimedia Peripherals	OpenVG graphics accelerator provides OpenVG 1.1 support as well as other accelerations, including Real-time hardware curve tesselation of lines, quadratic and cubic Bezier curves, 16x Line Anti-aliasing, and various Vector Drawing functions.
HDMI Tx	HDMI Tx interface	Multimedia Peripherals	The HDMI module provides HDMI standard interface port to an HDMI 1.4 compliant display.
HSI	MIPI HSI interface	Connectivity Peripherals	The MIPI HSI provides a standard MIPI interface to the applications processor.
I^2C-1 I^2C-2 I^2C-3	I^2C Interface	Connectivity Peripherals	I^2C provide serial interface for external devices. Data rates of up to 400 kbps are supported.
IOMUXC	IOMUX Control	System Control Peripherals	This module enables flexible IO multiplexing. Each IO pad has default and several alternate functions. The alternate functions are software configurable.
IPUv3H-1 IPUv3H-2	Image Processing Unit, ver. 3H	Multimedia Peripherals	IPUv3H enables connectivity to displays and video sources, relevant processing and synchronization and control capabilities, allowing autonomous operation. The IPUv3H supports concurrent output to two display ports and concurrent input from two camera ports, through the following interfaces: • Parallel Interfaces for both display and camera • Single/dual channel LVDS display interface • HDMI transmitter • MIPI/DSI transmitter • MIPI/CSI-2 receiver The processing includes: • Image conversions: resizing, rotation, inversion, and color space conversion • A high-quality de-interlacing filter • Video/graphics combining • Image enhancement: color adjustment and gamut mapping, gamma correction, and contrast enhancement • Support for display backlight reduction
KPP	Key Pad Port	Connectivity Peripherals	KPP Supports 8 x 8 external key pad matrix. KPP features are: • Open drain design • Glitch suppression circuit design • Multiple keys detection • Standby key press detection
LDB	LVDS Display Bridge	Connectivity Peripherals	LVDS Display Bridge is used to connect the IPU (Image Processing Unit) to External LVDS Display Interface. LDB supports two channels; each channel has following signals: • One clock pair • Four data pairs Each signal pair contains LVDS special differential pad (PadP, PadM).
MMDC	Multi-Mode DDR Controller	Connectivity Peripherals	DDR Controller has the following features: • Supports dual x32 for LPDDR2-800 • Supports up to 4 GByte DDR memory space

Table 8. Maximum Supply Currents (continued)

Power Supply	Conditions	Maximum Current		Unit
		Power Virus	CoreMark	
MISC				
DRAM_VREF	—	1		mA

1 The actual maximum current drawn from VDD_HIGH_IN will be as shown plus any additional current drawn from the VDD_HIGH_CAP outputs, depending upon actual application configuration (for example, NVCC_LVDS_2P5, NVCC_MIPI, or HDMI, PCIe, and SATA VPH supplies).

2 Under normal operating conditions, the maximum current on VDD_SNVS_IN is shown Table 8. The maximum VDD_SNVS_IN current may be higher depending on specific operating configurations, such as BOOT_MODE[1:0] not equal to 00, or use of the Tamper feature. During initial power on, VDD_SNVS_IN can draw up to 1 mA if the supply is capable of sourcing that current. If less than 1 mA is available, the VDD_SNVS_CAP charge time will increase.

3 This is the maximum current per active USB physical interface.

4 The DRAM power consumption is dependent on several factors such as external signal termination. DRAM power calculators are typically available from memory vendors which take into account factors such as signal termination.
See the *i.MX 6Dual/6Quad Power Consumption Measurement Application Note* (AN4509) for examples of DRAM power consumption during specific use case scenarios.

5 General equation for estimated, maximum power consumption of an IO power supply:
Imax = N x C x V x (0.5 x F)
Where:
N—Number of IO pins supplied by the power line
C—Equivalent external capacitive load
V—IO voltage
(0.5 xF)—Data change rate. Up to 0.5 of the clock rate (F)
In this equation, Imax is in Amps, C in Farads, V in Volts, and F in Hertz.

4.1.6 Low Power Mode Supply Currents

Table 9 shows the current core consumption (not including I/O) of the i.MX 6Dual/6Quad processors in selected low power modes.

Table 9. Stop Mode Current and Power Consumption

Mode	Test Conditions	Supply	Typical[1]	Unit
WAIT	• ARM, SoC, and PU LDOs are set to 1.225 V • HIGH LDO set to 2.5 V • Clocks are gated • DDR is in self refresh • PLLs are active in bypass (24 MHz) • Supply voltages remain ON	VDD_ARM_IN (1.4 V)	6	mA
		VDD_SOC_IN (1.4 V)	23	mA
		VDD_HIGH_IN (3.0 V)	3.7	mA
		Total	52	mW
STOP_ON	• ARM LDO set to 0.9 V • SoC and PU LDOs set to 1.225 V • HIGH LDO set to 2.5 V • PLLs disabled • DDR is in self refresh	VDD_ARM_IN (1.4 V)	7.5	mA
		VDD_SOC_IN (1.4 V)	22	mA
		VDD_HIGH_IN (3.0 V)	3.7	mA
		Total	52	mW

Table 9. Stop Mode Current and Power Consumption (continued)

Mode	Test Conditions	Supply	Typical[1]	Unit
STOP_OFF	• ARM LDO set to 0.9 V • SoC LDO set to 1.225 V • PU LDO is power gated • HIGH LDO set to 2.5 V • PLLs disabled • DDR is in self refresh	VDD_ARM_IN (1.4 V)	7.5	mA
		VDD_SOC_IN (1.4 V)	13.5	mA
		VDD_HIGH_IN (3.0 V)	3.7	mA
		Total	41	mW
STANDBY	• ARM and PU LDOs are power gated • SoC LDO is in bypass • HIGH LDO is set to 2.5 V • PLLs are disabled • Low voltage • Well Bias ON • Crystal oscillator is enabled	VDD_ARM_IN (0.9 V)	0.1	mA
		VDD_SOC_IN (0.9 V)	13	mA
		VDD_HIGH_IN (3.0 V)	3.7	mA
		Total	22	mW
Deep Sleep Mode (DSM)	• ARM and PU LDOs are power gated • SoC LDO is in bypass • HIGH LDO is set to 2.5 V • PLLs are disabled • Low voltage • Well Bias ON • Crystal oscillator and bandgap are disabled	VDD_ARM_IN (0.9 V)	0.1	mA
		VDD_SOC_IN (0.9 V)	2	mA
		VDD_HIGH_IN (3.0 V)	0.5	mA
		Total	3.4	mW
SNVS Only	• VDD_SNVS_IN powered • All other supplies off • SRTC running	VDD_SNVS_IN (2.8V)	41	µA
		Total	115	µW

[1] The typical values shown here are for information only and are not guaranteed. These values are average values measured on a worst-case wafer at 25°C.

4.4 PLL Electrical Characteristics

4.4.1 Audio/Video PLL Electrical Parameters

Table 14. Audio/Video PLL Electrical Parameters

Parameter	Value
Clock output range	650 MHz ~1.3 GHz
Reference clock	24 MHz
Lock time	<11250 reference cycles

4.4.2 528 MHz PLL

Table 15. 528 MHz PLL Electrical Parameters

Parameter	Value
Clock output range	528 MHz PLL output
Reference clock	24 MHz
Lock time	<11250 reference cycles

4.4.3 Ethernet PLL

Table 16. Ethernet PLL Electrical Parameters

Parameter	Value
Clock output range	500 MHz
Reference clock	24 MHz
Lock time	<11250 reference cycles

4.4.4 480 MHz PLL

Table 17. 480 MHz PLL Electrical Parameters

Parameter	Value
Clock output range	480 MHz PLL output
Reference clock	24 MHz
Lock time	<383 reference cycles

Table 23. LPDDR2 I/O DC Electrical Parameters[1] (continued)

Parameters	Symbol	Test Conditions	Min	Max	Unit
Pull-up/pull-down impedance mismatch	MMpupd	—	-15	+15	%
240 Ω unit calibration resolution	Rres	—	—	10	Ω
Keeper circuit resistance	Rkeep	—	110	175	kΩ

1 Note that the JEDEC LPDDR2 specification (JESD209_2B) supersedes any specification in this document.

2 The single-ended signals need to be within the respective limits (Vih(dc) max, Vil(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot (see Table 27).

4.6.5 LVDS I/O DC Parameters

The LVDS interface complies with TIA/EIA 644-A standard. See TIA/EIA STANDARD 644-A, "*Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits*" for details.

Table 24 shows the Low Voltage Differential Signalling (LVDS) I/O DC parameters.

Table 24. LVDS I/O DC Parameters

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output Differential Voltage	V_{OD}	Rload=100 Ω between padP and padN	250	450	mV
Output High Voltage	V_{OH}	I_{OH} = 0 mA	1.25	1.6	V
Output Low Voltage	V_{OL}	I_{OL} = 0 mA	0.9	1.25	
Offset Voltage	V_{OS}	—	1.125	1.375	

4.7 I/O AC Parameters

This section includes the AC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2
- LVDS I/O

The GPIO and DDR I/O load circuit and output transition time waveforms are shown in Figure 4 and Figure 5.

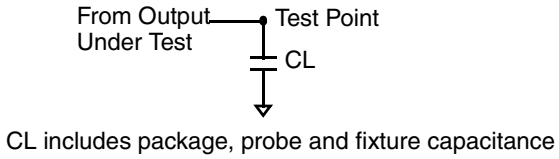

Figure 4. Load Circuit for Output

Table 32. Reset Timing Parameters

ID	Parameter	Min	Max	Unit
CC1	Duration of SRC_POR_B to be qualified as valid	1	—	XTALOSC_RTC_ XTALI cycle

4.9.2 WDOG Reset Timing Parameters

Figure 9 shows the WDOG reset timing and Table 33 lists the timing parameters.

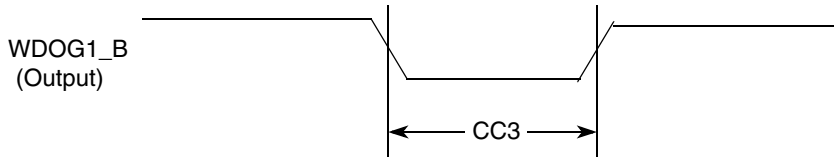

Figure 9. WDOG1_B Timing Diagram

Table 33. WDOG1_B Timing Parameters

ID	Parameter	Min	Max	Unit
CC3	Duration of WDOG1_B Assertion	1	—	XTALOSC_RTC_ XTALI cycle

NOTE

XTALOSC_RTC_XTALI is approximately 32 kHz.
XTALOSC_RTC_XTALI cycle is one period or approximately 30 µs.

NOTE

WDOG1_B output signals (for each one of the Watchdog modules) do not have dedicated pins, but are muxed out through the IOMUX. See the IOMUX manual for detailed information.

4.9.3 External Interface Module (EIM)

The following subsections provide information on the EIM. Maximum operating frequency for EIM data transfer is 104 MHz. Timing parameters in this section that are given as a function of register settings or clock periods are valid for the entire range of allowed frequencies (0–104 MHz).

4.12.5.1.2 MII Transmit Signal Timing (ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER, and ENET_TX_CLK)

The transmitter functions correctly up to an ENET_TX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. Additionally, the processor clock frequency must exceed twice the ENET_TX_CLK frequency.

Figure 41 shows MII transmit signal timings. Table 48 describes the timing parameters (M5–M8) shown in the figure.

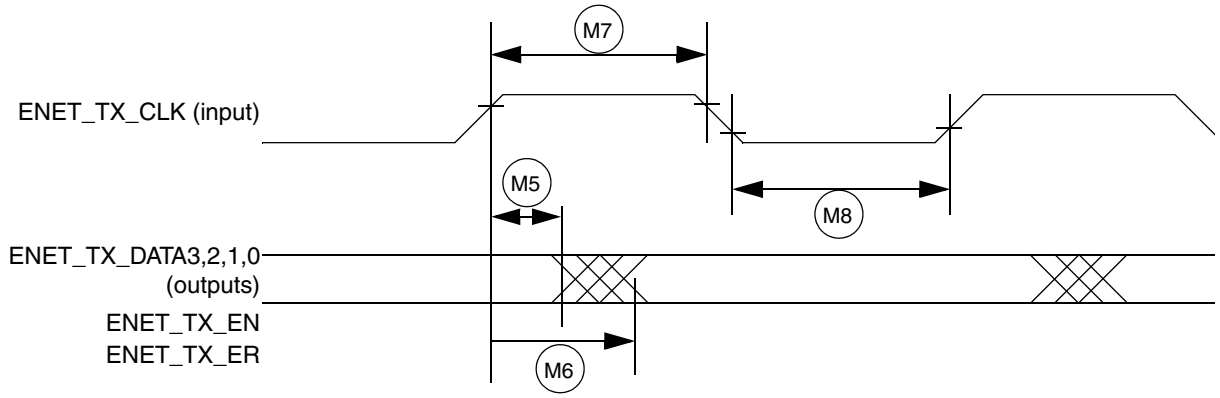

Figure 41. MII Transmit Signal Timing Diagram

Table 48. MII Transmit Signal Timing

ID	Characteristic[1]	Min	Max	Unit
M5	ENET_TX_CLK to ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER invalid	5	—	ns
M6	ENET_TX_CLK to ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER valid	—	20	ns
M7	ENET_TX_CLK pulse width high	35%	65%	ENET_TX_CLK period
M8	ENET_TX_CLK pulse width low	35%	65%	ENET_TX_CLK period

[1] ENET_TX_EN, ENET_TX_CLK, and ENET0_TXD0 have the same timing in 10-Mbps 7-wire interface mode.

4.12.5.1.3 MII Asynchronous Inputs Signal Timing (ENET_CRS and ENET_COL)

Figure 42 shows MII asynchronous input timings. Table 49 describes the timing parameter (M9) shown in the figure.

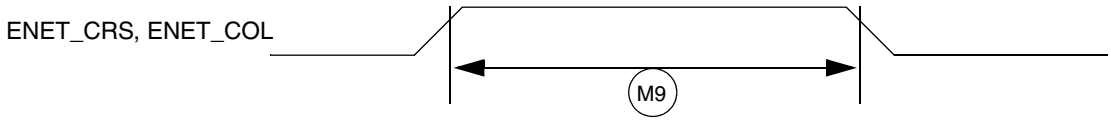

Figure 42. MII Async Inputs Timing Diagram

4.12.5.2 RMII Mode Timing

In RMII mode, ENET_CLK is used as the REF_CLK, which is a 50 MHz ± 50 ppm continuous reference clock. ENET_RX_EN is used as the ENET_RX_EN in RMII. Other signals under RMII mode include ENET_TX_EN, ENET0_TXD[1:0], ENET_RXD[1:0] and ENET_RX_ER.

Figure 44 shows RMII mode timings. Table 51 describes the timing parameters (M16–M21) shown in the figure.

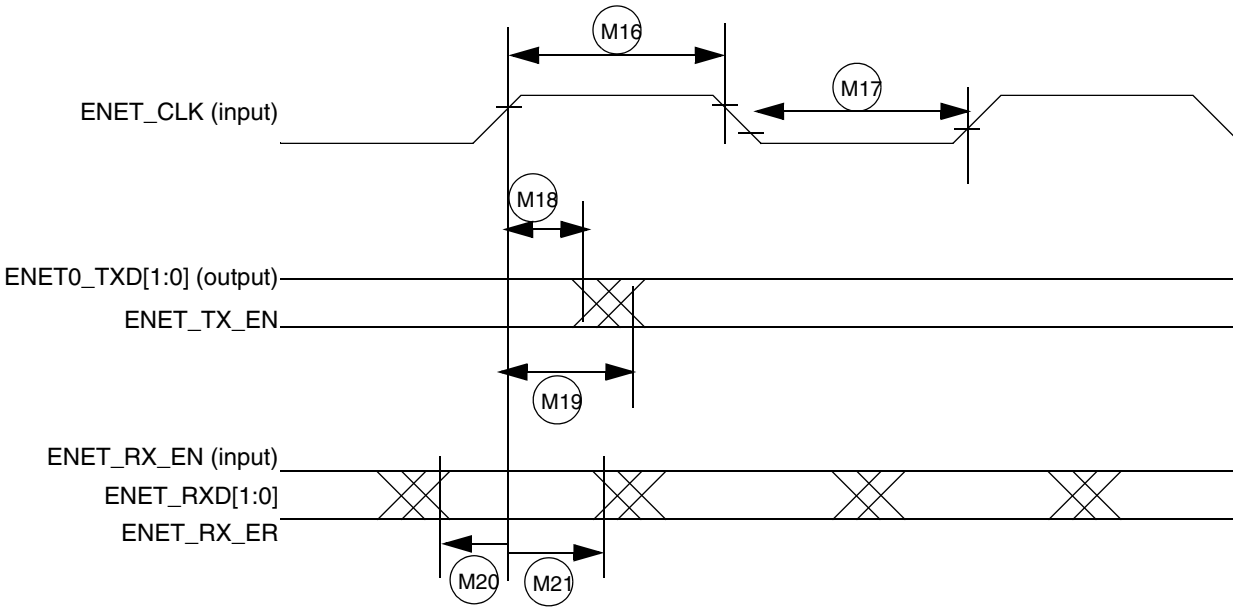

Figure 44. RMII Mode Signal Timing Diagram

Table 51. RMII Signal Timing

ID	Characteristic	Min	Max	Unit
M16	ENET_CLK pulse width high	35%	65%	ENET_CLK period
M17	ENET_CLK pulse width low	35%	65%	ENET_CLK period
M18	ENET_CLK to ENET0_TXD[1:0], ENET_TX_EN invalid	4	—	ns
M19	ENET_CLK to ENET0_TXD[1:0], ENET_TX_EN valid	—	13.5	ns
M20	ENET_RXD[1:0], ENET_RX_EN(ENET_RX_EN), ENET_RX_ER to ENET_CLK setup	4	—	ns
M21	ENET_CLK to ENET_RXD[1:0], ENET_RX_EN, ENET_RX_ER hold	2	—	ns

4.12.5.3 RGMII Signal Switching Specifications

The following timing specifications meet the requirements for RGMII interfaces for a range of transceiver devices.

Table 52. RGMII Signal Switching Specifications[1]

Symbol	Description	Min	Max	Unit
T_{cyc}[2]	Clock cycle duration	7.2	8.8	ns
T_{skewT}[3]	Data to clock output skew at transmitter	-100	900	ps
T_{skewR}[3]	Data to clock input skew at receiver	1	2.6	ns
Duty_G[4]	Duty cycle for Gigabit	45	55	%
Duty_T[4]	Duty cycle for 10/100T	40	60	%
Tr/Tf	Rise/fall time (20–80%)	—	0.75	ns

1 The timings assume the following configuration:
DDR_SEL = (11)b
DSE (drive-strength) = (111)b

2 For 10 Mbps and 100 Mbps, T_{cyc} will scale to 400 ns ±40 ns and 40 ns ±4 ns respectively.

3 For all versions of RGMII prior to 2.0; This implies that PC board design will require clocks to be routed such that an additional delay of greater than 1.2 ns and less than 1.7 ns will be added to the associated clock signal. For 10/100, the max value is unspecified.

4 Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest speed transitioned between.

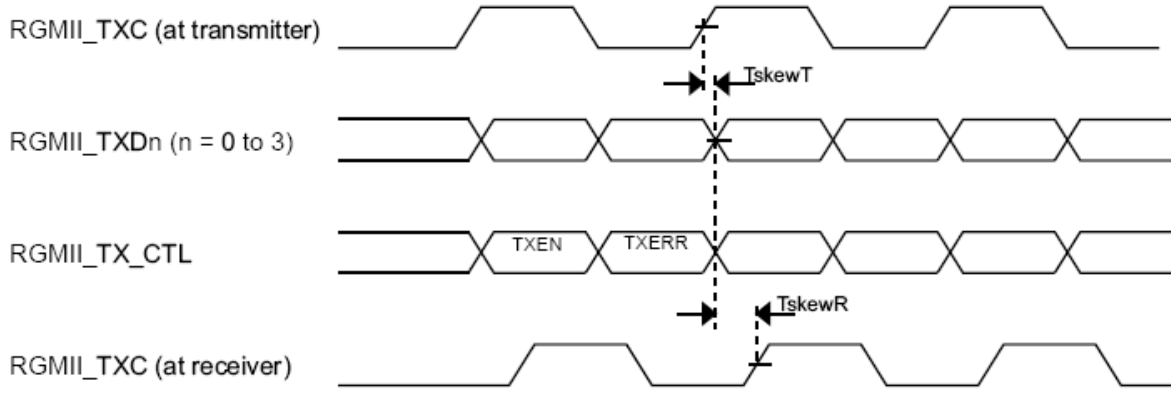

Figure 45. RGMII Transmit Signal Timing Diagram Original

Power-up time for the HDMI 3D Tx PHY while operating with the fastest input reference clock supported (340 MHz) is 133 µs.

4.12.7.2 Electrical Characteristics

The table below provides electrical characteristics for the HDMI 3D Tx PHY. The following three figures illustrate various definitions and measurement conditions specified in the table below.

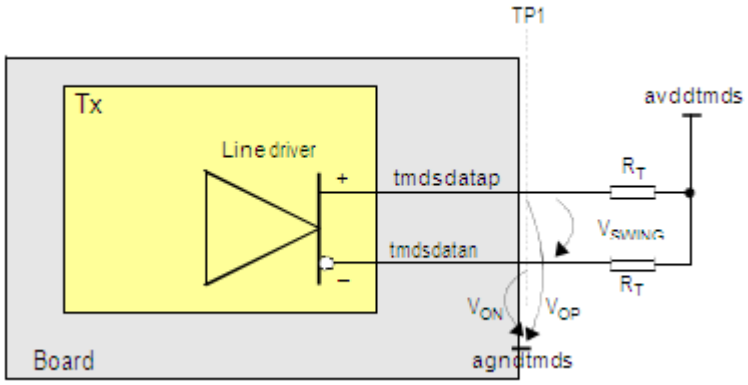

Figure 48. Driver Measuring Conditions

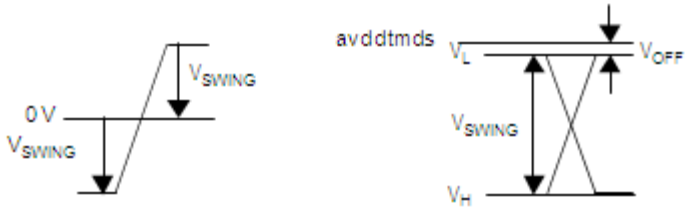

Figure 49. Driver Definitions

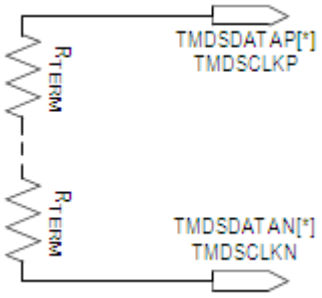

Figure 50. Source Termination

Table 53. Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Operating conditions for HDMI						
avddtmds	Termination supply voltage	—	3.15	3.3	3.45	V

stops receiving data from the stream. For the next line, the IPU2_CSIx_HSYNC timing repeats. For the next frame, the IPU2_CSIx_VSYNC timing repeats.

4.12.10.2.3 Non-Gated Clock Mode

The timing is the same as the gated-clock mode (described in Section 4.12.10.2.2, "Gated Clock Mode,") except for the IPU2_CSIx_HSYNC signal, which is not used (see Figure 58). All incoming pixel clocks are valid and cause data to be latched into the input FIFO. The IPU2_CSIx_PIX_CLK signal is inactive (states low) until valid data is going to be transmitted over the bus.

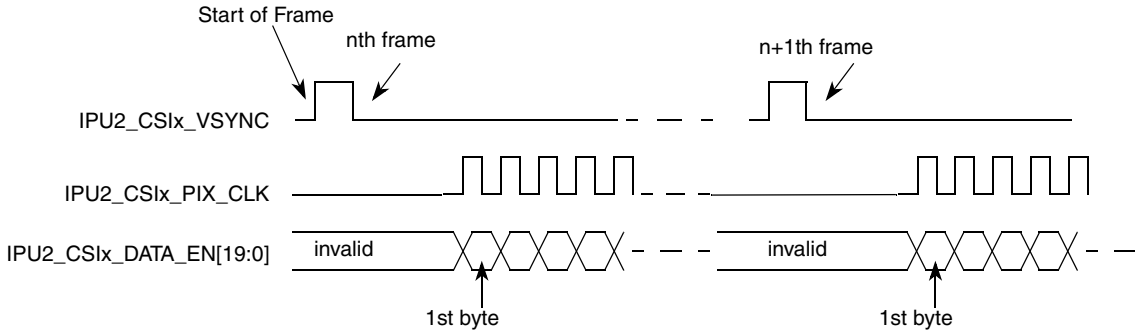

Figure 58. Non-Gated Clock Mode Timing Diagram

The timing described in Figure 58 is that of a typical sensor. Some other sensors may have a slightly different timing. The CSI can be programmed to support rising/falling-edge triggered IPU2_CSIx_VSYNC; active-high/low IPU2_CSIx_HSYNC; and rising/falling-edge triggered IPU2_CSIx_PIX_CLK.

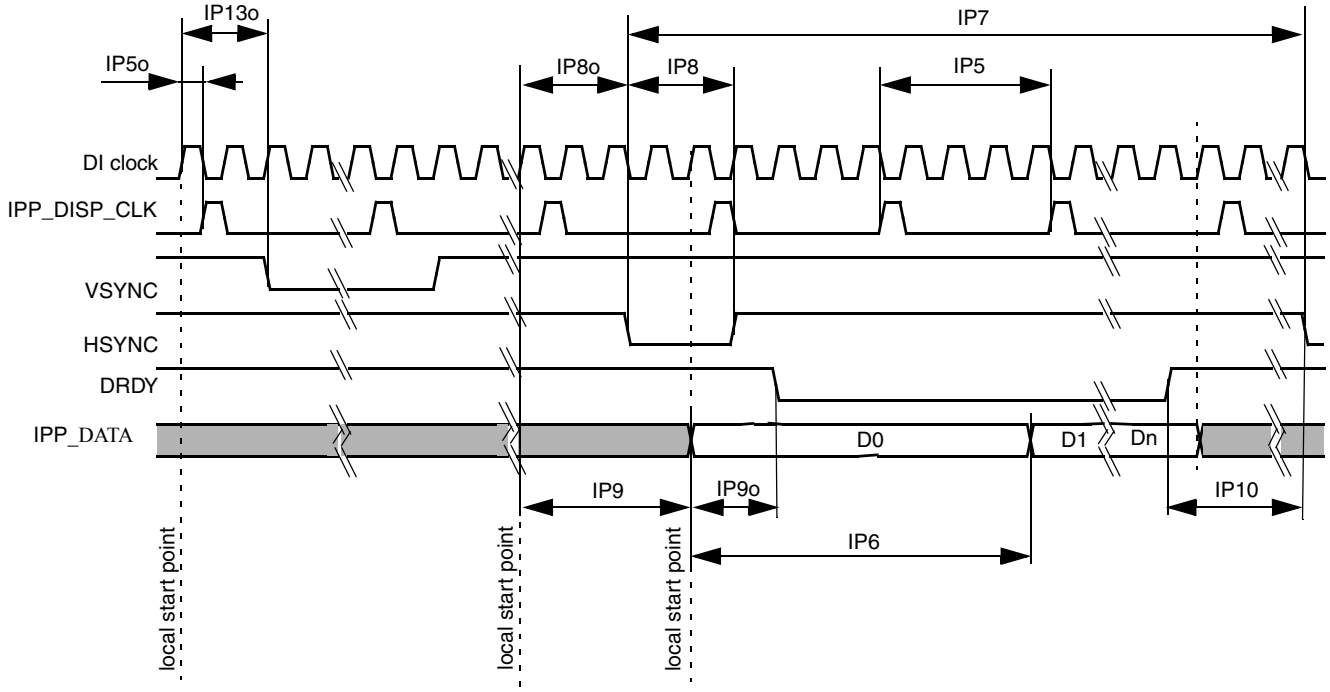

Figure 61. TFT Panels Timing Diagram—Horizontal Sync Pulse

Figure 62 depicts the vertical timing (timing of one frame). All parameters shown in the figure are programmable.

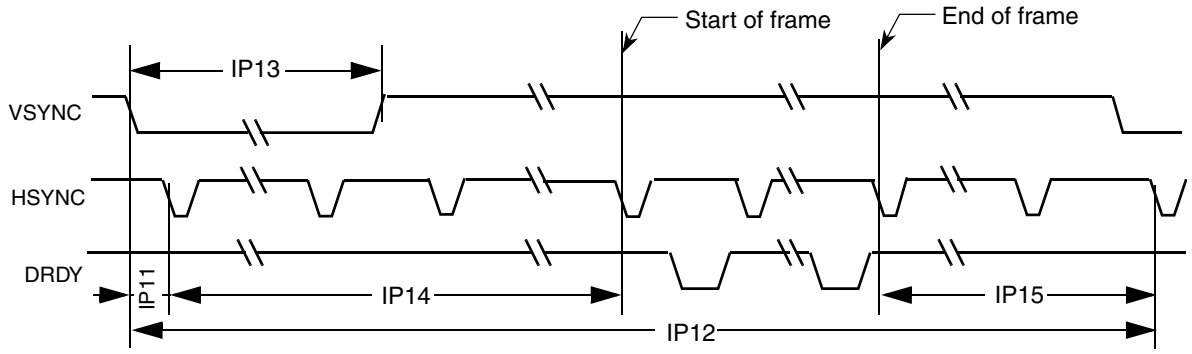

Figure 62. TFT Panels Timing Diagram—Vertical Sync Pulse

4.12.19.1 SSI Transmitter Timing with Internal Clock

Figure 86 depicts the SSI transmitter internal clock timing and Table 71 lists the timing parameters for the SSI transmitter internal clock.

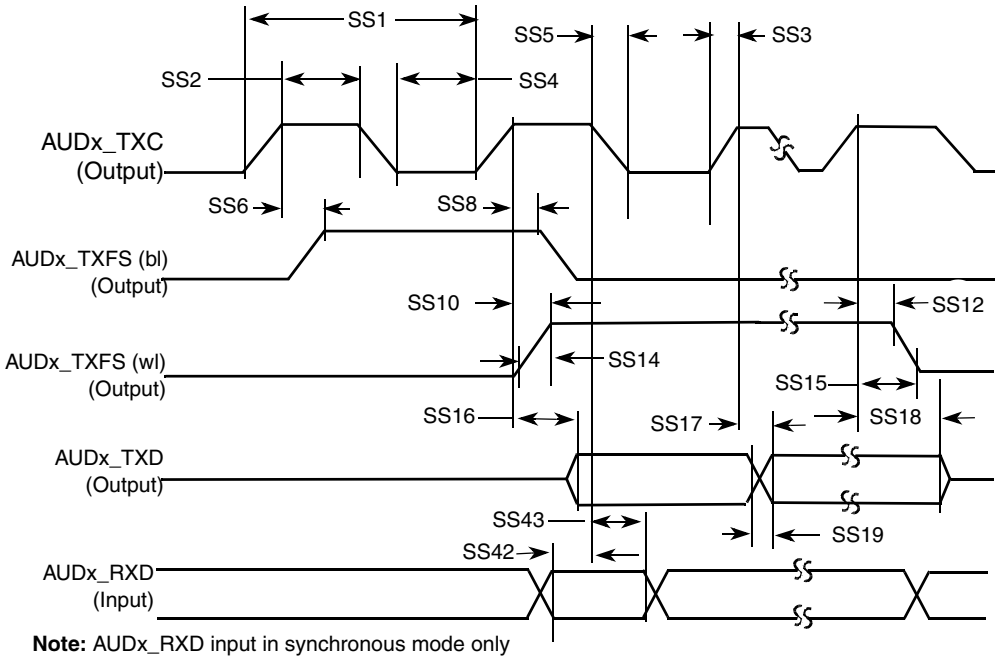

Figure 86. SSI Transmitter Internal Clock Timing Diagram

Table 71. SSI Transmitter Timing with Internal Clock

ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	AUDx_TXC/AUDx_RXC clock period	81.4	—	ns
SS2	AUDx_TXC/AUDx_RXC clock high period	36.0	—	ns
SS4	AUDx_TXC/AUDx_RXC clock low period	36.0	—	ns
SS6	AUDx_TXC high to AUDx_TXFS (bl) high	—	15.0	ns
SS8	AUDx_TXC high to AUDx_TXFS (bl) low	—	15.0	ns
SS10	AUDx_TXC high to AUDx_TXFS (wl) high	—	15.0	ns
SS12	AUDx_TXC high to AUDx_TXFS (wl) low	—	15.0	ns
SS14	AUDx_TXC/AUDx_RXC Internal AUDx_TXFS rise time	—	6.0	ns
SS15	AUDx_TXC/AUDx_RXC Internal AUDx_TXFS fall time	—	6.0	ns
SS16	AUDx_TXC high to AUDx_TXD valid from high impedance	—	15.0	ns
SS17	AUDx_TXC high to AUDx_TXD high/low	—	15.0	ns
SS18	AUDx_TXC high to AUDx_TXD high impedance	—	15.0	ns

Table 71. SSI Transmitter Timing with Internal Clock (continued)

ID	Parameter	Min	Max	Unit
Synchronous Internal Clock Operation				
SS42	AUDx_RXD setup before AUDx_TXC falling	10.0	—	ns
SS43	AUDx_RXD hold after AUDx_TXC falling	0.0	—	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal AUDx_TXC/AUDx_RXC and/or the frame sync AUDx_TXFS/AUDx_RXFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- The terms, WL and BL, refer to Word Length(WL) and Bit Length(BL).
- For internal Frame Sync operation using external clock, the frame sync timing is the same as that of transmit data (for example, during AC97 mode of operation).

4.12.20.2 UART RS-232 Serial Mode Timing

The following sections describe the electrical information of the UART module in the RS-232 mode.

4.12.20.2.1 UART Transmitter

Figure 90 depicts the transmit timing of UART in the RS-232 serial mode, with 8 data bit/1 stop bit format. Table 76 lists the UART RS-232 serial mode transmit timing characteristics.

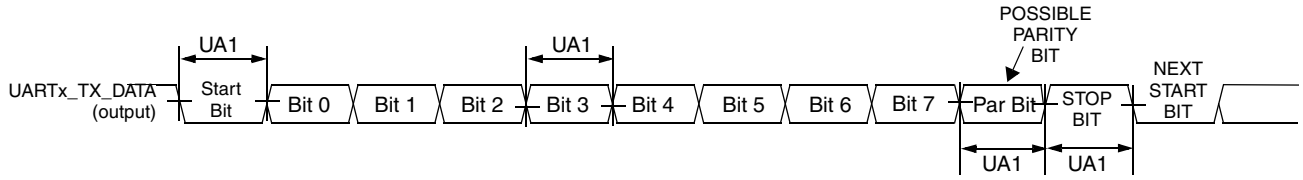

Figure 90. UART RS-232 Serial Mode Transmit Timing Diagram

Table 76. RS-232 Serial Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA1	Transmit Bit Time	t_{Tbit}	$1/F_{baud\_rate}$ [1] – T_{ref_clk} [2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—

[1] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

[2] T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

4.12.20.2.2 UART Receiver

Figure 91 depicts the RS-232 serial mode receive timing with 8 data bit/1 stop bit format. Table 77 lists serial mode receive timing characteristics.

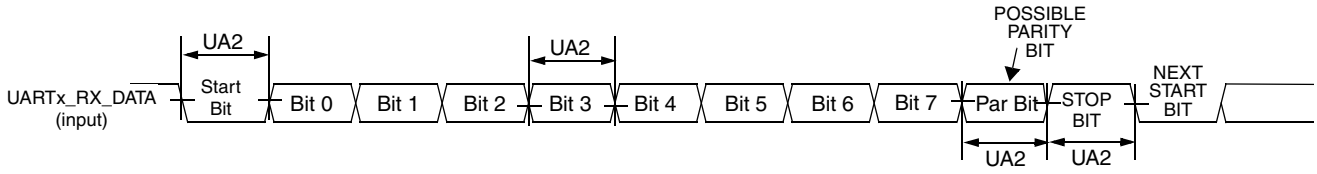

Figure 91. UART RS-232 Serial Mode Receive Timing Diagram

Table 77. RS-232 Serial Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA2	Receive Bit Time[1]	t_{Rbit}	$1/F_{baud\_rate}$ [2] – $1/(16 \times F_{baud\_rate})$	$1/F_{baud\_rate} + 1/(16 \times F_{baud\_rate})$	—

[1] The UART receiver can tolerate $1/(16 \times F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud\_rate})$.

[2] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

6.2.2 12 x 12 mm PoP Ground, Power, Sense, and Reference Contact Assignments

Table 84 shows the device connection list for ground, power, sense, and reference contact signals alpha-sorted by name.

Table 84. 12 x 12 mm PoP Ground, Power, Sense, and Reference Contact Assignments

Ball Name	PoP Bottom Ball Position	PoP Top Ball Position	Remark
CSI_REXT	H6	—	—
DNU	—	A1, A29, AJ1, AJ29	—
DRAM_VREF	AG10	B15, R2, U28, AH16	—
DSI_REXT	K6	—	—
FA_ANA	J7	—	This signal should be tied to GND.
GND	A15, A29, B4, C6, D3, F6, F7, H3, K13, K14, K15, L3, L6, L13, L14, L15, M3, M6, M13, M14, M15, N3, N6, N13, N14, N15, P14, R14, R19, R20, T14, T19, T20, U10, U11, U12, U13, U14, U15, U16, U17, U18, V10, V11, V12, V13, V14, V15, V16, V17, V18, W13, W14, W17, W18, Y13, Y14, Y17, Y18, AG5, AG7, AG8, AG11, AG13, AH11, AH12, AH13, AH14, AH15, AH16, AH17, AH18, AH19, AJ1, AJ2, AJ11, AJ12, AJ13, AJ14, AJ15, AJ16, AJ17, AJ18, AJ20, AJ29	A2, A6, A9, A11, A14, A28, B1, B14, B21, B24, B29, E28, F1, H28, J1, L29, M2, P1, P2, R28, V2, V28, AA28, AB2, AE2, AF28, AH1, AH5, AH14, AH18, AH29, AJ2, AJ7, AJ11, AJ16, AJ22, AJ28	—
GPANAIO	C10	—	Analog output for NXP use only. This output must remain unconnected.
HDMI_DDCCEC	R2	—	Analog ground reference for the Hot Plug detect signal.
HDMI_REF	P6	—	—
HDMI_VP	M7	—	—
HDMI_VPH	N7	—	—
NC	A1	—	No connect
NVCC_CSI	T7	—	Supply of the camera sensor interface
NVCC_DRAM	Y23, AA23, AB23, AC8, AC9, AC10, AC11, AC12, AC13, AC14, AC15, AC16, AC17, AC18, AC19, AC20, AC21, AC22, AC23, AD8, AD9, AD10, AD11, AD12, AD13, AD14, AD15, AD16, AD17, AD18, AD19, AD20, AD21	—	Supply of the DDR interface
NVCC_EIM0	K23	—	Supply of the EIM interface
NVCC_EIM1	M23	—	Supply of the EIM interface
NVCC_EIM2	P23	—	Supply of the EIM interface
NVCC_ENET	W23	—	Supply of the ENET interface
NVCC_GPIO	W7	—	Supply of the GPIO interface

Table 85. 12 x 12 mm Functional Contact Assignments (continued)

Ball Name	PoP Bottom Ball	PoP Top Ball	Power Group	Ball Type	Out of Reset Condition[1]			
					Default Mode	Default Function	Input/ Output	Value[2]
CSI_D3M	G2	—	NVCC_MIPI	—	—	CSI_DATA3_N	—	—
CSI_D3P	G1	—	NVCC_MIPI	—	—	CSI_DATA3_P	—	—
CSI0_DAT4	U6	—	NVCC_CSI	GPIO	ALT5	GPIO5_IO22	Input	PU (100k)
CSI0_DAT5	U7	—	NVCC_CSI	GPIO	ALT5	GPIO5_IO23	Input	PU (100k)
CSI0_DAT6	Y1	—	NVCC_CSI	GPIO	ALT5	GPIO5_IO24	Input	PU (100k)
CSI0_DAT7	Y2	—	NVCC_CSI	GPIO	ALT5	GPIO5_IO25	Input	PU (100k)
CSI0_DAT8	W2	—	NVCC_CSI	GPIO	ALT5	GPIO5_IO26	Input	PU (100k)
CSI0_DAT9	W1	—	NVCC_CSI	GPIO	ALT5	GPIO5_IO27	Input	PU (100k)
CSI0_DAT10	W3	—	NVCC_CSI	GPIO	ALT5	GPIO5_IO28	Input	PU (100k)
CSI0_DAT11	V1	—	NVCC_CSI	GPIO	ALT5	GPIO5_IO29	Input	PU (100k)
CSI0_DAT12	V3	—	NVCC_CSI	GPIO	ALT5	GPIO5_IO30	Input	PU (100k)
CSI0_DAT13	T6	—	NVCC_CSI	GPIO	ALT5	GPIO5_IO31	Input	PU (100k)
CSI0_DAT14	U2	—	NVCC_CSI	GPIO	ALT5	GPIO6_IO00	Input	PU (100k)
CSI0_DAT15	V2	—	NVCC_CSI	GPIO	ALT5	GPIO6_IO01	Input	PU (100k)
CSI0_DAT16	T2	—	NVCC_CSI	GPIO	ALT5	GPIO6_IO02	Input	PU (100k)
CSI0_DAT17	U1	—	NVCC_CSI	GPIO	ALT5	GPIO6_IO03	Input	PU (100k)
CSI0_DAT18	T1	—	NVCC_CSI	GPIO	ALT5	GPIO6_IO04	Input	PU (100k)
CSI0_DAT19	R3	—	NVCC_CSI	GPIO	ALT5	GPIO6_IO05	Input	PU (100k)
CSI0_DATA_EN	V6	—	NVCC_CSI	GPIO	ALT5	GPIO5_IO20	Input	PU (100k)
CSI0_MCLK	AA2	—	NVCC_CSI	GPIO	ALT5	GPIO5_IO19	Input	PU (100k)
CSI0_PIXCLK	AD1	—	NVCC_CSI	GPIO	ALT5	GPIO5_IO18	Input	PU (100k)
CSI0_VSYNC	AA1	—	NVCC_CSI	GPIO	ALT5	GPIO5_IO21	Input	PU (100k)
DI0_DISP_CLK	AF29	—	NVCC_LCD	GPIO	ALT5	GPIO4_IO16	Input	PU (100k)
DI0_PIN2	AD29	—	NVCC_LCD	GPIO	ALT5	GPIO4_IO18	Input	PU (100k)
DI0_PIN3	W24	—	NVCC_LCD	GPIO	ALT5	GPIO4_IO19	Input	PU (100k)
DI0_PIN4	U24	—	NVCC_LCD	GPIO	ALT5	GPIO4_IO20	Input	PU (100k)
DI0_PIN15	AD28	—	NVCC_LCD	GPIO	ALT5	GPIO4_IO17	Input	PU (100k)
DISP0_DAT0	AH29	—	NVCC_LCD	GPIO	ALT5	GPIO4_IO21	Input	PU (100k)
DISP0_DAT1	AD27	—	NVCC_LCD	GPIO	ALT5	GPIO4_IO22	Input	PU (100k)
DISP0_DAT2	AB27	—	NVCC_LCD	GPIO	ALT5	GPIO4_IO23	Input	PU (100k)
DISP0_DAT3	V23	—	NVCC_LCD	GPIO	ALT5	GPIO4_IO24	Input	PU (100k)
DISP0_DAT4	V24	—	NVCC_LCD	GPIO	ALT5	GPIO4_IO25	Input	PU (100k)
DISP0_DAT5	AH27	—	NVCC_LCD	GPIO	ALT5	GPIO4_IO26	Input	PU (100k)
DISP0_DAT6	U23	—	NVCC_LCD	GPIO	ALT5	GPIO4_IO27	Input	PU (100k)
DISP0_DAT7	AE28	—	NVCC_LCD	GPIO	ALT5	GPIO4_IO28	Input	PU (100k)
DISP0_DAT8	AJ26	—	NVCC_LCD	GPIO	ALT5	GPIO4_IO29	Input	PU (100k)
DISP0_DAT9	AG28	—	NVCC_LCD	GPIO	ALT5	GPIO4_IO30	Input	PU (100k)
DISP0_DAT10	AH26	—	NVCC_LCD	GPIO	ALT5	GPIO4_IO31	Input	PU (100k)
DISP0_DAT11	AJ27	—	NVCC_LCD	GPIO	ALT5	GPIO5_IO05	Input	PU (100k)
DISP0_DAT12	AF28	—	NVCC_LCD	GPIO	ALT5	GPIO5_IO06	Input	PU (100k)

Table 86. Signals with Differing Before Reset and After Reset States

Ball Name	Before Reset State	
	Input/Output	Value
EIM_A16	Input	PD (100K)
EIM_A17	Input	PD (100K)
EIM_A18	Input	PD (100K)
EIM_A19	Input	PD (100K)
EIM_A20	Input	PD (100K)
EIM_A21	Input	PD (100K)
EIM_A22	Input	PD (100K)
EIM_A23	Input	PD (100K)
EIM_A24	Input	PD (100K)
EIM_A25	Input	PD (100K)
EIM_DA0	Input	PD (100K)
EIM_DA1	Input	PD (100K)
EIM_DA2	Input	PD (100K)
EIM_DA3	Input	PD (100K)
EIM_DA4	Input	PD (100K)
EIM_DA5	Input	PD (100K)
EIM_DA6	Input	PD (100K)
EIM_DA7	Input	PD (100K)
EIM_DA8	Input	PD (100K)
EIM_DA9	Input	PD (100K)
EIM_DA10	Input	PD (100K)
EIM_DA11	Input	PD (100K)
EIM_DA12	Input	PD (100K)
EIM_DA13	Input	PD (100K)
EIM_DA14	Input	PD (100K)
EIM_DA15	Input	PD (100K)
EIM_EB0	Input	PD (100K)
EIM_EB1	Input	PD (100K)
EIM_EB2	Input	PD (100K)
EIM_EB3	Input	PD (100K)
EIM_LBA	Input	PD (100K)
EIM_RW	Input	PD (100K)
EIM_WAIT	Input	PD (100K)
GPIO_17	Output	Drive state unknown (x)