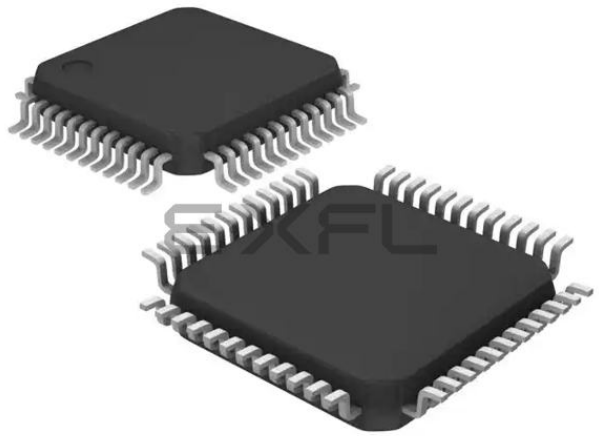
Renesas Electronics America Inc - DF71240AN50FPV Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	SH-2
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	SCI
Peripherals	POR, PWM, WDT
Number of I/O	23
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df71240an50fpv

1.4 Pin Functions

Table 1.2 summarizes the pin functions.

Table 1.2 Pin Functions

Classification	Symbol	I/O	Name	Function
Power supply	Vcc	I	Power supply	Power supply pin Connect all Vcc pins to the system. There will be no operation if any pins are open.
	Vss	I	Ground	Ground pin Connect all Vss pins to the system power supply (0V). There will be no operation if any pins are open.
	V_{CL}	O	Power supply for internal power-down	External capacitance pins for internal power-down power supply Connect these pins to Vss via a 0.1 to 0.47 μF capacitor (placed close to the pins).
Clock	PLLVss	I	PLL ground	Ground pin for the on-chip PLL oscillator
	EXTAL	I	External clock	Connected to a crystal resonator. An external clock signal may also be input to the EXTAL pin.
	XTAL	O	Crystal	Connected to a crystal resonator.
Operating mode control	MD1	I	Mode set	Sets the operating mode. Do not change values on this pin during operation.
	FWE	I	Flash memory write enable	Pin for flash memory Flash memory can be protected against programming or erasure through this pin.

Table 4.4 Frequency Division Ratios Specifiable with FRQCR

PLL Multiplication Ratio	FRQCR Division Ratio Setting				Clock Ratio				Clock Frequency (MHz)*				
	Iϕ	Bϕ	Pϕ	MPϕ	Iϕ	Bϕ	Pϕ	MPϕ	Input Clock	Iϕ	Bϕ	Pϕ	MPϕ
×8	1/8	1/8	1/8	1/8	1	1	1	1	10	10	10	10	10
	1/4	1/8	1/8	1/8	2	1	1	1	10	20	10	10	10
	1/4	1/4	1/4	1/4	2	2	2	2	10	20	20	20	20
	1/2	1/4	1/4	1/4	4	2	2	2	10	40	20	20	20
	1/2	1/2	1/2	1/2	4	4	4	4	10	40	40	40	40
	1/8	1/8	1/8	1/8	1	1	1	1	12.5	12.5	12.5	12.5	12.5
	1/4	1/8	1/8	1/8	2	1	1	1	12.5	25	12.5	12.5	12.5
	1/4	1/4	1/4	1/4	2	2	2	2	12.5	25	25	25	25
	1/2	1/4	1/4	1/4	4	2	2	2	12.5	50	25	25	25

Notes: * Clock frequencies when the input clock frequency is assumed to be the shown value. The internal clock (Iϕ) frequency must be 10 to 50 MHz and the peripheral clock (Pϕ) frequency must be 10 to 40 MHz. The bus clock (Bϕ) frequency must be equal to the peripheral clock (Pϕ) frequency.

1. The PLL multiplication ratio is fixed at ×8. The division ratio can be selected from ×1/2, ×1/4, and ×1/8 for each clock by the setting in the frequency control register.
2. The output frequency of the PLL circuit is the product of the frequency of the input from the crystal resonator or EXTAL pin and the multiplication ratio (×8) of the PLL circuit.
3. The input to the divider is always the output from the PLL circuit.
4. The internal clock (Iϕ) frequency is the product of the frequency of the input from the crystal resonator or EXTAL pin, the multiplication ratio (×8) of the PLL circuit, and the division ratio of the divider. The resultant frequency must be a maximum of 50 MHz (maximum operating frequency).
5. The peripheral clock (Pϕ) frequency is the product of the frequency of the input from the crystal resonator or EXTAL pin, the multiplication ratio (×8) of the PLL circuit, and the division ratio of the divider. The resultant frequency must be a maximum of 40 MHz.
6. When using the MTU2, the MTU2 clock (MPϕ) frequency must be equal to or higher than the peripheral clock frequency (Pϕ). The MTU2 clock (MPϕ) frequency are the product of the frequency of the input from the crystal resonator or EXTAL pin, the multiplication ratio (×8) of the PLL circuit, and the division ratio of the divider.
7. The frequency of the CK pin is always be equal to the bus clock (Bϕ) frequency.
8. The bus clock (Bϕ) frequency must be equal to the peripheral clock (Pϕ) frequency.

Table 6.3 Interrupt Exception Handling Vectors and Priorities

Interrupt Source	Name	Vector No.	Vector Table Starting Address	IPR	Default Priority
User break		12	H'00000030	—	High
External pin	NMI	11	H'0000002C	—	
	IRQ0 (only SH7125)	64	H'00000100	IPRA15 to IPRA12	
	IRQ1	65	H'00000104	IPRA11 to IPRA8	
	IRQ2	66	H'00000108	IPRA7 to IPRA4	
	IRQ3	67	H'0000010C	IPRA3 to IPRA0	
MTU2_0	TGIA_0	88	H'00000160	IPRD15 to IPRD12	
	TGIB_0	89	H'00000164		
	TGIC_0	90	H'00000168		
	TGID_0	91	H'0000016C		
	TCIV_0	92	H'00000170	IPRD11 to IPRD8	
	TGIE_0	93	H'00000174		
	TGIF_0	94	H'00000178		
MTU2_1	TGIA_1	96	H'00000180	IPRD7 to IPRD4	
	TGIB_1	97	H'00000184		
	TCIV_1	100	H'00000190	IPRD3 to IPRD0	
	TCIU_1	101	H'00000194		
MTU2_2	TGIA_2	104	H'000001A0	IPRE15 to IPRE12	
	TGIB_2	105	H'000001A4		
	TCIV_2	108	H'000001B0	IPRE11 to IPRE8	
	TCIU_2	109	H'000001B4		
MTU2_3	TGIA_3	112	H'000001C0	IPRE7 to IPRE4	
	TGIB_3	113	H'000001C4		
	TGIC_3	114	H'000001C8		
	TGID_3	115	H'000001CC		
	TCIV_3	116	H'000001D0	IPRE3 to IPRE0	Low

7.2.11 Break Control Register (BRCR)

BRCR sets the following conditions:

1. Channels A and B are used in two independent channel conditions or under the sequential condition.
2. A break is set before or after instruction execution.
3. Specify whether to include the number of execution times on channel B in comparison conditions.
4. Determine whether to include data bus on channels A and B in comparison conditions.
5. Enable PC trace.
6. Specify whether to request the user break interrupt when channels A and B match with comparison conditions.

BRCR is a 32-bit readable/writable register that has break conditions match flags and bits for setting a variety of break conditions.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	UBIDB	-	UBIDA	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R/W	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SCM FCA	SCM FCB	SCM FDA	SCM FDB	PCTE	PCBA	-	-	DBEA	PCBB	DBEB	-	SEQ	-	-	ETBE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R	R/W	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 20	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
19	UBIDB	0	R/W	User Break Disable B Enables or disables the user break interrupt request when the channel B break conditions are satisfied. 0: User break interrupt request is enabled when break conditions are satisfied 1: User break interrupt request is disabled when break conditions are satisfied

15. Counter Clearing by TGRA_3 Compare Match

In complementary PWM mode, by setting the CCE bit in the timer waveform control register (TWCR), it is possible to have TCNT_3, TCNT_4, and TCNTS cleared by TGRA_3 compare match.

Figure 9.62 illustrates an operation example.

Notes: 1. Use this function only in complementary PWM mode 1 (transfer at crest)
2. Do not specify synchronous clearing by another channel (do not set the SYNC0 to SYNC4 bits in the timer synchronous register (TSYR) to 1 or the CE0A, CE0B, CE0C, CE0D, CE1A, CE1B, CE1C, and CE1D bits in the timer synchronous clear register (TSYCR) to 1).
3. Do not set the PWM duty value to H'0000.
4. Do not set the PSYE bit in timer output control register 1 (TOCR1) to 1.

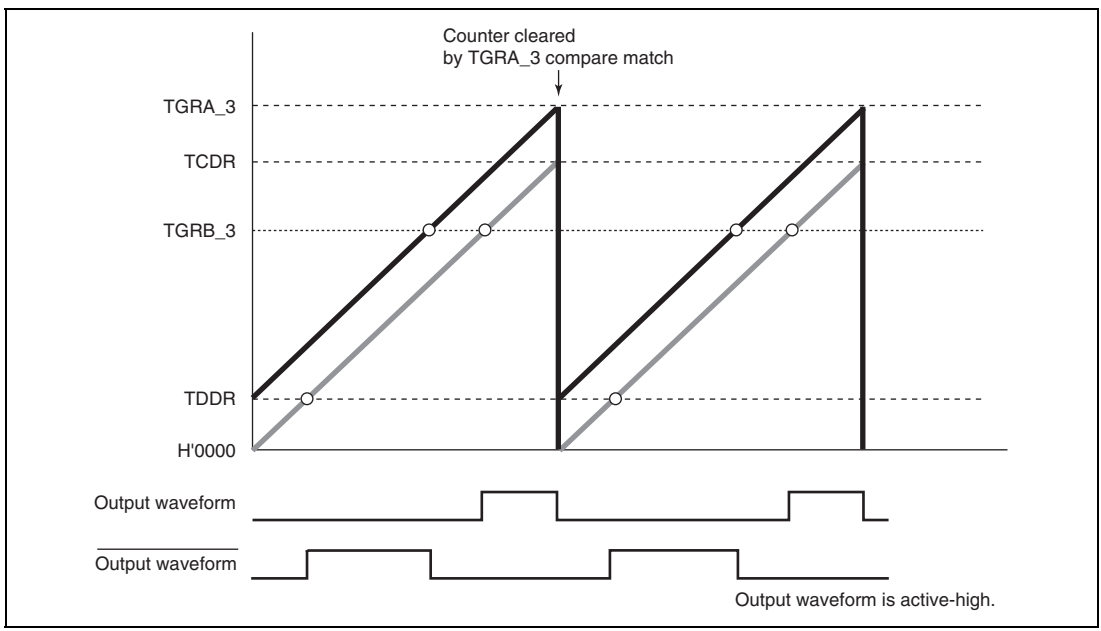

Figure 9.62 Example of Counter Clearing Operation by TGRA_3 Compare Match

9.6.2 Interrupt Signal Timing

TGF Flag Setting Timing in Case of Compare Match: Figures 9.99 and 9.100 show the timing for setting of the TGF flag in TSR on compare match, and TGI interrupt request signal timing.

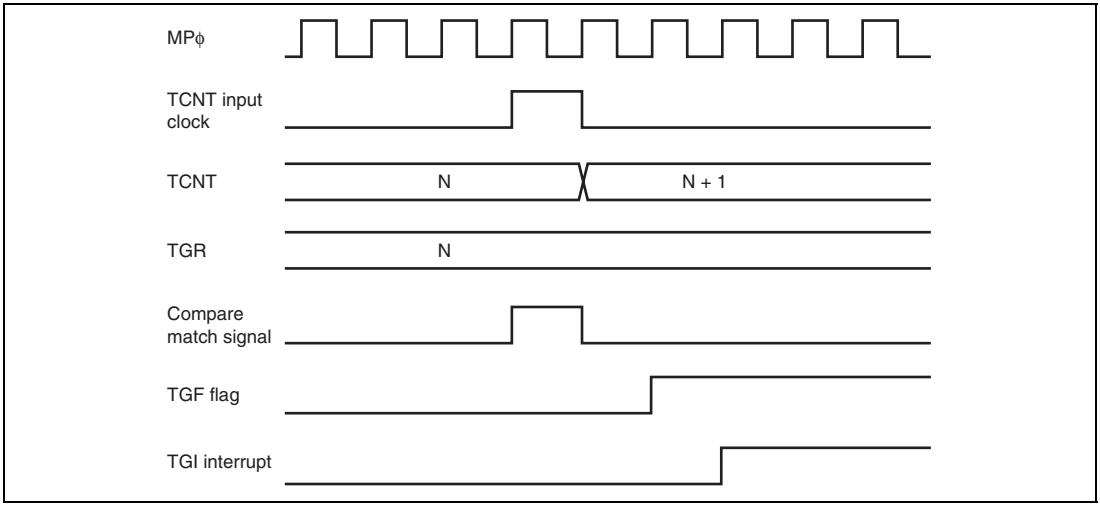

Figure 9.99 TGI Interrupt Timing (Compare Match) (Channels 0 to 4)

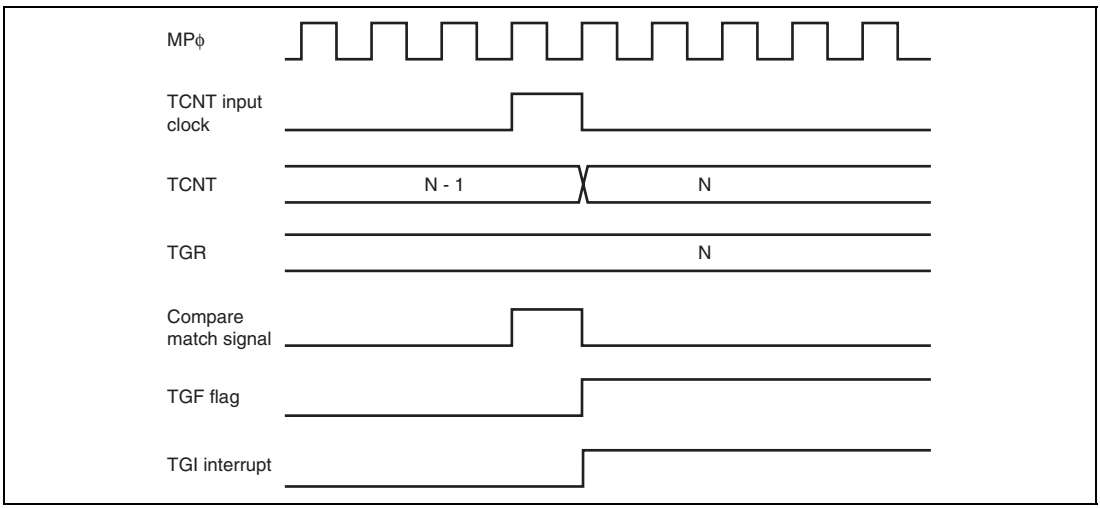

Figure 9.100 TGI Interrupt Timing (Compare Match) (Channel 5)

Operation when Error Occurs during Normal Mode Operation, and Operation is Restarted in PWM Mode 1: Figure 9.125 shows an explanatory diagram of the case where an error occurs in normal mode and operation is restarted in PWM mode 1 after re-setting.

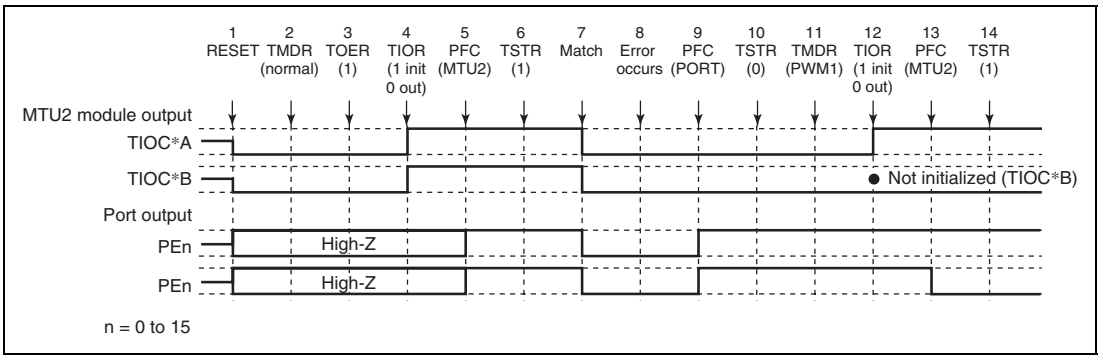

Figure 9.125 Error Occurrence in Normal Mode, Recovery in PWM Mode 1

1 to 10 are the same as in figure 9.124.

11. Set PWM mode 1.
12. Initialize the pins with TIOR. (In PWM mode 1, the TIOC*B side is not initialized. If initialization is required, initialize in normal mode, then switch to PWM mode 1.)
13. Set MTU2 output with the PFC.
14. Operation is restarted by TSTR.

Operation when Error Occurs during Reset-Synchronized PWM Mode Operation, and Operation is Restarted in PWM Mode 1: Figure 9.150 shows an explanatory diagram of the case where an error occurs in reset-synchronized PWM mode and operation is restarted in PWM mode 1 after re-setting.

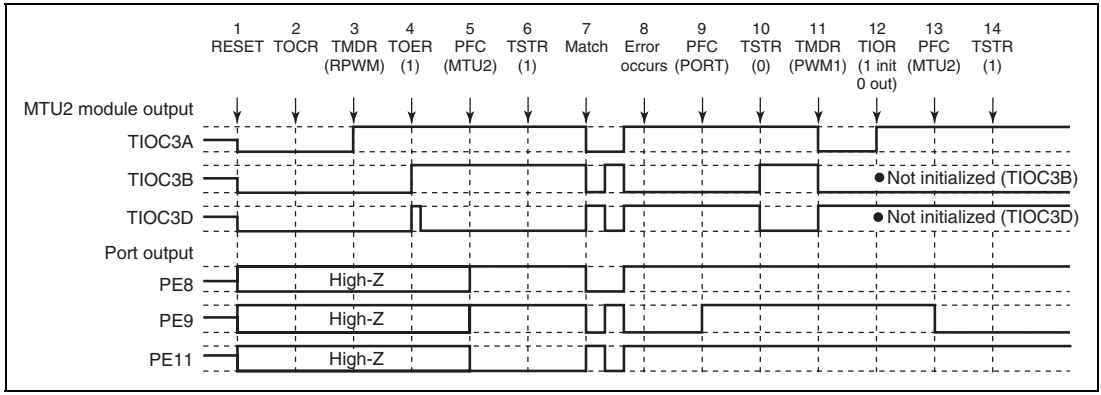

Figure 9.150 Error Occurrence in Reset-Synchronized PWM Mode, Recovery in PWM Mode 1

1 to 10 are the same as in figure 9.149.

11. Set PWM mode 1. (MTU2 positive phase output is low, and negative phase output is high.)
12. Initialize the pins with TIOR. (In PWM mode 1, the TIOC *B side is not initialized.)
13. Set MTU2 output with the PFC.
14. Operation is restarted by TSTR.

Bit	Bit Name	Initial value	R/W	Description
3	STOP	0	R/W	Stop Bit Length Selects one or two bits as the stop bit length in asynchronous mode. This setting is used only in asynchronous mode. It is ignored in clock synchronous mode because no stop bits are added. 0: One stop bit*[1] 1: Two stop bits*[2] When receiving, only the first stop bit is checked, regardless of the STOP bit setting. If the second stop bit is 1, it is treated as a stop bit, but if the second stop bit is 0, it is treated as the start bit of the next incoming character. Notes: 1. When transmitting, a single 1-bit is added at the end of each transmitted character. 2. When transmitting, two 1 bits are added at the end of each transmitted character.
2	MP	0	R/W	Multiprocessor Mode (only in asynchronous mode) Enables or disables multiprocessor mode. The PE and O/$\overline{E}$ bit settings are ignored in multiprocessor mode. 0: Multiprocessor mode disabled 1: Multiprocessor mode enabled
1, 0	CKS[1:0]	00	R/W	Clock Select 1 and 0 Select the internal clock source of the on-chip baud rate generator. Four clock sources are available. Pϕ, Pϕ/4, Pϕ/16 and Pϕ/64. For further information on the clock source, bit rate register settings, and baud rate, see section 12.3.10, Bit Rate Register (SCBRR). 00: Pϕ 01: Pϕ/4 10: Pϕ/16 11: Pϕ/64 Note: Pϕ: Peripheral clock

Bit	Bit Name	Initial value	R/W	Description
4	FER	0	R/(W)*	Framing Error Indicates that a framing error occurred during data reception in asynchronous mode, causing abnormal termination. 0: Indicates that reception is in progress or was completed successfully*[1] [Clearing conditions] • By a power-on reset or in standby mode • When 0 is written to FER after reading FER = 1 1: Indicates that a framing error occurred during reception [Setting condition] • When the SCI founds that the stop bit at the end of the received data is 0 after completing reception*[2] Notes: 1. The FER flag is not affected and retains its previous value when the RE bit in SCSCR is cleared to 0. 2. In 2-stop-bit mode, only the first stop bit is checked for a value to 1; the second stop bit is not checked. If a framing error occurs, the receive data is transferred to SCRDR but the RDRF flag is not set. Subsequent serial reception cannot be continued while the FER flag is set to 1.

Figure 12.5 shows an example of the operation for transmission.

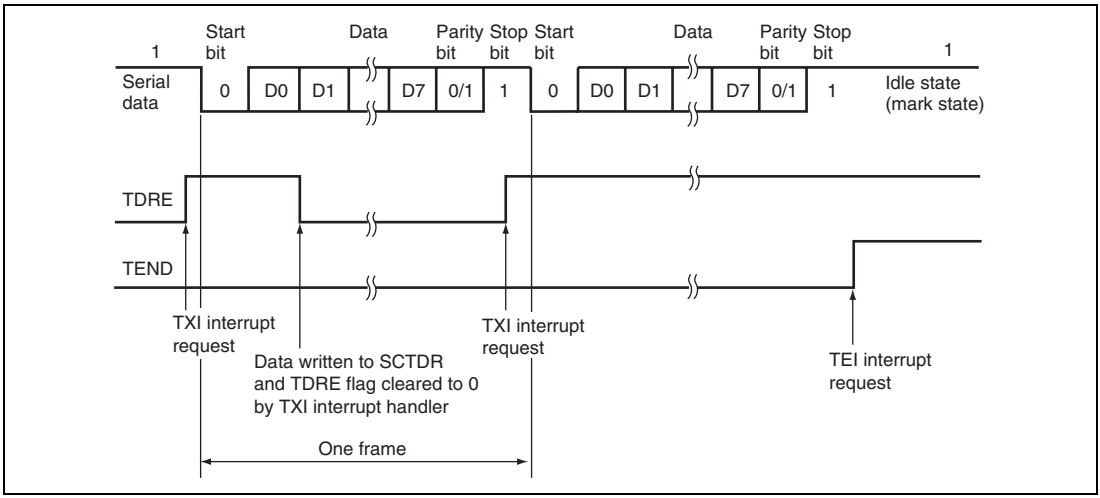

Figure 12.5 Example of Transmission in Asynchronous Mode (8-Bit Data, Parity, One Stop Bit)

Receiving Serial Data (Asynchronous Mode):

Figure 12.6 shows a sample flowchart for serial reception.

Use the following procedure for serial data reception after enabling the SCI for reception.

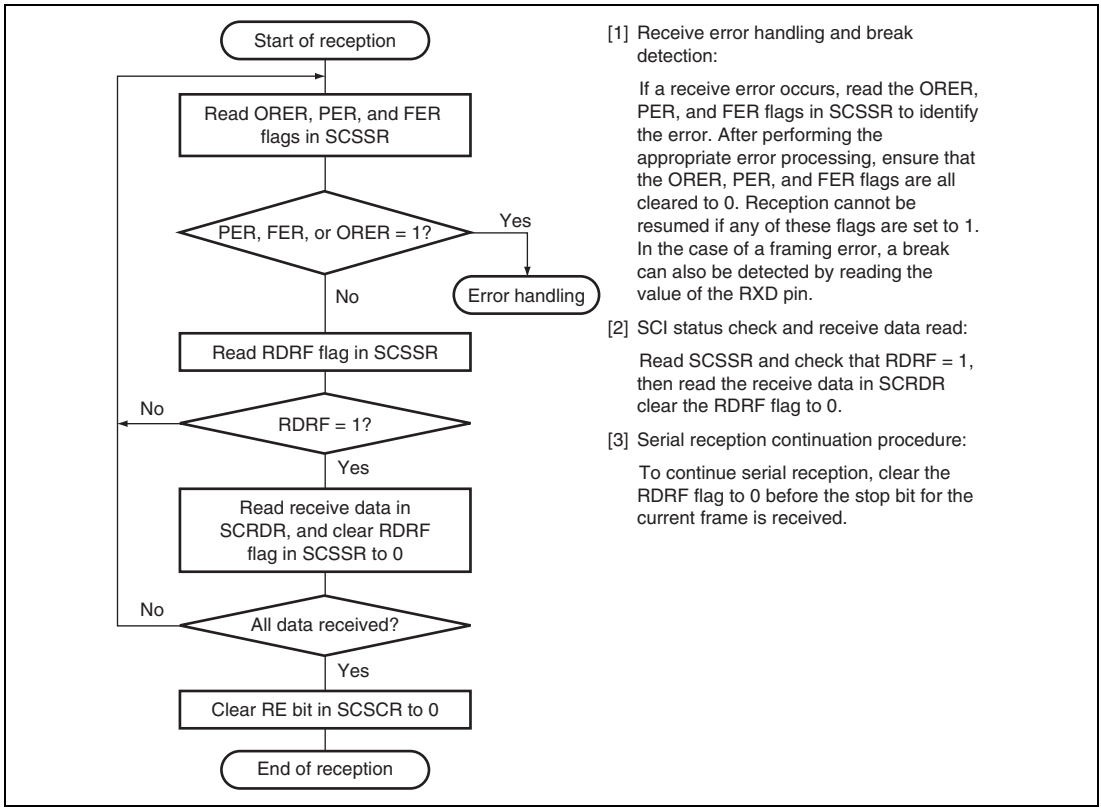

Figure 12.6 Sample Flowchart for Receiving Serial Data

Table 13.4 A/D Conversion Time (Single Mode)

		STC = 0											
		CKSL1 = 0						CKSL1 = 1					
		CKSL0 = 0			CKSL0 = 1			CKSL0 = 0			CKSL0 = 1		
Item	**Symbol**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**
A/D conversion start delay time	t_D	2	—	6	2	—	5	2	—	4	2	—	3
Input sampling time	t_{SPL}	—	24	—	—	18	—	—	12	—	—	6	—
A/D conversion time	t_{CONV}	202	—	206	152	—	155	102	—	104	52	—	53

		STC = 1											
		CKSL1 = 0						CKSL1 = 1					
		CKSL0 = 0			CKSL0 = 1			CKSL0 = 0			CKSL0 = 1		
Item	**Symbol**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**
A/D conversion start delay time	t_D	2	—	6	2	—	5	2	—	4	2	—	3
Input sampling time	t_{SPL}	—	36	—	—	27	—	—	18	—	—	9	—
A/D conversion time	t_{CONV}	258	—	262	194	—	197	130	—	132	66	—	67

Note: All values represent the number of states for Pϕ.

Table 13.5 A/D Conversion Time (Scan Mode)

				Conversion Time Calculation Example	
STC	**CKSL1**	**CKSL0**	**Conversion Time (State)**	**Pϕ = 25 MHz**	**Pϕ = 40 MHz**
0	0	0	200 (Fixed)	8 μs	5 μs
		1	150 (Fixed)	6 μs	3.8 μs
	1	0	100 (Fixed)	4 μs	2.5 μs
		1	50 (Fixed)	2 μs	Setting prohibited
1	0	0	256 (Fixed)	10.2 μs	6.4 μs
		1	192 (Fixed)	7.7 μs	4.8 μs
	1	0	128 (Fixed)	5.1 μs	3.2 μs
		1	64 (Fixed)	2.6 μs	Setting prohibited

- PBDRL (SH7124)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	PB5DR	-	PB3DR	-	PB1DR	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R	R/W	R	R/W	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5	PB5DR	0	R/W	See table 16.4.
4	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
3	PB3DR	0	R/W	See table 16.4.
2	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
1	PB1DR	0	R/W	See table 16.4.
0	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Table 16.4 Port B Data Register (PBDR) Read/Write Operations

- PBDRH Bit 0 and PBDRL Bits 5 and 3 to 1

PBIOR	Pin Function	Read	Write
0	General input	Pin state	Can write to PBDRH and PBDRL, but it has no effect on pin state
	Other than general input	Pin state	Can write to PBDRH and PBDRL, but it has no effect on pin state
1	General output	PBDRH or PBDRL value	Value written is output from pin
	Other than general output	PBDRH or PBDRL value	Can write to PBDRH and PBDRL, but it has no effect on pin state

Bit	Bit Name	Initial Value	R/W	Description
4	FLER	0	R	Flash Memory Error Indicates an error occurs during programming and erasing flash memory. When FLER is set to 1, flash memory enters the error protection state. When FLER is set to 1, high voltage is applied to the internal flash memory. To reduce the damage to flash memory, the reset signal must be released after the reset period of 100 μs, which is longer than normal. 0: Flash memory operates normally Programming/erasing protection for flash memory (error protection) is invalid. [Clearing condition] At a power-on reset 1: Indicates an error occurs during programming/erasing flash memory. Programming/erasing protection for flash memory (error protection) is valid. [Setting condition] See section 17.6.3, Error Protection.
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

(2) State Transition Diagram

Figure 17.8 gives an overview of the state transitions after the chip has been started up in boot mode. For details on boot mode, see section 17.8.1, Specifications of the Standard Serial Communications Interface in Boot Mode.

1. Bit-rate matching

   After the chip has been started up in boot mode, bit-rate matching between the SCI and the host proceeds.

2. Waiting for inquiry and selection commands

   The chip sends the requested information to the host in response to inquiries regarding the size and configuration of the user MAT, start addresses of the MATs, information on supported devices, etc.

3. Automatic erasure of the entire user MAT

   After all necessary inquiries and selections have been made and the command for transition to the programming/erasure state is sent by the host, the entire user MAT is automatically erased.

4. Waiting for programming/erasure command

— On receiving the programming selection command, the chip waits for data to be programmed. To program data, the host transmits the programming command code followed by the address where programming should start and the data to be programmed. This is repeated as required while the chip is in the programming-selected state. To terminate programming, H'FFFFFFFF should be transmitted as the first address of the area for programming. This makes the chip return to the programming/erasure command waiting state from the programming data waiting state.

— On receiving the erasure select command, the chip waits for the block number of a block to be erased. To erase a block, the host transmits the erasure command code followed by the number of the block to be erased. This is repeated as required while the chip is in the erasure-selected state. To terminate erasure, H'FF should be transmitted as the block number. This makes the chip return to the programming/erasure command waiting state from the erasure block number waiting state. Erasure should only be executed when a specific block is to be reprogrammed without executing a reset-start of the chip after the flash memory has been programmed in boot mode. If all desired programming is done in a single operation, such erasure processing is not necessary because all blocks are erased before the chip enters the programming/erasure/other command waiting state.

— In addition to the programming and erasure commands, commands for sum checking and blank checking (checking for erasure) of the user MAT, reading data from the user MAT, and acquiring current state information are provided.

Note that the command for reading from the user MAT can only read data that has been programmed after automatic erasure of the entire user MAT.

(2) Interrupts during programming/erasing

Though an interrupt processing can be executed at realtime during programming/erasing of the downloaded on-chip program, the following limitations and notes are applied.

1. When flash memory is being programmed or erased, the user MAT cannot be accessed. Prepare the interrupt vector table and interrupt processing routine in on-chip RAM. Make sure the flash memory being programmed or erased is not accessed by the interrupt processing routine. If flash memory is read, the read values are not guaranteed. If the relevant bank in flash memory that is being programmed or erased is accessed, the error protection state is entered, and programming or erasing is aborted. If a bank other than the relevant bank is accessed, the error protection state is not entered but the read values are not guaranteed.
2. Do not rewrite the program data specified by the FMPDR parameter. If new program data is to provided by the interrupt processing, temporarily save the new program data in another area. After confirming the completion of programming, save the new program data in the area specified by FMPDR or change the setting in FMPDR to indicated the other area in which the new program data was temporarily saved.
3. Make sure the interrupt processing routine does not rewrite the contents of the flash-memory related registers or data in the downloaded on-chip program area. During the interrupt processing, do not simultaneously perform download of the on-chip program by an SCO request or programming/erasing.
4. At the beginning of the interrupt processing routine, save the CPU register contents. Before returning from the interrupt processing, write the saved contents in the CPU registers again.
5. When a transition is made to sleep mode or software standby mode in the interrupt processing routine, the error protection state is entered and programming/erasing is aborted.
   If a transition is made to the reset state, the reset signal should only be released after providing a reset input over a period longer than the normal 100 μs to reduce the damage to flash memory.

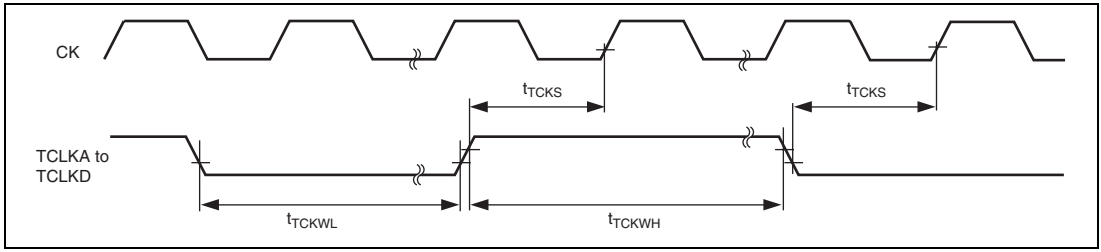

Figure 21.9 MTU2 Clock Input Timing

Table A.2 Pin States (SH7124)

Pin Function		Pin State					
		Reset State		Power-Down State			
Type	Pin Name	Power-On	Manual	Software Standby	Sleep	Oscillation Stop Detected	POE Function Used
Clock	XTAL	O	O	L	O	O	O
	EXTAL	I	I	I	I	I	I
System control	$\overline{\text{RES}}$	I	I	I	I	I	I
	$\overline{\text{MRES}}$	Z	I	Z	I	Z	I
	$\overline{\text{WDTOVF}}$	O*2	O	O	O	O	O
Operating mode control	MD1	I	I	I	I	I	I
	$\overline{\text{ASEMD0}}$	I*3	I*3	I*3	I*3	I*3	I*3
	FWE	I	I	I	I	I	I
Interrupt	NMI	I	I	I	I	I	I
	IRQ1 to IRQ3	Z	I	I	I	I	I
	$\overline{\text{IRQOUT}}$	Z	O	Z	O	Z	O
MTU2	TCLKA to TCLKD	Z	I	Z	I	I	I
	TIOC0A to TIOC0D	Z	I/O	K*1	I/O	I/O	Z
	TIOC3A, TIOC3C	Z	I/O	K*1	I/O	I/O	I/O
	TIOC3B, TIOC3D	Z	I/O	Z	I/O	Z	Z
	TIOC4A to TIOC4D	Z	I/O	Z	I/O	Z	Z
	TIC5U, TIC5V, TIC5W	Z	I	Z	I	I	I
POE	$\overline{\text{POE0}}$, $\overline{\text{POE1}}$, $\overline{\text{POE8}}$	Z	I	Z	I	I	I
SCI	SCK0, SCK2	Z	I/O	Z	I/O	I/O	I/O
	RXD0 to RXD2	Z	I	Z	I	I	I
	TXD0 to TXD2	Z	O	O*1	O	O	O
A/D Converter	AN0 to AN7	Z	I	Z	I	I	I