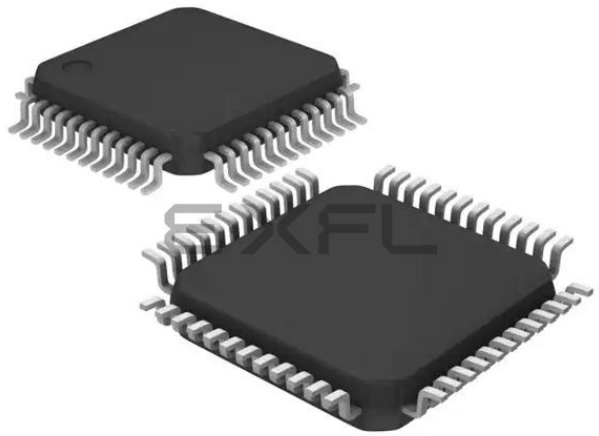

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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | SH-2 |
| Core Size | 32-Bit Single-Core |
| Speed | 50MHz |
| Connectivity | SCI |
| Peripherals | POR, PWM, WDT |
| Number of I/O | 23 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 4V ~ 5.5V |
| Data Converters | A/D 8x10b |
| Oscillator Type | External |
| Operating Temperature | -20°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-LQFP |
| Supplier Device Package | 48-LQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/df71241an50fpv |

# Preface

The SH7125 Group and SH7124 Group RISC (Reduced Instruction Set Computer) microcomputer include a Renesas Technology-original RISC CPU as its core, and the peripheral functions required to configure a system.

Target Users: This manual was written for users who will be using the SH7125 Group and SH7124 Group in the design of application systems. Target users are expected to understand the fundamentals of electrical circuits, logical circuits, and microcomputers.

Objective: This manual was written to explain the hardware functions and electrical characteristics of the SH7125 Group and SH7124 Group to the target users. Refer to the SH-1/SH-2/SH-DSP Software Manual for a detailed description of the instruction set.

Notes on reading this manual:

- In order to understand the overall functions of the chip
  Read the manual according to the contents. This manual can be roughly categorized into parts on the CPU, system control functions, peripheral functions and electrical characteristics.
- In order to understand the details of the CPU's functions
  Read the SH-1/SH-2/SH-DSP Software Manual.
- In order to understand the details of a register when its name is known
  Read the index that is the final part of the manual to find the page number of the entry on the register. The addresses, bits, and initial values of the registers are summarized in section 20, List of Registers.

| Examples: | | |
|---|---|---|
| | Register name: | The following notation is used for cases when the same or a similar function, e.g. serial communication interface, is implemented on more than one channel:<br>XXX_N (XXX is the register name and N is the channel number) |
| | Bit order: | The MSB is on the left and the LSB is on the right. |
| | Number notation: | Binary is B'xxxx, hexadecimal is H'xxxx, decimal is xxxx. |
| | Signal notation: | An overbar is added to a low-active signal: $\overline{\text{xxxx}}$ |

Related Manuals: The latest versions of all related manuals are available from our web site. Please ensure you have the latest versions of all documents you require.
http://www.renesas.com/

**Table 2.9 Instruction Formats**

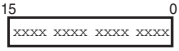
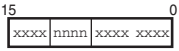
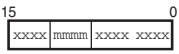
| Instruction Format | Source Operand | Destination Operand | Sample Instruction |
|---|---|---|---|
| 0 type<br>  | — | — | NOP |
| n type<br>  | — | nnnn: register direct | MOVT Rn |
| | Control register or system register | nnnn: register direct | STS MACH,Rn |
| | Control register or system register | nnnn: pre-decrement register indirect | STC.L SR,@-Rn |
| m type<br>  | mmmm: register direct | Control register or system register | LDC Rm,SR |
| | mmmm: post-increment register indirect | Control register or system register | LDC.L @Rm+,SR |
| | mmmm: register indirect | — | JMP @Rm |
| | PC relative using Rm | — | BRAF Rm |

**Table 6.4 Interrupt Response Time**

| Item | | Number of Cycles: NMI | Number of Cycles: IRQ | Number of Cycles: Peripheral Modules | Remarks |
|---|---|---|---|---|---|
| Interrupt priority decision and comparison with mask bits in SR | | 1 × Icyc + 2 × Pcyc | 1 × Icyc + 1 × Pcyc | 1 × Icyc + 2 × Pcyc | |
| Wait for completion of sequence currently being executed by CPU | | X (≥ 0) | X (≥ 0) | X (≥ 0) | The longest sequence is for interrupt or address-error exception handling (X = 7 × Icyc + m1 + m2 + m3 + m4). If an interrupt-masking instruction follows, however, the time may be even longer. |
| Time from start of interrupt exception handling until fetch of first instruction of exception handling routine starts | | 8 × Icyc + m1 + m2 + m3 | 8 × Icyc + m1 + m2 + m3 | 8 × Icyc + m1 + m2 + m3 | Performs the saving PC and SR, and vector address fetch. |
| Interrupt response time | Total: | 9 × Icyc + 2 × Pcyc + m1 + m2 + m3 + X | 9 × Icyc + 1 × Pcyc + m1 + m2 + m3 + X | 9 × Icyc + 2 × Pcyc + m1 + m2 + m3 + X | |
| | Minimum*: | 12 × Icyc + 2 × Pcyc | 12 × Icyc + 1 × Pcyc | 12 × Icyc + 2 × Pcyc | SR, PC, and vector table are all in on-chip RAM. |
| | Maximum: | 16 × Icyc + 2 × Pcyc + 2 × (m1 + m2 + m3) + m4 | 16 × Icyc + 1 × Pcyc + 2 (m1 + m2 + m3) + m4 | 16 × Icyc + 2 × Pcyc + 2 (m1 + m2 + m3) + m4 | |

Notes: * In the case that m1 = m2 = m3 = m4 = 1 × Icyc.
m1 to m4 are the number of cycles needed for the following memory accesses.
m1: SR save (longword write)
m2: PC save (longword write)
m3: Vector address read (longword read)
m4: Fetch first instruction of interrupt service routine

### 9.3.9 Timer A/D Converter Start Request Control Register (TADCR)

TADCR is a 16-bit readable/writable register that enables or disables A/D converter start requests and specifies whether to link A/D converter start requests with interrupt skipping operation. The MTU2 has one TADCR in channel 4.

| Bit: | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | BF[1:0] | | - | - | - | - | - | - | UT4AE | DT4AE | UT4BE | DT4BE | ITA3AE | ITA4VE | ITB3AE | ITB4VE |
| Initial value: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0* | 0 | 0* | 0* | 0* | 0* | 0* |
| R/W: | R/W | R/W | R | R | R | R | R | R | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Note: * Do not set to 1 when complementary PWM mode is not selected.

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 15, 14 | BF[1:0] | 00 | R/W | TADCOBRA_4/TADCOBRB_4 Transfer Timing Select<br>Select the timing for transferring data from TADCOBRA_4 and TADCOBRB_4 to TADCORA_4 and TADCORB_4.<br>For details, see table 9.29. |
| 13 to 8 | — | All 0 | R | Reserved<br>These bits are always read as 0. The write value should always be 0. |
| 7 | UT4AE | 0 | R/W | Up-Count TRG4AN Enable<br>Enables or disables A/D converter start requests (TRG4AN) during TCNT_4 up-count operation.<br>0: A/D converter start requests (TRG4AN) disabled during TCNT_4 up-count operation<br>1: A/D converter start requests (TRG4AN) enabled during TCNT_4 up-count operation |
| 6 | DT4AE | 0* | R/W | Down-Count TRG4AN Enable<br>Enables or disables A/D converter start requests (TRG4AN) during TCNT_4 down-count operation.<br>0: A/D converter start requests (TRG4AN) disabled during TCNT_4 down-count operation<br>1: A/D converter start requests (TRG4AN) enabled during TCNT_4 down-count operation |

### 9.3.30 Timer Waveform Control Register (TWCR)

TWCR is an 8-bit readable/writable register that controls the waveform when synchronous counter clearing occurs in TCNT_3 and TCNT_4 in complementary PWM mode and specifies whether to clear the counters at TGRA_3 compare match. The CCE bit and WRE bit in TWCR must be modified only while TCNT stops.

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | CCE | - | - | - | - | - | - | WRE |
| Initial value: | 0* | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W: | R/(W) | R | R | R | R | R | R | R/(W) |

Note: * Do not set to 1 when complementary PWM mode is not selected.

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 7 | CCE | 0* | R/(W) | Compare Match Clear Enable<br>Specifies whether to clear counters at TGRA_3 compare match in complementary PWM mode.<br>0: Does not clear counters at TGRA_3 compare match<br>1: Clears counters at TGRA_3 compare match<br>[Setting condition]<br>• When 1 is written to CCE after reading CCE = 0 |
| 6 to 1 | — | All 0 | R | Reserved<br>These bits are always read as 0. The write value should always be 0. |

| Bit | Bit Name | Initial value | R/W | Description |
|---|---|---|---|---|
| 8 | PIE1 | 0 | R/W | Port Interrupt Enable 1<br>This bit enables/disables interrupt requests when any one of the POE0F to POE3F bits of the ICSR1 is set to 1.<br>0: Interrupt requests disabled<br>1: Interrupt requests enabled |
| 7, 6 | POE3M[1:0] | 00 | R/W*[2] | POE3 mode 1, 0<br>(Supported only by the SH7125. Write 00 to these bits in the SH7124.)<br>These bits select the input mode of the $\overline{\text{POE3}}$ pin.<br>00: Accept request on falling edge of POE3 input<br>01: Accept request when POE3 input has been sampled for 16 P$\phi$/8 clock pulses and all are low level.<br>10: Accept request when POE3 input has been sampled for 16 P$\phi$/16 clock pulses and all are low level.<br>11: Accept request when POE3 input has been sampled for 16 P$\phi$/128 clock pulses and all are low level. |
| 5, 4 | — | All 0 | R/W*[2] | Reserved<br>These bits are always read as 0. The write value should always be 0. |
| 3, 2 | POE1M[1:0] | 00 | R/W*[2] | POE1 mode 1, 0<br>These bits select the input mode of the $\overline{\text{POE1}}$ pin.<br>00: Accept request on falling edge of POE1 input<br>01: Accept request when POE1 input has been sampled for 16 P$\phi$/8 clock pulses and all are low level.<br>10: Accept request when POE1 input has been sampled for 16 P$\phi$/16 clock pulses and all are low level.<br>11: Accept request when POE1 input has been sampled for 16 P$\phi$/128 clock pulses and all are low level. |

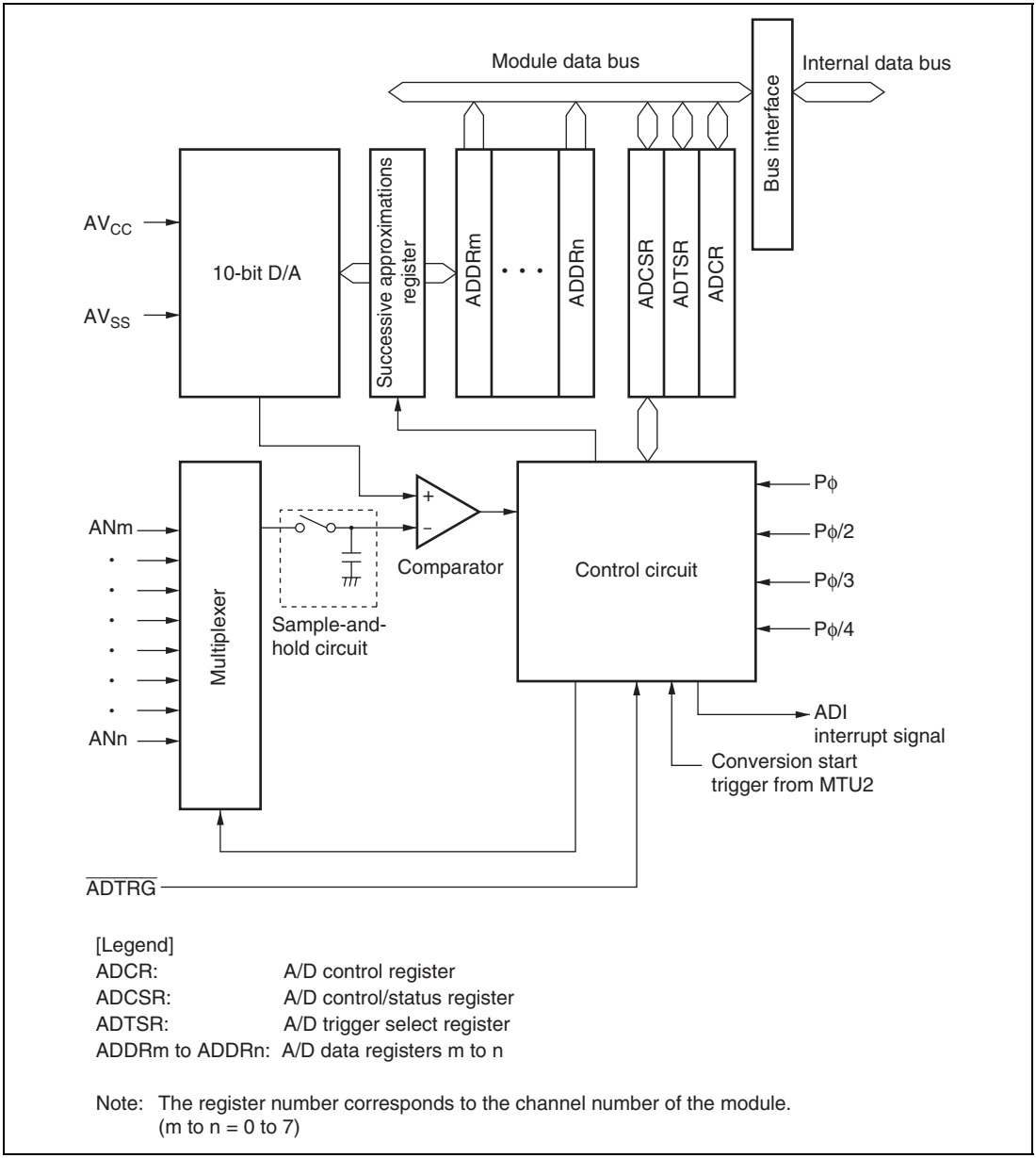
| Bit | Bit Name | Initial value | R/W | Description |
|---|---|---|---|---|
| 13 | MTU2P2CZE | 1 | R/W* | MTU2 Port 2 Output Comparison/High-Impedance Enable<br>This bit specifies whether to compare output levels for the MTU2 high-current PE12/TIOC4A and PE14/TIOC4C pins and to place them in high-impedance state when the OSF1 bit is set to 1 while the OEC1 bit is 1 or when any one of the POE0F, POE1F, POE3F, and MTU2CH34HIZ bits is set to 1.<br>0: Does not compare output levels or place the pins in high-impedance state<br>1: Compares output levels and places the pins in high-impedance state |
| 12 | MTU2P3CZE | 1 | R/W* | MTU2 Port 3 Output Comparison/High-Impedance Enable<br>This bit specifies whether to compare output levels for the MTU2 high-current PE13/TIOC4B and PE15/TIOC4D pins and to place them in high-impedance state when the OSF1 bit is set to 1 while the OEC1 bit is 1 or when any one of the POE0F, POE1F, POE3F, and MTU2CH34HIZ bits is set to 1.<br>0: Does not compare output levels or place the pins in high-impedance state<br>1: Compares output levels and places the pins in high-impedance state |
| 11 | — | 0 | R | Reserved<br>This bit is always read as 0. The write value should always be 0. |
| 10 to 8 | — | All 1 | R/W* | Reserved<br>These bits are always read as 1. The write value should always be 1. |
| 7 to 0 | — | 0 | R | Reserved<br>These bits are always read as 0. The write value should always be 0. |

Note: * Can be modified only once after a power-on reset.

**Table 12.12 Maximum Bit Rates with External Clock Input (Clock Synchronous Mode)**

| Pϕ (MHz) | External Input Clock (MHz) | Maximum Bit Rate (bits/s) |
|---|---|---|
| 10 | 1.6667 | 1666666.7 |
| 12 | 2.0000 | 2000000.0 |
| 14 | 2.3333 | 2333333.3 |
| 16 | 2.6667 | 2666666.7 |
| 18 | 3.0000 | 3000000.0 |
| 20 | 3.3333 | 3333333.3 |
| 22 | 3.6667 | 3666666.7 |
| 24 | 4.0000 | 4000000.0 |
| 26 | 4.3333 | 4333333.3 |
| 28 | 4.6667 | 4666666.7 |
| 30 | 5.0000 | 5000000.0 |
| 32 | 5.3333 | 5333333.3 |
| 34 | 5.6667 | 5666666.7 |
| 36 | 6.0000 | 6000000.0 |
| 38 | 6.3333 | 6333333.3 |
| 40 | 6.6667 | 6666666.7 |

Figure 13.1 shows a block diagram of the A/D converter.




[Legend]
ADCR: A/D control register
ADCSR: A/D control/status register
ADTSR: A/D trigger select register
ADDRm to ADDRn: A/D data registers m to n

Note: The register number corresponds to the channel number of the module.
(m to n = 0 to 7)

**Figure 13.1 Block Diagram of A/D Converter (for One Module)**

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 3 to 0 | TRG0S[3:0] | 0000 | R/W | A/D Trigger 0 Select 3 to 0<br>Select an external trigger or MTU2 trigger to start A/D conversion for group 0 when A/D module 0 is in single mode, 4-channel scan mode, or 2-channel scan mode.<br>0000: External trigger pin ($\overline{\text{ADTRG}}$) input<br>0001: TRGA input capture/compare match for each MTU2 channel or TCNT_4 underflow (trough) in complementary PWM mode (TRGAN)<br>0010: MTU2 channel 0 compare match (TRG0N)<br>0011: MTU2 A/D conversion start request delaying (TRG4AN)<br>0100: MTU2 A/D conversion start request delaying (TRG4BN)<br>0101: Setting prohibited<br>0110: Setting prohibited<br>0111: Setting prohibited<br>1xxx: Setting prohibited<br>When switching the selector, first clear the ADST bit in the A/D control register (ADCR) to 0.<br>Specify different trigger sources for the group 0 and group 1 conversion requests so that a group 0 conversion request is not generated simultaneously with a group 1 conversion request in 2-channel scan mode. |

[Legend]

x: Don't care

- PEDRL (SH7124)

| Bit: | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | PE15DR | PE14DR | PE13DR | PE12DR | PE11DR | PE10DR | PE9DR | PE8DR | - | - | - | - | PE3DR | PE2DR | PE1DR | PE0DR |
| Initial value: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W: | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R | R | R | R | R/W | R/W | R/W | R/W |

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 15 | PE15DR | 0 | R/W | See table 16.6. |
| 14 | PE14DR | 0 | R/W | |
| 13 | PE13DR | 0 | R/W | |
| 12 | PE12DR | 0 | R/W | |
| 11 | PE11DR | 0 | R/W | |
| 10 | PE10DR | 0 | R/W | |
| 9 | PE9DR | 0 | R/W | |
| 8 | PE8DR | 0 | R/W | |
| 7 to 4 | — | All 0 | R | Reserved<br>These bits are always read as 0. The write value should always be 0. |
| 3 | PE3DR | 0 | R/W | See table 16.6. |
| 2 | PE2DR | 0 | R/W | |
| 1 | PE1DR | 0 | R/W | |
| 0 | PE0DR | 0 | R/W | |

**Table 16.6 Port E Data Register L (PEDRL) Read/Write Operations**

- PEDRL Bits 15 to 0

| PEIOR | Pin Function | Read | Write |
|---|---|---|---|
| 0 | General input | Pin state | Can write to PEDRL, but it has no effect on pin state |
| | Other than general input | Pin state | Can write to PEDRL, but it has no effect on pin state |
| 1 | General output | PEDRL value | Value written is output from pin |
| | Other than general output | PEDRL value | Can write to PEDRL, but it has no effect on pin state |

## 16.4 Port F

Port F in the SH7125 and SH7124 is an input-only port with the eight pins shown in figure 16.7.

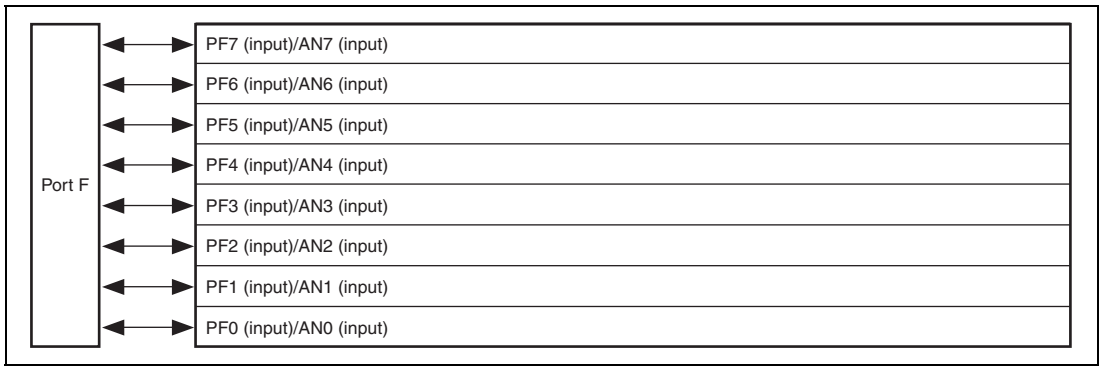



**Figure 16.7 Port F (SH7125, SH7124)**

### 16.4.1 Register Descriptions

Port F is an 8-bit input-only port in the SH7125 and SH7124. Port F has the following register. For details on register addresses and register states during each processing, refer to section 20, List of Registers.

**Table 16.7 Register Configuration**

| Register Name | Abbreviation | R/W | Initial Value | Address | Access Size |
|---|---|---|---|---|---|
| Port F data register L | PFDRL | R | — | H'FFFFD382 | 8, 16 |

(1) Download Control

The on-chip program is automatically downloaded by setting the SCO bit to 1. The on-chip RAM area to be downloaded is the area as much as 3 Kbytes starting from the start address specified by FTDAR. For the address map of the on-chip RAM, see figure 17.10.

The download control is set by using the programming/erasing interface registers. The return value is given by the DPFR parameter.

(a) Download pass/fail result parameter (DPFR: one byte of start address of on-chip RAM specified by FTDAR)

This parameter indicates the return value of the download result. The value of this parameter can be used to determine if downloading is executed or not. Since the confirmation whether the SCO bit is set to 1 is difficult, the certain determination must be performed by setting one byte of the start address of the on-chip RAM area specified by FTDAR to a value other than the return value of download (for example, H'FF) before the download start (before setting the SCO bit to 1). For the checking method of download results, see section 17.5.2 (2), Programming Procedure in User Program Mode.

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | - | - | - | - | - | SS | FK | SF |
| Initial value: | - | - | - | - | - | - | - | - |
| R/W: | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 7 to 3 | — | Undefined | R/W | Unused<br>Return 0. |
| 2 | SS | Undefined | R/W | Source Select Error Detect<br>The on-chip program which can be downloaded can be specified as only one type. When more than two types of the program are selected, the program is not selected, or the program is selected without mapping, an error occurs.<br>0: Download program can be selected normally<br>1: Download error occurs (Multi-selection or program which is not mapped is selected) |

### (6) Inquiry on operating frequency

In response to the inquiry on operating frequency, the boot program returns the number of operating frequencies and the maximum and minimum values.

| | |
|---|---|
| Command | H'23 |

— Command H'23 (1 byte): Inquiry on operating frequency

| | | | |
|---|---|---|---|
| Response | H'33 | Size | No. of frequency types |
| | Operating freq. (min) | | Operating freq. (max) |
| | … | | |
| | SUM | | |

— Response H'33 (1 byte): Response to the inquiry on operating frequency

— Size (1 byte): The total length of the number of frequency types, and maximum and minimum values of operating frequency fields.

— Number of frequency types (1 byte): The number of operating clock frequencies required within the device.
For example, the value two indicates main and peripheral operating clock frequencies.

— Minimum value of operating frequency (2 bytes): The minimum frequency of a frequency-multiplied or -divided clock signal.
The value in this field and in the maximum value field is the frequency in MHz to two decimal places, multiplied by 100 (for example, if the frequency is 20.00 MHz, the value multiplied by 100 is 2000, so H'07D0 is returned here).

— Maximum value of operating frequency (2 bytes): The maximum frequency of a frequency-multiplied or -divided clock signal.
As many pairs of minimum values are included as there are frequency types.

— SUM (1 byte): Checksum

### (7) Inquiry on user MATs

In response to the inquiry on user MATs, the boot program returns the number of user MAT areas and their addresses.

| Command | H'25 |
|---|---|

— Command H'25 (1 byte): Inquiry on user MAT information

| Response | H'35 | Size | No. of areas | |
|---|---|---|---|---|
| | First address of the area | | | Last address of the area |
| | … | | | |
| | SUM | | | |

— Response H'35 (1 byte): Response to the inquiry on user MATs
— Size (1 byte): The total length of the number of areas and first and last address fields.
— Number of areas (1 byte): The number of user MAT areas.
H'01 is returned if the entire user MAT area is continuous.
— First address of the area (4 bytes)
— Last address of the area (4 bytes)
As many pairs of first and last address field are included as there are areas.
— SUM (1 byte): Checksum

### (8) Inquiry on erasure blocks

In response to the inquiry on erasure blocks, the boot program returns the number of erasure blocks in the user MAT and the addresses where each block starts and ends.

| Command | H'26 |
|---|---|

— Command H'26 (1 byte): Inquiry on erasure blocks

| Response | H'36 | Size | No. of blocks | |
|---|---|---|---|---|
| | First address of the block | | | Last address of the block |
| | … | | | |
| | SUM | | | |

# Section 18 RAM

This LSI has an on-chip high-speed static RAM. The on-chip RAM is connected to the CPU by a 32-bit data bus (L bus), enabling 8, 16, or 32-bit width access to data in the on-chip RAM.

The on-chip RAM is allocated to different addresses according to each product as shown in figure 18.1. The on-chip RAM can be accessed from the CPU (via the L bus). An access from the L bus (CPU) is a 1-cycle access. In addition, the contents of the on-chip RAM are retained in sleep mode or software standby mode, and at a power-on reset or manual reset.

The on-chip RAM can be enabled or disabled by means of the RAME bit in the RAM control register (RAMCR). For details on the RAM control register (RAMCR), refer to section 19.3.7, RAM Control Register (RAMCR).

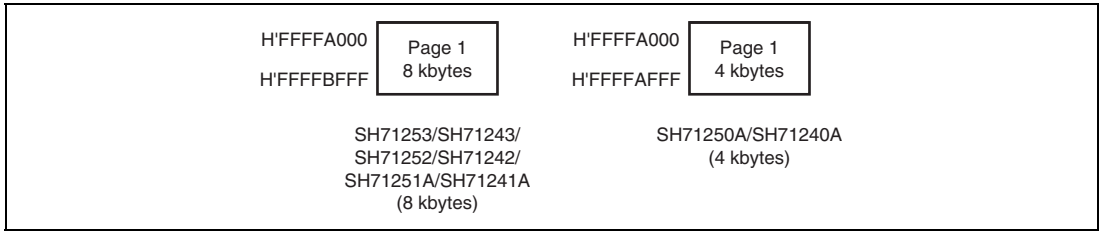
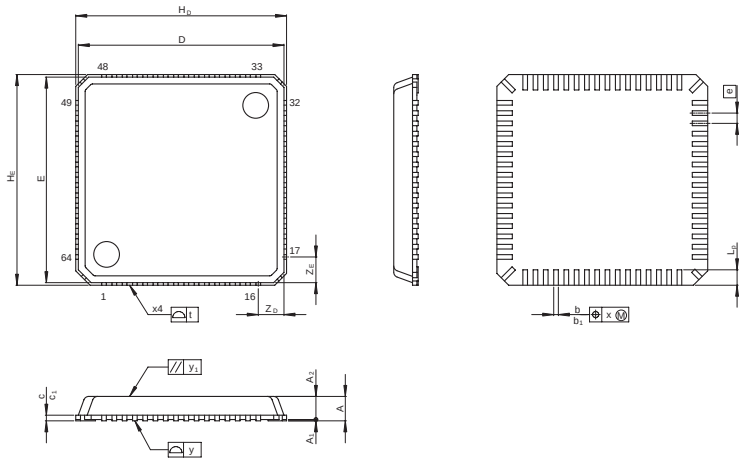



**Figure 18.1 On-chip RAM Addresses**

| Register Name | Abbreviation | Number of Bits | Address | Module | Access Size | Number of Access States |
|---|---|---|---|---|---|---|
| Timer interrupt skipping counter | TITCNT | 8 | H'FFFFC231 | MTU2 | 8 | MPϕ reference |
| Timer buffer transfer set register | TBTER | 8 | H'FFFFC232 | | 8 | B: 2, W: 2, L: 4 |
| Timer dead time enable register | TDER | 8 | H'FFFFC234 | | 8 | |
| Timer output level buffer register | TOLBR | 8 | H'FFFFC236 | | 8 | |
| Timer buffer operation transfer mode register_3 | TBTM_3 | 8 | H'FFFFC238 | | 8, 16 | |
| Timer buffer operation transfer mode register_4 | TBTM_4 | 8 | H'FFFFC239 | | 8 | |
| Timer A/D converter start request control register | TADCR | 16 | H'FFFFC240 | | 16 | |
| Timer A/D converter start request cycle set register A_4 | TADCORA_4 | 16 | H'FFFFC244 | | 16, 32 | |
| Timer A/D converter start request cycle set register B_4 | TADCORB_4 | 16 | H'FFFFC246 | | 16 | |
| Timer A/D converter start request cycle set buffer register A_4 | TADCOBRA_4 | 16 | H'FFFFC248 | | 16, 32 | |
| Timer A/D converter start request cycle set buffer register B_4 | TADCOBRB_4 | 16 | H'FFFFC24A | | 16 | |
| Timer waveform control register | TWCR | 8 | H'FFFFC260 | | 8 | |
| Timer start register | TSTR | 8 | H'FFFFC280 | | 8, 16 | |
| Timer synchronous register | TSYR | 8 | H'FFFFC281 | | 8 | |
| Timer read/write enable register | TRWER | 8 | H'FFFFC284 | | 8 | |
| Timer control register_0 | TCR_0 | 8 | H'FFFFC300 | | 8, 16, 32 | |
| Timer mode register_0 | TMDR_0 | 8 | H'FFFFC301 | | 8 | |
| Timer I/O control register H_0 | TIORH_0 | 8 | H'FFFFC302 | | 8, 16 | |
| Timer I/O control register L_0 | TIORL_0 | 8 | H'FFFFC303 | | 8 | |
| Timer interrupt enable register_0 | TIER_0 | 8 | H'FFFFC304 | | 8, 16, 32 | |
| Timer status register_0 | TSR_0 | 8 | H'FFFFC305 | | 8 | |
| Timer counter_0 | TCNT_0 | 16 | H'FFFFC306 | | 16 | |
| Timer general register A_0 | TGRA_0 | 16 | H'FFFFC308 | | 16, 32 | |
| Timer general register B_0 | TGRB_0 | 16 | H'FFFFC30A | | 16 | |

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-VQFN64-8x8-0.40 | PVQN0064LB-A | TNP-64B/TNP-64BV | 0.12g |




| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | — | 8.0 | — |
| E | — | 8.0 | — |
| $A_2$ | — | 0.89 | — |
| A | — | — | 0.95 |
| $A_1$ | 0.005 | 0.02 | 0.04 |
| b | 0.13 | 0.18 | 0.23 |
| $b_1$ | — | 0.16 | — |
| e | — | 0.4 | — |
| $L_p$ | 0.50 | 0.60 | 0.70 |
| x | — | — | 0.05 |
| y | — | — | 0.05 |
| $y_1$ | — | — | 0.2 |
| t | — | — | 0.2 |
| $H_D$ | — | 8.2 | — |
| $H_E$ | — | 8.2 | — |
| $Z_D$ | — | 1.0 | — |
| $Z_E$ | — | 1.0 | — |
| c | 0.17 | 0.22 | 0.25 |
| $c_1$ | — | 0.20 | — |

**Figure C.4 VQFN-64**

# Index